

#### Features

- Integrated analog input Class D audio amplifier driver in a small 16 pin package
- Floating inputs enable easy half bridge implementation
- Programmable bidirectional over-current protection with self-reset function
- Programmable preset deadtime for improved THD performances
- Start and stop click noise reduction
- High noise immunity
- $\pm 100$  V ratings deliver up to 500 W in output power
- Operates up to 800 kHz
- Leadfree, RoHS compliant
- Automotive Qualified<sup>T</sup>

#### Product Summary

|                                 |               |                 |
|---------------------------------|---------------|-----------------|
| $V_{\text{OFFSET}}$ (max)       |               | $\pm 100$ V     |
| Gate driver                     | Io+ (typical) | 1.0 A           |
|                                 | Io- (typical) | 1.2 A           |
| Selectable Deadtime             |               | 25/40/65/105 ns |
| OC protection delay (max)       |               | 500 ns          |
| DC offset                       |               | <20 mV          |
| PWM frequency                   |               | ~800 kHz        |
| Error amplifier open loop gain  |               | >60 dB          |
| THD+N* (1kHz, 50W, 4 $\Omega$ ) |               | 0.01 %          |
| Residual Noise* (AES-17 Filter) |               | 200 $\mu$ Vrms  |

\* measured with recommended circuit

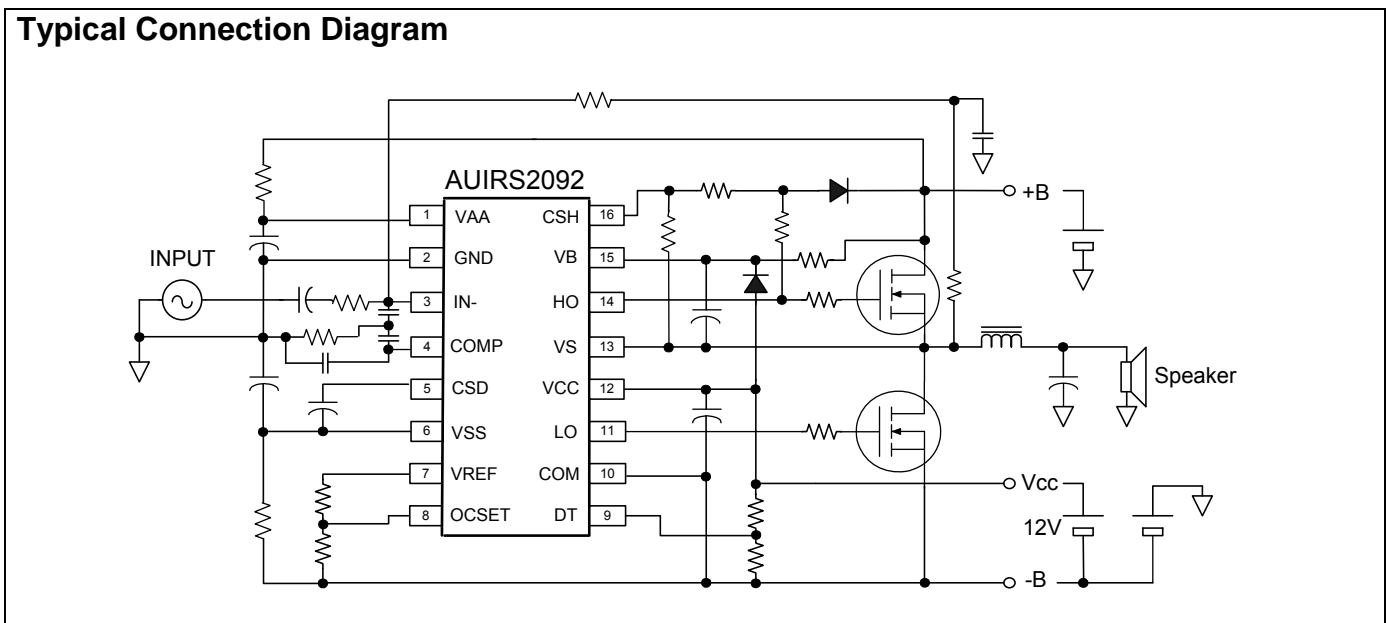
#### Typical Applications

- Automotive mini component stereo systems
- Automotive powered speaker systems
- Automotive audio power amplifiers

#### Package Options



#### Typical Connection Diagram



| <b>Table of Contents</b>                    | <b>Page</b> |
|---|-------------|
| Description                                 | 3           |
| Simplified Block Diagram                    | 4           |
| Typical Application Diagram                 | 4           |
| Qualification Information                   | 5           |
| Absolute Maximum Ratings                    | 6           |
| Recommended Operating Conditions            | 7           |
| Electrical Characteristics                  | 8-10        |
| Waveform Definitions                        | 11          |
| Functional Block Diagram                    | 12          |
| Input/Output Pin Equivalent Circuit Diagram | 13          |
| Lead Definitions                            | 14          |
| Lead Assignments                            | 14          |
| Parameter Temperature Trends                | 15-19       |
| Package Details                             | 19          |
| Tape and Reel Details                       | 20          |
| Part Marking Information                    | 21          |
| Ordering Information                        | 21          |

## **Description**

The AUIRS2092 is a high voltage, high performance Class D audio amplifier driver with PWM modulator and protection. In conjunction with two external MOSFET and a few external components, a complete Class D audio amplifier with protection can be realized.

International Rectifier's proprietary noise isolation technology allows high current gate drive stage and high speed low noise error amplifier reside on a single small silicon die.

Open elements of PWM modulator section allow flexible PWM topology implementation.



**Qualification Information<sup>†</sup>**

|                                   |                      |   |  |
|-----------------------------------|----------------------|---|--|
| <b>Qualification Level</b>        |                      | Automotive<br>(per AEC-Q100 <sup>††</sup> )   |  |
|                                   |                      | Comments: This family of ICs has passed an Automotive qualification. IR's Industrial and Consumer qualification level is granted by extension of the higher Automotive level. |  |
| <b>Moisture Sensitivity Level</b> |                      | SOIC16N   | MSL3 <sup>†††</sup> 260°C<br>(per IPC/JEDEC J-STD-020) |
| <b>ESD</b>                        | Machine Model        | Class M2 (+/-150V)<br>(per AEC-Q100-003)  |  |
|                                   | Human Body Model     | Class H1B (+/-750V)<br>(per AEC-Q100-002)   |  |
|                                   | Charged Device Model | Class C3A (+/-750V)<br>(per AEC-Q100-011)   |  |
| <b>IC Latch-Up Test</b>           |                      | Class II, Level B <sup>††††</sup><br>(per AEC-Q100-004)   |  |
| <b>RoHS Compliant</b>             |                      | Yes   |  |

† Qualification standards can be found at International Rectifier's web site <http://www.irf.com/>

†† Exceptions to AEC-Q100 requirements are noted in the qualification report.

††† Higher MSL ratings may be available for the specific package types listed here. Please contact your International Rectifier sales representative for further information.

†††† CSD pin stressed to +/-20mA, CSH pin stressed to +/-40mA, DT and OCSET pins stressed to +/-20mA

**Absolute Maximum Ratings**

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM lead. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only; and functional operation of the device at these or any other condition beyond those indicated in the "Recommended Operating Conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Ambient temperature ( $T_A$ ) is 25°C, unless otherwise specified.

| Symbol       | Definition   | Min                                | Max                                | Units |
|--------------|--|------------------------------------|------------------------------------|-------|
| $V_B$        | High side floating supply voltage                          | -0.3                               | 220                                | V     |
| $V_S$        | High side floating supply voltage (Note2)                  | $V_B - 20$                         | $V_B + 0.3$                        |       |
| $V_{HO}$     | High side floating output voltage                          | $V_S - 0.3$                        | $V_B + 0.3$                        |       |
| $V_{CSH}$    | CSH pin input voltage                                      | $V_S - 0.3$                        | $V_B + 0.3$                        |       |
| $V_{CC}$     | Low side fixed supply voltage (Note2)                      | -0.3                               | 20                                 |       |
| $V_{LO}$     | Low side output voltage                                    | -0.3                               | $V_{CC} + 0.3$                     |       |
| $V_{AA}$     | Floating input positive supply voltage (Note2)             | (See $I_{AAZ}$ )                   | 210                                |       |
| $V_{SS}$     | Floating input negative supply voltage (Note2)             | -1<br>(See $I_{SSZ}$ )             | GND + 0.3                          |       |
| $V_{GND}$    | Floating input supply ground voltage                       | $V_{SS} - 0.3$<br>(See $I_{SSZ}$ ) | $V_{AA} + 0.3$<br>(See $I_{AAZ}$ ) |       |
| $I_{IN-}$    | Inverting input current (Note1)                            | ---                                | ±3                                 | mA    |
| $V_{CSD}$    | SD pin input voltage                                       | $V_{SS} - 0.3$                     | $V_{AA} + 0.3$                     | V     |
| $V_{COMP}$   | COMP pin input voltage                                     | $V_{SS} - 0.3$                     | $V_{AA} + 0.3$                     |       |
| $V_{DT}$     | DT pin input voltage                                       | -0.3                               | $V_{CC} + 0.3$                     |       |
| $V_{OCSET}$  | OCSET pin input voltage                                    | -0.3                               | $V_{CC} + 0.3$                     |       |
| $I_{AAZ}$    | Floating input positive supply zener clamp current (Note2) | ---                                | 20                                 | mA    |
| $I_{SSZ}$    | Floating input negative supply zener clamp current (Note2) | ---                                | 20                                 |       |
| $I_{CCZ}$    | Low side supply zener clamp current (Note3)                | ---                                | 10                                 |       |
| $I_{BSZ}$    | Floating supply zener clamp current (Note3)                | ---                                | 10                                 |       |
| $I_{OREF}$   | Reference output current                                   | ---                                | 5                                  |       |
| $dV_S/dt$    | Allowable $V_S$ voltage slew rate                          | ---                                | 50                                 | V/ns  |
| $dV_{SS}/dt$ | Allowable $V_{SS}$ voltage slew rate (Note3)               | ---                                | 50                                 | V/ms  |
| $P_d$        | Maximum power dissipation @ $T_A \leq +25^\circ\text{C}$   | ---                                | 1.0                                | W     |
| $R_{thJA}$   | Thermal resistance, Junction to ambient                    | ---                                | 115                                | °C/W  |
| $T_J$        | Junction Temperature                                       | ---                                | 150                                | °C    |
| $T_S$        | Storage Temperature  | -55                                | 150                                | °C    |
| $T_L$        | Lead temperature (soldering, 10 seconds)                   | ---                                | 300                                | °C    |

Note1: IN- contains clamping diode to GND.

Note2:  $V_{DD} - IN+$ , GND -  $V_{SS}$ ,  $V_{CC} - COM$  and  $V_B - V_S$  contain internal shunt zener diodes. Please note that the voltage ratings of these can be limited by the clamping current.

Note3: For the rising and falling edges of step signal of 10 V.  $V_{SS} = 15\text{ V to } 200\text{ V}$ .

### Recommended Operating Conditions

For proper operation, the device should be used within the recommended conditions below. The  $V_S$  and COM offset ratings are tested with supplies biased at  $V_{AA}-V_{SS}=10\text{ V}$ ,  $V_{CC}=12\text{ V}$  and  $V_B-V_S=12\text{ V}$ . All voltage parameters are absolute voltages referenced to COM; all currents are defined positive into any lead.

| Symbol       | Definition   | Min.              | Max.              | Units |    |
|--------------|--|-------------------|-------------------|-------|----|
| $V_B$        | High side floating supply absolute voltage                 | $V_S + 10$        | $V_S + 18$        | V     |    |
| $V_S$        | High side floating supply offset voltage                   | (Note 1)          | 200               |       |    |
| $I_{AAZ}$    | Floating input positive supply zener clamp current         | 1                 | 11                | mA    |    |
| $I_{SSZ}$    | Floating input negative supply zener clamp current         | 1                 | 11                |       |    |
| $V_{SS}$     | Floating input supply absolute voltage                     | 0                 | 200               | V     |    |
| $V_{HO}$     | High side floating output voltage                          | $V_S$             | $V_B$             |       |    |
| $V_{CC}$     | Low side fixed supply voltage                              | 10                | 18                |       |    |
| $V_{LO}$     | Low side output voltage                                    | 0                 | $V_{CC}$          |       |    |
| $V_{GND}$    | GND pin input voltage                                      | $V_{SS}$ (Note 3) | $V_{AA}$ (Note 3) |       |    |
| $V_{IN-}$    | Inverting input voltage                                    | $V_{GND} - 0.5$   | $V_{GND} + 0.5$   |       |    |
| $V_{CSD}$    | CSD pin input voltage                                      | $V_{SS}$          | $V_{AA}$          |       |    |
| $V_{COMP}$   | COMP pin input voltage                                     | $V_{SS}$          | $V_{AA}$          |       |    |
| $C_{COMP}$   | COMP pin phase compensation capacitor to GND               | 1                 | -                 |       | nF |
| $V_{DT}$     | DT pin input voltage                                       | 0                 | $V_{CC}$          |       | V  |
| $I_{OREF}$   | Reference output current to COM (Note 2)                   | 0.3               | 0.8               | mA    |    |
| $V_{OCSET}$  | OCSET pin input voltage                                    | 0.5               | 5                 |       |    |
| $V_{CSH}$    | CSH pin input voltage                                      | $V_S$             | $V_B$             | V     |    |
| $dV_{SS}/dt$ | Allowable $V_{SS}$ voltage slew rate upon power-up (Note4) | -                 | 50                | V/ms  |    |
| $I_{PW}$     | Input pulse width  | 10 (Note 5)       | -                 | ns    |    |
| $f_{SW}$     | Switching Frequency  | -                 | 800               | kHz   |    |
| $T_A$        | Ambient Temperature  | -40               | 125               | °C    |    |

Note 1: Logic operational for  $V_S$  equal to  $-5\text{ V}$  to  $+200\text{ V}$ . Logic state held for  $V_S$  equal to  $-5\text{ V}$  to  $-V_{BS}$ .

Note 2: Nominal voltage for  $V_{REF}$  is  $5.1\text{ V}$ .  $I_{OREF}$  of  $0.3 - 0.8\text{ mA}$  dictates total external resistor value on  $V_{REF}$  to be  $6.3\text{ k}\Omega$  to  $16.7\text{ k}\Omega$ .

Note 3: GND input voltage is limited by  $I_{AAZ}$  and  $I_{SSZ}$ .

Note 4:  $V_{SS}$  ramps up from  $0\text{ V}$  to  $200\text{ V}$ .

Note 5: Output logic status may not respond correctly if input pulse width is smaller than the minimum pulse width.

**Electrical Characteristics**

Unless otherwise noted, these specifications apply for an operating junction temperature range of  $-40^{\circ}\text{C} \leq T_j \leq 125^{\circ}\text{C}$  with bias conditions of  $V_{CC}, V_{BS} = 12\text{ V}$ ,  $V_{SS} = V_S = \text{COM} = 0\text{ V}$ ,  $V_{AA} = 10\text{ V}$ ,  $C_L = 1\text{ nF}$ .

| Symbol  | Definition   | Min  | Typ  | Max  | Units   | Test Conditions  |
|---|--|------|------|------|---|--|
| <b>Low Side Supply</b>  |  |      |      |      |   |  |
| UV <sub>CC+</sub>   | V <sub>CC</sub> supply UVLO positive threshold   | 8.4  | 8.9  | 9.8  | V   |  |
| UV <sub>CC-</sub>   | V <sub>CC</sub> supply UVLO negative threshold   | 8.2  | 8.7  | 9.4  |   |  |
| UV <sub>CC</sub> HYS  | UV <sub>CC</sub> hysteresis  | -    | 0.2  | -    |   |  |
| I <sub>QCC</sub>  | Low side quiescent current   | -    | -    | 3    | mA  | V <sub>DT</sub> =V <sub>CC</sub>   |
| V <sub>CLAMPL</sub>   | Low side zener diode clamp voltage   | 19.6 | 20.4 | 21.6 | V   | I <sub>CC</sub> =5 mA  |
| <b>High Side Floating Supply</b>  |  |      |      |      |   |  |
| UV <sub>BS+</sub>   | High side well UVLO positive threshold   | 8.0  | 8.5  | 9.7  | V   |  |
| UV <sub>BS-</sub>   | High side well UVLO negative threshold   | 7.8  | 8.3  | 9.0  |   |  |
| UV <sub>BS</sub> HYS  | UV <sub>BS</sub> hysteresis  | -    | 0.2  | -    |   |  |
| I <sub>QBS</sub>  | High side quiescent current  | -    | -    | 1    | mA  |  |
| I <sub>LKH</sub>  | High to Low side leakage current   | -    | -    | 50   | μA  | V <sub>B</sub> =V <sub>S</sub> =200 V  |
| V <sub>CLAMPH</sub>   | High side zener diode clamp voltage  | 19.6 | 20.4 | 21.6 | V   | I <sub>BS</sub> =5 mA  |
| <b>Floating Input Supply</b>  |  |      |      |      |   |  |
| UV <sub>AA+</sub>   | VA+, VA- floating supply UVLO positive threshold from V <sub>SS</sub>                    | 8.2  | 8.7  | 9.7  | V   | V <sub>SS</sub> =0 V, GND pin floating   |
| UV <sub>AA-</sub>   | VA+, VA- floating supply UVLO negative threshold from V <sub>SS</sub>                    | 7.7  | 8.2  | 9.0  |   | V <sub>SS</sub> =0 V, GND pin floating   |
| UV <sub>AA</sub> HYS  | UV <sub>AA</sub> hysteresis  | -    | 0.5  | -    |   | V <sub>SS</sub> =0 V, GND pin floating   |
| I <sub>QAA0</sub>   | Floating Input positive quiescent supply current   | -    | 0.5  | 2    | mA  | V <sub>AA</sub> =10 V, V <sub>SS</sub> =0 V, V <sub>CSD</sub> =V <sub>SS</sub>                         |
| I <sub>QAA1</sub>   | Floating Input positive quiescent supply current   | -    | 6.5  | 11   |   | V <sub>AA</sub> =10 V, V <sub>SS</sub> =0 V, V <sub>CSD</sub> =V <sub>AA</sub> , T <sub>j</sub> = -40C |
|   |  | -    | 8    | 11   |   | V <sub>AA</sub> =10 V, V <sub>SS</sub> =0 V, V <sub>CSD</sub> =V <sub>AA</sub> , T <sub>j</sub> = 25C  |
|   |  | -    | 9.5  | 12.5 |   | V <sub>AA</sub> =10 V, V <sub>SS</sub> =0 V, V <sub>CSD</sub> =V <sub>AA</sub> , T <sub>j</sub> = 125C |
| I <sub>QAA2</sub>   | Floating Input positive quiescent supply current   | -    | 6.5  | 11   |   | V <sub>AA</sub> =10 V, V <sub>SS</sub> =0 V, V <sub>CSD</sub> =GND, T <sub>j</sub> = -40C              |
|   |  | -    | 8    | 11   |   | V <sub>AA</sub> =10 V, V <sub>SS</sub> =0 V, V <sub>CSD</sub> =GND, T <sub>j</sub> = 25C               |
|   |  | -    | 9.5  | 12.5 | V <sub>AA</sub> =10 V, V <sub>SS</sub> =0 V, V <sub>CSD</sub> =GND, T <sub>j</sub> = 125C |  |
| I <sub>LKM</sub>  | Floating input side to Low side leakage current  | -    | -    | 50   | μA  | V <sub>AA</sub> =V <sub>SS</sub> =V <sub>GND</sub> =100 V  |
| V <sub>CLAMPM+</sub>  | V <sub>AA</sub> floating supply zener diode clamp voltage, positive, with respect to GND | 6.0  | 7.0  | 8.0  | V   | I <sub>AA</sub> =5 mA, I <sub>SS</sub> =5 mA, V <sub>GND</sub> =0 V, V <sub>CSD</sub> =V <sub>SS</sub> |
| V <sub>CLAMPM-</sub>  | V <sub>SS</sub> floating supply zener diode clamp voltage, negative, with respect to GND | -8.0 | -7.0 | -6.0 |   | I <sub>AA</sub> =5 mA, I <sub>SS</sub> =5 mA, V <sub>GND</sub> =0 V, V <sub>CSD</sub> =V <sub>SS</sub> |
| <b>Audio Input (V<sub>GND</sub>=0, V<sub>AA</sub>=5V, V<sub>SS</sub>=-5V)</b> |  |      |      |      |   |  |
| V <sub>OS</sub>   | Input offset voltage   | -20  | 0    | 20   | mV  | T <sub>j</sub> = -40C  |
|   |  | -15  | 0    | 15   | mV  | T <sub>j</sub> = 25C   |
|   |  | -18  | 0    | 18   | mV  | T <sub>j</sub> = 125C  |
| I <sub>BIN</sub>  | Input bias current   | -    | -    | 40   | nA  |  |

|                       |   |                      |                      |                      |  |   |
|-----------------------|---|----------------------|----------------------|----------------------|--|---|
| BW                    | Small signal bandwidth  | -                    | 9                    | -                    | MHz  | $C_{COMP}=2\text{ nF}$ ,<br>$R_f=3.3\text{ k}\Omega$                        |
| $V_{COMP}$            | OTA Output voltage  | VAA-1                | -                    | VSS+1                | V  |   |
| $g_m$                 | OTA transconductance  | -                    | 100                  | -                    | mS   | $V_{IN}=10\text{ mV}$   |
| $G_v$                 | OTA gain  | 60                   | -                    | -                    | dB   |   |
| $V_{Nrms}$            | OTA input noise voltage   | -                    | 250                  | -                    | mVrms  | BW=20 kHz,<br>Resolution<br>BW=22 Hz<br>Fig.5                               |
| SR                    | Slew rate   | -                    | $\pm 5$              | -                    | V/us   | $C_{COMP}=1\text{ nF}$  |
| CMRR                  | Common-mode rejection ratio   | -                    | 60                   | -                    | dB   |   |
| PSRR                  | Supply voltage rejection ratio  | -                    | 65                   | -                    |  |   |
| <b>PWM comparator</b> |   |                      |                      |                      |  |   |
| $V_{thPwm}$           | PWM comparator threshold in COMP  | -                    | $(V_{AA}-V_{SS})/2$  | -                    | V  |   |
| $f_{OTA}$             | COMP pin star-up local oscillation frequency  | 0.7                  | 1.0                  | 1.3                  | MHz  | $V_{CSD} = GND$   |
| <b>Protection</b>     |   |                      |                      |                      |  |   |
| $V_{REF}$             | Reference output voltage  | 4.8                  | 5.1                  | 5.5                  | V  | $I_{OREF} = 0.5\text{ mA}$<br>OCSET=1.2 V,<br>Fig.6<br>$V_s=200\text{ V}$ , |
| $V_{thOCL}$           | Low side OC threshold in Vs   | 1.1                  | 1.2                  | 1.3                  |  |   |
| $V_{thOCH}$           | High side OC threshold in $V_{CSH}$   | 1.1+ Vs              | 1.2+ Vs              | 1.3+ Vs              |  |   |
| $V_{th1}$             | CSD pin shutdown release threshold  | $0.62 \times V_{DD}$ | $0.70 \times V_{DD}$ | $0.78 \times V_{DD}$ |  |   |
| $V_{th2}$             | CSD pin self reset threshold  | $0.26 \times V_{DD}$ | $0.30 \times V_{DD}$ | $0.34 \times V_{DD}$ |  |   |
| $I_{CSD+}$            | CSD pin discharge current   | 60                   | 100                  | 150                  | $\mu A$  | $V_{CSD} = V_{SS} + 5\text{ V}$<br>$V_{CSD} = V_{SS} + 5\text{ V}$          |
| $I_{CSD-}$            | CSD pin charge current  | 60                   | 100                  | 150                  |  |   |
| $t_{SD}$              | Shutdown propagation delay from $V_{CSD} > V_{SS} + V_{thOCH}$ to Shutdown                        | -                    | -                    | 250                  | ns   |   |
| $t_{OCH}$             | Propagation delay time from $V_{CSH} > V_{thOCH}$ to Shutdown                                     | -                    | -                    | 650                  |  | Fig.3   |
| $t_{OCL}$             | Propagation delay time from $V_s > V_{thOCL}$ to Shutdown   | -                    | -                    | 650                  |  | Fig.4   |
| <b>Gate Driver</b>    |   |                      |                      |                      |  |   |
| $I_{o+}$              | Output high short circuit current (Source)  | -                    | 1.0                  | -                    | A  | $V_o=0\text{ V}$ , $PW < 10\ \mu s$   |
| $I_{o-}$              | Output low short circuit current (Sink)   | -                    | 1.2                  | -                    | A  | $V_o=12\text{ V}$ , $PW < 10\ \mu s$  |
| $V_{OL}$              | Low level out put voltage<br>LO – COM, HO - VS  | -                    | -                    | 0.1                  | V  | $I_o=2\text{ mA}$   |
| $V_{OH}$              | High level out put voltage<br>VCC – LO, VB - HO   | -                    | -                    | 2.3                  |  |   |
| $t_{on}$              | High and low side turn-on propagation delay   | -                    | 360                  | -                    | ns   | $V_{DT} = V_{CC}$   |
| $t_{off}$             | High and low side turn-off propagation delay  | -                    | 335                  | -                    |  | $V_{DT} = V_{CC}$   |
| $t_r$                 | Turn-on rise time   | -                    | 20                   | 50                   |  |   |
| $t_f$                 | Turn-off fall time  | -                    | 15                   | 35                   |  |   |
| DT1                   | Deadtime: LO turn-off to HO turn-on ( $DT_{LO-HO}$ ) & HO turn-off to LO turn-on ( $DT_{HO-LO}$ ) | 5                    | 20                   | 35                   |  | $V_{DT} > V_{DT1}$ ,<br>$T_j = -40C$  |
|                       |   | 15                   | 25                   | 35                   |  | $V_{DT} > V_{DT1}$ ,<br>$T_j = 25C$   |
|                       |   | 20                   | 35                   | 50                   |  | $V_{DT} > V_{DT1}$ ,<br>$T_j = 125C$  |
| DT2                   | Deadtime: LO turn-off to HO turn-on ( $DT_{LO-HO}$ ) & HO turn-off to LO turn-on ( $DT_{HO-LO}$ ) | 20                   | 35                   | 55                   | $V_{DT1} > V_{DT} > V_{DT2}$ ,<br>$T_j = -40C$ |   |
|                       |   | 25                   | 40                   | 55                   | $V_{DT1} > V_{DT} > V_{DT2}$ ,<br>$T_j = 25C$  |   |
|                       |   | 30                   | 50                   | 70                   | $V_{DT1} > V_{DT} > V_{DT2}$ ,<br>$T_j = 125C$ |   |
| DT3                   | Deadtime: LO turn-off to HO turn-on ( $DT_{LO-HO}$ ) & HO turn-off to LO turn-on ( $DT_{HO-LO}$ ) | 40                   | 65                   | 95                   | $V_{DT2} > V_{DT} > V_{DT3}$ ,<br>$T_j = -40C$ |   |
|                       |   | 50                   | 65                   | 85                   | $V_{DT2} > V_{DT} > V_{DT3}$ ,<br>$T_j = 25C$  |   |

|           |  |               |               |               |   |  |
|-----------|--|---------------|---------------|---------------|---|--|
|           |  | 50            | 80            | 105           |   | $V_{DT2} > V_{DT} > V_{DT3}$ ,<br>$T_j = 125C$ |
| DT4       | Deadtime: LO turn-off to HO turn-on<br>( $DT_{LO-HO}$ ) & HO turn-off to LO turn-on<br>( $DT_{HO-LO}$ ) $V_{DT} = V_{DT4}$ | 65            | 110           | 150           |   | $V_{DT3} > V_{DT} > V_{DT4}$ ,<br>$T_j = -40C$ |
|           |  | 85            | 105           | 135           |   | $V_{DT3} > V_{DT} > V_{DT4}$ ,<br>$T_j = 25C$  |
|           |  | 80            | 115           | 155           |   | $V_{DT3} > V_{DT} > V_{DT4}$ ,<br>$T_j = 125C$ |
|           |  |               |               |               |   |  |
| $V_{DT1}$ | DT mode select threshold 2   | $0.51xV_{cc}$ | $0.57xV_{cc}$ | $0.63xV_{cc}$ | V |  |
| $V_{DT2}$ | DT mode select threshold 3   | $0.32xV_{cc}$ | $0.36xV_{cc}$ | $0.40xV_{cc}$ |   |  |
| $V_{DT3}$ | DT mode select threshold 4   | $0.21xV_{cc}$ | $0.23xV_{cc}$ | $0.25xV_{cc}$ |   |  |

Waveform Definitions

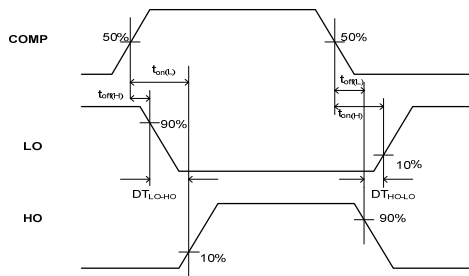


Figure 1: Switching Time Waveform Definitions

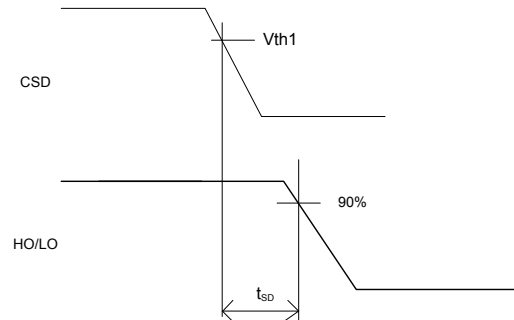


Figure 2: CSD to Shutdown Waveform Definitions

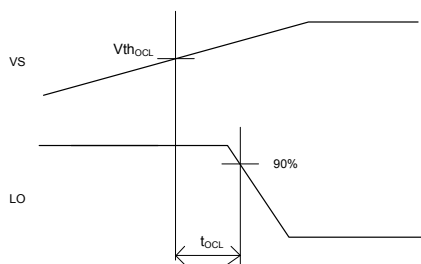


Figure 3:  $V_S > V_{thOCL}$  to Shutdown Waveform

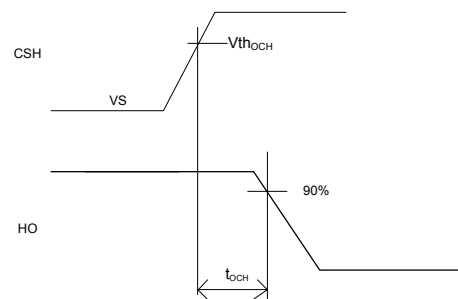


Figure 4:  $V_{CSH} > V_{thOCH}$  to Shutdown Waveform

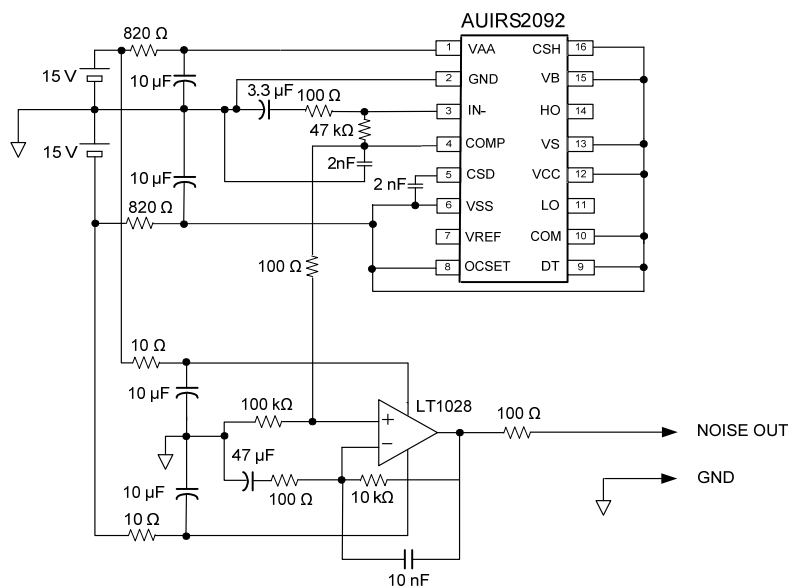
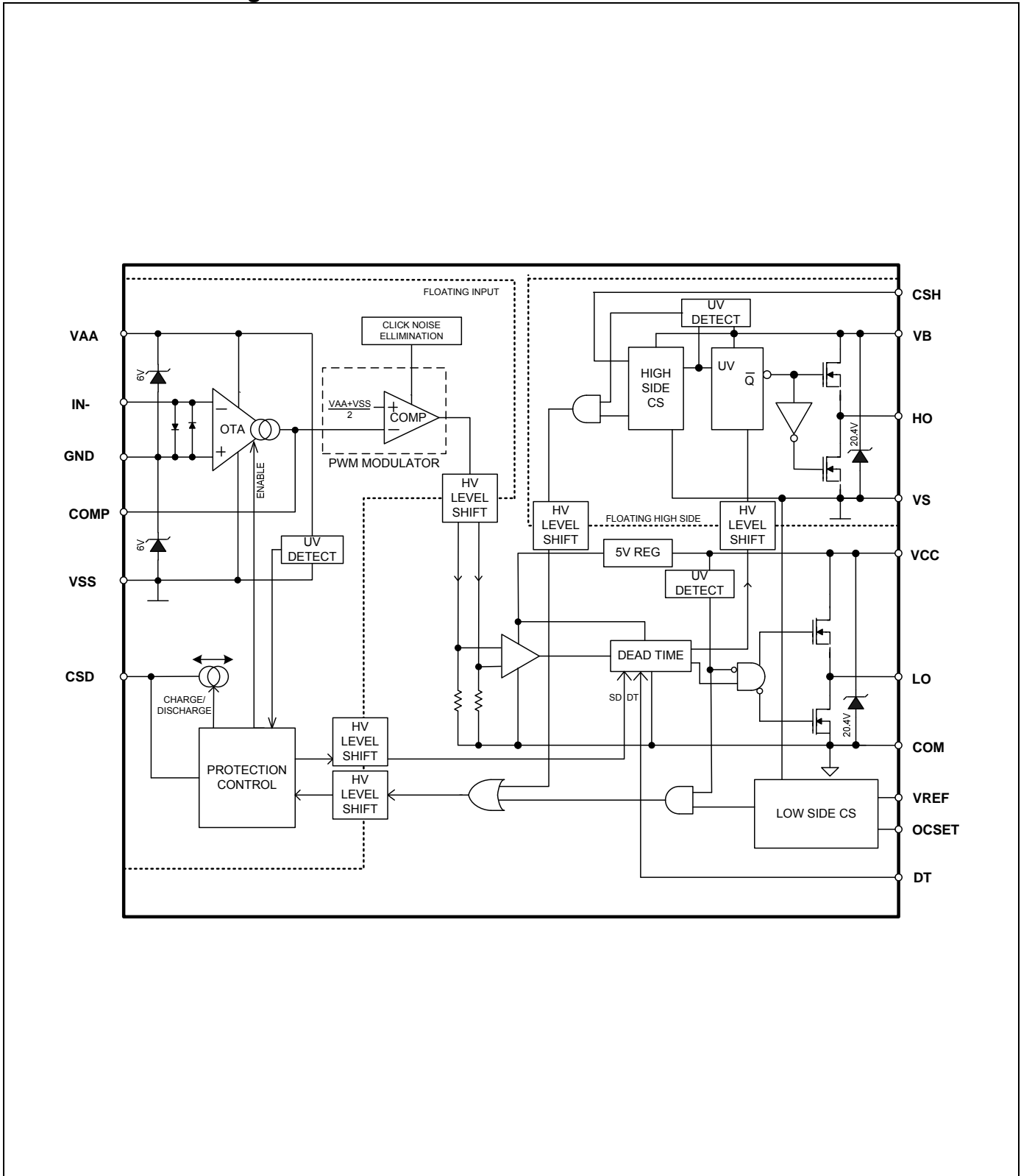
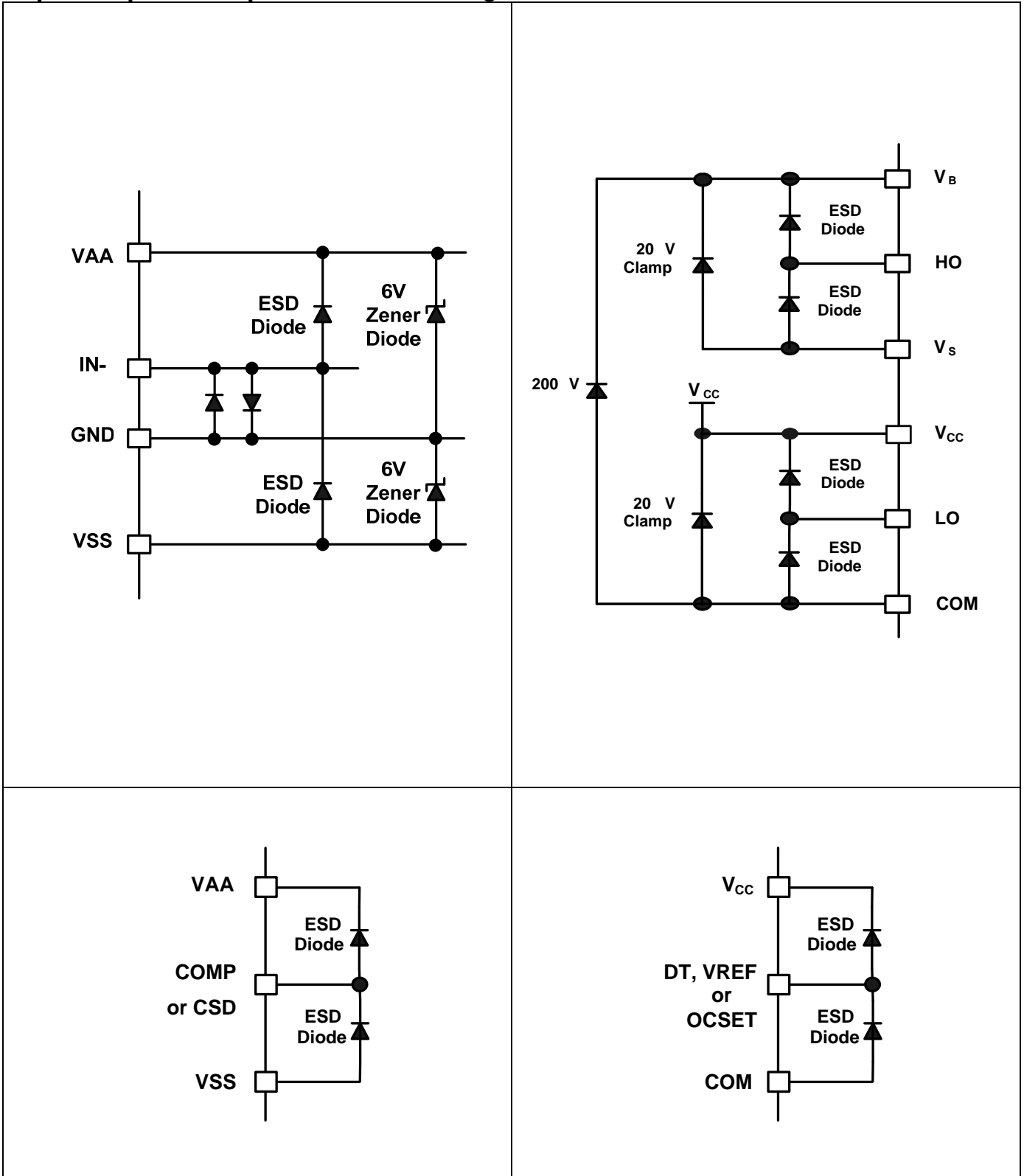


Figure 5: OTA input noise voltage measurement circuit

**Functional Block Diagram: AUIRS2092**



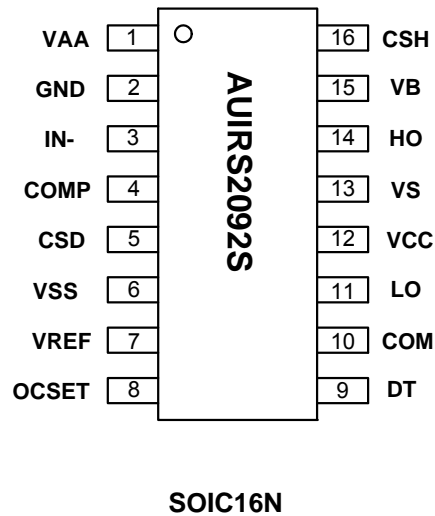
**Input/Output Pin Equivalent Circuit Diagrams: AUIRS2092**



**Lead Definitions: AUIRS2092**

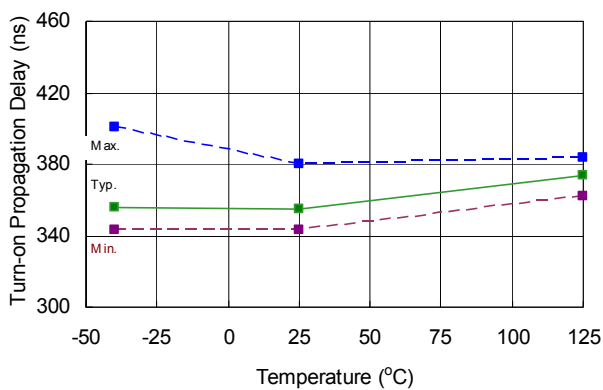
| Pin # | Symbol | Description                                |
|-------|--------|--|
| 1     | VAA    | Floating input positive supply             |
| 2     | GND    | Floating input supply return               |
| 3     | IN-    | Analog inverting input                     |
| 4     | COMP   | Phase compensation input, comparator input |
| 5     | CSD    | Shutdown timing capacitor                  |
| 6     | VSS    | Floating input negative supply             |
| 7     | VREF   | 5V reference voltage to program OCSET pin  |
| 8     | OCSET  | Low side over current threshold setting    |
| 9     | DT     | Deadtime program input                     |
| 10    | COM    | Low side supply return                     |
| 11    | LO     | Low side output                            |
| 12    | VCC    | Low side supply                            |
| 13    | VS     | High side floating supply return           |
| 14    | HO     | High side output                           |
| 15    | VB     | High side floating supply                  |
| 16    | CSH    | High side over current sensing input       |

**Lead Assignments**

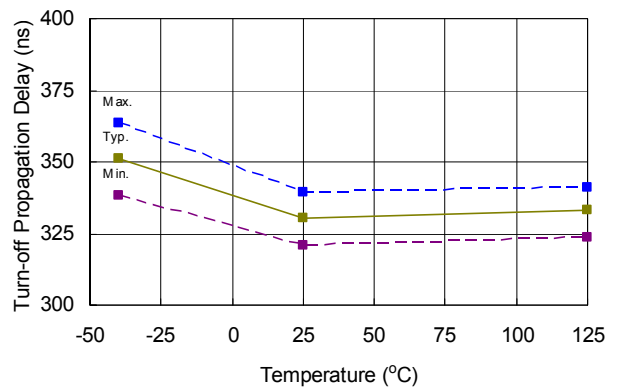


**Parameter Temperature Trends**

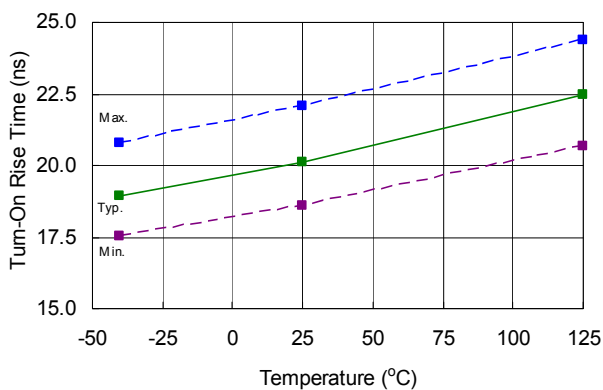
Figures illustrated in this chapter provide information on the experimental performance of the AUIRS2092S HVIC. The line plotted in each figure is generated from actual lab data. A large number of individual samples were tested at three temperatures (-40 °C, 25 °C, and 125 °C) in order to generate the experimental curve. The line consists of three data points (one data point at each of the tested temperatures) that have been connected together to illustrate the understood trend. The individual data points on the Typ. curve were determined by calculating the averaged experimental value of the parameter (for a given temperature).



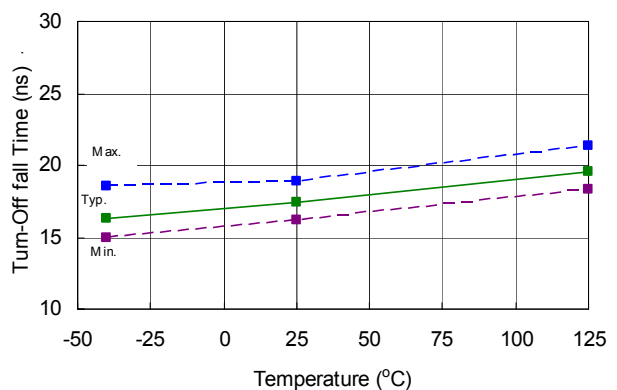
**Figure 6:  $t_{ON}$  vs. temperature**



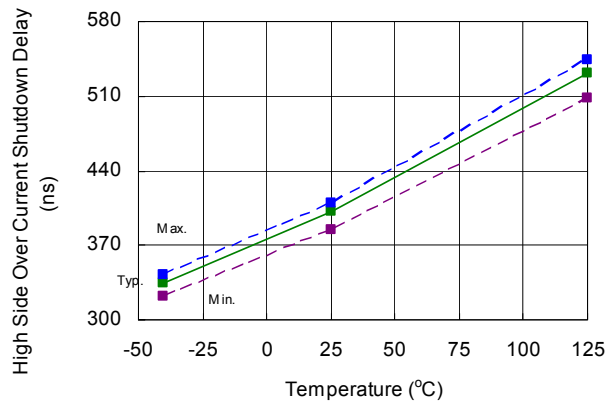
**Figure 7:  $t_{OFF}$  vs. temperature**



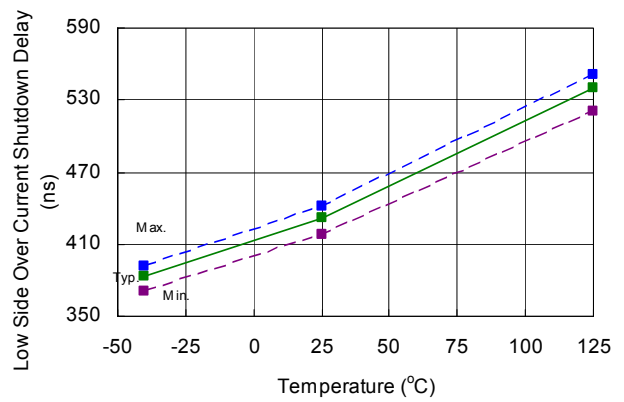
**Figure 8:  $T_R$  vs. temperature**



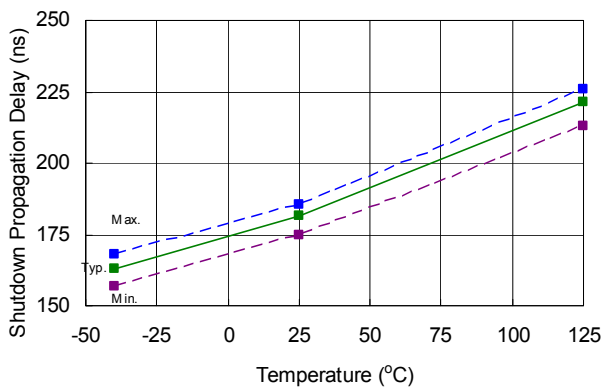
**Figure 9:  $T_F$  vs. temperature**



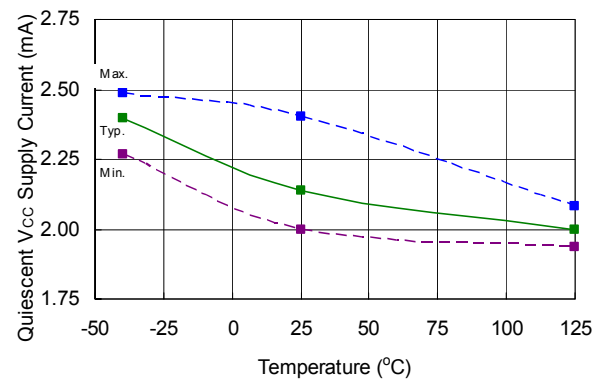
**Figure 10:  $T_{OCH}$  vs. temperature**



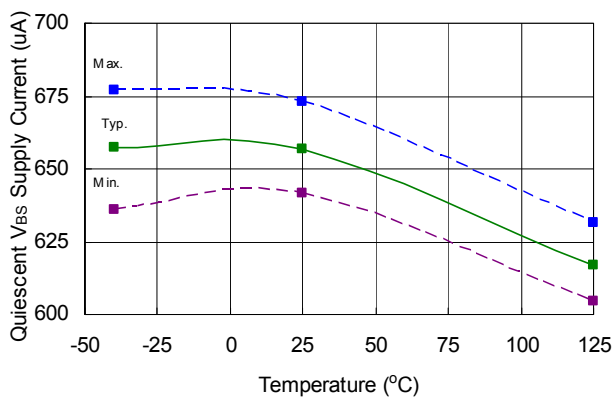
**Figure 11:  $T_{OCL}$  vs. temperature**



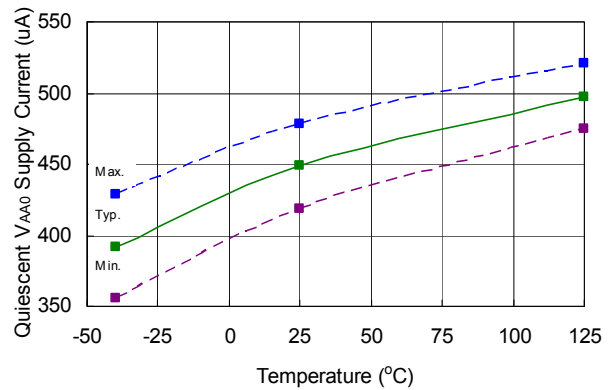
**Figure 12:  $T_{SD}$  vs. temperature**



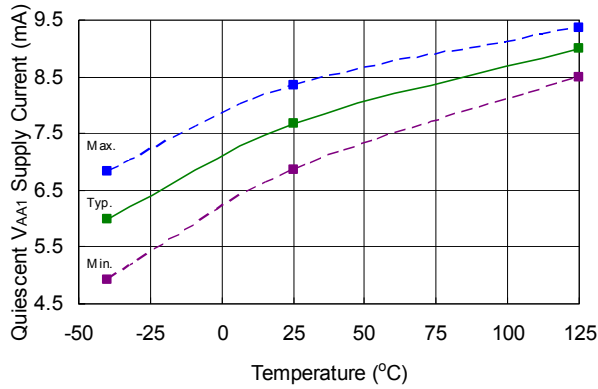
**Figure 13:  $I_{QCC}$  vs. temperature**



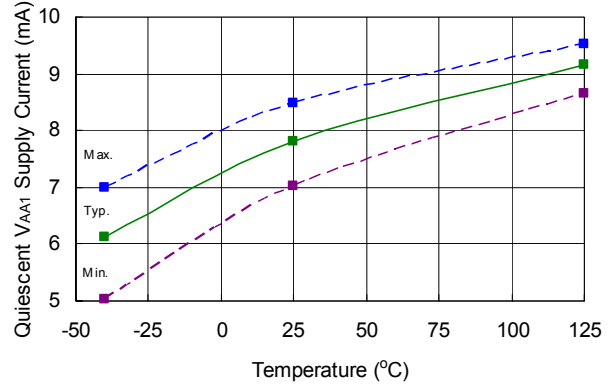
**Figure 14:  $I_{QBS}$  vs. temperature**



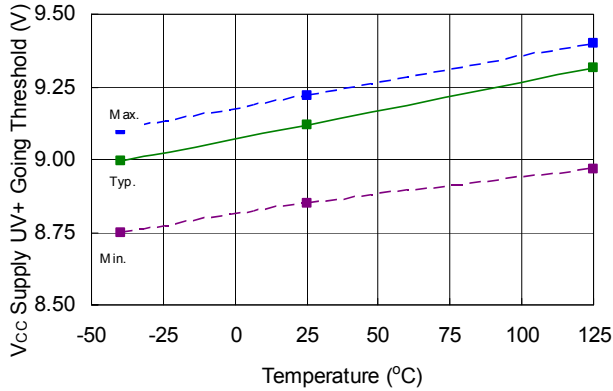
**Figure 15:  $I_{QAA0}$  vs. temperature**



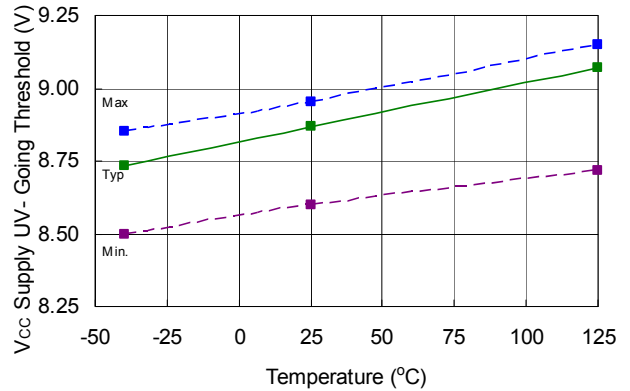
**Figure 16:  $I_{QAA1}$  vs. temperature**



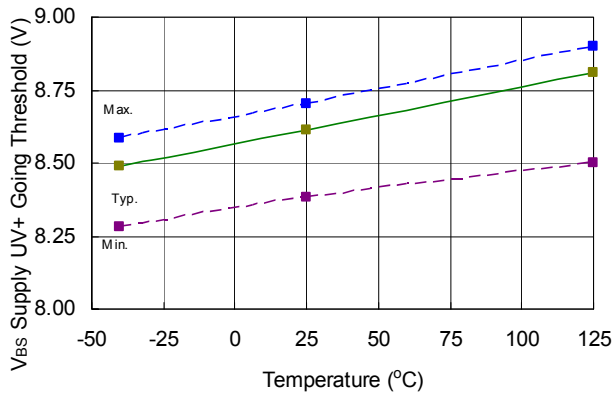
**Figure 17:  $I_{QAA2}$  vs. temperature**



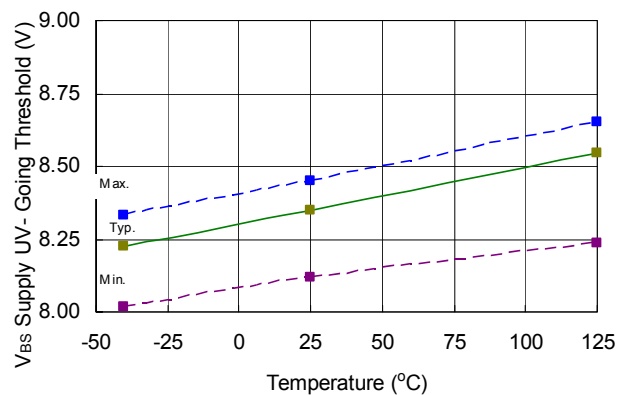
**Figure 18:  $V_{CCUV+}$  vs. temperature**



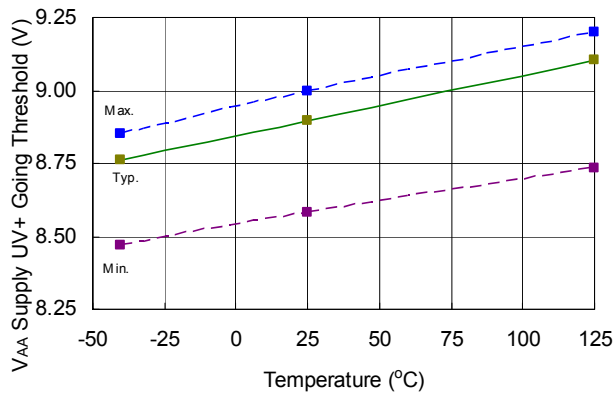
**Figure 19:  $V_{CCUV-}$  vs. temperature**



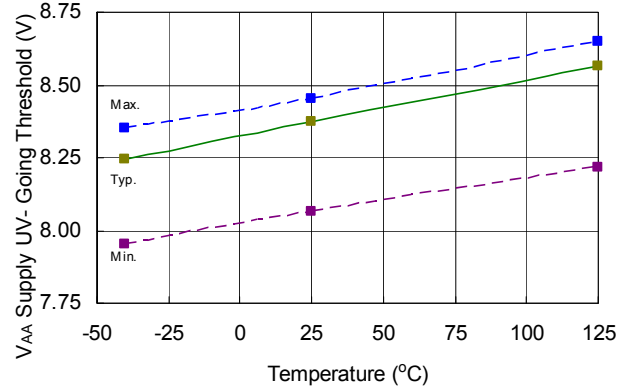
**Figure 20:  $V_{BSUV+}$  vs. temperature**



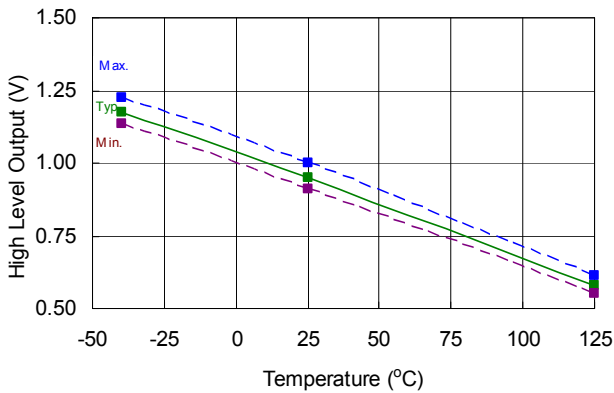
**Figure 21:  $V_{BSUV-}$  vs. temperature**



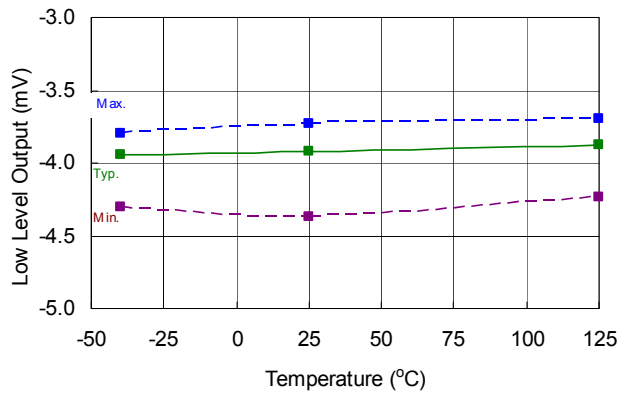
**Figure 22:  $V_{AAUV+}$  vs. temperature**



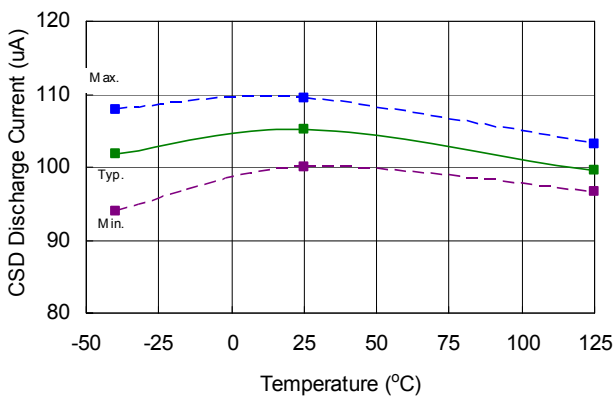
**Figure 23:  $V_{AAUV-}$  vs. temperature**



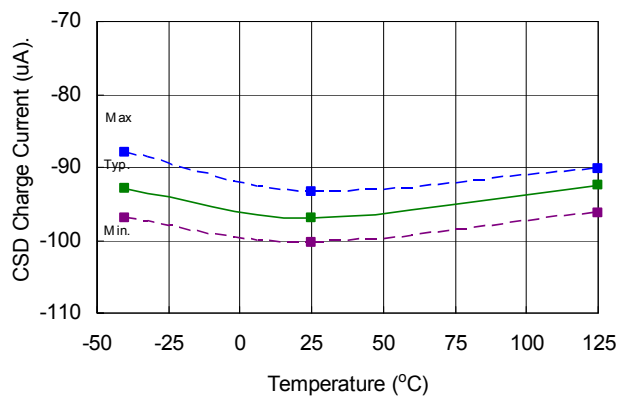
**Figure 24:  $V_{OH}$  ( $I_O = 0A$ ) vs. temperature**



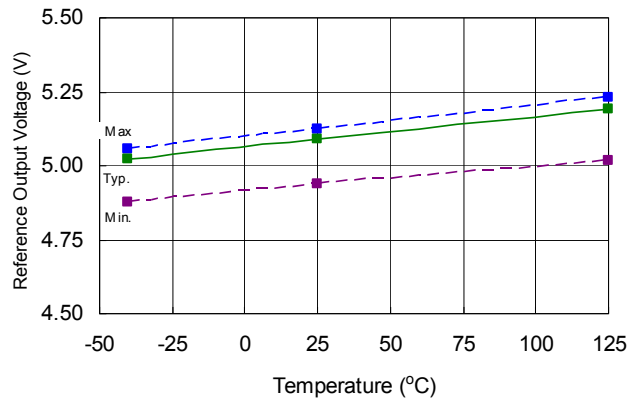
**Figure 25:  $V_{OL}$  ( $I_O = 0A$ ) vs. temperature**



**Figure 26:  $I_{CSD+}$  vs. temperature**

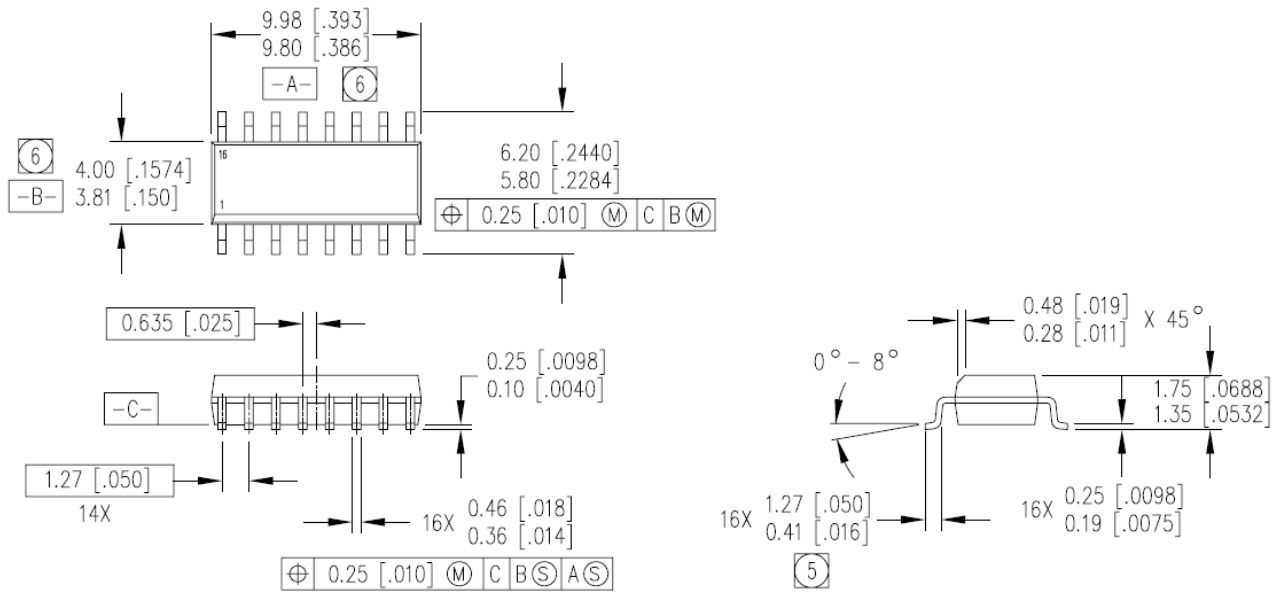


**Figure 27:  $I_{CSD-}$  vs. temperature**



**Figure 28: V<sub>REF</sub> vs. temperature**

**Package Details: SOIC16N**

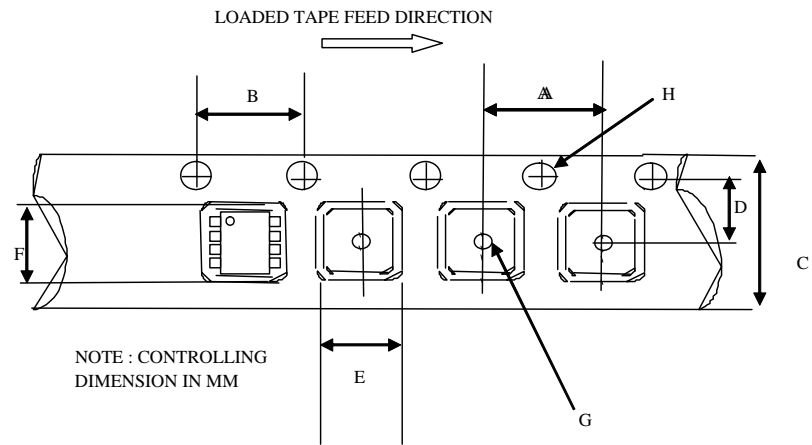


**NOTES:**

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AC.

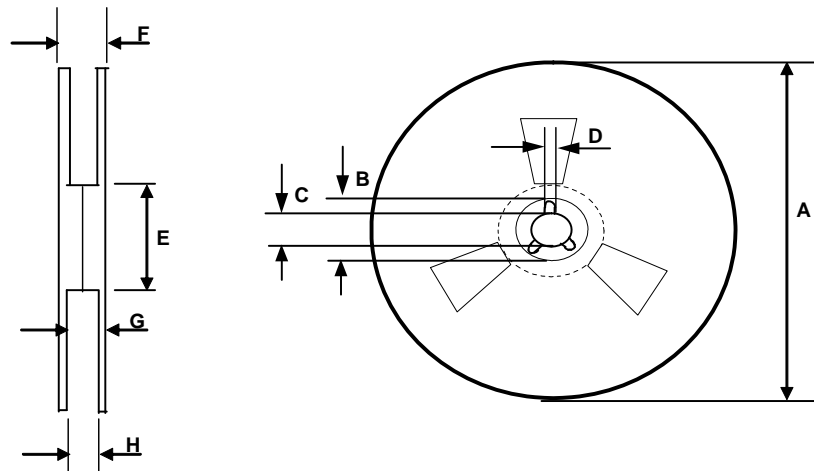
- (5) DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.
- (6) DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.15 [.006].

**Tape and Reel Details: SOIC16N**



CARRIER TAPE DIMENSION FOR 16SOICN

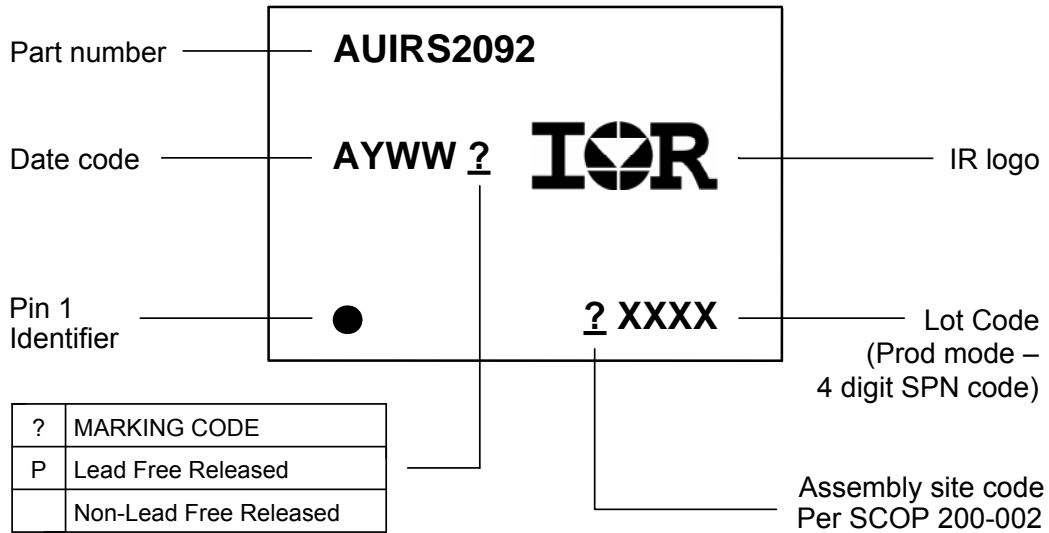
| Code | Metric |       | Imperial |       |
|------|--------|-------|----------|-------|
|      | Min    | Max   | Min      | Max   |
| A    | 7.90   | 8.10  | 0.311    | 0.318 |
| B    | 3.90   | 4.10  | 0.153    | 0.161 |
| C    | 15.70  | 16.30 | 0.618    | 0.641 |
| D    | 7.40   | 7.60  | 0.291    | 0.299 |
| E    | 6.40   | 6.60  | 0.252    | 0.260 |
| F    | 10.20  | 10.40 | 0.402    | 0.409 |
| G    | 1.50   | n/a   | 0.059    | n/a   |
| H    | 1.50   | 1.60  | 0.059    | 0.062 |



REEL DIMENSIONS FOR 16SOICN

| Code | Metric |        | Imperial |        |
|------|--------|--------|----------|--------|
|      | Min    | Max    | Min      | Max    |
| A    | 329.60 | 330.25 | 12.976   | 13.001 |
| B    | 20.95  | 21.45  | 0.824    | 0.844  |
| C    | 12.80  | 13.20  | 0.503    | 0.519  |
| D    | 1.95   | 2.45   | 0.767    | 0.096  |
| E    | 98.00  | 102.00 | 3.858    | 4.015  |
| F    | n/a    | 22.40  | n/a      | 0.881  |
| G    | 18.50  | 21.10  | 0.728    | 0.830  |
| H    | 16.40  | 18.40  | 0.645    | 0.724  |

**Part Marking Information**



**Ordering Information**

| Base Part Number | Package Type | Standard Pack |          | Complete Part Number |
|------------------|--------------|---------------|----------|----------------------|
|                  |              | Form          | Quantity |                      |
| AUIRS2092        | SOIC16N      | Tube/Bulk     | 45       | AUIRS2092S           |
|                  |              | Tape and Reel | 2500     | AUIRS2092STR         |

**IMPORTANT NOTICE**

Unless specifically designated for the automotive market, International Rectifier Corporation and its subsidiaries (IR) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or services without notice. Part numbers designated with the "AU" prefix follow automotive industry and / or customer specific requirements with regards to product discontinuance and process change notification. All products are sold subject to IR's terms and conditions of sale supplied at the time of order acknowledgment.

IR warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with IR's standard warranty. Testing and other quality control techniques are used to the extent IR deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

IR assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using IR components. To minimize the risks with customer products and applications, customers should provide adequate design and operating safeguards.

Reproduction of IR information in IR data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alterations is an unfair and deceptive business practice. IR is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of IR products or serviced with statements different from or beyond the parameters stated by IR for that product or service voids all express and any implied warranties for the associated IR product or service and is an unfair and deceptive business practice. IR is not responsible or liable for any such statements.

IR products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or in other applications intended to support or sustain life, or in any other application in which the failure of the IR product could create a situation where personal injury or death may occur. Should Buyer purchase or use IR products for any such unintended or unauthorized application, Buyer shall indemnify and hold International Rectifier and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that IR was negligent regarding the design or manufacture of the product.

IR products are neither designed nor intended for use in military/aerospace applications or environments unless the IR products are specifically designated by IR as military-grade or "enhanced plastic." Only products designated by IR as military-grade meet military specifications. Buyers acknowledge and agree that any such use of IR products which IR has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

IR products are neither designed nor intended for use in automotive applications or environments unless the specific IR products are designated by IR as compliant with ISO/TS 16949 requirements and bear a part number including the designation "AU". Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, IR will not be responsible for any failure to meet such requirements.

For technical support, please contact IR's Technical Assistance Center  
<http://www.irf.com/technical-info/>

**WORLD HEADQUARTERS:**  
101 N. Sepulveda Blvd., El Segundo, California 90245  
Tel: (310) 252-7105

**Revision History**

| Date           | Comment  |
|----------------|--|
| April 30, 2010 | Converted from Industrial version  |
| Aug. 5, 2010   | Added tri-temp graphs;   |
| Aug. 23, 2010  | Updated Iqaa1,2,VOH,VOL,DT1,2,3,4, TOCH,TOCL,VOS, ICSD+/-, VREF, UVAA/CC/BS+/-; added Iqaa1-25,Iqaa2-25,DT1,2,3,4-25 parameters. |
| Sep. 1, 2010   | Corrected DT1-25 max to 35. Added ESD and latchup classification   |
| Jan. 19, 2011  | Updated DT1-to-4, Vos, Iqaa1,2 tri-temp spec   |
| Jan. 20, 2011  | Added leadfree and automotive grade heading  |
| Jan. 21, 2011  | Added typical for IO on front page, merged DT,Vos, Iqaa repeated descriptions.   |
| Mar. 11,2011   | Changed notice address   |
|                |  |
|                |  |
|                |  |

# Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[Infineon:](#)

[AUIRS2092STR](#)