



October 2014

FDMS86201

N-Channel Shielded Gate PowerTrench[®] MOSFET

120 V, 49 A, 11.5 mΩ

Features

- Shielded Gate MOSFET Technology
- Max $r_{DS(on)}$ = 11.5 mΩ at $V_{GS} = 10\text{ V}$, $I_D = 11.6\text{ A}$
- Max $r_{DS(on)}$ = 14.5 mΩ at $V_{GS} = 6\text{ V}$, $I_D = 10.7\text{ A}$
- Advanced Package and Silicon combination for low $r_{DS(on)}$ and high efficiency
- MSL1 robust package design
- 100% UIL tested
- RoHS Compliant

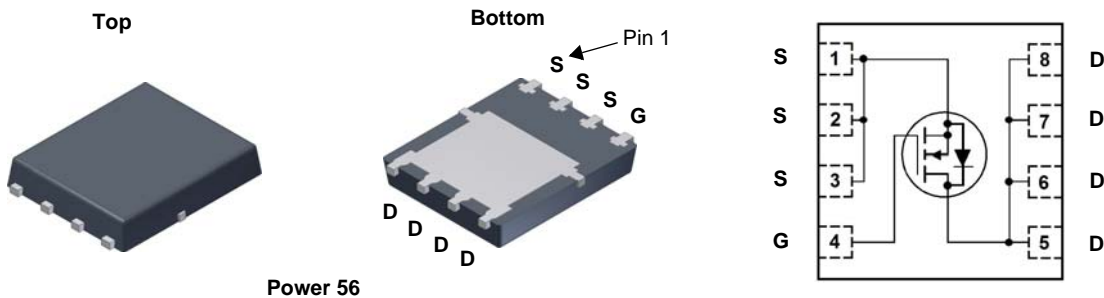


General Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench[®] process that incorporates Shielded Gate technology. This process has been optimized for the on-state resistance and yet maintain superior switching performance.

Application

- DC-DC Conversion



Power 56

MOSFET Maximum Ratings $T_A = 25\text{ °C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DS}	Drain to Source Voltage	120	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Current -Continuous $T_C = 25\text{ °C}$	49	A
	-Continuous $T_A = 25\text{ °C}$ (Note 1a)	11.6	
	-Pulsed	160	
E_{AS}	Single Pulse Avalanche Energy (Note 3)	264	mJ
P_D	Power Dissipation $T_C = 25\text{ °C}$	104	W
	Power Dissipation $T_A = 25\text{ °C}$ (Note 1a)	2.5	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.2	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	50	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS86201	FDMS86201	Power 56	13 "	12 mm	3000 units

Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}$, $V_{GS} = 0\text{ V}$	120			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, referenced to $25\text{ }^\circ\text{C}$		95		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 96\text{ V}$, $V_{GS} = 0\text{ V}$			1	μA
I_{GSS}	Gate to Source Leakage Current, Forward	$V_{GS} = \pm 20\text{ V}$, $V_{DS} = 0\text{ V}$			100	nA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\text{ }\mu\text{A}$	2.0	2.6	4.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, referenced to $25\text{ }^\circ\text{C}$		-10		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}$, $I_D = 11.6\text{ A}$		9.6	11.5	m Ω
		$V_{GS} = 6\text{ V}$, $I_D = 10.7\text{ A}$		11.8	14.5	
		$V_{GS} = 10\text{ V}$, $I_D = 11.6\text{ A}$, $T_J = 125\text{ }^\circ\text{C}$		15.7	21.5	
g_{FS}	Forward Transconductance	$V_{DS} = 10\text{ V}$, $I_D = 11.6\text{ A}$		39		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 60\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$		2056	2735	pF
C_{oss}	Output Capacitance			322	430	pF
C_{riss}	Reverse Transfer Capacitance			15	25	pF
R_g	Gate Resistance			1.2		Ω

Switching Characteristics

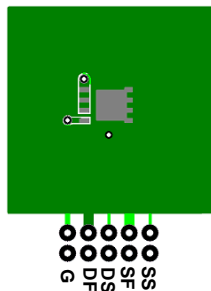
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 60\text{ V}$, $I_D = 11.6\text{ A}$, $V_{GS} = 10\text{ V}$, $R_{GEN} = 6\text{ }\Omega$		13	24	ns	
t_r	Rise Time			7.7	16	ns	
$t_{d(off)}$	Turn-Off Delay Time			27	44	ns	
t_f	Fall Time			7.1	15	ns	
Q_g	Total Gate Charge		$V_{GS} = 0\text{ V to }10\text{ V}$		32	46	nC
Q_g	Total Gate Charge	$V_{GS} = 0\text{ V to }5\text{ V}$	$V_{DD} = 60\text{ V}$, $I_D = 11.6\text{ A}$		18	26	nC
Q_{gs}	Gate to Source Charge				8.1		nC
Q_{gd}	Gate to Drain "Miller" Charge				7.1		nC

Drain-Source Diode Characteristics

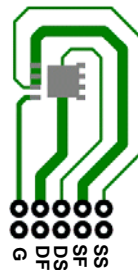
V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}$, $I_S = 2\text{ A}$ (Note 2)		0.69	1.2	V
		$V_{GS} = 0\text{ V}$, $I_S = 11.6\text{ A}$ (Note 2)		0.78	1.3	
t_{rr}	Reverse Recovery Time	$I_F = 11.6\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$		66	106	ns
Q_{rr}	Reverse Recovery Charge			88	140	nC

Notes:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a $1.5 \times 1.5\text{ in.}$ board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) $50\text{ }^\circ\text{C/W}$ when mounted on a 1 in^2 pad of 2 oz copper



b) $125\text{ }^\circ\text{C/W}$ when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width $< 300\text{ }\mu\text{s}$, Duty cycle $< 2.0\%$.

3. Starting $T_J = 25\text{ }^\circ\text{C}$; N-ch: $L = 1\text{ mH}$, $I_{AS} = 23\text{ A}$, $V_{DD} = 120\text{ V}$, $V_{GS} = 10\text{ V}$. 100% test at $L = 0.1\text{ mH}$, $I_{AS} = 50\text{ A}$.

Typical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

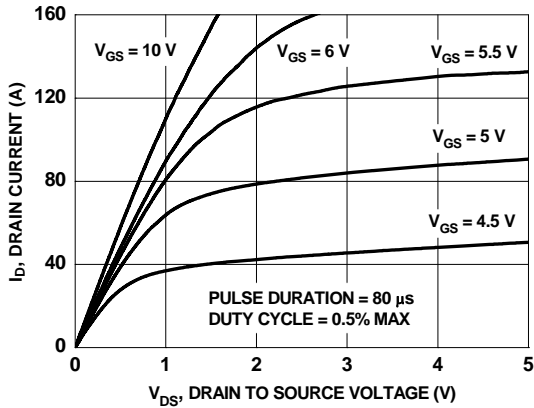


Figure 1. On Region Characteristics

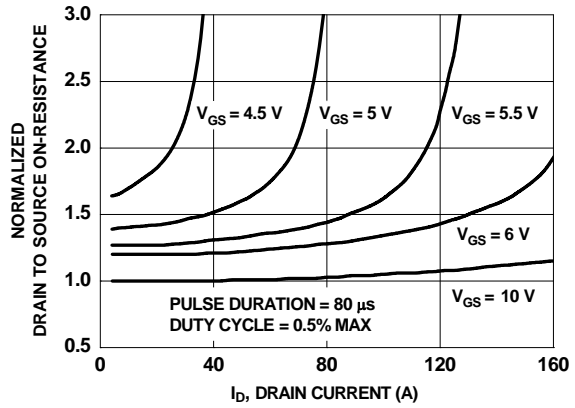


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

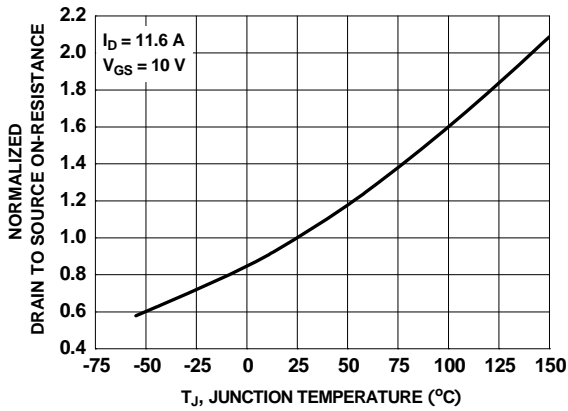


Figure 3. Normalized On Resistance vs Junction Temperature

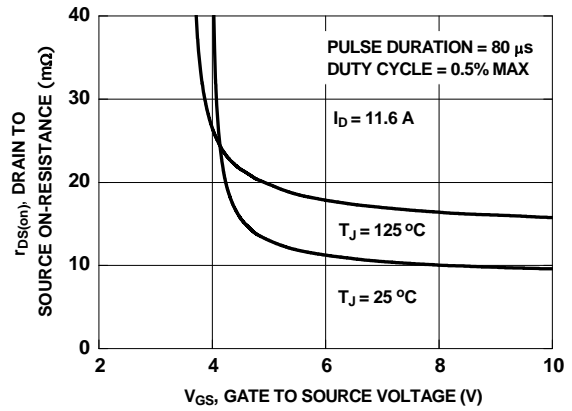


Figure 4. On-Resistance vs Gate to Source Voltage

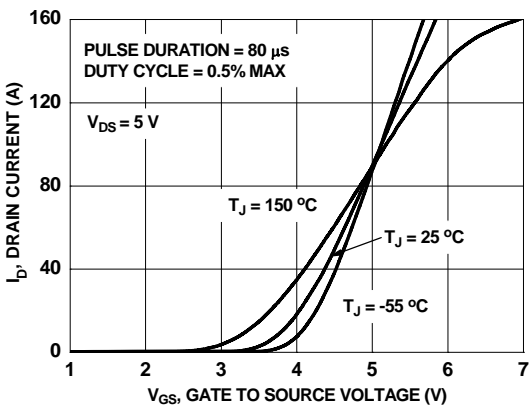


Figure 5. Transfer Characteristics

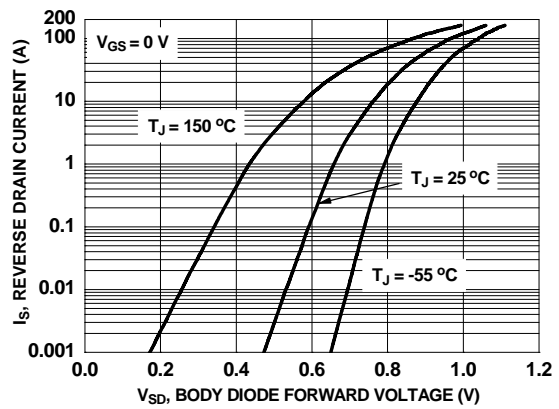


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

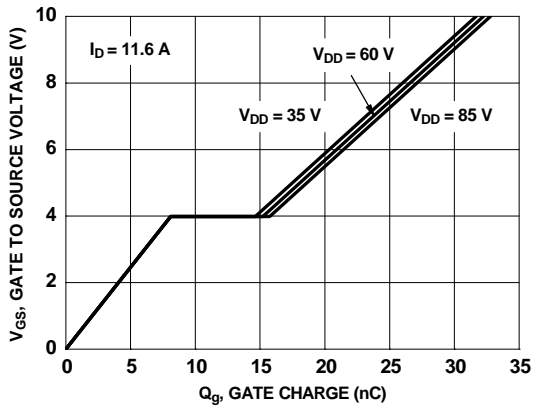


Figure 7. Gate Charge Characteristics

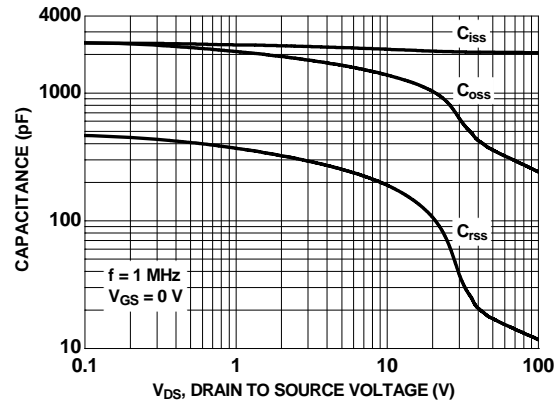


Figure 8. Capacitance vs Drain to Source Voltage

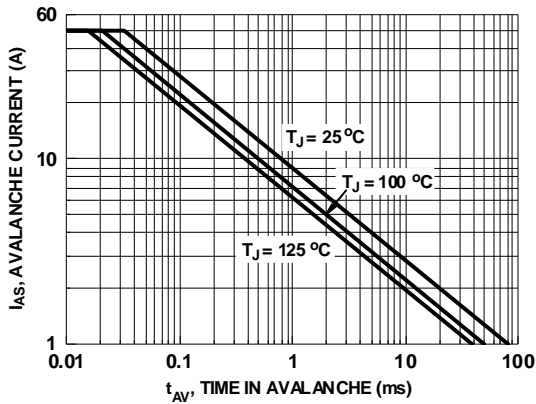


Figure 9. Unclamped Inductive Switching Capability

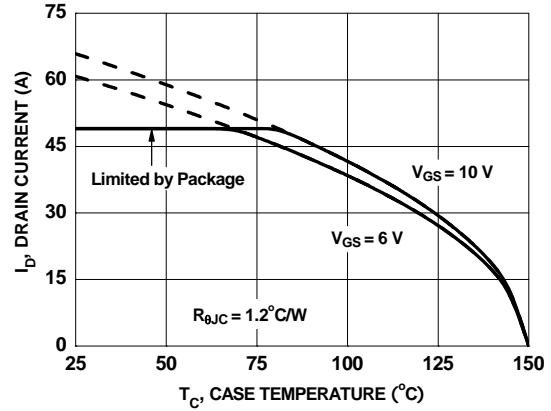


Figure 10. Maximum Continuous Drain Current vs Case Temperature

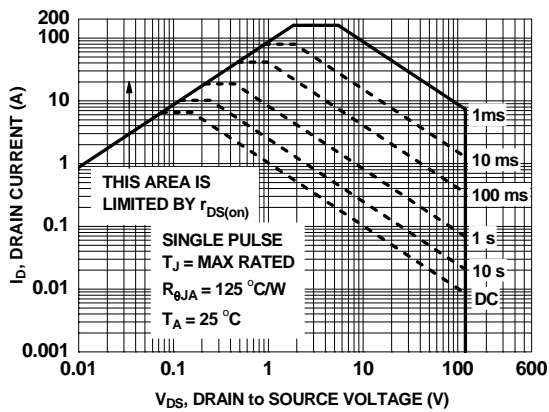


Figure 11. Forward Bias Safe Operating Area

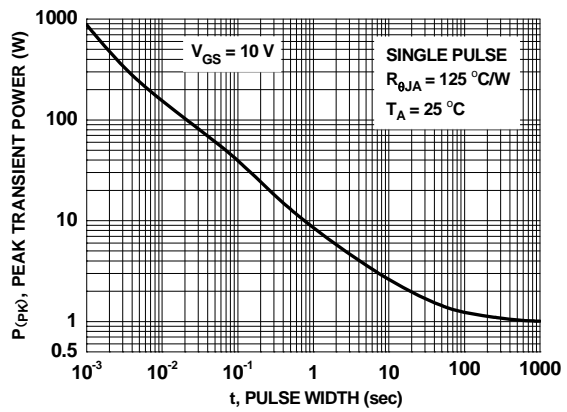


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

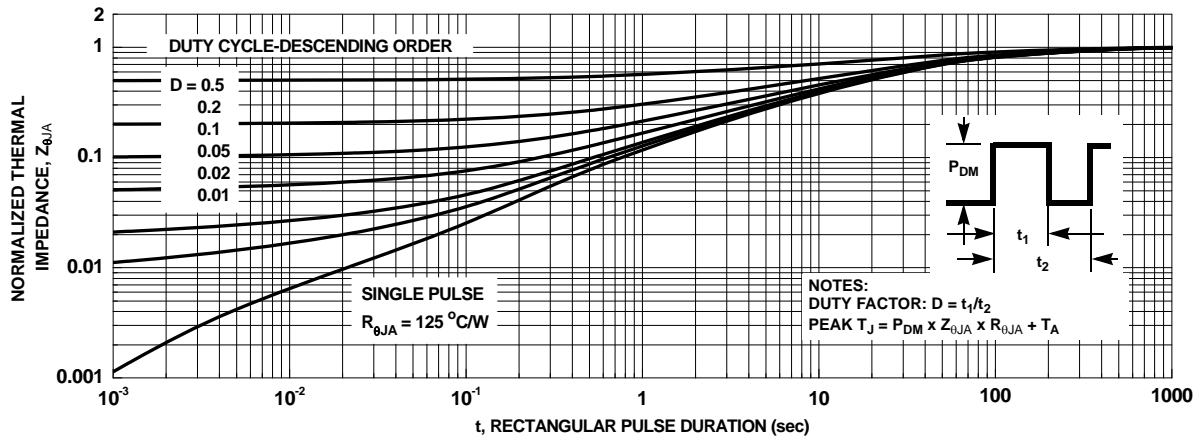
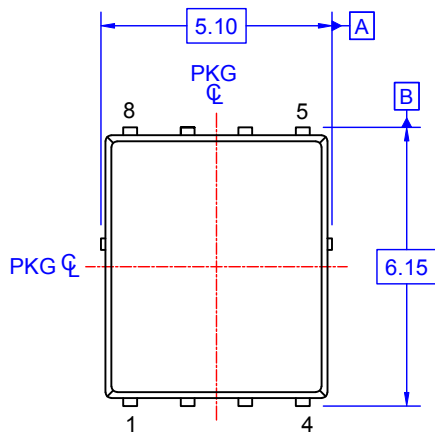
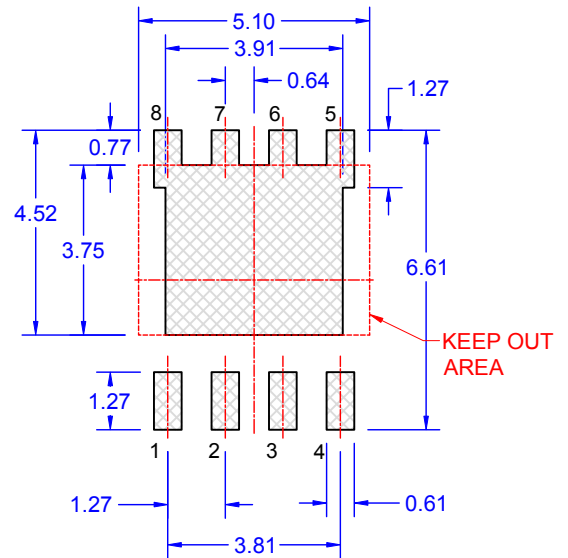
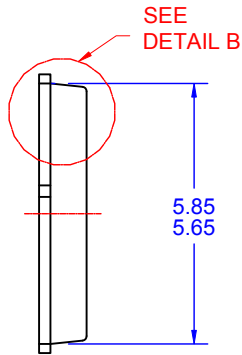


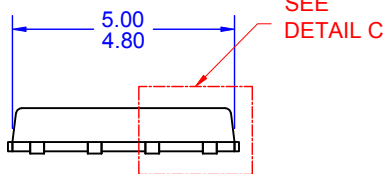
Figure 13. Junction-to-Ambient Transient Thermal Response Curve



TOP VIEW

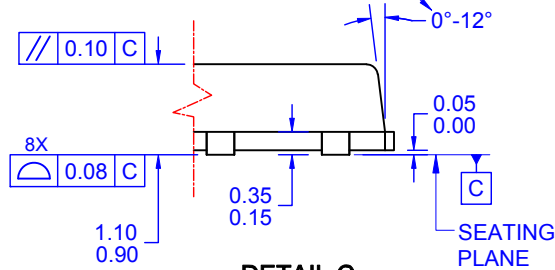


LAND PATTERN RECOMMENDATION



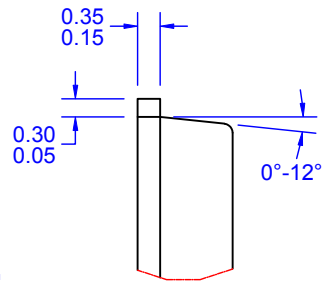
SIDE VIEW

OPTIONAL DRAFT ANGLE MAY APPEAR ON FOUR SIDES OF THE PACKAGE



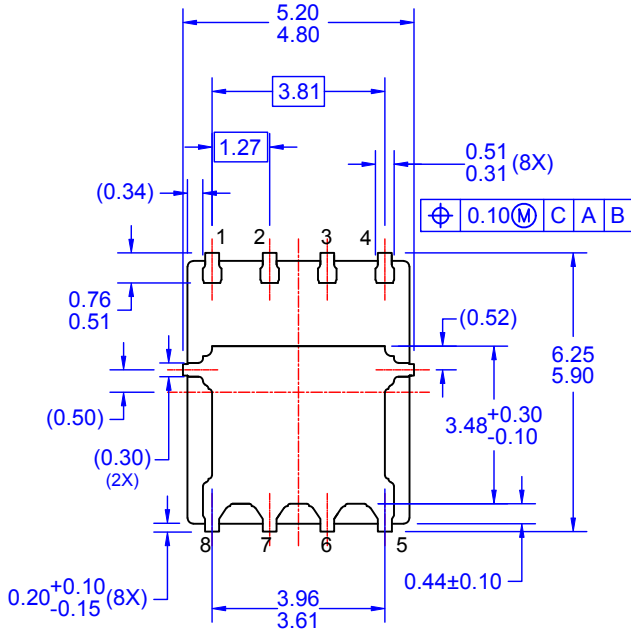
DETAIL C

SCALE: 2:1



DETAIL B

SCALE: 2:1



BOTTOM VIEW

NOTES: UNLESS OTHERWISE SPECIFIED

- A. PACKAGE STANDARD REFERENCE: JEDEC MO-240, ISSUE A, VAR. AA, DATED OCTOBER 2002.
- B. DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
- C. ALL DIMENSIONS ARE IN MILLIMETERS.
- D. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
- E. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.
- F. DRAWING FILE NAME: PQFN08AREV9





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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

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