



June 2014

# FQA160N08

## N-Channel QFET<sup>®</sup> MOSFET

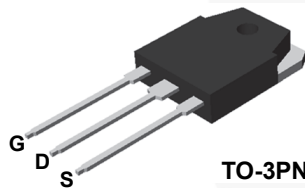
80 V, 160 A, 7 mΩ

### Description

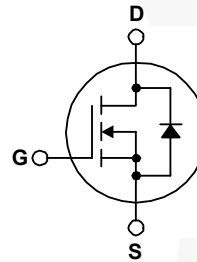
This N-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, audio amplifier, DC motor control, and variable switching power applications.

### Features

- 160 A, 80 V,  $R_{DS(on)} = 7 \text{ m}\Omega$  (Max.) @  $V_{GS} = 10 \text{ V}$ ,  $I_D = 80 \text{ A}$
- Low Gate Charge (Typ. 220 nC)
- Low Crss (Typ. 530 pF)
- 100% Avalanche Tested
- 175°C Maximum Junction Temperature Rating



TO-3PN



### Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	FQA160N08	Unit
$V_{DSS}$	Drain-Source Voltage	80	V
$I_D$	Drain Current - Continuous ( $T_C = 25^\circ\text{C}$ ) - Continuous ( $T_C = 100^\circ\text{C}$ )	160	A
		113	A
$I_{DM}$	Drain Current - Pulsed (Note 1)	640	A
$V_{GSS}$	Gate-Source Voltage	$\pm 25$	V
$E_{AS}$	Single Pulsed Avalanche Energy (Note 2)	1600	mJ
$I_{AR}$	Avalanche Current (Note 1)	160	A
$E_{AR}$	Repetitive Avalanche Energy (Note 1)	37.5	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	6.5	V/ns
$P_D$	Power Dissipation ( $T_C = 25^\circ\text{C}$ ) - Derate above $25^\circ\text{C}$	375	W
		2.5	W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +175	$^\circ\text{C}$
$T_L$	Maximum lead temperature for soldering, 1/8" from case for 5 seconds.	300	$^\circ\text{C}$

### Thermal Characteristics

Symbol	Parameter	FQA160N08	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	0.4	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max.	40	$^\circ\text{C}/\text{W}$

FQA160N08 — N-Channel QFET<sup>®</sup> MOSFET

## Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FQA160N08	FQA160N08	TO-3PN	Tube	N/A	N/A	30 units

## Electrical Characteristics

$T_C = 25^\circ\text{C}$  unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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### Off Characteristics

$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	80	--	--	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$	--	0.08	--	$V/^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 80\text{ V}, V_{GS} = 0\text{ V}$	--	--	1	$\mu\text{A}$
		$V_{DS} = 64\text{ V}, T_C = 150^\circ\text{C}$	--	--	10	$\mu\text{A}$
$I_{GSSF}$	Gate-Body Leakage Current, Forward	$V_{GS} = 25\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA
$I_{GSSR}$	Gate-Body Leakage Current, Reverse	$V_{GS} = -25\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA

### On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	2.0	--	4.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 80\text{ A}$	--	0.0056	0.007	$\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 30\text{ V}, I_D = 80\text{ A}$	--	92	--	S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	6100	7900	pF
$C_{oss}$	Output Capacitance		--	2400	3100	pF
$C_{rss}$	Reverse Transfer Capacitance		--	530	690	pF

### Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 40\text{ V}, I_D = 160\text{ A},$ $R_G = 25\ \Omega$	--	85	180	ns	
$t_r$	Turn-On Rise Time		--	970	2000	ns	
$t_{d(off)}$	Turn-Off Delay Time		(Note4)	--	260	530	ns
$t_f$	Turn-Off Fall Time		(Note4)	--	410	830	ns
$Q_g$	Total Gate Charge	$V_{DS} = 64\text{ V}, I_D = 160\text{ A},$ $V_{GS} = 10\text{ V}$	--	225	290	nC	
$Q_{gs}$	Gate-Source Charge		(Note4)	--	43	--	nC
$Q_{gd}$	Gate-Drain Charge		(Note4)	--	120	--	nC

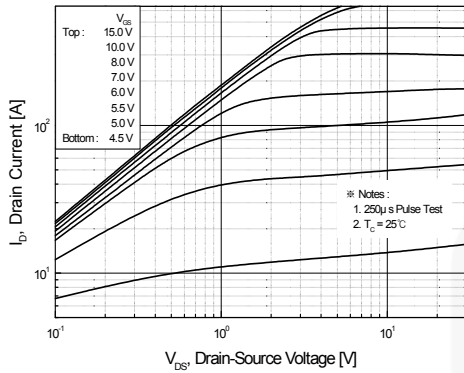
### Drain-Source Diode Characteristics and Maximum Ratings

$I_S$	Maximum Continuous Drain-Source Diode Forward Current	(Note 5)	--	--	160	A
$I_{SM}$	Maximum Pulsed Drain-Source Diode Forward Current		--	--	640	A
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 160\text{ A}$	--	--	1.5	V
$t_{rr}$	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_S = 160\text{ A},$	--	125	--	ns
$Q_{rr}$	Reverse Recovery Charge	$di_F / dt = 100\text{ A}/\mu\text{s}$	--	510	--	nC

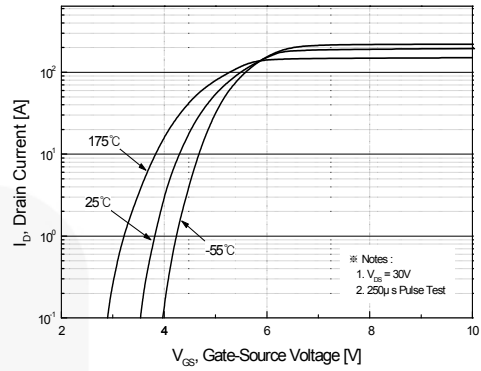
#### Notes:

1. Repetitive rating : pulse-width limited by maximum junction temperature.
2.  $L = 0.115\text{ mH}, I_{AS} = 140\text{ A}, V_{DD} = 25\text{ V}, R_G = 25\ \Omega$ , starting  $T_J = 25^\circ\text{C}$ .
3.  $I_{SD} \leq 140\text{ A}, di/dt \leq 300\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$ , starting  $T_J = 25^\circ\text{C}$ .
4. Essentially independent of operating temperature.
5. Continuous drain current calculated by maximum junction temperature : limited by package.

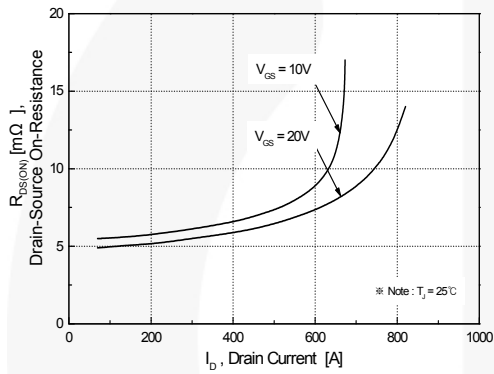
## Typical Characteristics



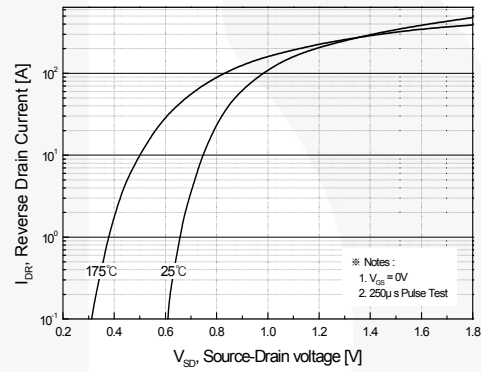
**Figure 1. On-Region Characteristics**



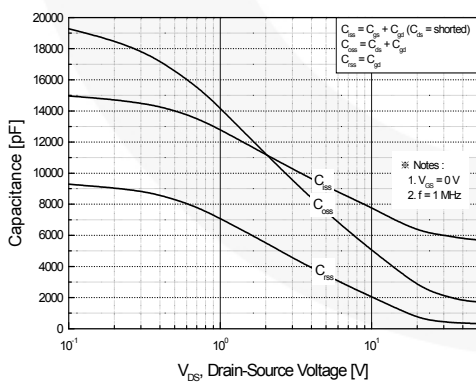
**Figure 2. Transfer Characteristics**



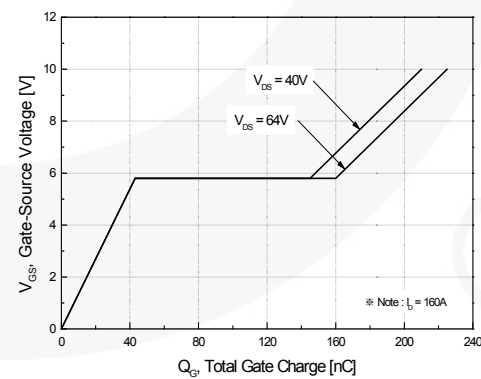
**Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage**



**Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature**

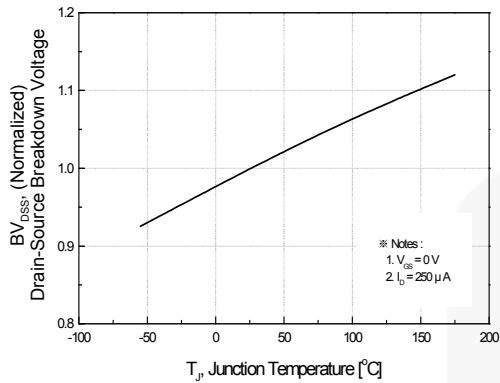


**Figure 5. Capacitance Characteristics**

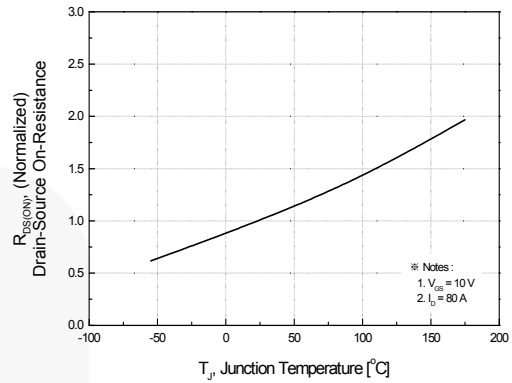


**Figure 6. Gate Charge Characteristics**

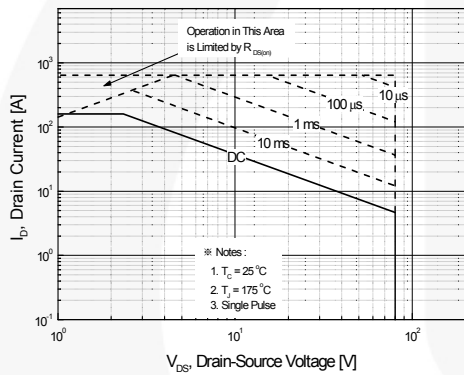
**Typical Characteristics** (Continued)



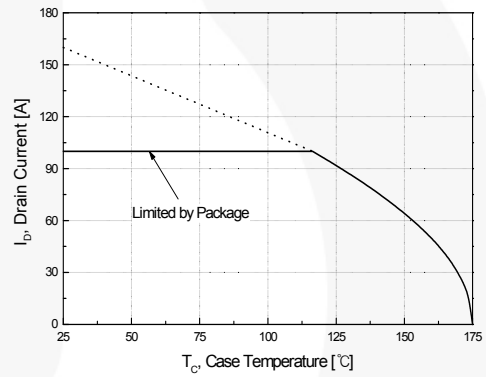
**Figure 7. Breakdown Voltage Variation vs. Temperature**



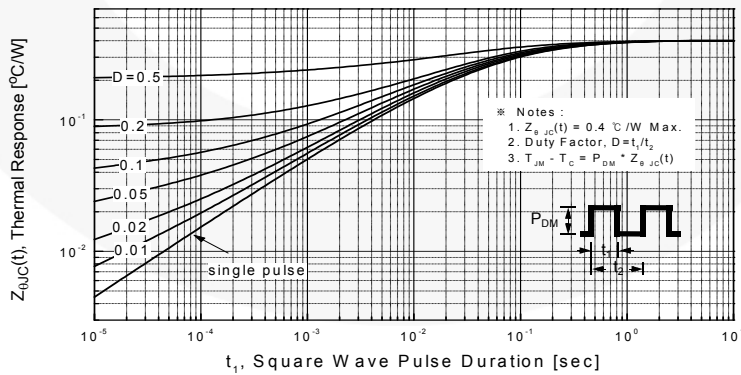
**Figure 8. On-Resistance Variation vs. Temperature**



**Figure 9. Maximum Safe Operating Area**



**Figure 10. Maximum Drain Current vs. Case Temperature**



**Figure 11. Transient Thermal Response Curve**

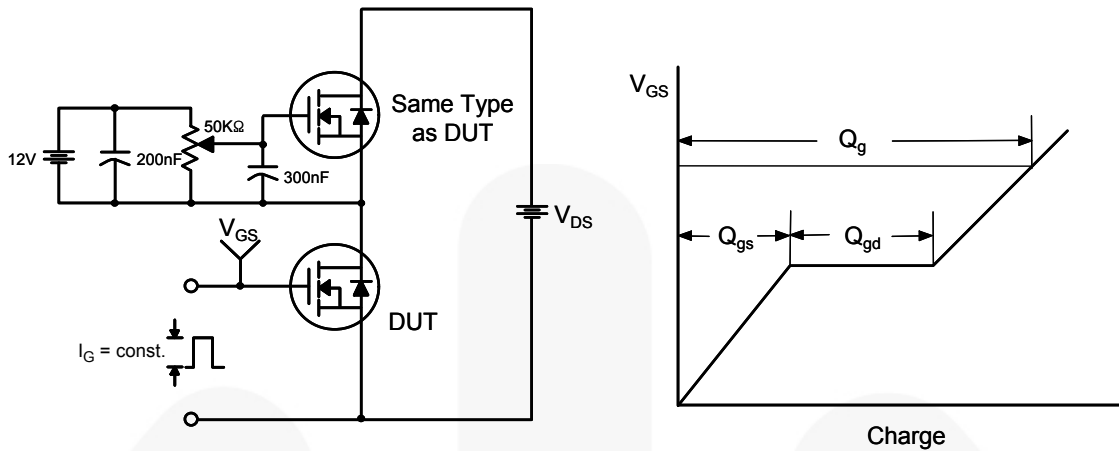


Figure 12. Gate Charge Test Circuit & Waveform

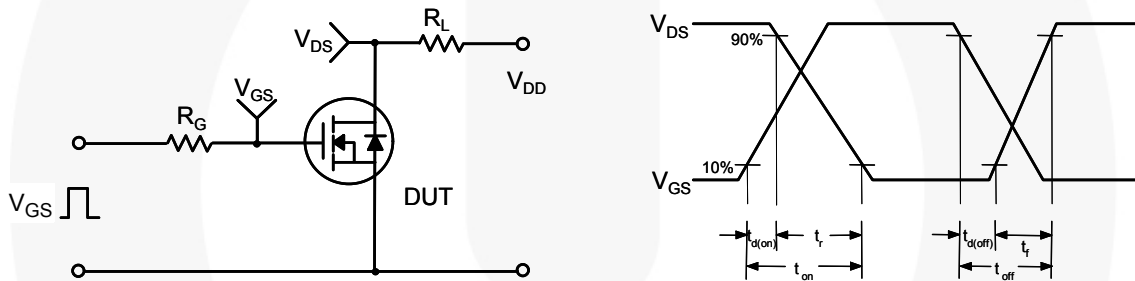


Figure 13. Resistive Switching Test Circuit & Waveforms

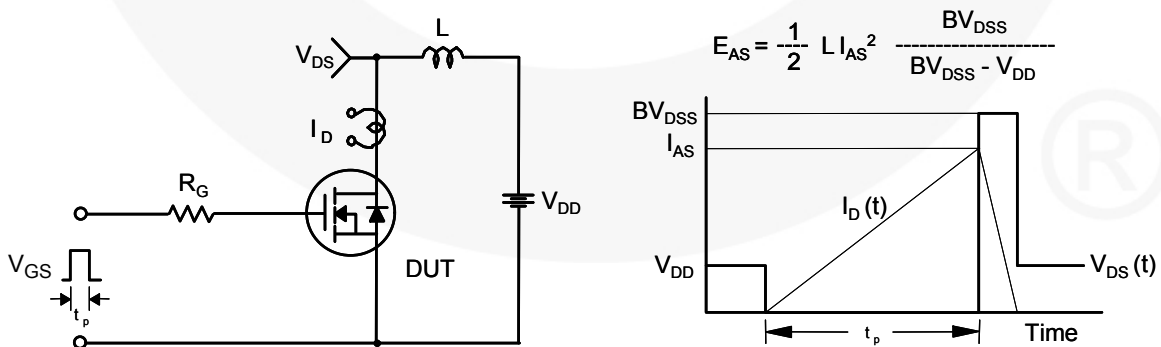


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

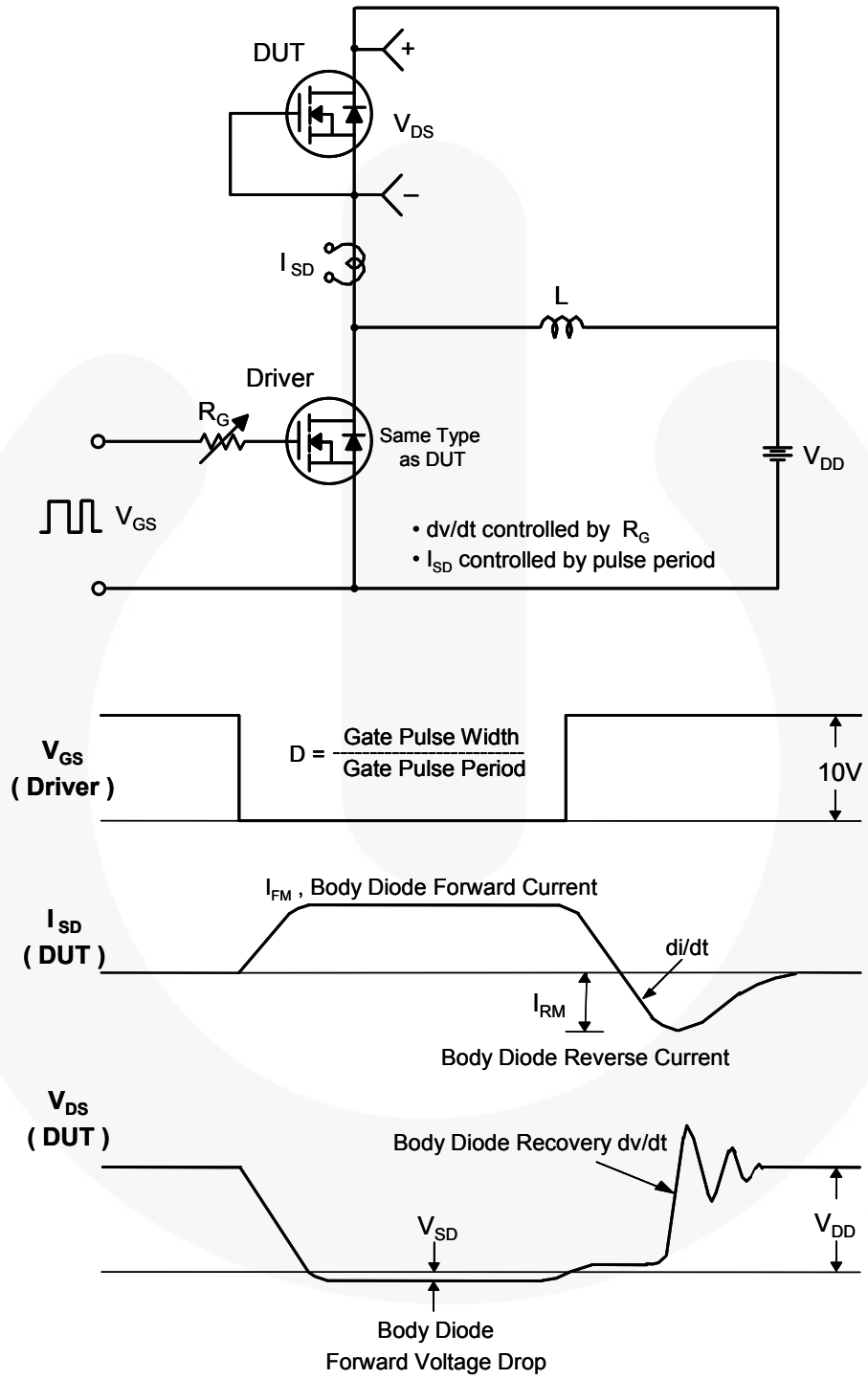
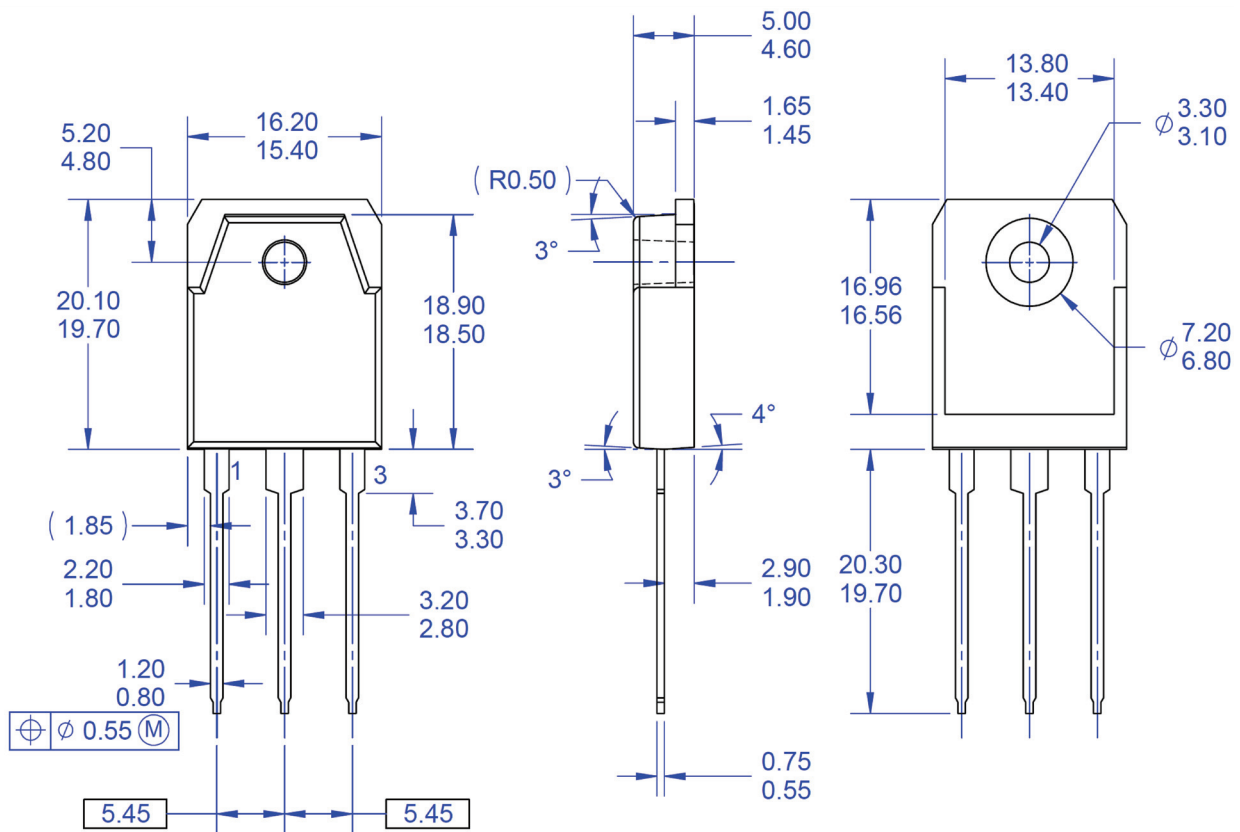


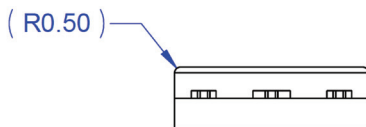
Figure 15. Peak Diode Recovery  $dv/dt$  Test Circuit & Waveforms

## Mechanical Dimensions



NOTES: UNLESS OTHERWISE SPECIFIED

- THIS PACKAGE CONFORMS TO EIAJ SC-65 PACKAGING STANDARD.
- ALL DIMENSIONS ARE IN MILLIMETERS.
- DIMENSION AND TOLERANCING PER ASME14.5-2009.
- DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- DRAWING FILE NAME: TO3PN03AREV1.
- FAIRCHILD SEMICONDUCTOR.



**Figure 16. TO3PN, 3-Lead, Plastic, EIAJ SC-65**

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| FETBench™                | OPTOPLANAR®                                     | SyncFET™                              | 仙童™              |
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