



December 2015

FQT4N25TF

N-Channel QFET[®] MOSFET

250 V, 0.83 A, 1.75 Ω

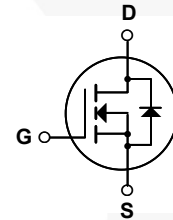
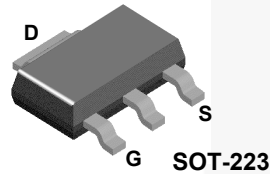
FQT4N25TF N-Channel MOSFET

Description

This N-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor[®]'s proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.

Features

- 0.83 A, 250 V, $R_{DS(on)}=1.75 \Omega(\text{Max.})@V_{GS}=10 \text{ V}, I_D=0.415 \text{ A}$
- Low Gate Charge (Typ. 4.3 nC)
- Low C_{rss} (Typ. 4.8 pF)



Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	FQT4N25TF	Unit
V_{DSS}	Drain-Source Voltage	250	V
I_D	Drain Current - Continuous ($T_C = 25^\circ\text{C}$) - Continuous ($T_C = 70^\circ\text{C}$)	0.83	A
		0.66	A
I_{DM}	Drain Current - Pulsed (Note 1)	3.3	A
V_{GSS}	Gate-Source Voltage	± 30	V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	52	mJ
I_{AR}	Avalanche Current (Note 1)	0.83	A
E_{AR}	Repetitive Avalanche Energy (Note 1)	0.25	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	5.5	V/ns
P_D	Power Dissipation ($T_C = 25^\circ\text{C}$) - Derate above 25°C	2.5	W
		0.02	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	Typ	Max	Unit
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient *	--	50	$^\circ\text{C}/\text{W}$

* When mounted on the minimum pad size recommended (PCB Mount)

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FQT4N25TF	FQT4N25	SOT-223	Tape and Reel	13"	12 mm	2500 units

Electrical Characteristics

$T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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Off Characteristics

BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	250	--	--	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, Referenced to 25°C	--	0.22	--	V/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 250\text{ V}, V_{GS} = 0\text{ V}$	--	--	1	μA
		$V_{DS} = 200\text{ V}, T_C = 125^\circ\text{C}$	--	--	10	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = 30\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -30\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	3.0	--	5.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 0.415\text{ A}$	--	1.38	1.75	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 50\text{ V}, I_D = 0.415\text{ A}$ (Note 4)	--	1.28	--	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	155	200	pF
C_{oss}	Output Capacitance		--	35	45	pF
C_{rss}	Reverse Transfer Capacitance		--	4.8	6.5	pF

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 125\text{ V}, I_D = 3.6\text{ A},$ $R_G = 25\ \Omega$	--	6.8	25	ns
t_r	Turn-On Rise Time		--	45	100	ns
$t_{d(off)}$	Turn-Off Delay Time		--	6.4	25	ns
t_f	Turn-Off Fall Time		(Note 4, 5)	--	22	55
Q_g	Total Gate Charge	$V_{DS} = 200\text{ V}, I_D = 3.6\text{ A},$ $V_{GS} = 10\text{ V}$	--	4.3	5.6	nC
Q_{GS}	Gate-Source Charge		--	1.3	--	nC
Q_{gd}	Gate-Drain Charge		(Note 4, 5)	--	2.1	--

Drain-Source Diode Characteristics and Maximum Ratings

I_S	Maximum Continuous Drain-Source Diode Forward Current	--	--	0.83	A	
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current	--	--	3.3	A	
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 0.83\text{ A}$	--	--	1.5	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_S = 3.6\text{ A},$	--	110	--	ns
Q_{rr}	Reverse Recovery Charge	$dI_F / dt = 100\text{ A}/\mu\text{s}$ (Note 4)	--	0.35	--	μC

Notes:

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. $L = 120\text{mH}, I_{AS} = 0.83\text{ A}, V_{DD} = 50\text{ V}, R_G = 25\ \Omega$, Starting $T_J = 25^\circ\text{C}$
3. $I_{SD} \leq 3.6\text{ A}, di/dt \leq 300\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$
4. Pulse Test : Pulse width $\leq 300\ \mu\text{s}$, Duty cycle $\leq 2\%$
5. Essentially independent of operating temperature

Typical Characteristics

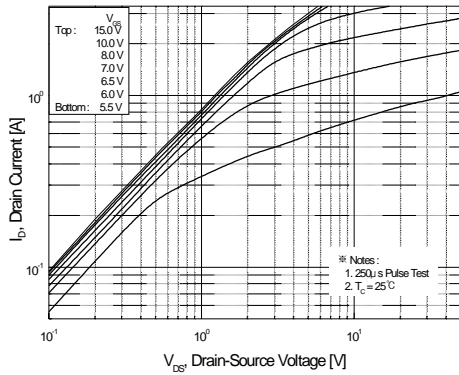


Figure 1. On-Region Characteristics

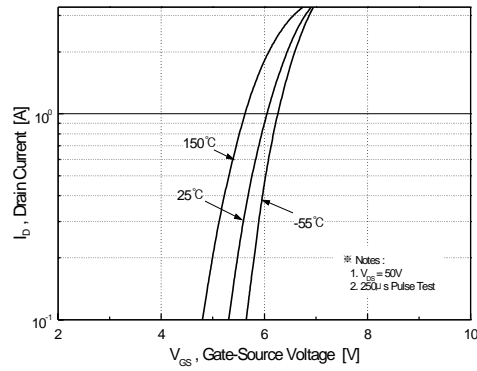


Figure 2. Transfer Characteristics

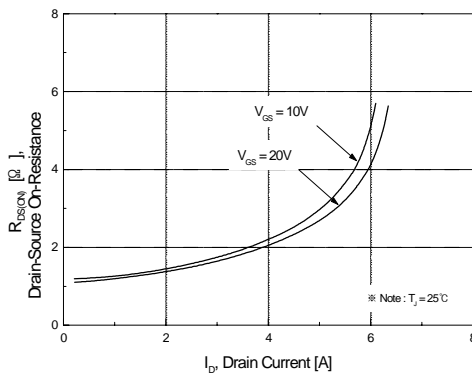


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

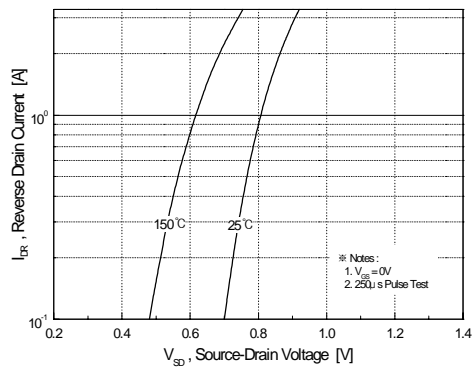


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

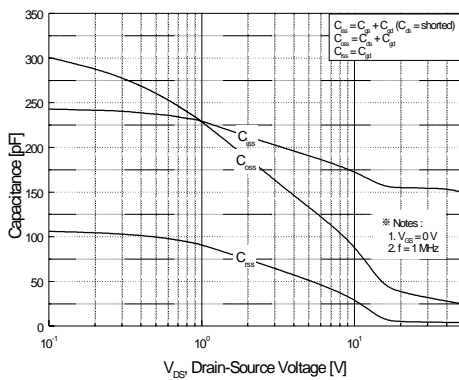


Figure 5. Capacitance Characteristics

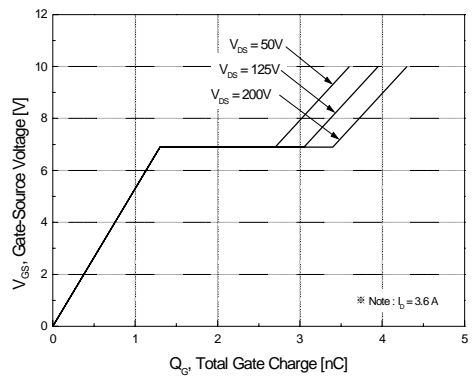


Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)

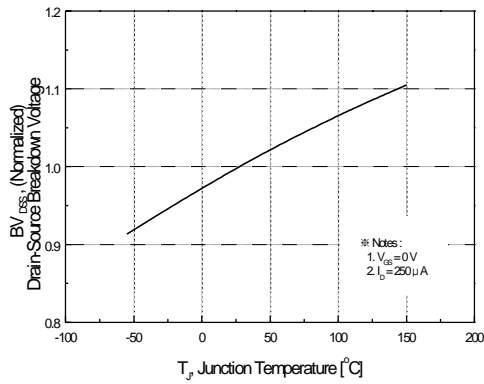


Figure 7. Breakdown Voltage Variation vs. Temperature

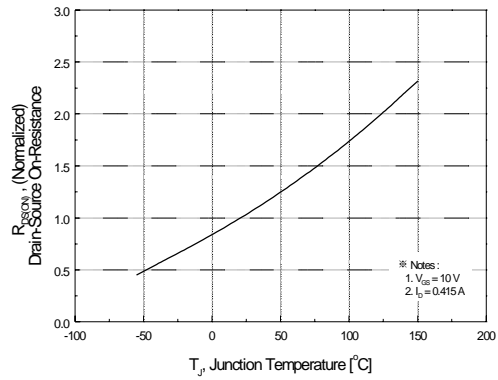


Figure 8. On-Resistance Variation vs. Temperature

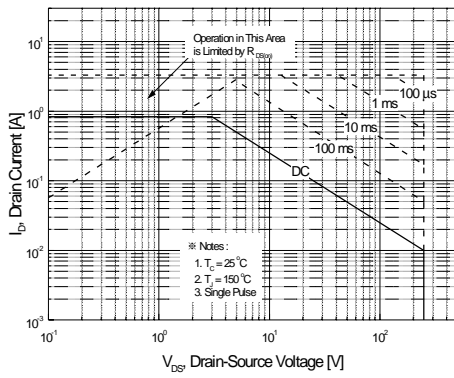


Figure 9. Maximum Safe Operating Area

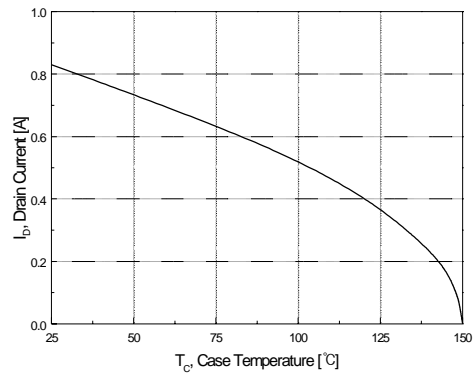


Figure 10. Maximum Drain Current vs. Case Temperature

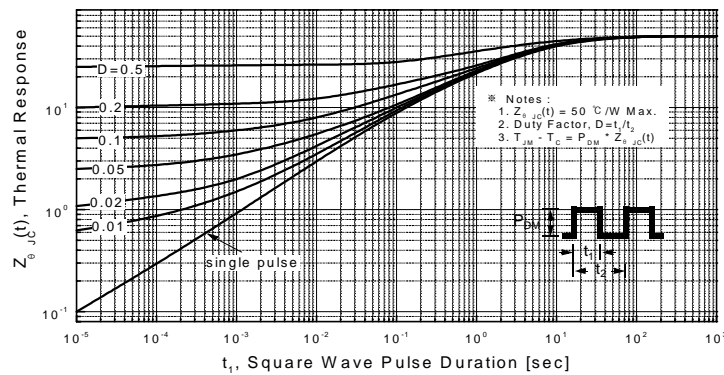
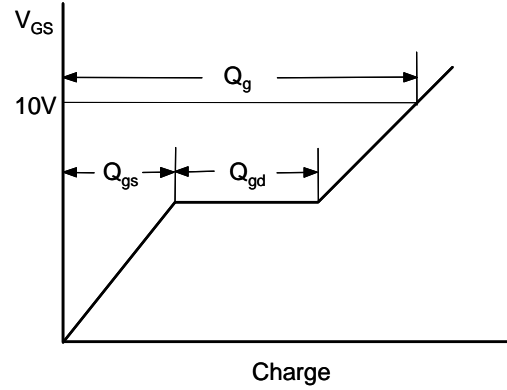
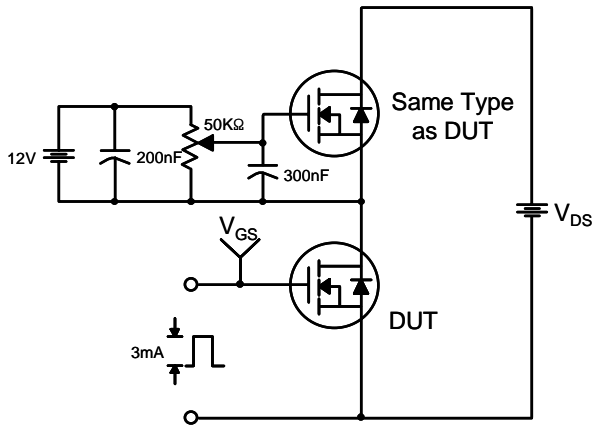
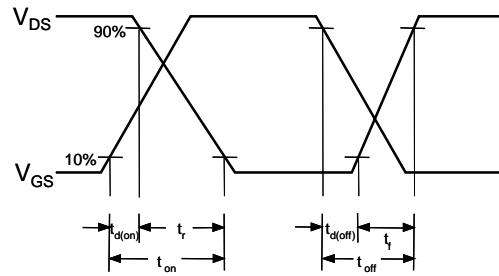
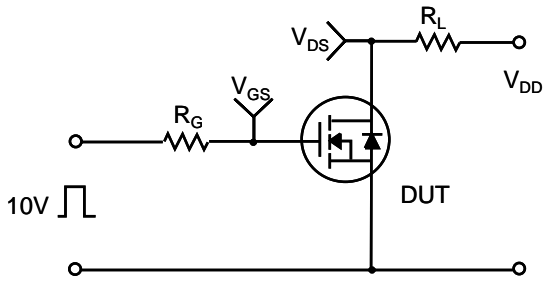


Figure 11. Transient Thermal Response Curve

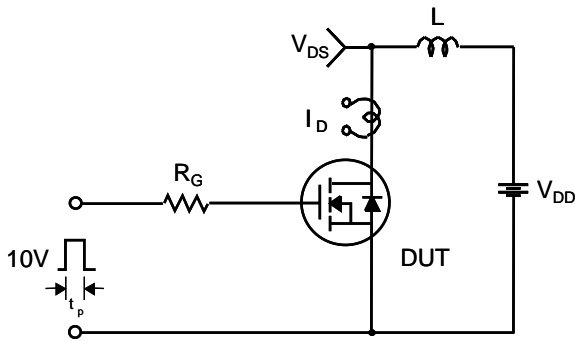
Gate Charge Test Circuit & Waveform



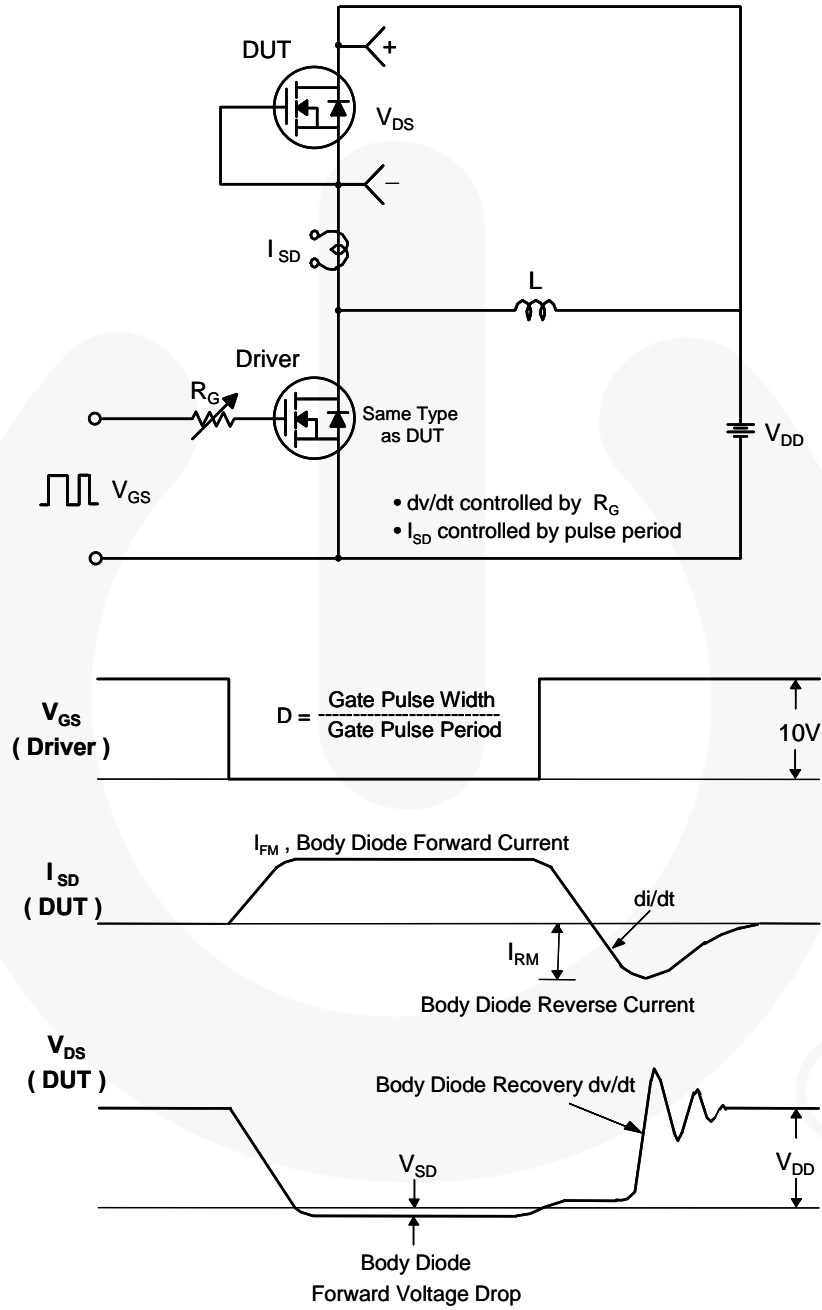
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms



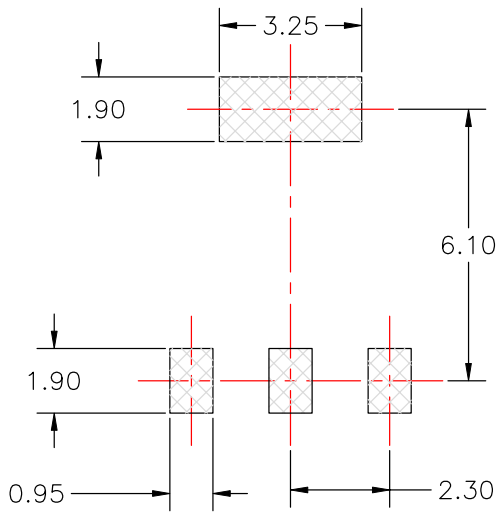
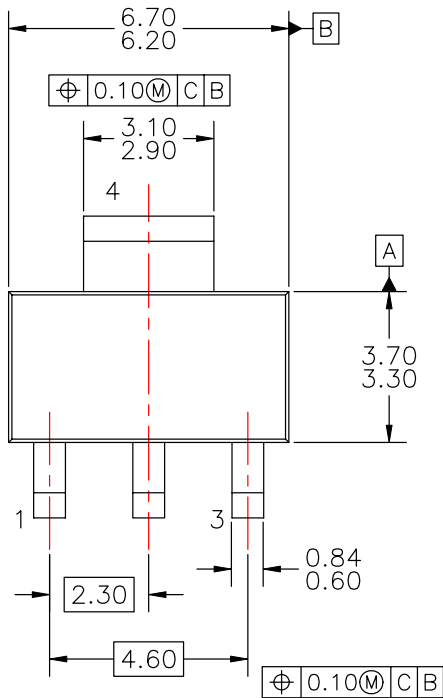
Peak Diode Recovery dv/dt Test Circuit & Waveforms



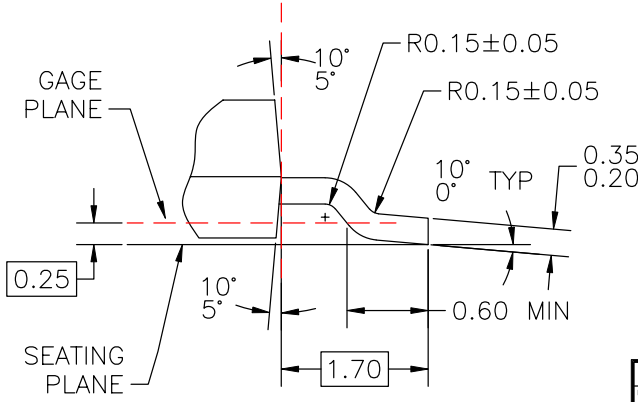
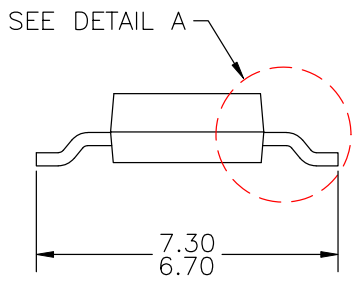
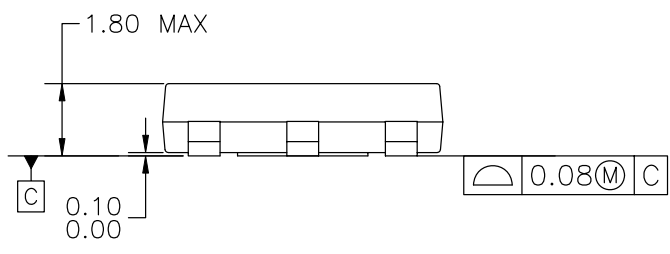
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APPROVED
July-14-2008

REVISIONS			
LTR	DESCRIPTION	DATE	NAME/SITE
A	RELEASE TO DOCUMENT CONTROL	JAN.25,1996	TL/FSCP
2	CHG DWG TEMPLATE FR NATIONAL TO FAIRCHILD; CHG DIM STYLE FR DUAL INCH[MM] TO SINGLE, MM; CHG LD WID FR 0.74 ±0.03 TO 0.60-0.84; REMOVE PKG THICK DIM (1.6); CHG TOTAL PKG HT FR 1.8 ±0.05 TO 1.80 MAX; CHG FOOT LANDING DIM FR 0.91 MIN TO 0.60 MIN; CHG LD THICKNESS FR 0.35 ±0.03 TO 0.20-0.35; ADD DRAFT ANGLE OF MOLDED BODY TOP & BOT; CHG LD LGTH TO PKG EDGE DIM TO BASIC; CHG LD PITCH FR 2.29 BS TO 2.30 BS; CHG BODY WID FR 3.56 ±0.33 TO 3.3; CHG BODY LN FR 6.53 ±0.33 TO 6.3; CHG TOTAL PKG WID FR 6.94 ±0.33 TO 7.3; CHG PAD SIZE FR 0.99 MAX TO 0.95; CHG PAD PITCH FR 2.286 TO 2.30; CHG THERMAL TAB SIZE FR 3.28 MAX TO 3.25; CHG PAD SIZE FR 1.5 TO 1.90; CHG PAD SPACE FR 6.3 TO 6.10; CHG NOTE '2' TO 'A' W/O DATE; DEL NOTE ON LD FINISH; ADD NOTES B, C, D, E & F.	12FEB08	LZSC/FSCP



LAND PATTERN RECOMMENDATION



DETAIL A
SCALE: 2:1

- NOTES: UNLESS OTHERWISE SPECIFIED
- A) DRAWING BASED ON JEDEC REGISTRATION TO-261, VARIATION AA.
 - B) DIMENSIONS ARE INCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
 - C) ALL DIMENSIONS ARE IN MILLIMETERS.
 - D) DRAWING CONFORMS TO ASME Y14.5M-1994.
 - E) LANDPATTERN NAME: SOT230P700X180-4BN
 - F) DRAWING FILENAME: MKT-MA04AREV2

APPROVALS	DATE	FAIRCHILD SEMICONDUCTOR™
DRAWN: J.U. COMPARATIVO JR.	26FEB2008	
CHECKED: L.Z. STA CRUZ		
APPROVED: M.R. GESTOLE		
G.S. BAJE		MOLDED PACKAGE SOT-223, 4 LEAD
PROJECTION 		SCALE: 1:1
		SIZE: A3
		DRAWING NUMBER: MKT-MA04A
		REV: 2
		FORMERLY: N/A
		SHEET: 1 OF 1



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| AttitudeEngine™ | FRFET® | Power Supply WebDesigner™ | TinyBoost® |
| Awinda® | Global Power Resource SM | PowerTrench® | TinyBuck® |
| AX-CAP®* | GreenBridge™ | PowerXS™ | TinyCalc™ |
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PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

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