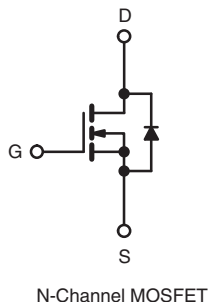
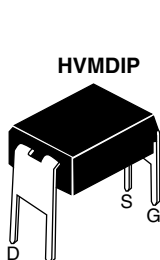


## Power MOSFET

### PRODUCT SUMMARY

|                           |                        |     |
|---------------------------|------------------------|-----|
| $V_{DS}$ (V)              | 400                    |     |
| $R_{DS(on)}$ ( $\Omega$ ) | $V_{GS} = 10\text{ V}$ | 1.8 |
| $Q_g$ (Max.) (nC)         | 20                     |     |
| $Q_{gs}$ (nC)             | 3.3                    |     |
| $Q_{gd}$ (nC)             | 11                     |     |
| Configuration             | Single                 |     |



### FEATURES

- Dynamic dV/dt rating
- Repetitive avalanche rated
- For automatic insertion
- End stackable
- Fast switching
- Ease of paralleling
- Simple drive requirements
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



### DESCRIPTION

Third generation power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The 4 pin DIP package is a low cost machine-insertible case style which can be stacked in multiple combinations on standard 0.1" pin centers. The dual drain servers as a thermal link to the mounting surface for power dissipation levels up to 1 W.

### ORDERING INFORMATION

|                |             |
|----------------|-------------|
| Package        | HVMDIP      |
| Lead (Pb)-free | IRFD320PbF  |
|                | SiHFD320-E3 |
| SnPb           | IRFD320     |
|                | SiHFD320    |

### ABSOLUTE MAXIMUM RATINGS ( $T_A = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted)

| PARAMETER                                                 |                         |                         | SYMBOL                            | LIMIT       | UNIT |
|-----------------------------------------------------------|-------------------------|-------------------------|-----------------------------------|-------------|------|
| Drain-Source Voltage                                      |                         |                         | V <sub>DS</sub>                   | 400         | V    |
| Gate-Source Voltage                                       |                         |                         | V <sub>GS</sub>                   | ± 20        |      |
| Continuous Drain Current                                  | V <sub>GS</sub> at 10 V | T <sub>A</sub> = 25 °C  | I <sub>D</sub>                    | 0.49        | A    |
|                                                           |                         | T <sub>A</sub> = 100 °C |                                   | 0.31        |      |
| Pulsed Drain Current <sup>a</sup>                         |                         |                         | I <sub>DM</sub>                   | 3.9         |      |
| Linear Derating Factor                                    |                         |                         |                                   | 0.0083      | W/°C |
| Single Pulse Avalanche Energy <sup>b</sup>                |                         |                         | E <sub>AS</sub>                   | 48          | mJ   |
| Avalanche Current <sup>a</sup>                            |                         |                         | I <sub>AR</sub>                   | 0.49        | A    |
| Repetitive Avalanche Energy <sup>a</sup>                  |                         |                         | E <sub>AR</sub>                   | 0.10        | mJ   |
| Maximum Power Dissipation                                 | T <sub>A</sub> = 25 °C  |                         | P <sub>D</sub>                    | 1.0         | W    |
| Peak Diode Recovery dV/dt <sup>c</sup>                    |                         |                         | dV/dt                             | 4.0         | V/ns |
| Operating Junction and Storage Temperature Range          |                         |                         | T <sub>J</sub> , T <sub>stg</sub> | -55 to +150 | °C   |
| Soldering Recommendations (Peak Temperature) <sup>d</sup> | for 10 s                |                         |                                   | 300         |      |

#### Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = 50\text{ V}$ , starting  $T_J = 25\text{ }^{\circ}\text{C}$ ,  $L = 21\text{ mH}$ ,  $R_g = 25\text{ }\Omega$ ,  $I_{AS} = 2.0\text{ A}$  (see fig. 12).
- $I_{SD} \leq 2.0\text{ A}$ ,  $dI/dt \leq 40\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 150\text{ }^{\circ}\text{C}$ .
- 1.6 mm from case.

**THERMAL RESISTANCE RATINGS**

| PARAMETER                   | SYMBOL     | TYP. | MAX. | UNIT |
|-----------------------------|------------|------|------|------|
| Maximum Junction-to-Ambient | $R_{thJA}$ | -    | 120  | °C/W |

**SPECIFICATIONS** ( $T_J = 25\text{ °C}$ , unless otherwise noted)

| PARAMETER                                 | SYMBOL                           | TEST CONDITIONS                                                                                                            |                                                                                    | MIN. | TYP. | MAX.  | UNIT |
|-------------------------------------------|----------------------------------|----------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------|------|------|-------|------|
| Static                                    |                                  |                                                                                                                            |                                                                                    |      |      |       |      |
| Drain-Source Breakdown Voltage            | V <sub>DS</sub>                  | V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA                                                                             |                                                                                    | 400  | -    | -     | V    |
| V <sub>DS</sub> Temperature Coefficient   | ΔV <sub>DS</sub> /T <sub>J</sub> | Reference to 25 °C, I <sub>D</sub> = 1 mA                                                                                  |                                                                                    | -    | 0.51 | -     | V/°C |
| Gate-Source Threshold Voltage             | V <sub>GS(th)</sub>              | V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA                                                                |                                                                                    | 2.0  | -    | 4.0   | V    |
| Gate-Source Leakage                       | I <sub>GSS</sub>                 | V <sub>GS</sub> = ± 20 V                                                                                                   |                                                                                    | -    | -    | ± 100 | nA   |
| Zero Gate Voltage Drain Current           | I <sub>DSS</sub>                 | V <sub>DS</sub> = 400 V, V <sub>GS</sub> = 0 V                                                                             |                                                                                    | -    | -    | 25    | μA   |
|                                           |                                  | V <sub>DS</sub> = 320 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C                                                    |                                                                                    | -    | -    | 250   |      |
| Drain-Source On-State Resistance          | R <sub>DS(on)</sub>              | V <sub>GS</sub> = 10 V                                                                                                     | I <sub>D</sub> = 0.21 A <sup>b</sup>                                               | -    | -    | 1.8   | Ω    |
| Forward Transconductance                  | g <sub>fs</sub>                  | V <sub>DS</sub> = 50 V, I <sub>D</sub> = 1.2 A                                                                             |                                                                                    | 1.7  | -    | -     | S    |
| Dynamic                                   |                                  |                                                                                                                            |                                                                                    |      |      |       |      |
| Input Capacitance                         | C <sub>iss</sub>                 | V <sub>GS</sub> = 0 V,<br>V <sub>DS</sub> = 25 V,<br>f = 1.0 MHz, see fig. 5                                               |                                                                                    | -    | 410  | -     | pF   |
| Output Capacitance                        | C <sub>oss</sub>                 |                                                                                                                            |                                                                                    | -    | 120  | -     |      |
| Reverse Transfer Capacitance              | C <sub>rss</sub>                 |                                                                                                                            |                                                                                    | -    | 47   | -     |      |
| Total Gate Charge                         | Q <sub>g</sub>                   | V <sub>GS</sub> = 10 V                                                                                                     | I <sub>D</sub> = 2.0 A, V <sub>DS</sub> = 320 V,<br>see fig. 6 and 13 <sup>b</sup> | -    | -    | 20    | nC   |
| Gate-Source Charge                        | Q <sub>gs</sub>                  |                                                                                                                            |                                                                                    | -    | -    | 3.3   |      |
| Gate-Drain Charge                         | Q <sub>gd</sub>                  |                                                                                                                            |                                                                                    | -    | -    | 11    |      |
| Turn-On Delay Time                        | t <sub>d(on)</sub>               | V <sub>DD</sub> = 200 V, I <sub>D</sub> = 3.3 A,<br>R <sub>g</sub> = 18 Ω, R <sub>D</sub> = 56 Ω, see fig. 10 <sup>b</sup> |                                                                                    | -    | 10   | -     | ns   |
| Rise Time                                 | t <sub>r</sub>                   |                                                                                                                            |                                                                                    | -    | 14   | -     |      |
| Turn-Off Delay Time                       | t <sub>d(off)</sub>              |                                                                                                                            |                                                                                    | -    | 30   | -     |      |
| Fall Time                                 | t <sub>f</sub>                   |                                                                                                                            |                                                                                    | -    | 13   | -     |      |
| Internal Drain Inductance                 | L <sub>D</sub>                   | Between lead,<br>6 mm (0.25") from<br>package and center of<br>die contact                                                 |                                                                                    | -    | 4.0  | -     | nH   |
| Internal Source Inductance                | L <sub>S</sub>                   |                                                                                                                            |                                                                                    | -    | 6.0  | -     |      |
| Drain-Source Body Diode Characteristics   |                                  |                                                                                                                            |                                                                                    |      |      |       |      |
| Continuous Source-Drain Diode Current     | I <sub>S</sub>                   | MOSFET symbol<br>showing the<br>integral reverse<br>p - n junction diode                                                   |                                                                                    | -    | -    | 0.49  | A    |
| Pulsed Diode Forward Current <sup>a</sup> | I <sub>SM</sub>                  |                                                                                                                            |                                                                                    | -    | -    | 3.9   |      |
| Body Diode Voltage                        | V <sub>SD</sub>                  | T <sub>J</sub> = 25 °C, I <sub>S</sub> = 0.49 A, V <sub>GS</sub> = 0 V <sup>b</sup>                                        |                                                                                    | -    | -    | 1.6   | V    |
| Body Diode Reverse Recovery Time          | t <sub>rr</sub>                  | T <sub>J</sub> = 25 °C, I <sub>F</sub> = 3.3 A, dI/dt = 100 A/μs <sup>b</sup>                                              |                                                                                    | -    | 270  | 600   | ns   |
| Body Diode Reverse Recovery Charge        | Q <sub>rr</sub>                  |                                                                                                                            |                                                                                    | -    | 1.4  | 3.0   | μC   |
| Forward Turn-On Time                      | t <sub>on</sub>                  | Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> and L <sub>D</sub> )                          |                                                                                    |      |      |       |      |

**Notes**

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).  
b. Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$ .



**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

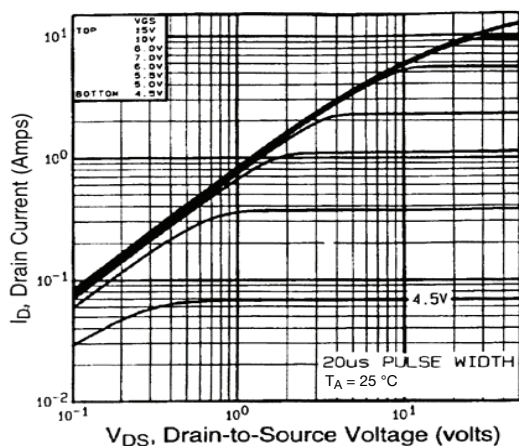


Fig. 1 - Typical Output Characteristics,  $T_A = 25\text{ }^{\circ}\text{C}$

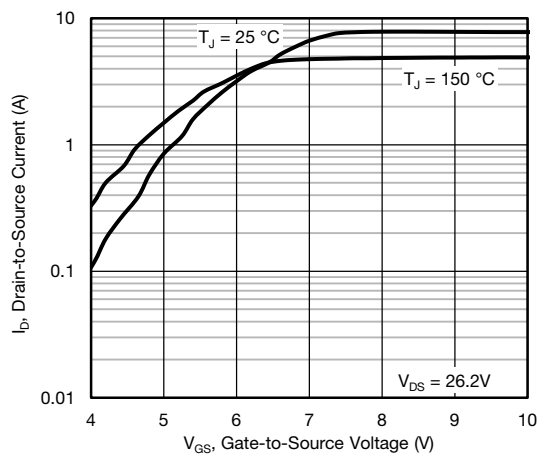


Fig. 3 - Typical Transfer Characteristics

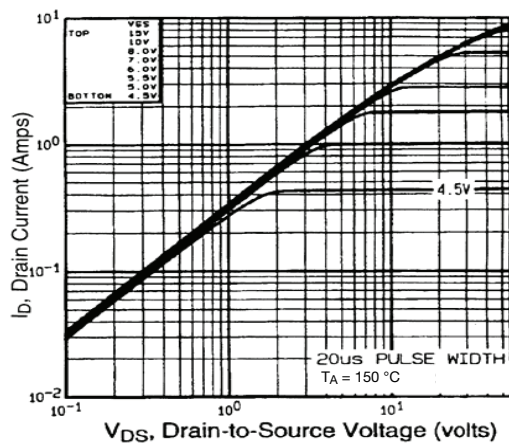


Fig. 2 - Typical Output Characteristics,  $T_A = 150\text{ }^{\circ}\text{C}$

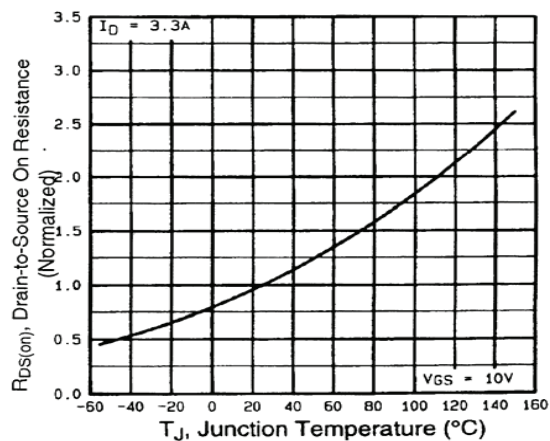
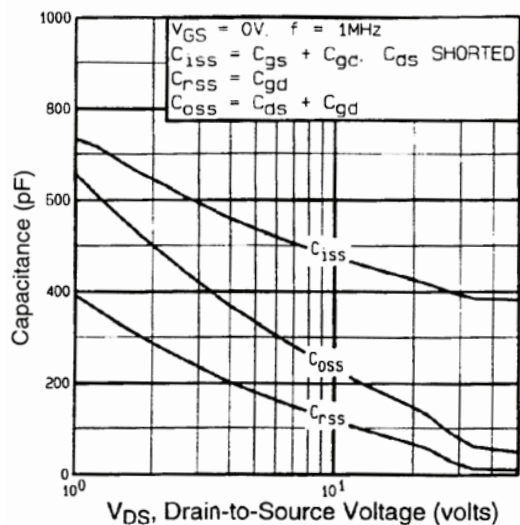
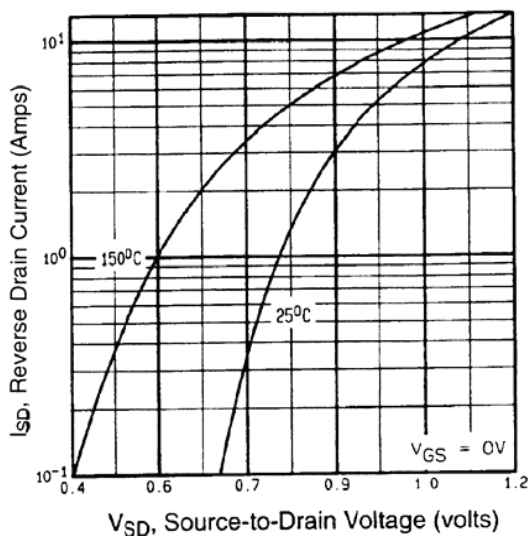
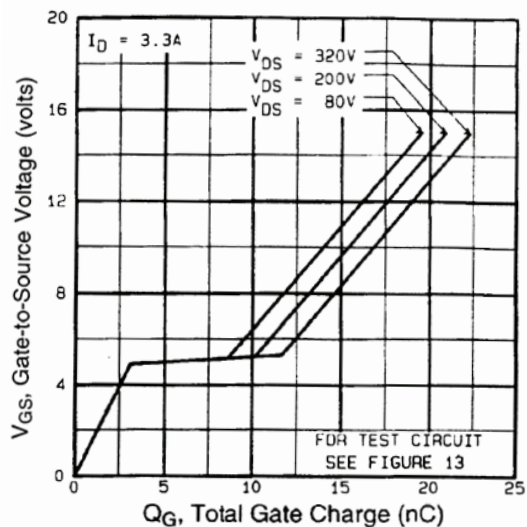
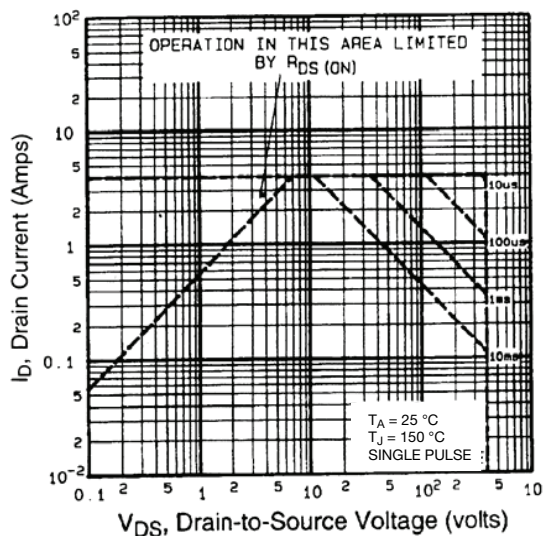
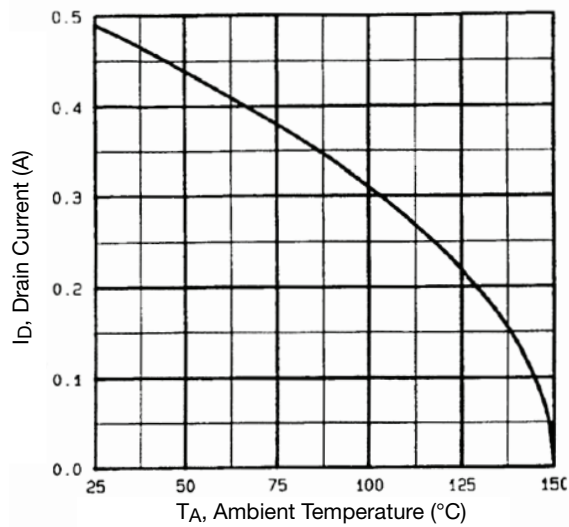
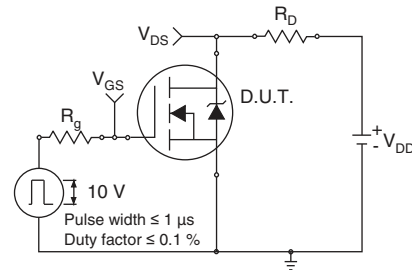
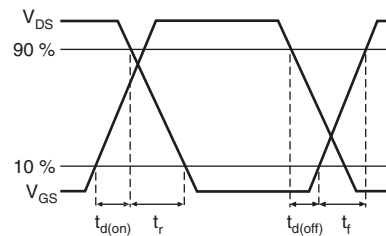
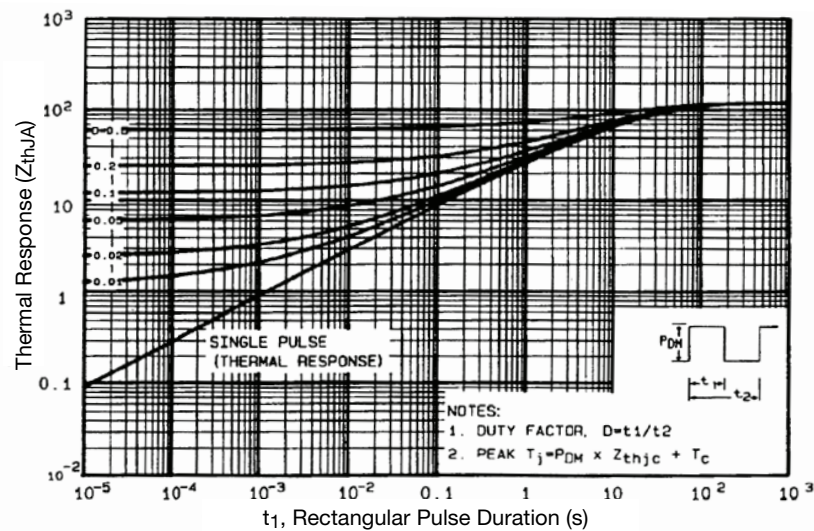
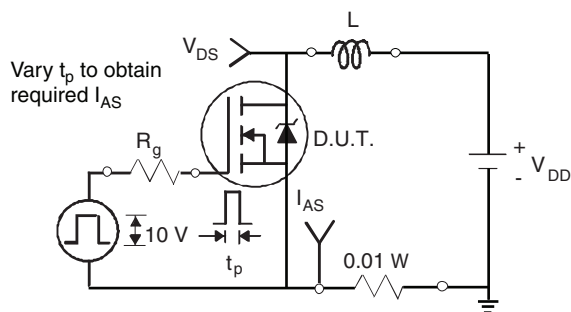
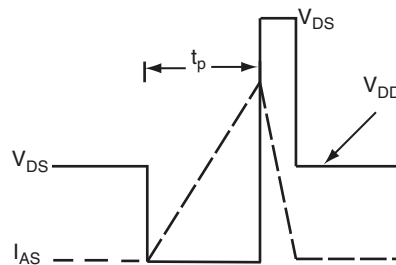
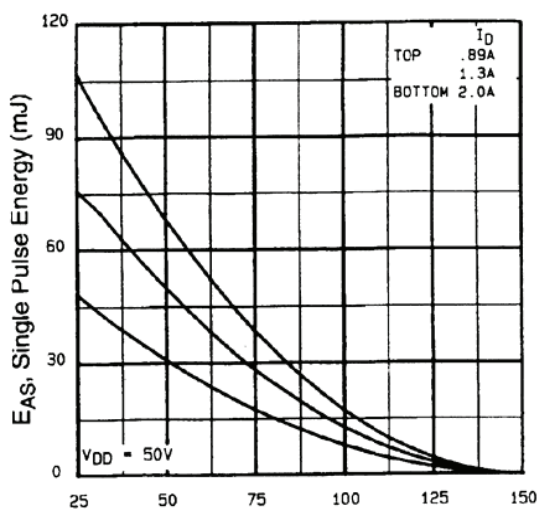
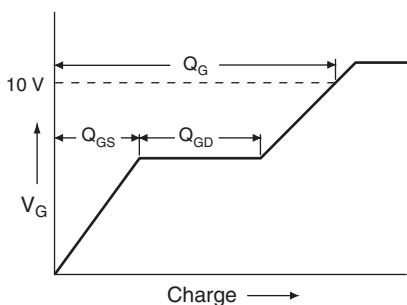
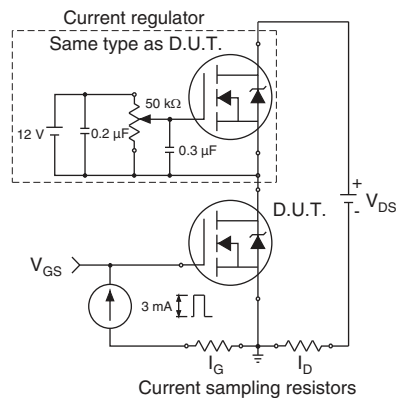
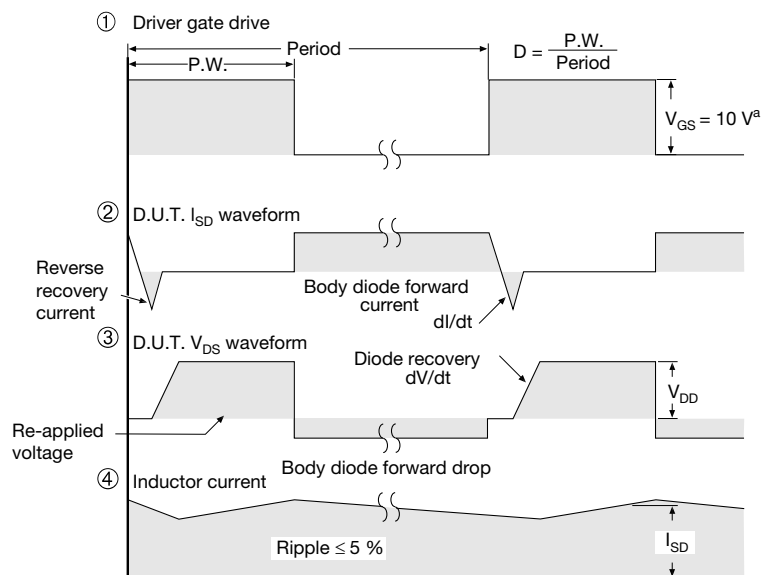
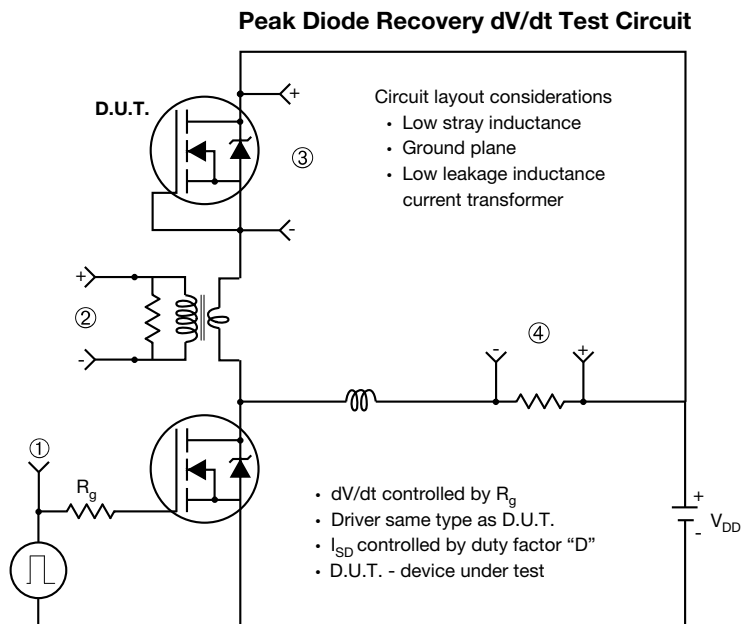


Fig. 4 - Normalized On-Resistance vs. Temperature


**Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage**

**Fig. 7 - Typical Source-Drain Diode Forward Voltage**

**Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage**

**Fig. 8 - Maximum Safe Operating Area**


**Fig. 9 - Maximum Drain Current vs. Ambient Temperature**

**Fig. 10a - Switching Time Test Circuit**

**Fig. 10b - Switching Time Waveforms**

**Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Ambient**


**Fig. 12a - Unclamped Inductive Test Circuit**

**Fig. 12b - Unclamped Inductive Waveforms**

**Fig. 12c - Maximum Avalanche Energy vs. Drain Current**

**Fig. 13a - Basic Gate Charge Waveform**

**Fig. 13b - Gate Charge Test Circuit**


**Note**

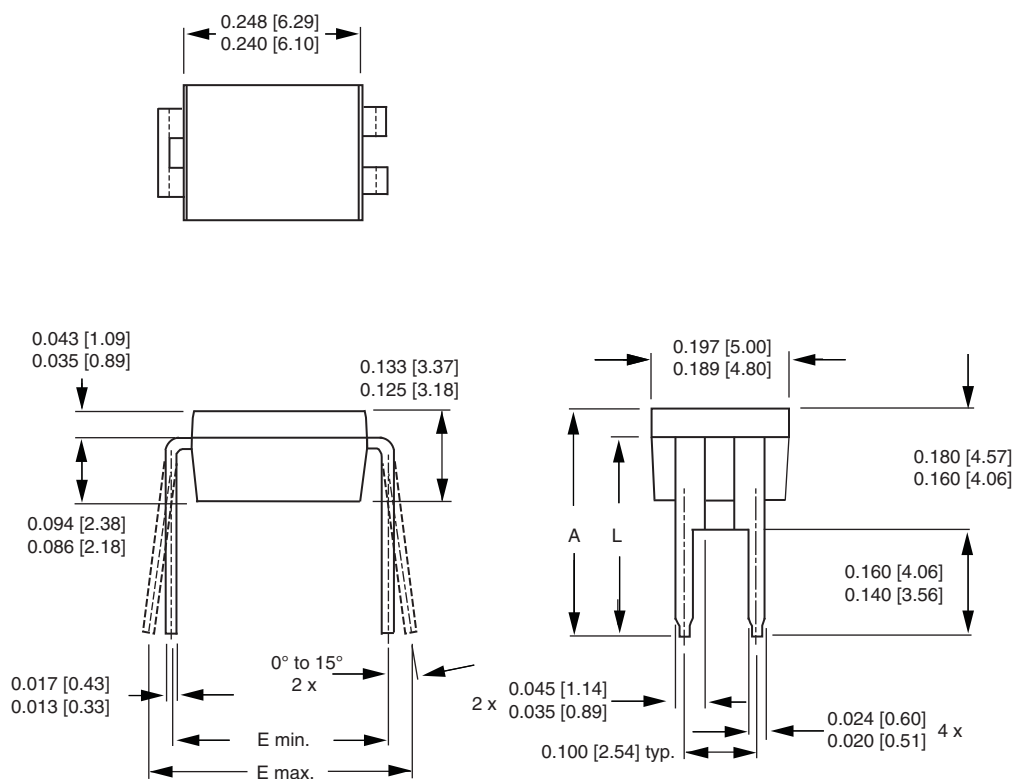
a.  $V_{GS} = 5 V$  for logic level devices

**Fig. 14 - For N-Channel**

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## HVM DIP (High voltage)



| DIM. | INCHES |       | MILLIMETERS |       |
|------|--------|-------|-------------|-------|
|      | MIN.   | MAX.  | MIN.        | MAX.  |
| A    | 0.310  | 0.330 | 7.87        | 8.38  |
| E    | 0.300  | 0.425 | 7.62        | 10.79 |
| L    | 0.270  | 0.290 | 6.86        | 7.36  |

ECN: X10-0386-Rev. B, 06-Sep-10  
DWG: 5974

### Note

- Package length does not include mold flash, protrusions or gate burrs. Package width does not include interlead flash or protrusions.





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**Please note that some Vishay documentation may still make reference to RoHS Directive 2002/95/EC. We confirm that all the products identified as being compliant to Directive 2002/95/EC conform to Directive 2011/65/EU.**

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