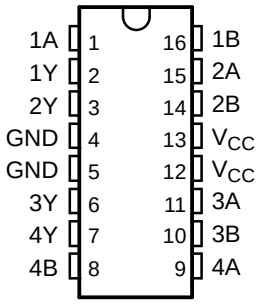
# 74AC11000
# QUADRUPLE 2-INPUT POSITIVE-NAND GATE

SCLS054B–APRIL 1987–REVISED JUNE 2005

## FEATURES

- **Center-Pin $V_{CC}$ and GND Configurations Minimize High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typ Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline (D) Packages and Standard Plastic 300-mil DIPs (N)**

**D OR N PACKAGE**
**(TOP VIEW)**




## DESCRIPTION

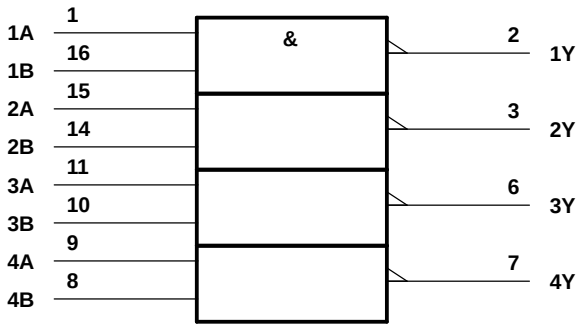
This device contains four independent 2-input NAND gates. It performs the Boolean function $Y = \overline{A \bullet B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

The 74AC11000 is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE**
**(EACH GATE)**

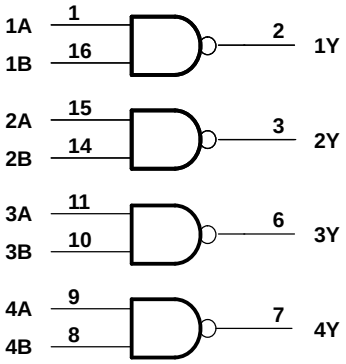
| INPUTS | | OUTPUT |
|---|---|---|
| **A** | **B** | **Y** |
| H | H | L |
| L | X | H |
| X | L | H |

**LOGIC SYMBOL(1)**




(1) This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

### LOGIC DIAGRAM (POSITIVE LOGIC)




## Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage range | | –0.5 | 7 | V |
| $V_I$ | Input voltage range(2) | | –0.5 | $V_{CC}$ + 0.5 | V |
| $V_O$ | Output voltage range(2) | | –0.5 | $V_{CC}$ + 0.5 | V |
| $I_{IK}$ | Input clamp current | $V_I < 0$ or $V_I > V_{CC}$ | | ±20 | mA |
| $I_{OK}$ | Output clamp current | $V_O < 0$ or $V_O > V_{CC}$ | | ±50 | mA |
| $I_O$ | Continuous output current | $V_O$ = 0 to $V_{CC}$ | | ±50 | mA |
| | Continuous current through $V_{CC}$ or GND | | | ±100 | mA |
| | Maximum power dissipation at $T_A$ = 55°C (in still air)(3) | D package | | 1.3 | W |
| | | N package | | 1.1 | |
| $T_{stg}$ | Storage temperature range | | –65 | 150 | °C |

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the N package, which has a trace length of zero.

## Recommended Operating Conditions

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 3 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 3 V | 2.1 | | | V |
| | | $V_{CC}$ = 4.5 V | 3.15 | | | |
| | | $V_{CC}$ = 5.5 V | 3.85 | | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 3 V | | | 0.9 | V |
| | | $V_{CC}$ = 4.5 V | | | 1.35 | |
| | | $V_{CC}$ = 5.5 V | | | 1.65 | |
| $V_I$ | Input voltage | | 0 | | $V_{CC}$ | V |
| $V_O$ | Output voltage | | 0 | | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 3 V | | | –4 | mA |
| | | $V_{CC}$ = 4.5 V | | | –24 | |
| | | $V_{CC}$ = 5.5 V | | | –24 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 3 V | | | 12 | mA |
| | | $V_{CC}$ = 4.5 V | | | 24 | |
| | | $V_{CC}$ = 5.5 V | | | 24 | |
| $\Delta t/\Delta v$ | Input transition rise fall rate | | 0 | | 10 | ns/V |
| $T_A$ | Operating free-air temperature | | –40 | | 85 | °C |

## Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | | | |
| $V_{OH}$ | $I_{OH}$ = –50 µA | 3 V | 2.9 | | | 2.9 | | V |
| | | 4.5 V | 4.4 | | | 4.4 | | |
| | | 5.5 V | 5.4 | | | 5.4 | | |
| | $I_{OH}$ = –4 mA | 3 V | 2.58 | | | 2.48 | | |
| | $I_{OH}$ = –24 mA | 4.5 V | 3.94 | | | 3.8 | | |
| | | 5.5 V | 4.94 | | | 4.8 | | |
| | $I_{OH}$ = –75 mA(1) | 5.5 V | | | | 3.85 | | |
| $V_{OL}$ | $I_{OL}$ = 50 µA | 3 V | | | 0.1 | | 0.1 | V |
| | | 4.5 V | | | 0.1 | | 0.1 | |
| | | 5.5 V | | | 0.1 | | 0.1 | |
| | $I_{OL}$ = 12 mA | 3 V | | | 0.36 | | 0.44 | |
| | $I_{OL}$ = 24 mA | 4.5 V | | | 0.36 | | 0.44 | |
| | | 5.5 V | | | 0.36 | | 0.44 | |
| | $I_{OL}$ = 75 mA(1) | 5.5 V | | | | | 1.65 | |
| $I_I$ | $V_I$ = $V_{CC}$ or GND | 5.5 V | | | ±0.1 | | ±1 | µA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 4 | | 40 | µA |
| $C_i$ | $V_I$ = $V_{CC}$ or GND | 5 V | | 3.5 | | | | pF |

(1) Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

## Switching Characteristics

over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $T_A$ = 25°C | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A or B | Y | 1.5 | 7.2 | 9.8 | 1.5 | 11.1 | ns |
| $t_{PHL}$ | | | 1.5 | 5.8 | 8.6 | 1.5 | 9.6 | |

## Switching Characteristics

over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

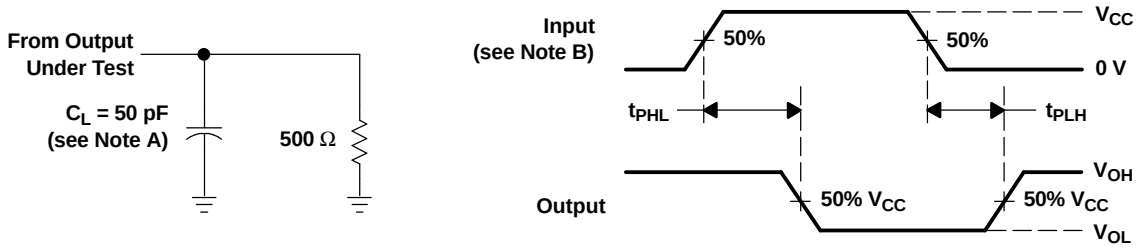
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $T_A$ = 25°C | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A or B | Y | 1.5 | 5 | 6.5 | 1.5 | 7.4 | ns |
| $t_{PHL}$ | | | 1.5 | 4.4 | 6.1 | 1.5 | 6.8 | |

## Operating Characteristics

$V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | TYP | UNIT |
|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance per gate | $C_L$ = 50 pF, f = 1 MHz | 33 | pF |

## PARAMETER MEASUREMENT INFORMATION




LOAD CIRCUIT VOLTAGE WAVEFORMS

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 3 ns, $t_f$ = 3 ns.
C. The outputs are measured one at a time with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 74AC11000D | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | AC11000 | Samples |
| 74AC11000DR | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | AC11000 | Samples |
| 74AC11000N | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -40 to 85 | 74AC11000N | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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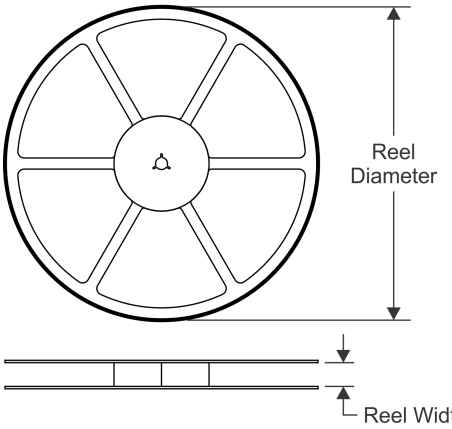
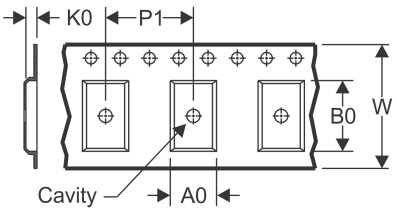
## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

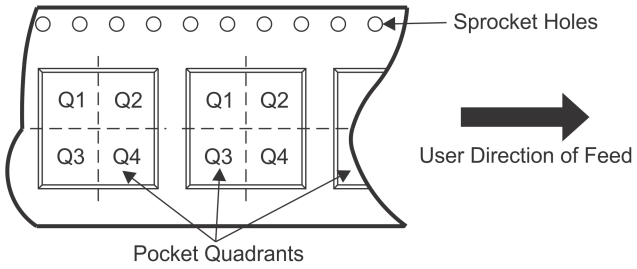



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

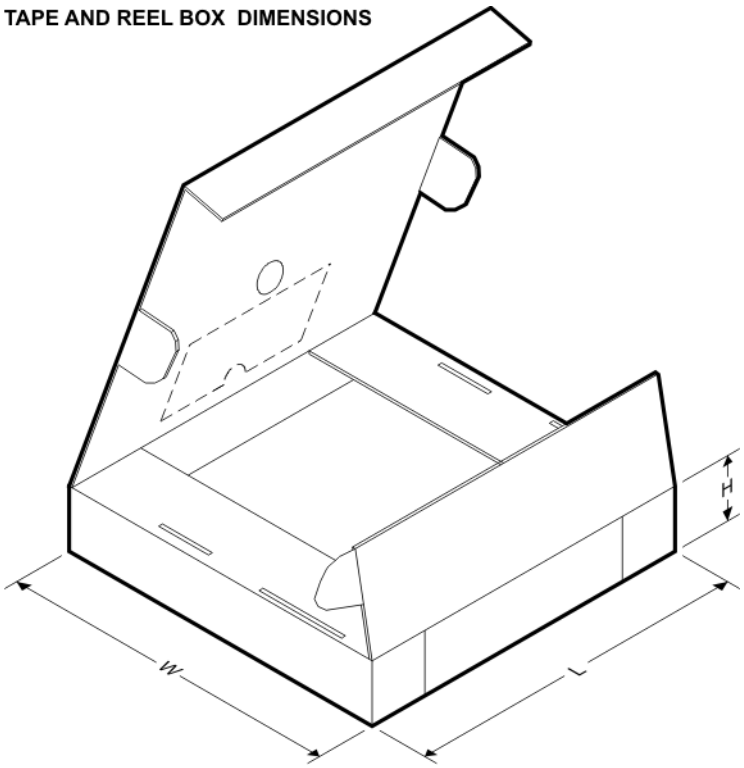
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 74AC11000DR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



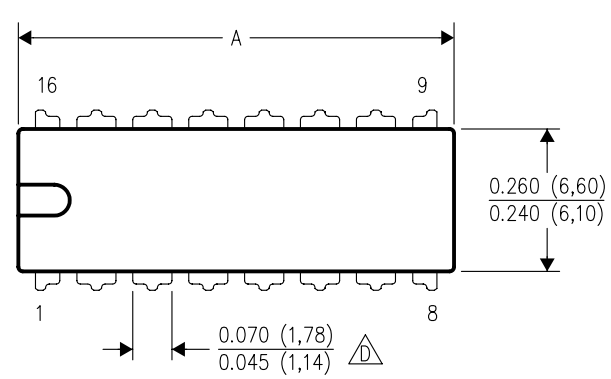

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| 74AC11000DR | SOIC | D | 16 | 2500 | 333.2 | 345.9 | 28.6 |

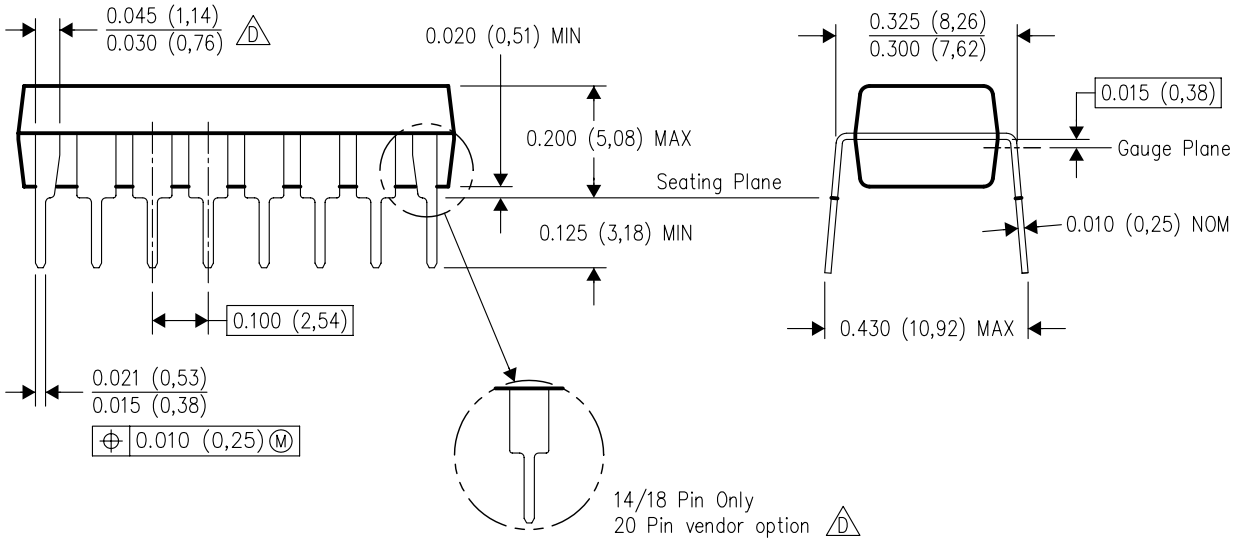
## N (R–PDIP–T**)

## PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |

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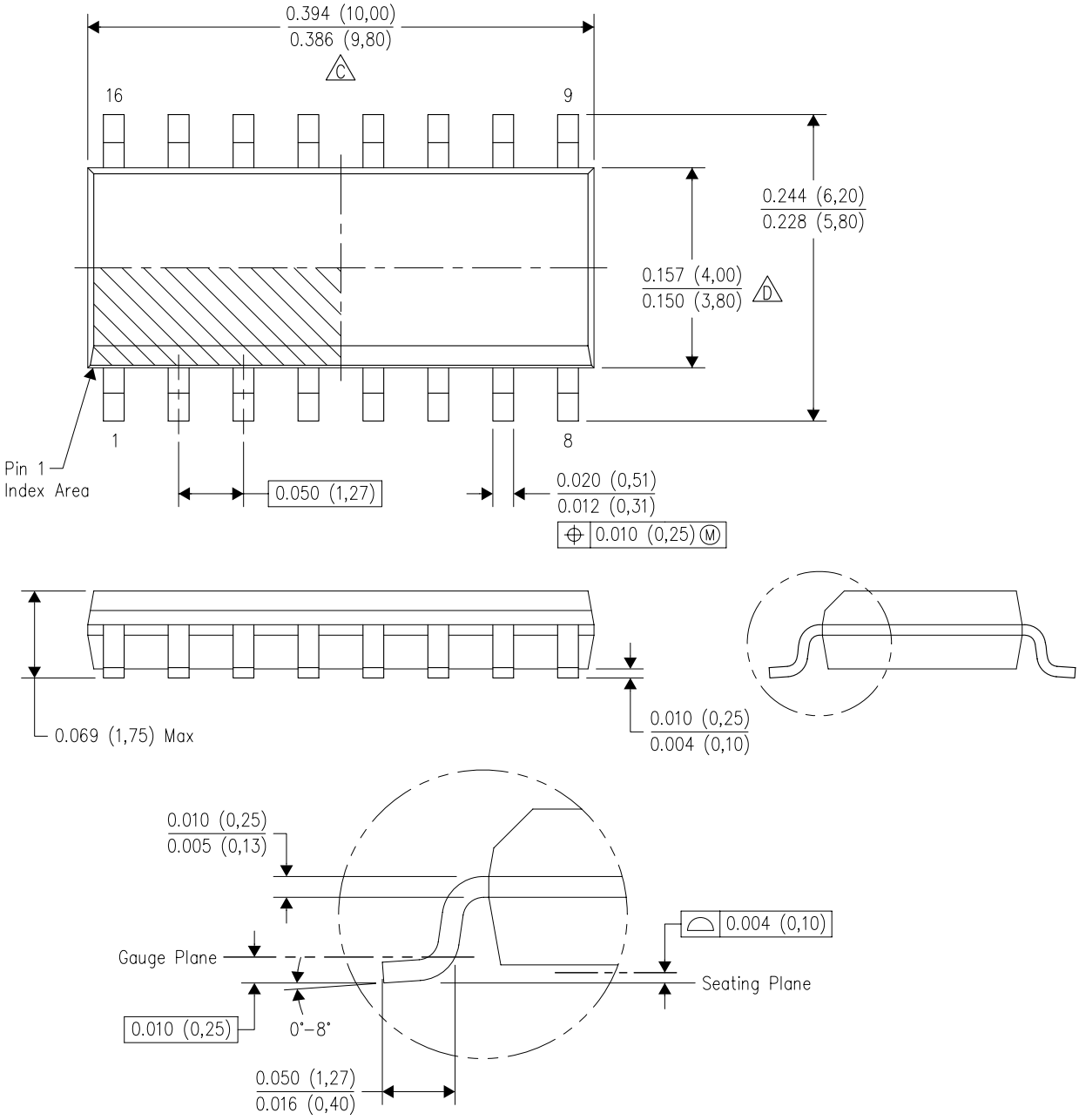
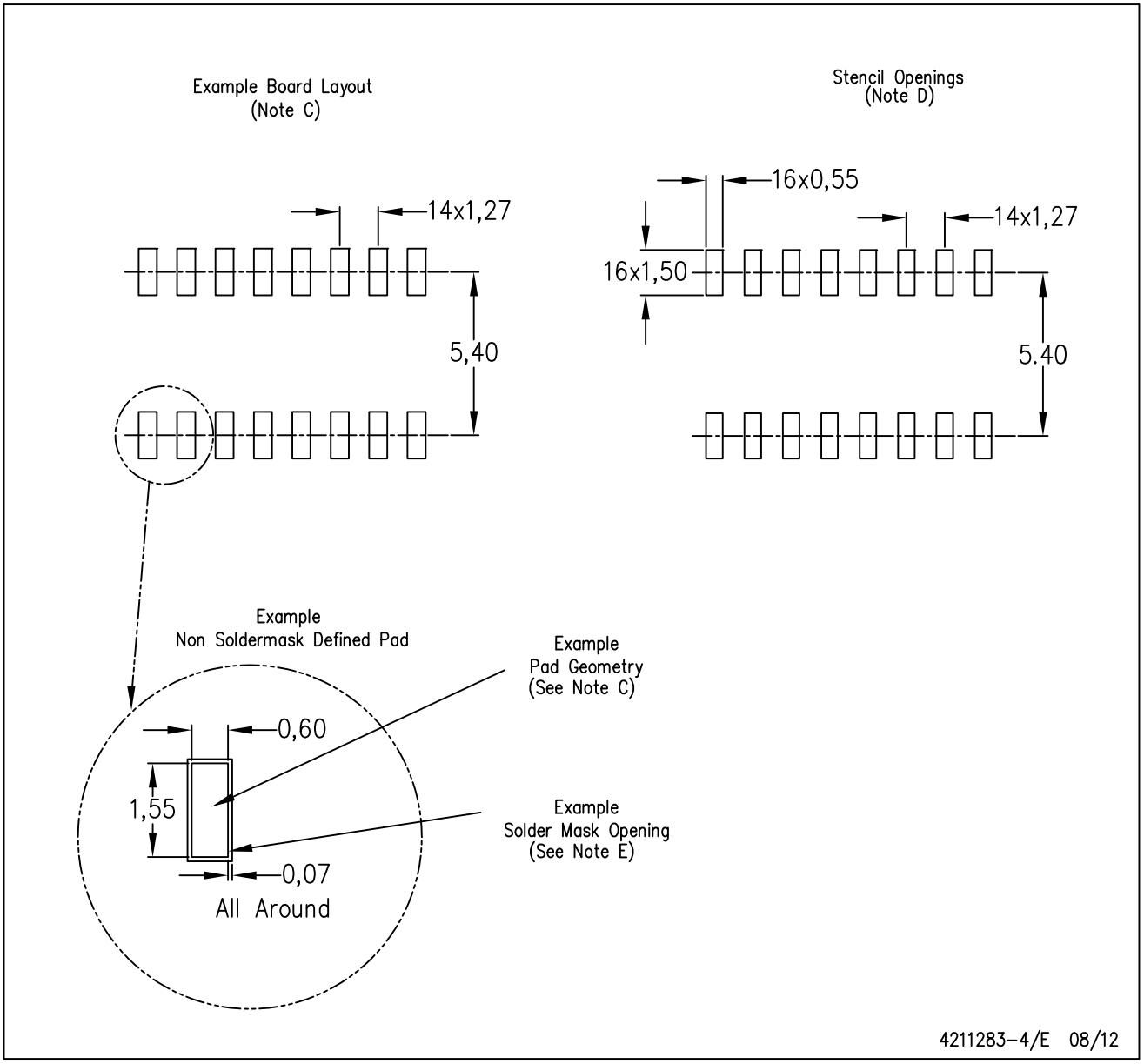
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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