DS90CF386/DS90CF366 +3.3V LVDS Receiver 24-Bit Flat Panel Display (FPD) Link - 85 MHz, +3.3V LVDS Receiver 18-Bit Flat Panel Display (FPD) Link - 85 MHz

Check for Samples: DS90CF366, DS90CF386

FEATURES

- **20 to 85 MHz Shift Clock Support**
- **Rx Power Consumption <142 mW (typ) @85MHz Grayscale**
- **Rx Power-Down Mode <1.44 mW (max)**
- **ESD Rating >7 kV (HBM), >700V (EIAJ)**
- **Supports VGA, SVGA, XGA and Single Pixel SXGA.**
- **PLL Requires No External Components**
- **Compatible with TIA/EIA-644 LVDS Standard**
- **Low Profile 56-Lead or 48-lead TSSOP Package**
- **DS90CF386 Also Available in a 64 Ball, 0.8mm Fine Pitch Ball Grid Array (NFBGA) Package**

DESCRIPTION

The DS90CF386 receiver converts the four LVDS data streams (Up to 2.38 Gbps throughput or 297.5 Megabytes/sec bandwidth) back into parallel 28 bits of CMOS/TTL data (24 bits of RGB and 4 bits of Hsync, Vsync, DE and CNTL). Also available is the DS90CF366 that converts the three LVDS data streams (Up to 1.78 Gbps throughput or 223 Megabytes/sec bandwidth) back into parallel 21 bits of CMOS/TTL data (18 bits of RGB and 3 bits of Hsync, Vsync and DE). Both Receivers' outputs are Falling edge strobe. A Rising edge or Falling edge strobe transmitter (DS90C385/DS90C365) will interoperate with a Falling edge strobe Receiver without any translation logic.

The DS90CF386 is also offered in a 64 ball, 0.8mm fine pitch ball grid array (NFBGA) package which provides a 44 % reduction in PCB footprint compared to the 56L TSSOP package.

This chipset is an ideal means to solve EMI and cable size problems associated with wide, high speed TTL interfaces.

BLOCK DIAGRAM

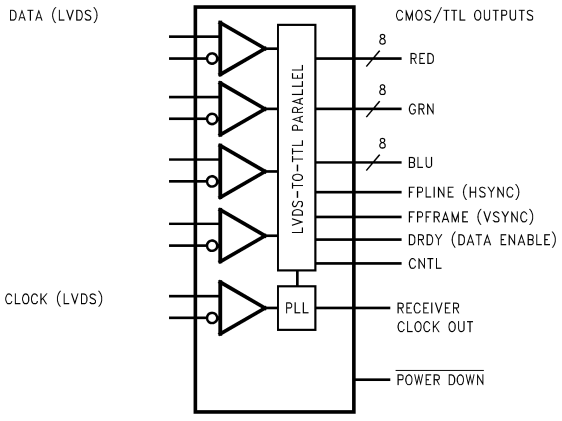


Figure 1. DS90CF386
See Package Number DGG-56 (TSSOP) or NZC0064A-64 (NFBGA)

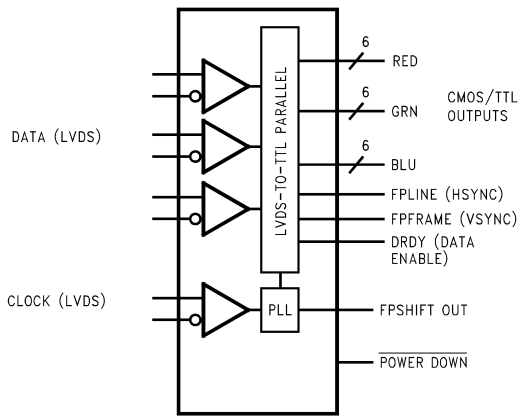


Figure 2. DS90CF366
See Package Number DGG-48 (TSSOP)

Absolute Maximum Ratings[1][2]

Supply Voltage (V_{CC})			−0.3V to +4V
CMOS/TTL Output Voltage			−0.3V to (V_{CC} + 0.3V)
LVDS Receiver Input Voltage			−0.3V to (V_{CC} + 0.3V)
Junction Temperature			+150°C
Storage Temperature			−65°C to +150°C
Lead Temperature(Soldering, 4 sec for TSSOP)			+260°C
Solder Reflow Temperature (Soldering, 20 sec for NFBGA)			+220°C
Maximum Package Power Dissipation Capacity @ 25°C	DGG0056A (TSSOP) Package	DS90CF386MTD	1.61 W
	DGG0048A (TSSOP) Package	DS90CF366MTD	1.89 W
Package Derating		DS90CF386MTD	12.4 mW/°C above +25°C
		DS90CF366MTD	15 mW/°C above +25°C
Maximum Package Power Dissipation Capacity @ 25°C	NZC0064A Package	DS90CF386SLC	2.0 W
Package Derating		DS90CF386SLC	10.2 mW/°C above +25°C
ESD Rating		(HBM, 1.5 kΩ, 100 pF)	> 7 kV
		(EIAJ, 0Ω, 200 pF)	> 700V

(1) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(2) "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be ensured. They are not meant to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

Recommended Operating Conditions

	Min	Nom	Max	Units
Supply Voltage (V_{CC})	3.0	3.3	3.6	V
Operating Free Air Temperature (T_A)	−10	+25	+70	°C
Receiver Input Range	0		2.4	V
Supply Noise Voltage (V_{CC})			100	mV_{PP}

Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS/TTL DC SPECIFICATIONS						
V_{IH}	High Level Input Voltage		2.0		VCC	V
V_{IL}	Low Level Input Voltage		GND		0.8	V
V_{OH}	High Level Output Voltage	I_{OH} = - 0.4 mA	2.7	3.3		V
V_{OL}	Low Level Output Voltage	I_{OL} = 2 mA		0.06	0.3	V
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA		-0.79	-1.5	V
I_{IN}	Input Current	V_{IN} = 0.4V, 2.5V or V_{CC}		+1.8	+15	uA
		V_{IN} = GND	-10	0		uA
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V		-60	-120	mA
LVDS RECEIVER DC SPECIFICATIONS						
V_{TH}	Differential Input High Threshold	V_{CM} = +1.2V			+100	mV
V_{TL}	Differential Input Low Threshold		−100			mV
I_{IN}	Input Current	V_{IN} = +2.4V, V_{CC} = 3.6V			±10	µA
		V_{IN} = 0V, V_{CC} = 3.6V			±10	µA

(1) Typical values are given for V_{CC} = 3.3V and T_A = +25C.

Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges unless otherwise specified(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
RECEIVER SUPPLY CURRENT							
ICCRW	Receiver Supply Current Worst Case	C_L = 8 pF, Worst Case Pattern, DS90CF386 Figure 3, Figure 6	f = 32.5 MHz		49	70	mA
			f = 37.5 MHz		53	75	mA
			f = 65 MHz		81	114	mA
			f = 85 MHz		96	135	mA
ICCRW	Receiver Supply Current Worst Case	C_L = 8 pF, Worst Case Pattern, DS90CF366 Figure 3, Figure 6	f = 32.5 MHz		49	60	mA
			f = 37.5 MHz		53	65	mA
			f = 65 MHz		78	100	mA
			f = 85 MHz		90	115	mA
ICCRG	Receiver Supply Current, 16 Grayscale	C_L = 8 pF, 16 Grayscale Pattern, Figure 4, Figure 5, Figure 6	f = 32.5 MHz		28	45	mA
			f = 37.5 MHz		30	47	mA
			f = 65 MHz		43	60	mA
			f = 85 MHz		43	70	mA
ICCRZ	Receiver Supply Current Power Down(2)	$\overline{\text{Power Down}}$ = Low Receiver Outputs Stay Low during Power Down Mode			140	400	µA

(2) Current into device pins is defined as positive. Current out of device pins is defined as negative. Voltages are referenced to ground unless otherwise specified (except V_{OD} and ΔV_{OD}).

Receiver Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified(1)

Symbol	Parameter		Min	Typ(1)	Max	Units
CLHT	CMOS/TTL Low-to-High Transition Time Figure 6			2.0	3.5	ns
CHLT	CMOS/TTL High-to-Low Transition Time Figure 6			1.8	3.5	ns
RSPos0	Receiver Input Strobe Position for Bit 0 Figure 13, Figure 14	f = 85 MHz	0.49	0.84	1.19	ns
RSPos1	Receiver Input Strobe Position for Bit 1		2.17	2.52	2.87	ns
RSPos2	Receiver Input Strobe Position for Bit 2		3.85	4.20	4.55	ns
RSPos3	Receiver Input Strobe Position for Bit 3		5.53	5.88	6.23	ns
RSPos4	Receiver Input Strobe Position for Bit 4		7.21	7.56	7.91	ns
RSPos5	Receiver Input Strobe Position for Bit 5		8.89	9.24	9.59	ns
RSPos6	Receiver Input Strobe Position for Bit 6		10.57	10.92	11.27	ns
RSKM	RxIN Skew Margin(2) Figure 15	f = 85 MHz	290			ps
RCOP	RxCLK OUT Period Figure 7		11.76	T	50	ns
RCOH	RxCLK OUT High Time Figure 7	f = 85 MHz	4.5	5	7	ns
RCOL	RxCLK OUT Low Time Figure 7		4.0	5	6.5	ns
RSRC	RxOUT Setup to RxCLK OUT Figure 7		2.0			ns
RHRC	RxOUT Hold to RxCLK OUT Figure 7		3.5			ns
RCCD	RxCLK IN to RxCLK OUT Delay @ 25°C, V_{CC} = 3.3V Figure 8		5.5	7.0	9.5	ns
RPLLS	Receiver Phase Lock Loop Set Figure 9				10	ms
RPDD	Receiver Power Down Delay Figure 12				1	µs

(1) Typical values are given for V_{CC} = 3.3V and T_A = +25C.
(2) Receiver Skew Margin is defined as the valid data sampling region at the receiver inputs. This margin takes into account the transmitter pulse positions (min and max) and the receiver input setup and hold time (internal data sampling window - RSPos). This margin allows for LVDS interconnect skew, inter-symbol interference (both dependent on type/length of cable), and clock jitter (less than 150 ps).

AC Timing Diagrams

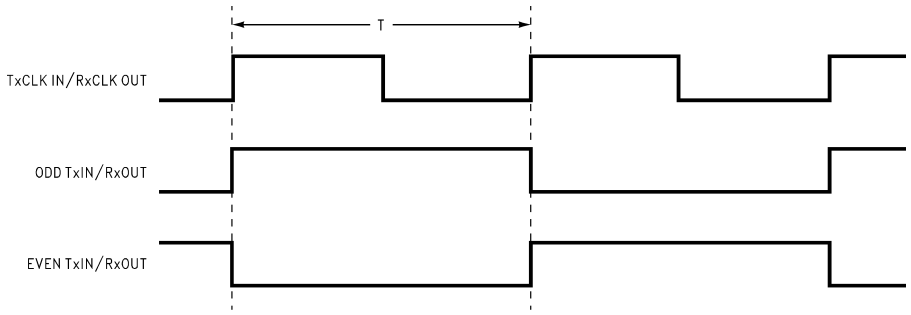
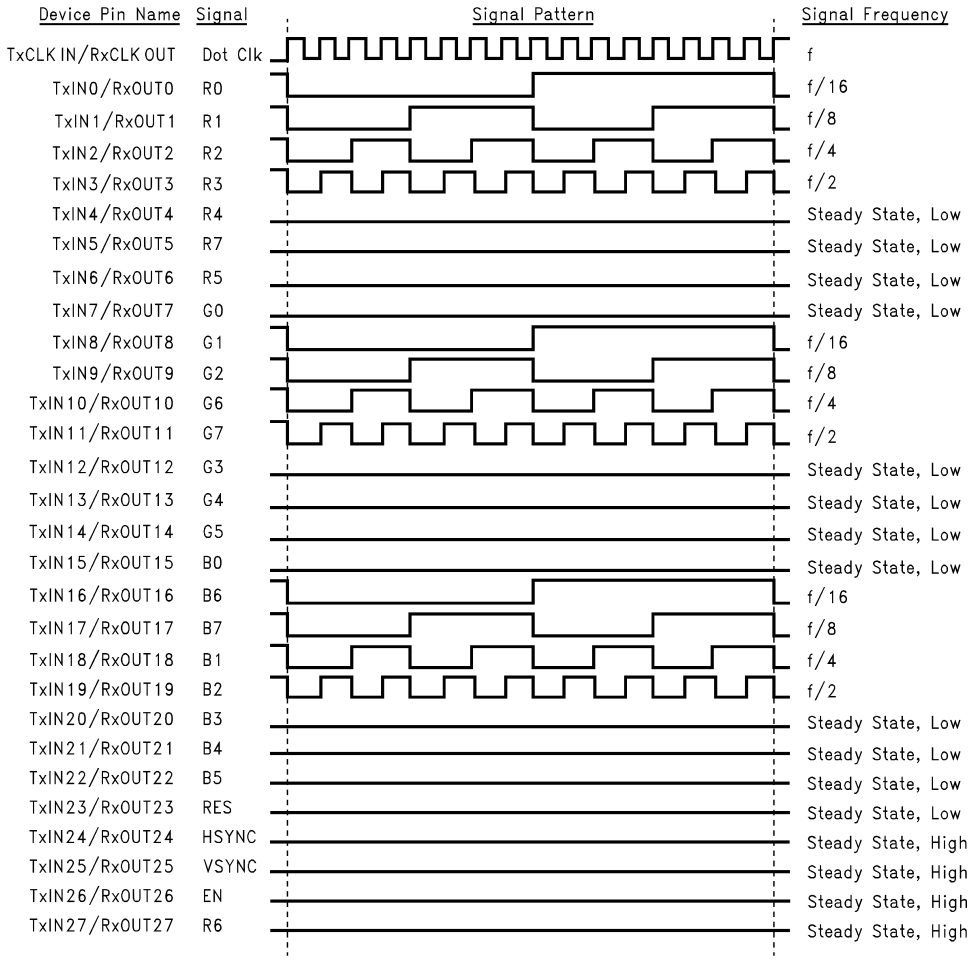


Figure 3. "Worst Case" Test Pattern



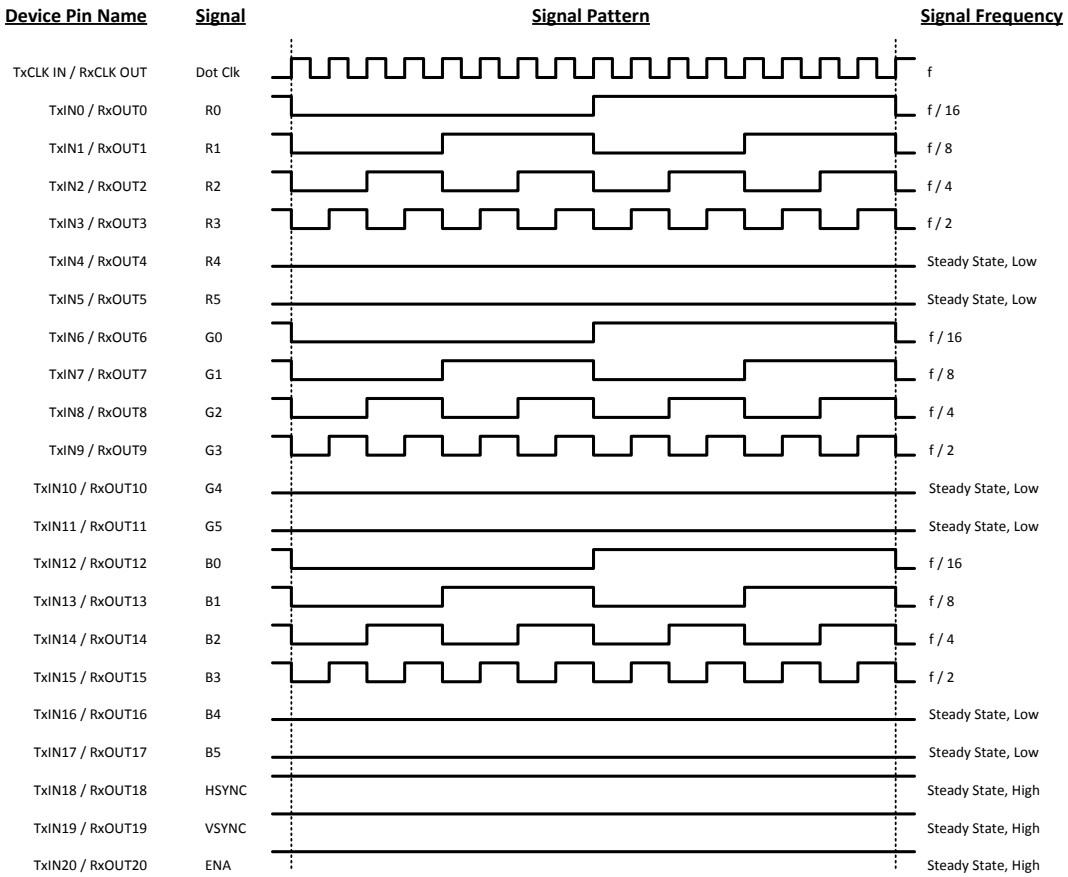
(1) The worst case test pattern produces a maximum toggling of digital circuits, LVDS I/O and CMOS/TTL I/O.

(2) The 16 grayscale test pattern tests device power consumption for a "typical" LCD display pattern. The test pattern approximates signal switching needed to produce groups of 16 vertical stripes across the display.

(3) Figure 3 and Figure 5 show a falling edge data strobe (TxCLK IN/RxCLK OUT).

(4) Recommended pin to signal mapping. Customer may choose to define differently.

Figure 4. "16 Grayscale" Test Pattern (DS90CF386)



(1) The worst case test pattern produces a maximum toggling of digital circuits, LVDS I/O and CMOS/TTL I/O.

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(3) Figure 3 and Figure 5 show a falling edge data strobe (TxCLK IN/RxCLK OUT).

(4) Recommended pin to signal mapping. Customer may choose to define differently.

Figure 5. “16 Grayscale” Test Pattern (DS90CF366)

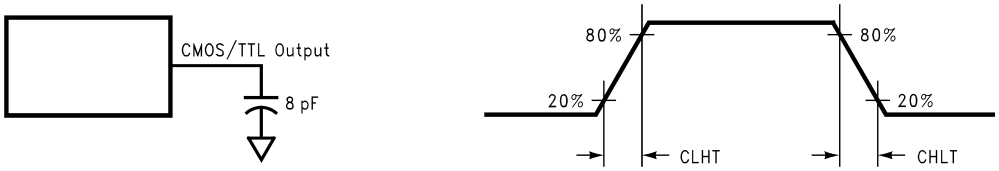


Figure 6. DS90CF386/DS90CF366 (Receiver) CMOS/TTL Output Load and Transition Times

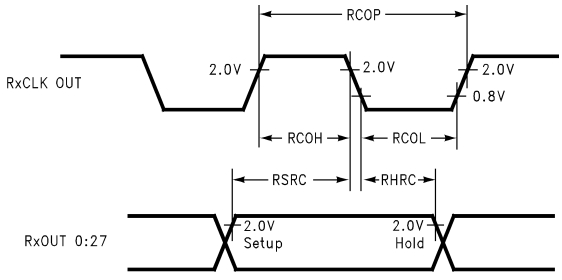


Figure 7. DS90CF386/DS90CF366 (Receiver) Setup/Hold and High/Low Times

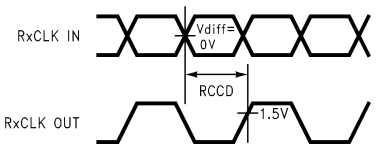


Figure 8. DS90CF386/DS90CF366 (Receiver) Clock In to Clock Out Delay

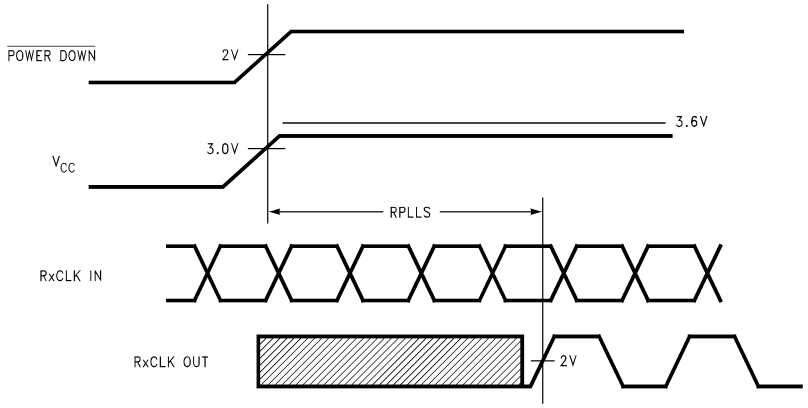


Figure 9. DS90CF386/DS90CF366 (Receiver) Phase Lock Loop Set Time

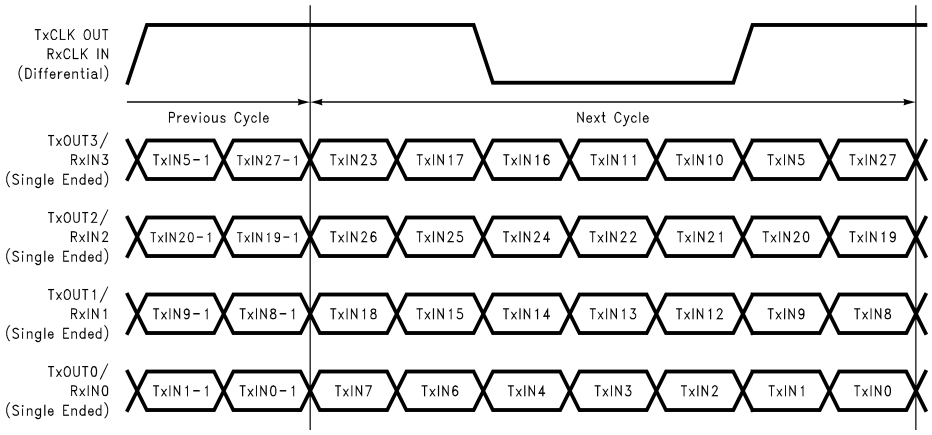


Figure 10. 28 Parallel TTL Data Inputs Mapped to LVDS Outputs - DS90CF386

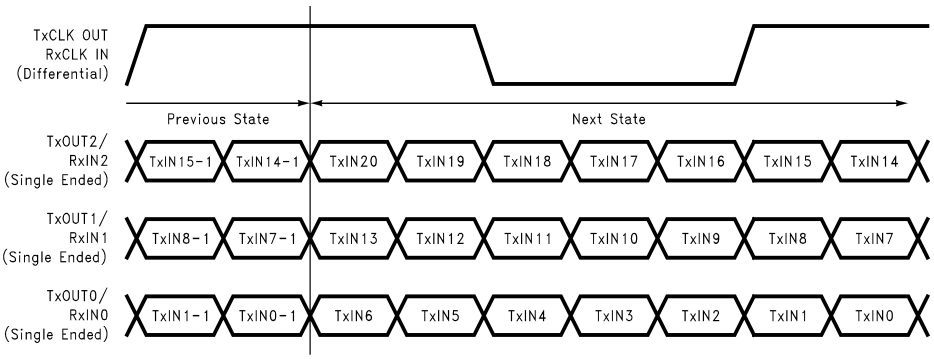


Figure 11. 21 Parallel TTL Data Inputs Mapped to LVDS Outputs - DS90CF366

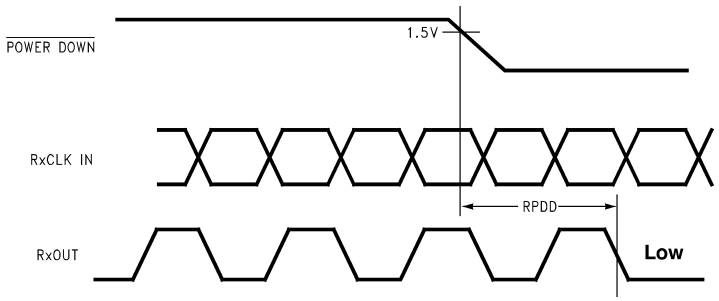


Figure 12. DS90CF386/DS90CF366 (Receiver) Power Down Delay

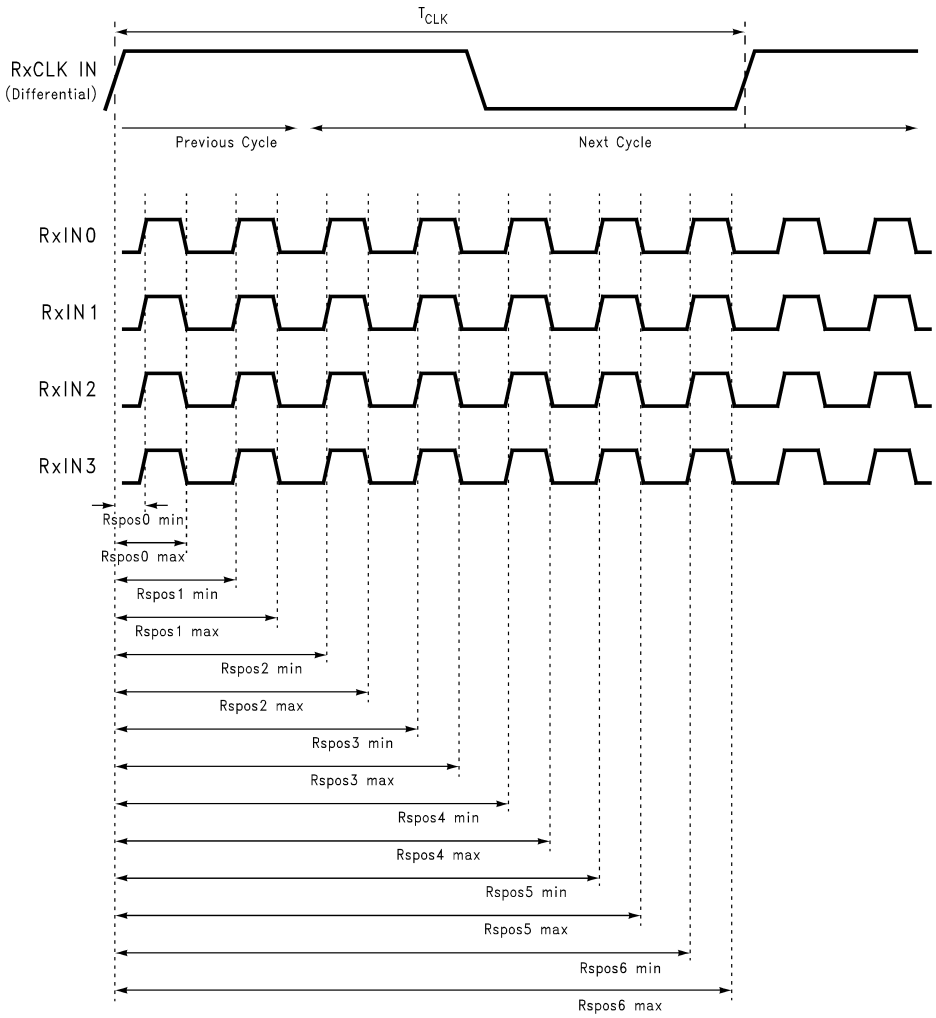


Figure 13. DS90CF386 (Receiver) LVDS Input Strobe Position

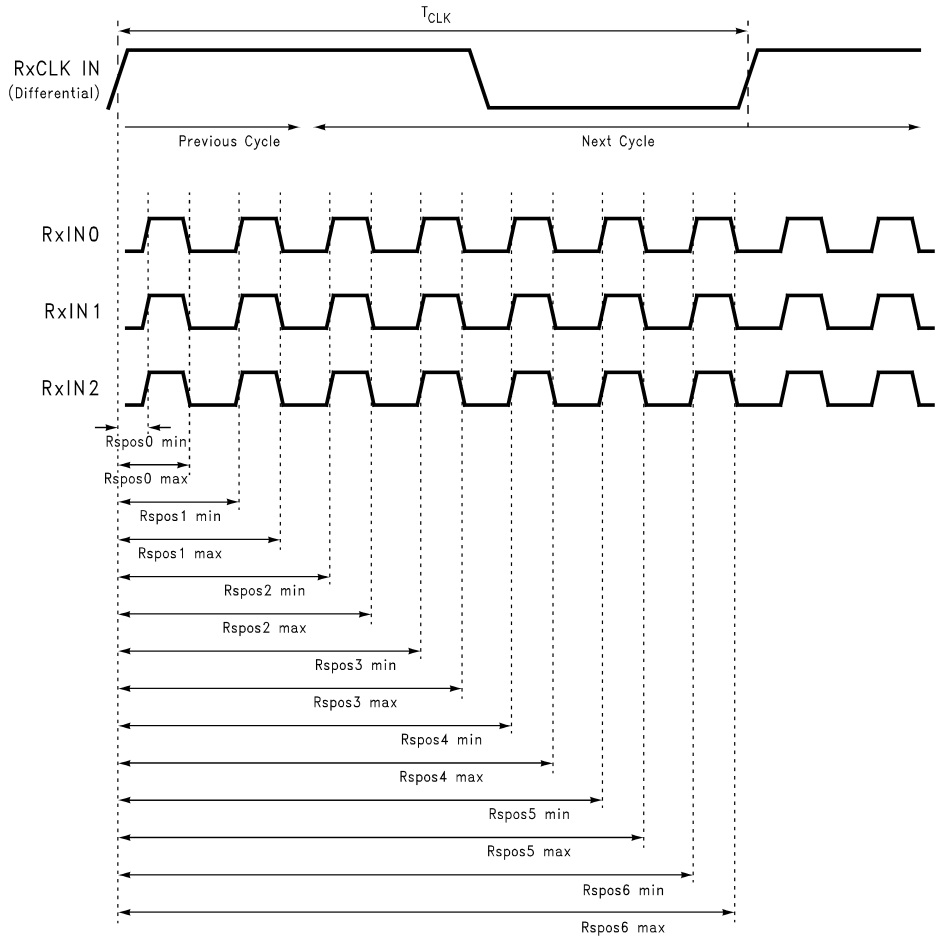
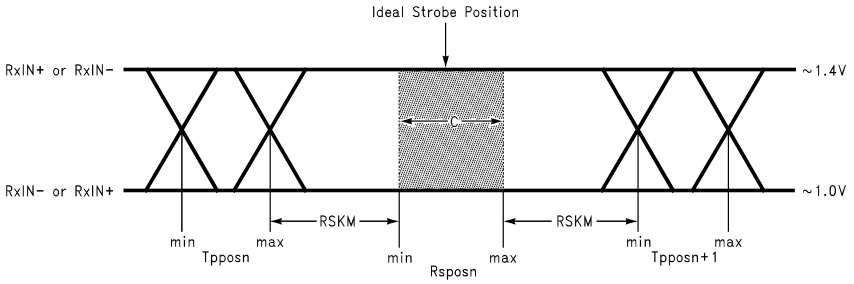


Figure 14. DS90CF366 (Receiver) LVDS Input Strobe Position



C—Setup and Hold Time (Internal data sampling window) defined by Rspos (receiver input strobe position) min and max
Tppos—Transmitter output pulse position (min and max)
RSKM = Cable Skew (type, length) + Source Clock Jitter (cycle to cycle)(1) + ISI (Inter-symbol interference)(2)
Cable Skew—typically 10 ps–40 ps per foot, media dependent

(1) Cycle-to-cycle jitter is less than 250 ps at 85 MHz.

(2) ISI is dependent on interconnect length; may be zero.

Figure 15. Receiver LVDS Input Skew Margin

DS90CF386 DGG0056A Package PIN DESCRIPTIONS—24-Bit FPD Link Receiver

Pin Name	I/O	No.	Description
RxIN+	I	4	Positive LVDS differential data inputs.
RxIN−	I	4	Negative LVDS differential data inputs.
RxOUT	O	28	TTL level data outputs. This includes: 8 Red, 8 Green, 8 Blue, and 3 control lines—FPLINE, FPFRAME, DRDY (also referred to as HSYNC, VSYNC, Data Enable).
RxCLK IN+	I	1	Positive LVDS differential clock input.
RxCLK IN−	I	1	Negative LVDS differential clock input.
RxCLK OUT	O	1	TTL level clock output. The falling edge acts as data strobe.
$\overline{\text{PWR DOWN}}$	I	1	TTL level input. When asserted (low input) the receiver outputs are low.
V_{CC}	I	4	Power supply pins for TTL outputs.
GND	I	5	Ground pins for TTL outputs.
PLL V_{CC}	I	1	Power supply for PLL.
PLL GND	I	2	Ground pin for PLL.
LVDS V_{CC}	I	1	Power supply pin for LVDS inputs.
LVDS GND	I	3	Ground pins for LVDS inputs.

DS90CF366 DGG0048A Package PIN DESCRIPTIONS—18-Bit FPD Link Receiver

Pin Name	I/O	No.	Description
RxIN+	I	3	Positive LVDS differential data inputs.
RxIN−	I	3	Negative LVDS differential data inputs.
RxOUT	O	21	TTL level data outputs. This includes: 6 Red, 6 Green, 6 Blue, and 3 control lines—FPLINE, FPFRAME, DRDY (also referred to as HSYNC, VSYNC, Data Enable).
RxCLK IN+	I	1	Positive LVDS differential clock input.
RxCLK IN−	I	1	Negative LVDS differential clock input.
RxCLK OUT	O	1	TTL level clock output. The falling edge acts as data strobe.
$\overline{\text{PWR DOWN}}$	I	1	TTL level input. When asserted (low input) the receiver outputs are low.
V_{CC}	I	4	Power supply pins for TTL outputs.
GND	I	5	Ground pins for TTL outputs.
PLL V_{CC}	I	1	Power supply for PLL.
PLL GND	I	2	Ground pin for PLL.
LVDS V_{CC}	I	1	Power supply pin for LVDS inputs.
LVDS GND	I	3	Ground pins for LVDS inputs.

DS90CF386 — 64 ball NFBGA package PIN DESCRIPTIONS — FPD Link Receiver

Pin Name	I/O	No.	Description
RxIN+	I	4	Positive LVDS differential data inputs.
RxIN−	I	4	Negative LVDS differential data inputs.
RxOUT	O	28	TTL level data outputs. This includes: 8 Red, 8 Green, 8 Blue, and 4 control lines—FPLINE, FPFRAME, DRDY (also referred to as HSYNC, VSYNC, Data Enable).
RxCLK IN+	I	1	Positive LVDS differential clock input.
RxCLK IN−	I	1	Negative LVDS differential clock input.
FPSHIFT OUT	O	1	TTL level clock output. The falling edge acts as data strobe. Pin name RxCLK OUT.
$\overline{\text{PWR DOWN}}$	I	1	TTL level input. When asserted (low input) the receiver outputs are low.
V_{CC}	I	4	Power supply pins for TTL outputs.
GND	I	5	Ground pins for TTL outputs.
PLL V_{CC}	I	1	Power supply for PLL.
PLL GND	I	2	Ground pin for PLL.
LVDS V_{CC}	I	1	Power supply pin for LVDS inputs.
LVDS GND	I	3	Ground pins for LVDS inputs.
NC		6	Pins not connected.

DS90CF386 Pin Descriptions — 64 ball NFBGA Package — FPD Link Receiver

By Pin			By Pin Type		
Pin	Pin Name	Type	Pin	Pin Name	Type
A1	RxOUT17	O	A4	GND	G
A2	VCC	P	B1	GND	G
A3	RxOUT15	O	B6	GND	G
A4	GND	G	D8	GND	G
A5	RxOUT12	O	E3	GND	G
A6	RxOUT8	O	E5	LVDS GND	G
A7	RxOUT7	O	G3	LVDS GND	G
A8	RxOUT6	O	G7	LVDS GND	G
B1	GND	G	H5	LVDS GND	G
B2	NC		F6	PLL GND	G
B3	RxOUT16	O	G8	PLL GND	G
B4	RxOUT11	O	E6	PWR DWN	I
B5	VCC	P	H6	RxCLKIN-	I
B6	GND	G	H7	RxCLKIN+	I
B7	RxOUT5	O	H2	RxIN0-	I
B8	RxOUT3	O	H3	RxIN0+	I
C1	RxOUT21	O	F4	RxIN1-	I
C2	NC		G4	RxIN1+	I
C3	RxOUT18	O	G5	RxIN2-	I
C4	RxOUT14	O	F5	RxIN2+	I
C5	RxOUT9	O	G6	RxIN3-	I
C6	RxOUT4	O	H8	RxIN3+	I
C7	NC		E7	RxCLKOUT	O
C8	RxOUT1	O	E8	RxOUT0	O
D1	VCC	P	C8	RxOUT1	O
D2	RxOUT20	O	D5	RxOUT10	O
D3	RxOUT19	O	B4	RxOUT11	O
D4	RxOUT13	O	A5	RxOUT12	O
D5	RxOUT10	O	D4	RxOUT13	O

DS90CF386 Pin Descriptions — 64 ball NFBGA Package — FPD Link Receiver (continued)

By Pin			By Pin Type		
D6	VCC	P	C4	RxOUT14	O
D7	RxOUT2	O	A3	RxOUT15	O
D8	GND	G	B3	RxOUT16	O
E1	RxOUT22	O	A1	RxOUT17	O
E2	RxOUT24	O	C3	RxOUT18	O
E3	GND	G	D3	RxOUT19	O
E4	LVDS VCC	P	D7	RxOUT2	O
E5	LVDS GND	G	D2	RxOUT20	O
E6	PWR DWN	I	C1	RxOUT21	O
E7	RxCLKOUT	O	E1	RxOUT22	O
E8	RxOUT0	O	F1	RxOUT23	O
F1	RxOUT23	O	E2	RxOUT24	O
F2	RxOUT26	O	G1	RxOUT25	O
F3	NC		F2	RxOUT26	O
F4	RxIN1-	I	H1	RxOUT27	O
F5	RxIN2+	I	B8	RxOUT3	O
F6	PLL GND	G	C6	RxOUT4	O
F7	PLL VCC	P	B7	RxOUT5	O
F8	NC		A8	RxOUT6	O
G1	RxOUT25	O	A7	RxOUT7	O
G2	NC		A6	RxOUT8	O
G3	LVDS GND	G	C5	RxOUT9	O
G4	RxIN1+	I	E4	LVDS VCC	P
G5	RxIN2-	I	H4	LVDS VCC	P
G6	RxIN3-	I	F7	PLL VCC	P
G7	LVDS GND	G	A2	VCC	P
G8	PLL GND	G	B5	VCC	P
H1	RxOUT27	O	D1	VCC	P
H2	RxIN0-	I	D6	VCC	P
H3	RxIN0+	I	B2	NC	
H4	LVDS VCC	P	C2	NC	
H5	LVDS GND	G	C7	NC	
H6	RxCLKIN-	I	F3	NC	
H7	RxCLKIN+	I	F8	NC	
H8	RxIN3+	I	G2	NC	

Pin Diagrams for TSSOP Packages

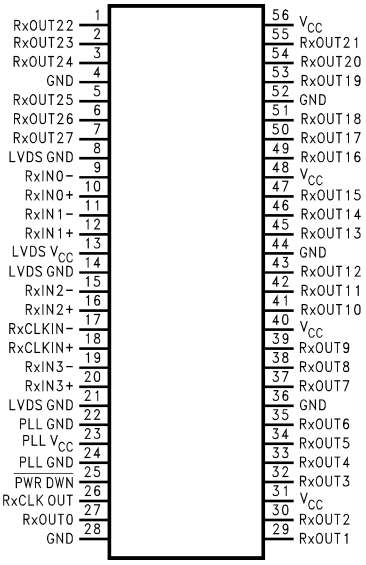


Figure 16. DS90CF386MTD

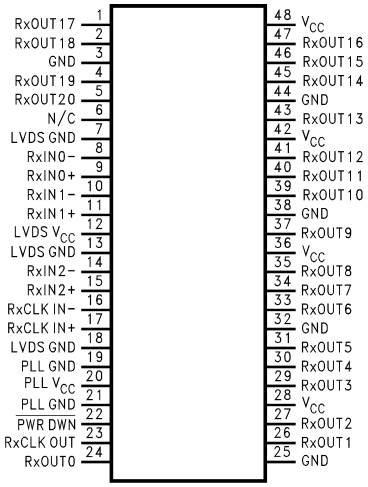


Figure 17. DS90CF366MTD

APPLICATIONS INFORMATION

POWER SEQUENCING AND POWERDOWN MODE

Outputs of the transmitter remain in TRI-STATE until the power supply reaches 2V. Clock and data outputs will begin to toggle 10 ms after V_{CC} has reached 3V and the Powerdown pin is above 1.5V. Either device may be placed into a powerdown mode at any time by asserting the Powerdown pin (active low). Total power dissipation for each device will decrease to 5 µW (typical).

The transmitter input clock may be applied prior to powering up and enabling the transmitter. The transmitter input clock may also be applied after power up; however, the use of the PWR DOWN pin is required. Do not power up and enable (PWR DOWN = HIGH) the transmitter without a valid clock signal applied to the TxCLK IN pin.

The FPD Link chipset is designed to protect itself from accidental loss of power to either the transmitter or receiver. If power to the transmit board is lost, the receiver clocks (input and output) stop. The data outputs (RxOUT) retain the states they were in when the clocks stopped. When the receiver board loses power, the receiver inputs are controlled by a failsafe bias circuitry. The LVDS inputs are High-Z during initial power on and power off conditions. Current is limited (5 mA per input) by the fixed current mode drivers, thus avoiding the potential for latchup when powering the device.

REVISION HISTORY

Changes from Revision H (April 2013) to Revision I	Page
• Changed layout of National Data Sheet to TI format	12

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS90CF366MTD/NOPB	ACTIVE	TSSOP	DGG	48	38	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-10 to 70	DS90CF366MTD >B	Samples
DS90CF366MTDX/NOPB	ACTIVE	TSSOP	DGG	48	1000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-10 to 70	DS90CF366MTD >B	Samples
DS90CF386MTD	NRND	TSSOP	DGG	56	34	TBD	Call TI	Call TI	-10 to 70	DS90CF386MTD >B	
DS90CF386MTD/NOPB	ACTIVE	TSSOP	DGG	56	34	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-10 to 70	DS90CF386MTD >B	Samples
DS90CF386MTDX/NOPB	ACTIVE	TSSOP	DGG	56	1000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-10 to 70	DS90CF386MTD >B	Samples
DS90CF386SLC/NOPB	ACTIVE	NFBGA	NZC	64	360	Green (RoHS & no Sb/Br)	SNAGCU	Level-4-260C-72 HR	-10 to 70	DS90CF386 SLC >B	Samples
DS90CF386SLCX/NOPB	ACTIVE	NFBGA	NZC	64	2000	Green (RoHS & no Sb/Br)	SNAGCU	Level-4-260C-72 HR	-10 to 70	DS90CF386 SLC >B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

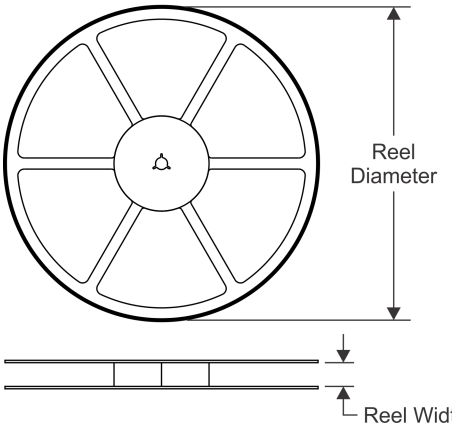
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

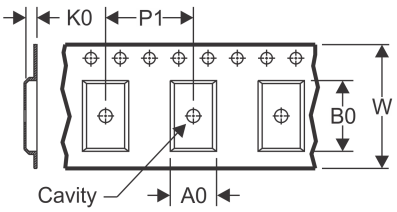
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

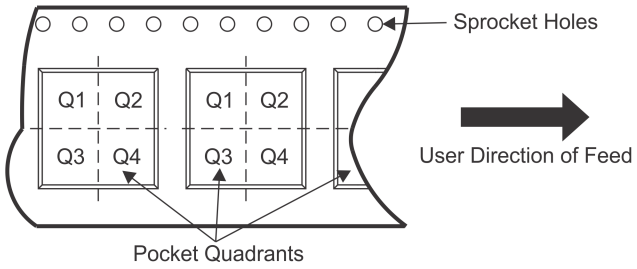


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

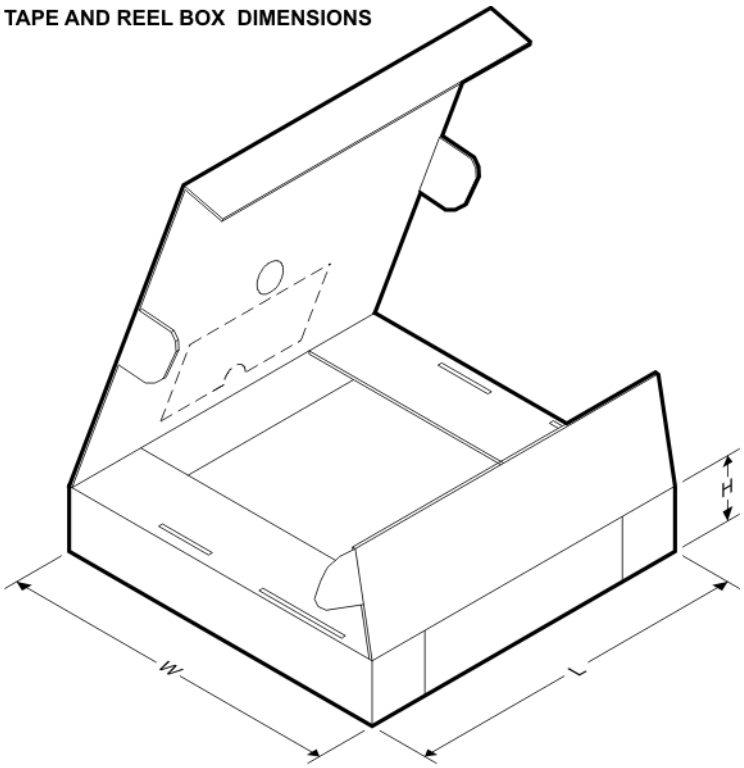
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS90CF366MTDX/NOPB	TSSOP	DGG	48	1000	330.0	24.4	8.6	13.2	1.6	12.0	24.0	Q1
DS90CF386MTDX/NOPB	TSSOP	DGG	56	1000	330.0	24.4	8.6	14.5	1.8	12.0	24.0	Q1
DS90CF386SLCX/NOPB	NFBGA	NZC	64	2000	330.0	16.4	8.3	8.3	2.3	12.0	16.0	Q1

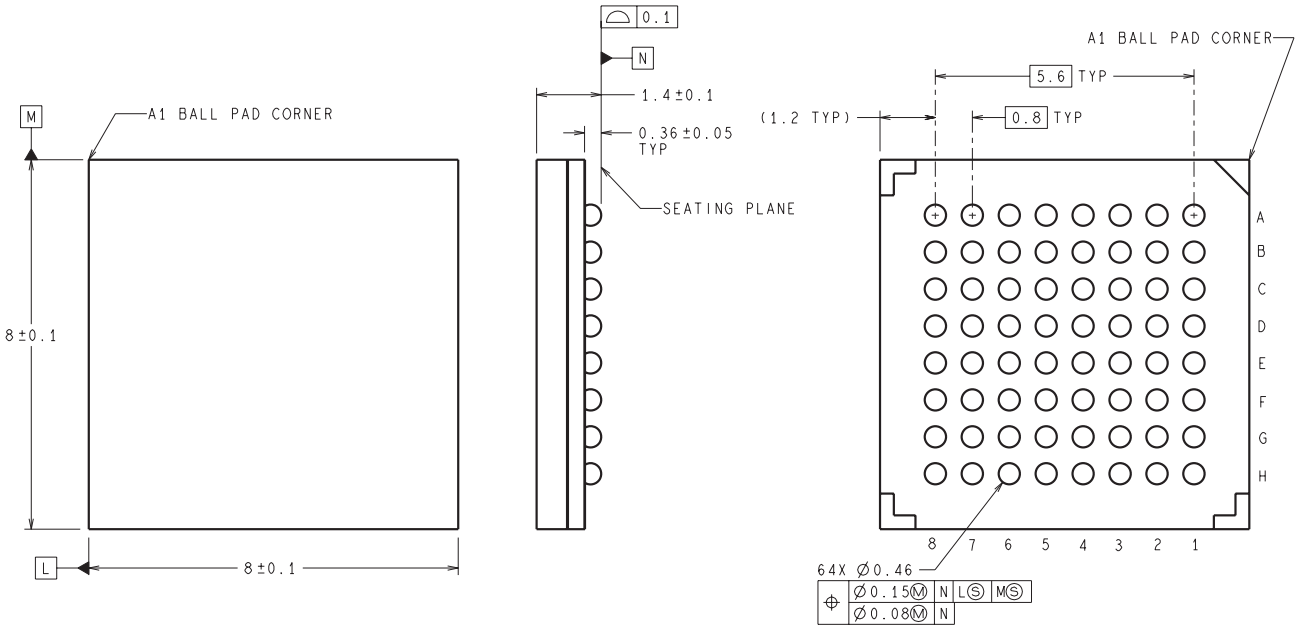
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS90CF366MTDX/NOPB	TSSOP	DGG	48	1000	367.0	367.0	45.0
DS90CF386MTDX/NOPB	TSSOP	DGG	56	1000	367.0	367.0	45.0
DS90CF386SLCX/NOPB	NFBGA	NZC	64	2000	367.0	367.0	38.0

NZC0064A



DIMENSIONS ARE IN MILLIMETERS

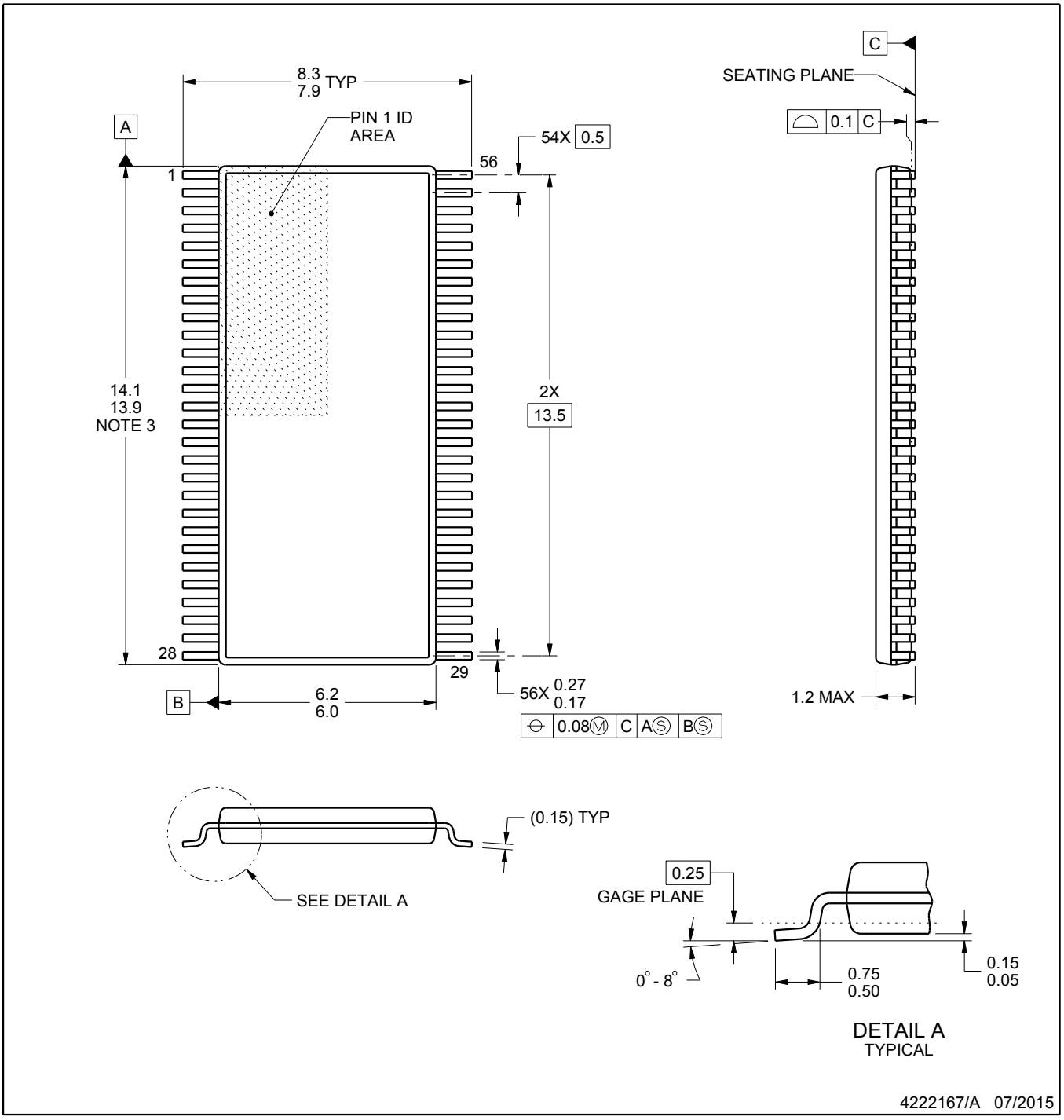
SLC64A (Rev C)

PACKAGE OUTLINE

DGG0056A

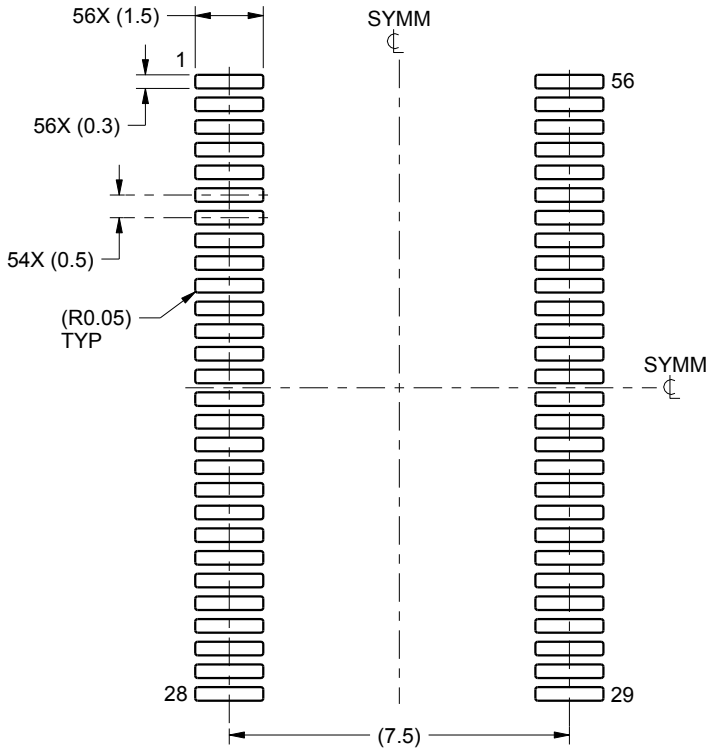
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

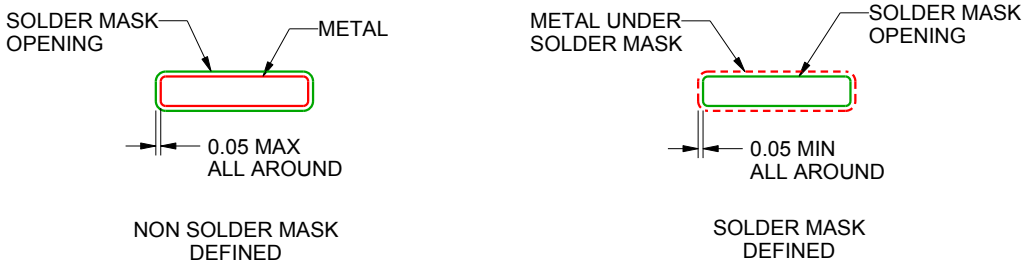


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
SCALE:6X

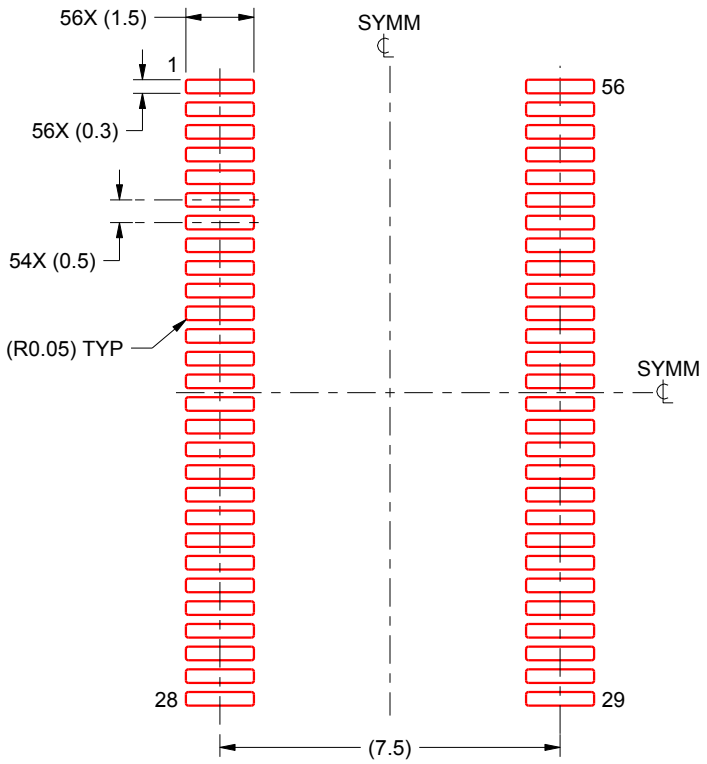


SOLDER MASK DETAILS

4222167/A 07/2015

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

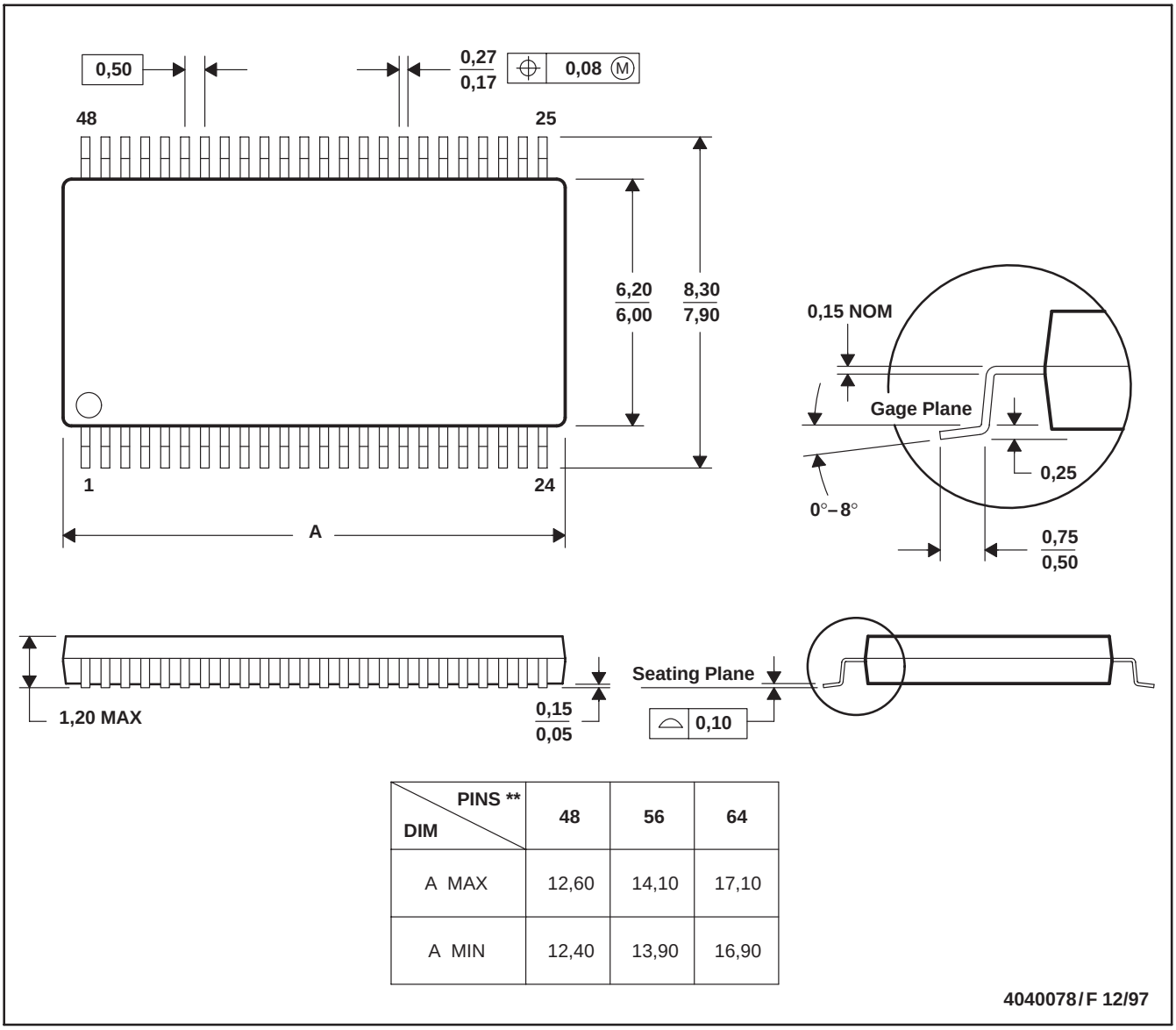
4222167/A 07/2015

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DGG (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



DIM \ PINS **	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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