

## DS90CP04 1.5 Gbps 4x4 LVDS Crosspoint Switch

Check for Samples: [DS90CP04](#)

### FEATURES

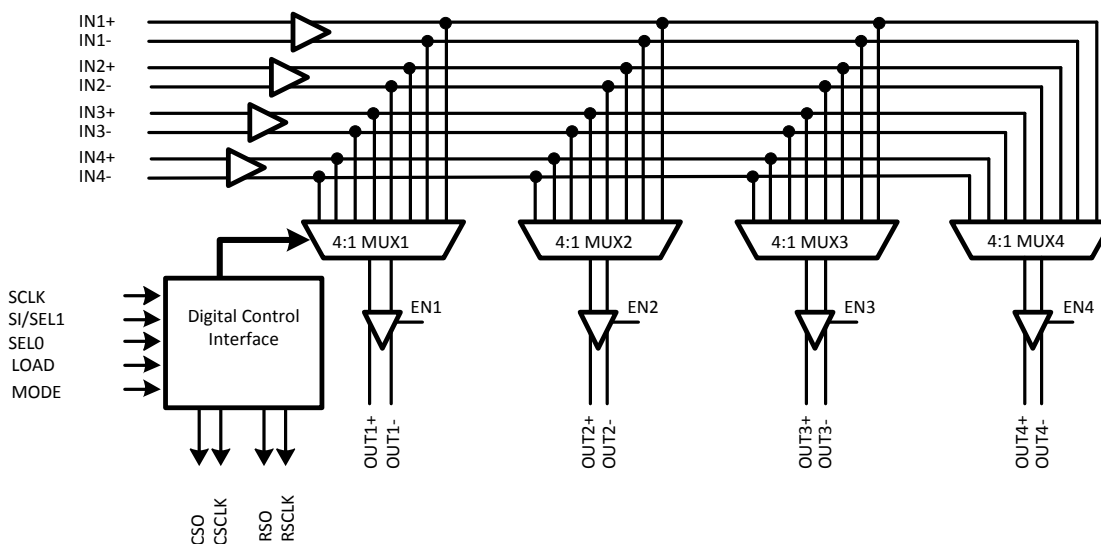
- DC - 1.5 Gbps Low Jitter, Low Skew Operation
- Pin and Serial Interface Configurable, Fully Differential, Non-blocking Architecture
- Wide Input Common Mode Voltage Range Enables Easy Interface to LVDS/LVPECL/2.5V-CML Drivers
- TRI-STATE LVDS Outputs
- Serial Control Interface with Read-back Capability
- Double Register Loading
- Single +2.5V Supply
- Small 6x6 mm WQFN-32 Space Saving Package
- Fabricated with Advanced CMOS Process Technology

### DESCRIPTION

DS90CP04 is a 4x4 digital cross-point switch with broadside input and output pins for efficient board layout. It utilizes Low Voltage Differential Swing (LVDS) technology for low power, high-speed operation. Data paths are fully differential from input to output for low noise. The non-blocking architecture allows connections of any input to any output or outputs. The switch matrix consists of four differential 4:1 multiplexes. Each output channel connects to one of the four inputs common to all multiplexers.

A simple serial control interface or a configuration select port is activated by the state of the MODE pin. When utilizing the serial control interface a single load command will update the new switch configuration for all outputs simultaneously.

### Functional Block Diagrams



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

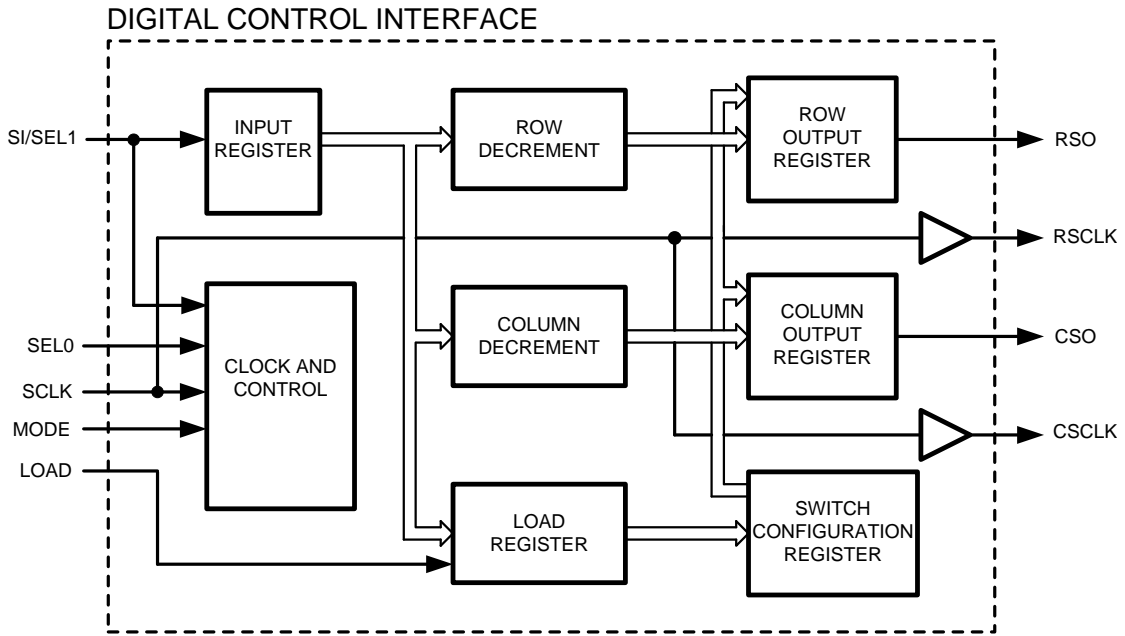


Figure 1. Functional Block Diagram

Connection Diagram

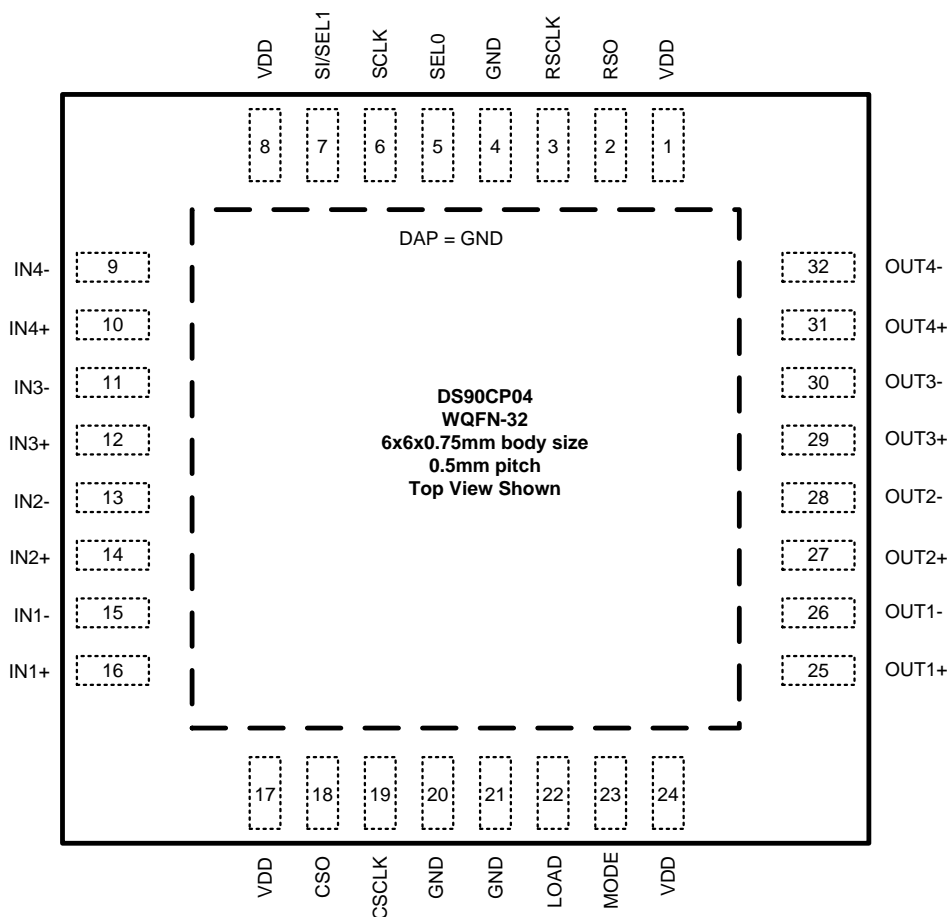


Figure 2. Connection Diagram - 32 Pin (Top View)  
See Package Number NJE0032A

PIN DESCRIPTIONS

| Pin Name                                       | Pin Number | I/O, Type | Description  |
|--|------------|-----------|--|
| <b>DIFFERENTIAL INPUTS COMMON TO ALL MUXES</b> |            |           |  |
| IN1+<br>IN1-                                   | 16<br>15   | I, LVDS   | Inverting and non-inverting differential inputs.   |
| IN2+<br>IN2-                                   | 14<br>13   | I, LVDS   | Inverting and non-inverting differential inputs.   |
| IN3+<br>IN3-                                   | 12<br>11   | I, LVDS   | Inverting and non-inverting differential inputs.   |
| IN4+<br>IN4-                                   | 10<br>9    | I, LVDS   | Inverting and non-inverting differential inputs.   |
| <b>SWITCHED DIFFERENTIAL OUTPUTS</b>           |            |           |  |
| OUT1+<br>OUT1-                                 | 25<br>26   | O, LVDS   | Inverting and non-inverting differential outputs. OUT1± can be connected to any one pair IN1±, IN2±, IN3±, or IN4± |
| OUT2+<br>OUT2-                                 | 27<br>28   | O, LVDS   | Inverting and non-inverting differential outputs. OUT2± can be connected to any one pair IN1±, IN2±, IN3±, or IN4± |
| OUT3+<br>OUT3-                                 | 29<br>30   | O, LVDS   | Inverting and non-inverting differential outputs. OUT3± can be connected to any one pair IN1±, IN2±, IN3±, or IN4± |
| OUT4+<br>OUT4-                                 | 31<br>32   | O, LVDS   | Inverting and non-inverting differential outputs. OUT4± can be connected to any one pair IN1±, IN2±, IN3±, or IN4± |

**PIN DESCRIPTIONS (continued)**

| Pin Name                         | Pin Number        | I/O, Type | Description  |
|----------------------------------|-------------------|-----------|--|
| <b>DIGITAL CONTROL INTERFACE</b> |                   |           |  |
| SCLK                             | 6                 | I, LVCMOS | Control clock to latch in programming data at SI. SCLK can be 0 MHz to 100 MHz. SCLK should be burst of clock pulses active only while accessing the device. After completion of programming, SCLK should be kept at logic low to minimize potential noise injection into the high-speed differential data paths.  |
| SI / SEL1                        | 7                 | I, LVCMOS | Programming data to select the switch configuration. Data is latched into the input buffer register at the rising edge of SCLK.  |
| SEL0                             | 5                 | I, LVCMOS | Programming data to select the switch configuration.   |
| CSO<br>RSO                       | 18<br>2           | O, LVCMOS | With MODE low, control data is shifted out at CSO (RSO) for cascading to the next device in the serial chain. The control data at CSO (RSO) is identical to that shifted in at SI with the exception of the device column (row) address being decremented by one internally before propagating to the next device in the chain. CSO (RSO) is clocked out at the rising edge of SCLK. |
| CSCLK<br>RSCLK                   | 19<br>3           | O, LVCMOS | With MODE low, these pins function as a buffered control clock from SCLK. CSCLK (RSCLK) is used for cascading the serial control bus to the next device in the serial chain.   |
| LOAD                             | 22                | I, LVCMOS | When LOAD is high and SCLK makes a LH transition, the device transfers the programming data in the load register into the configuration registers. The new switch configuration for all outputs takes effect. LOAD needs to remain high for only one SCLK cycle to complete the process, holding LOAD high longer repeats the transfer to the configuration register.                |
| MODE                             | 23                | I, LVCMOS | When MODE is low, the SCLK is active and a buffered SCLK signal is present at the CLKOUT output. When MODE is high, the SCLK signal is uncoupled from register and state machine internals. Internal registers will see an active low signal until MODE is brought Low again.  |
| <b>POWER</b>                     |                   |           |  |
| V <sub>DD</sub>                  | 1, 8, 17,<br>24   | I, Power  | V <sub>DD</sub> = 2.5V ±5%. At least 4 low ESR 0.01 µF bypass capacitors should be connected from V <sub>DD</sub> to GND plane.  |
| GND                              | 4, 20, 21,<br>DAP | I, Power  | Ground reference to LVDS and CMOS circuitry. DAP is the exposed metal contact at the bottom of the WQFN-32 package. The DAP is used as the primary GND connection to the device. It should be connected to the ground plane with at least 4 vias for optimal AC and thermal performance.   |

**Serial Interface Truth Table**

| LOAD | MODE | SCLK | Resulting Action  |
|------|------|------|---|
| 0    | 0    | LH   | The current state on SI is clocked into the input shift register.   |
| 0    | 1    | LH   | Uncouples SCLK input from internal registers and state machine inputs. The RSCLK and CSCLK outputs will drive an active Low signal until MODE is brought Low again. See Configuration Select Truth Table below. |
| LH   | 0    | X    | Loads OUT1–OUT4 configuration information from last valid frame. Places contents of load register into the configuration register. The switch configuration is updated asynchronously from the SCLK input.      |
| 1    | 1    | LH   | Uncouples SCLK input from internal registers and state machine inputs. The RSCLK and CSCLK outputs will drive an active Low signal until MODE is brought Low again. See Configuration Select Truth Table below. |

**Configuration Select Truth Table**

| MODE | SEL1 | SEL0 | Resulting Action   |
|------|------|------|--|
| 0    | X    | X    | The SEL0/1 pins only function in configuration select mode. See below. |
| 1    | 0    | 0    | Distribution: IN1 - OUT1 OUT2 OUT3 OUT4                                |
| 1    | 0    | 1    | Distribution: IN2 - OUT1 OUT2 OUT3 OUT4                                |
| 1    | 1    | 0    | Redundancy: IN1 - OUT1 OUT2 and IN3 - OUT3 OUT4                        |
| 1    | 1    | 1    | Broadside: IN1 - OUT1, IN2 - OUT2, IN3 - OUT3, IN4 - OUT4              |

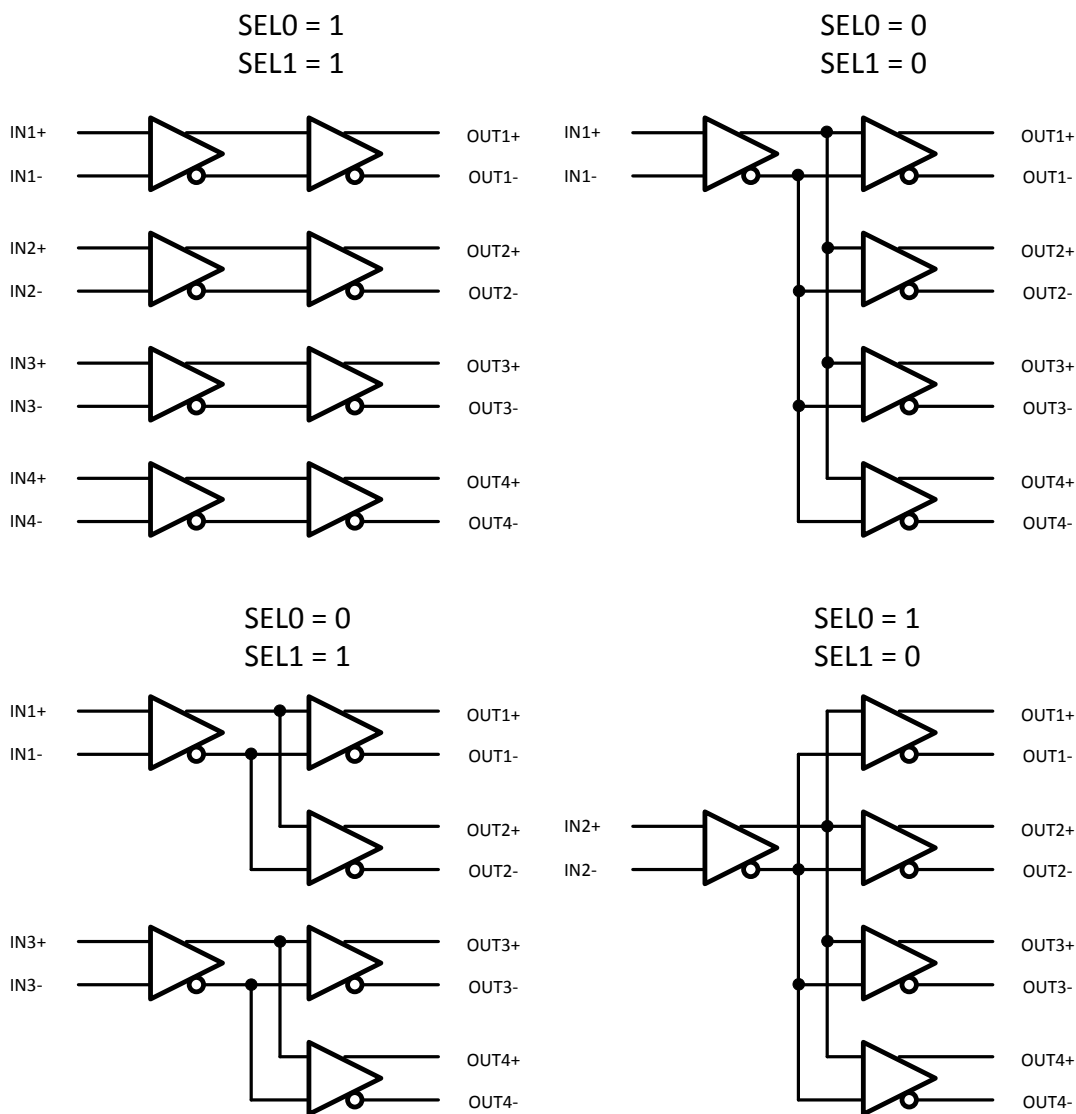


Figure 3. DS90CP04 Configuration Select Decode



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

**Absolute Maximum Ratings** <sup>(1)(2)</sup>

|   |                              |
|---|------------------------------|
| Supply Voltage ( $V_{DD}$ )               | -0.3V to +3V                 |
| CMOS/TTL Input Voltage                    | -0.3V to ( $V_{DD} + 0.3V$ ) |
| LVDS Receiver Input Voltage               | -0.3V to +3.3V               |
| LVDS Driver Output Voltage                | -0.3V to +3V                 |
| LVDS Output Short Circuit Current         | 40mA                         |
| Junction Temperature                      | +150°C                       |
| Storage Temperature                       | -65°C to +150°C              |
| Lead Temperature<br>(Soldering, 4 sec.)   | +260°C                       |
| Maximum Package Power Dissipation at 25°C |                              |
| WQFN-32                                   | 3200 mW                      |
| Derating above 25°C                       | 38 mW/°C                     |
| Thermal Resistance, $\theta_{JA}$         | 26.4°C/W                     |
| ESD Rating                                |                              |
| HBM, 1.5 k $\Omega$ , 100 pF              |                              |
| LVDS Outputs                              | >1.0 kV                      |
| LVDS Inputs                               | >1.5 kV                      |
| All Other Pins                            | >4.0 kV                      |
| EIAJ, 0 $\Omega$ , 200 pF                 | >100V                        |

- (1) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.  
(2) "Absolute Maximum Ratings" are the ratings beyond which the safety of the device cannot be ensured. They are not meant to imply that the device should be operated at these limits.

**Recommended Operating Conditions**

|                                  | Min   | Typ | Max   | Unit |
|----------------------------------|-------|-----|-------|------|
| Supply Voltage ( $V_{DD}$ - GND) | 2.375 | 2.5 | 2.625 | V    |
| Receiver Input Voltage           | 0.05  |     | 3.3   | V    |
| Operating Free Air Temperature   | -40   | 25  | 85    | °C   |
| Junction Temperature             |       |     | 110   | °C   |

**Electrical Characteristics**

Over recommended operating supply and temperature ranges unless other specified. <sup>(1)</sup>

| Symbol   | Parameter                 | Conditions                                | Min  | Typ <sup>(2)</sup> | Max      | Units   |
|--|---------------------------|---|------|--------------------|----------|---------|
| <b>LVCMOS/LVTTL DC SPECIFICATIONS (SCLK, SI/SEL1, SEL0, LOAD, MODE, CSCLK, RSCLK, CSO, RSO)</b>                          |                           |   |      |                    |          |         |
| $V_{IH}$   | High Level Input Voltage  |   | 1.7  |                    | $V_{DD}$ | V       |
| $V_{IL}$   | Low Level Input Voltage   |   | GND  |                    | 0.7      | V       |
| $I_{IH}$   | High Level Input Current  | $V_{IN} = V_{DD} = V_{DDMAX}$             | -10  |                    | +10      | $\mu$ A |
| $I_{IL}$   | Low Level Input Current   | $V_{IN} = V_{SS}, V_{DD} = V_{DDMAX}$     | -10  |                    | +10      | $\mu$ A |
| $C_{IN1}$  | Input Capacitance         | Any Digital Input Pin to $V_{SS}$         |      | 3.5                |          | pF      |
| $C_{OUT1}$   | Output Capacitance        | Any Digital Output Pin to $V_{SS}$        |      | 5.5                |          | pF      |
| $V_{CL}$   | Input Clamp Voltage       | $I_{CL} = -18$ mA                         | -1.5 | -0.8               |          | V       |
| $V_{OH}$   | High Level Output Voltage | $I_{OH} = -4.0$ mA, $V_{DD} = V_{DDMIN}$  | 1.9  |                    |          | V       |
|  |                           | $I_{OH} = -100$ $\mu$ A, $V_{DD} = 2.5$ V | 2.4  |                    |          | V       |
| $V_{OL}$   | Low Level Output Voltage  | $I_{OL} = 4.0$ mA, $V_{DD} = V_{DDMIN}$   |      |                    | 0.4      | V       |
|  |                           | $I_{OL} = 100$ $\mu$ A, $V_{DD} = 2.5$ V  |      |                    | 0.1      | V       |
| <b>LVDS INPUT DC SPECIFICATIONS (IN1<math>\pm</math>, IN2<math>\pm</math>, IN3<math>\pm</math>, IN4<math>\pm</math>)</b> |                           |   |      |                    |          |         |

- (1) "Absolute Maximum Ratings" are the ratings beyond which the safety of the device cannot be ensured. They are not meant to imply that the device should be operated at these limits.  
(2) Typical parameters are measured at  $V_{DD} = 2.5$ V,  $T_A = 25^\circ$ C. They are for reference purposes, and are not production-tested.

## Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges unless other specified. <sup>(1)</sup>

| Symbol   | Parameter  | Conditions  | Min   | Typ <sup>(2)</sup> | Max             | Units |
|--|--|---|-------|--------------------|-----------------|-------|
| V <sub>TH</sub>  | Differential Input High Threshold <sup>(3)</sup>         | V <sub>CM</sub> = 0.05V or 1.2V or 2.45V, V <sub>DD</sub> = 2.5V  |       | 0                  | 50              | mV    |
| V <sub>TL</sub>  | Differential Input Low Threshold                         | V <sub>CM</sub> = 0.05V or 1.2V or 2.45V, V <sub>DD</sub> = 2.5V  | -50   | 0                  |                 | mV    |
| V <sub>ID</sub>  | Differential Input Voltage                               | V <sub>DD</sub> = 2.5V, V <sub>CM</sub> = 0.05V to 2.45V  | 100   |                    | V <sub>DD</sub> | mV    |
| V <sub>CMR</sub>   | Common Mode Voltage Range                                | V <sub>ID</sub> = 100 mV, V <sub>DD</sub> = 2.5V  | 0.05  |                    | 3.25            | V     |
| C <sub>IN2</sub>   | Input Capacitance  | IN+ or IN- to V <sub>SS</sub>   |       | 3.5                |                 | pF    |
| I <sub>IN</sub>  | Input Current  | V <sub>IN</sub> = 2.5V, V <sub>DD</sub> = V <sub>DDMAX</sub> or 0V                                      | -10   |                    | +10             | μA    |
|  |  | V <sub>IN</sub> = 0V, V <sub>DD</sub> = V <sub>DDMAX</sub> or 0V  | -10   |                    | +10             | μA    |
| <b>LVDS OUTPUT DC SPECIFICATIONS (OUT1±, OUT2±, OUT3±, OUT4±)</b>      |  |   |       |                    |                 |       |
| V <sub>OD</sub>  | Differential Output Voltage <sup>(3)</sup>               | R <sub>L</sub> = 100Ω between OUT+ and OUT- (see Figure 4)  | 250   | 400                | 475             | mV    |
| ΔV <sub>OD</sub>   | Change in V <sub>OD</sub> between Complementary States   |   | -35   |                    | 35              | mV    |
| V <sub>OS</sub>  | Offset Voltage <sup>(4)</sup>                            |   | 1.125 | 1.25               | 1.375           | V     |
| ΔV <sub>OS</sub>   | Change in V <sub>OS</sub> between Complementary States   |   | -35   |                    | 35              | mV    |
| I <sub>OZ</sub>  | Output TRI-STATE Current                                 | TRI-STATE Output<br>V <sub>OUT</sub> = V <sub>DD</sub> or V <sub>SS</sub>                               | -10   |                    | +10             | μA    |
| I <sub>OFF</sub>   | Power Off Leakage Current                                | V <sub>DD</sub> = 0V, V <sub>OUT</sub> = 2.5V or GND  | -10   |                    | +10             | μA    |
| I <sub>OS</sub>  | Output Short Circuit Current, One Complementary Output   | OUT+ or OUT- Short to GND   |       | -15                | -40             | mA    |
|  |  | OUT+ or OUT- Short to V <sub>DD</sub>   |       | 15                 | 40              | mA    |
| I <sub>OSB</sub>   | Output Short Circuit Current, both Complementary Outputs | OUT+ and OUT- Short to GND  |       | -15                | -30             | mA    |
|  |  | OUT+ and OUT- Short to V <sub>CM</sub>  |       | 15                 | 30              | mA    |
| C <sub>OUT2</sub>  | Output Capacitance                                       | OUT+ or OUT- to GND when TRI-STATE  |       | 5.5                |                 | pF    |
| <b>SUPPLY CURRENT</b>  |  |   |       |                    |                 |       |
| I <sub>CCD</sub>   | Total Supply Current                                     | All inputs and outputs enabled, terminated with differential load of 100Ω between OUT+ and OUT-.        |       | 220                | 300             | mA    |
| I <sub>CCZ</sub>   | TRI-STATE Supply Current                                 | TRI-STATE All Outputs   |       | 10                 | 20              | mA    |
| <b>SWITCHING CHARACTERISTICS—LVDS OUTPUTS <sup>(5), (6), (7)</sup></b> |  |   |       |                    |                 |       |
| t <sub>LHT</sub>   | Differential Low to High Transition Time                 | Use an alternating 1 and 0 pattern at 200 Mb/s, measure between 20% and 80% of V <sub>OD</sub> .        | 100   | 135                | 160             | ps    |
| t <sub>HLT</sub>   | Differential High to Low Transition Time                 |   | 100   | 135                | 160             | ps    |
| t <sub>PLHD</sub>  | Differential Low to High Propagation Delay               | Use an alternating 1 and 0 pattern at 200 Mb/s, measure at 50% V <sub>OD</sub> between input to output. | 500   | 750                | 1200            | ps    |
| t <sub>PHLD</sub>  | Differential High to Low Propagation Delay               |   | 500   | 750                | 1200            | ps    |
| t <sub>SKD1</sub>  | Pulse Skew   | t <sub>PLHD</sub> - t <sub>PHLD</sub>   |       | 0                  | 30              | ps    |

(3) Differential output voltage V<sub>OD</sub> is defined as |OUT+ - OUT-|. Differential input voltage V<sub>ID</sub> is defined as |IN+ - IN-|.

(4) Output offset voltage V<sub>OS</sub> is defined as the average of the LVDS single-ended output voltages at logic high and logic low states.

(5) Differential output voltage V<sub>OD</sub> is defined as |OUT+ - OUT-|. Differential input voltage V<sub>ID</sub> is defined as |IN+ - IN-|.

(6) Characterized from any input to any one differential LVDS output running at the specified data rate and data pattern, with all other 3 channels running K28.5 pattern at 1.25 Gb/s asynchronously to the channel under test. Jitter is not production-tested, but ensured through characterization on sample basis. Random Jitter is measured peak to peak with a histogram including 1000 histogram window hits. K28.5 pattern is repeating bit streams of (0011111010 1100000101). This deterministic jitter or DJ pattern is measured to a histogram mean with a sample size of 350 hits. Like RJ the Total Jitter or TJ is measured peak to peak with a histogram including 3500 window hits.

(7) The LVCMOS input and output AC specifications may also be verified and tested using an input attenuation network instead of a power splitter.

## Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges unless other specified. <sup>(1)</sup>

| Symbol   | Parameter                                 | Conditions  | Min | Typ <sup>(2)</sup> | Max | Units |
|--|---|---|-----|--------------------|-----|-------|
| t <sub>SKCC</sub>  | Output Channel to Channel Skew            | Difference in propagation delay (t <sub>PLHD</sub> or t <sub>PHLD</sub> ) among all output channels in Broadcast mode (any one input to all outputs). | 0   | 50                 | 100 | ps    |
| t <sub>JIT</sub>   | Jitter <sup>(6)</sup>                     | Alternating 1 and 0 Pattern   |     |                    |     |       |
|  |   | 750 MHz   |     | 1.6                | 2.5 | psrms |
|  |   | 1.25 GHz  |     | 1.6                | 2.5 | psrms |
|  |   | K28.5 Pattern   |     |                    |     |       |
|  |   | 1.5 Gb/s  |     | 10                 | 40  | psp-p |
|  |   | 2.5 Gb/s  |     | 27                 | 60  | psp-p |
|  |   | PRBS 2 <sup>23</sup> -1 Pattern   |     |                    |     |       |
|  |   | 1.5 Gb/s  |     | 25                 | 40  | psp-p |
|  |   | 2.5 Gb/s  |     | 40                 | 70  | psp-p |
| t <sub>ON</sub>  | LVDS Output Enable Time                   | Time from LOAD = LH or SELx to OUT± change from TRI-STATE to active.  | 50  | 150                | 300 | ns    |
| t <sub>OFF</sub>   | LVDS Output Disable Time                  | Time from LOAD = LH or SELx to OUT± change from active to TRI-STATE.  |     | 3                  | 5   | ns    |
| t <sub>SW</sub>  | LVDS Switching Time                       | Time from LOAD = LH to new switch configuration effective for OUT±.   |     | 50                 | 150 | ns    |
| t <sub>SEL</sub>   | SELx to OUT±                              | Configuration select to new data at OUT±.   |     | 50                 | 150 | ns    |
| <b>SWITCHING CHARACTERISTICS — Serial control Interface <sup>(8)</sup></b> |   |   |     |                    |     |       |
| F <sub>SCLK</sub>  | SCLK Clock Frequency                      |   | 0   |                    | 100 | MHz   |
| T <sub>DCCLK</sub>   | CSCLK Duty Cycle<br>RSCLK Duty Cycle      | Input SCLK Duty Cycle set at 50%  | 45  |                    | 55  | %     |
| t <sub>S</sub>   | SI–SCLK or MODE–SCLK Setup Time           | From SI or MODE Input Data to SCLK Rising Edge  | 1.5 |                    |     | ns    |
| t <sub>H</sub>   | SCLK–SI or SCLK–MODE Hold Time            | From SCLK Rising Edge to SI or MODE Input Data  | 1   |                    |     | ns    |
| t <sub>DSO</sub>   | SCLK to RSO or CSO Delay                  | From SCLK to RSO or CSO   | 1.5 |                    | 4   | ns    |
| t <sub>DSCLK</sub>   | SCLK to RSCLK or CSCLK Delay              | From SCLK to RSCLK or CSCLK   | 4.0 |                    | 8.5 | ns    |
| t <sub>DSDF</sub>  | SCLK to RSCLK or CSCLK–SCLK to RSO or CSO | Propagation Delay Difference between t <sub>DSO</sub> and t <sub>DSCLK</sub>  | 1.5 |                    | 4.5 | ns    |
| T <sub>RISE</sub>  | Logic Low to High Transition Time         | 20% to 80% at RSO, CSO, RSCLK, or CSCLK   |     | 1.5                |     | ns    |
| T <sub>FALL</sub>  | Logic High to Low Transition Time         | 80% to 20% at RSO, CSO, RSCLK, or CSCLK   |     | 1.5                |     | ns    |

(8) Output offset voltage V<sub>OS</sub> is defined as the average of the LVDS single-ended output voltages at logic high and logic low states.

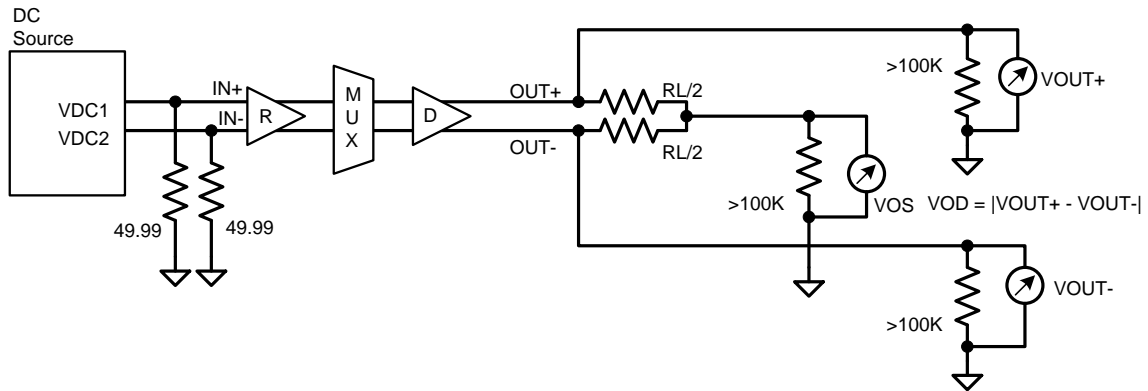


Figure 4. Differential Driver DC Test Circuit

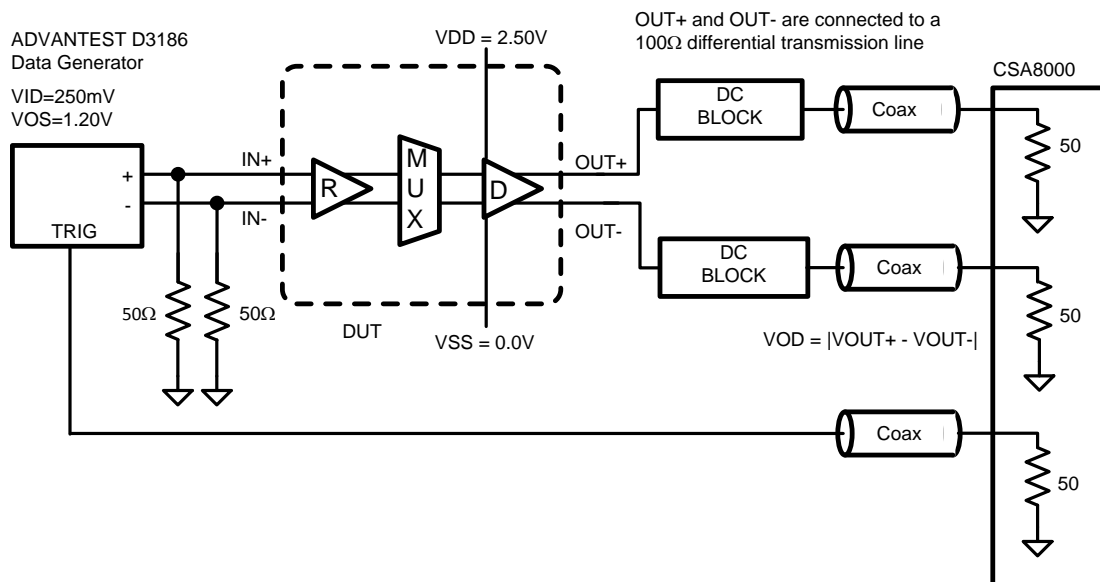


Figure 5. Differential Driver AC Test Circuit

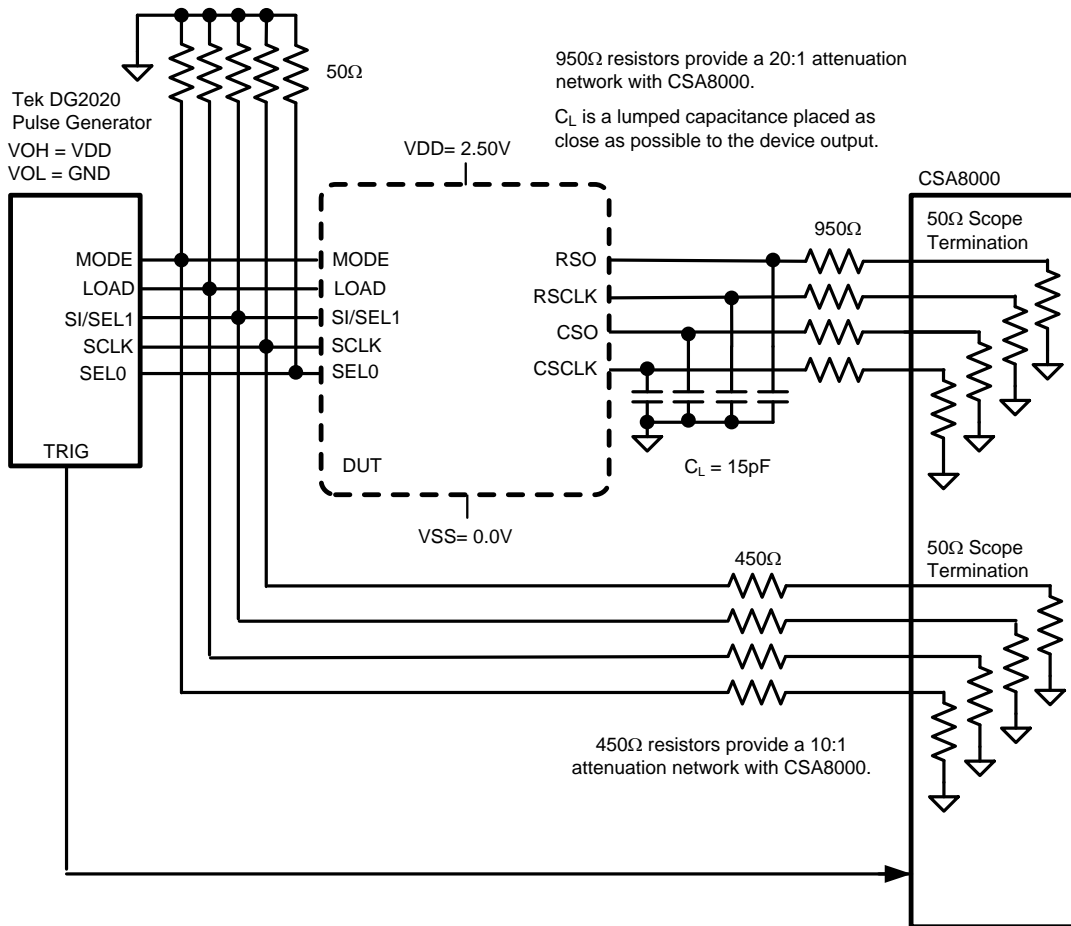


Figure 6. LVC MOS Driver AC Test Circuit <sup>(9)</sup>

(9) The LVC MOS input and output AC specifications may also be verified and tested using an input attenuation network instead of a power splitter.

Parameter Measurement Information

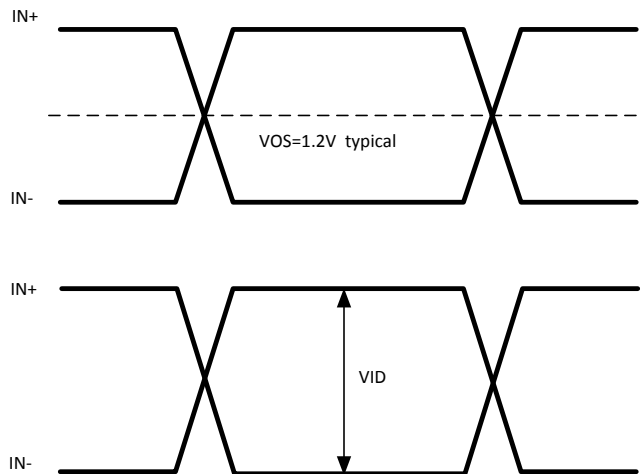


Figure 7. LVDS Signals

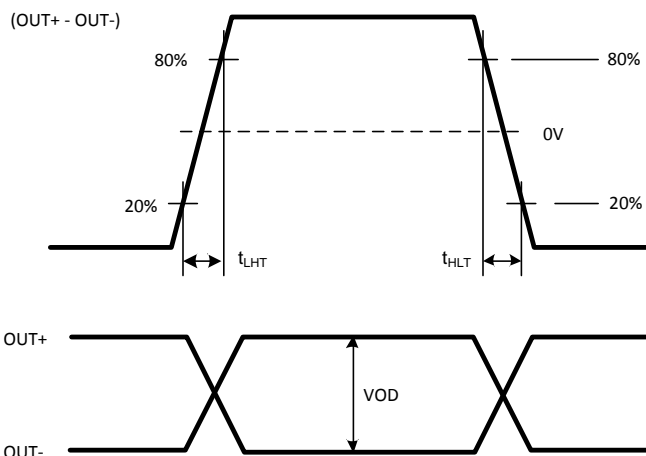


Figure 8. LVDS Output Transition Time

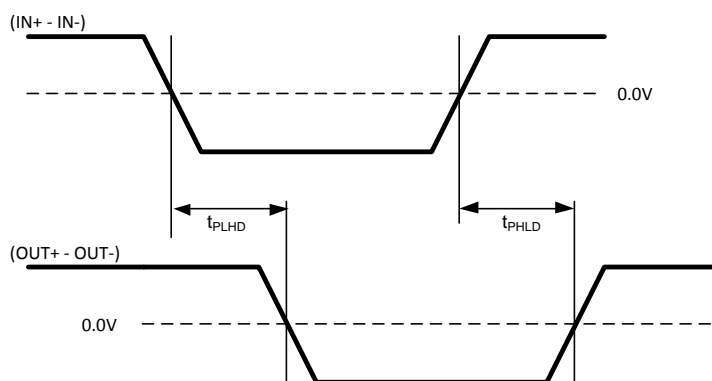


Figure 9. LVDS Output Propagation Delay

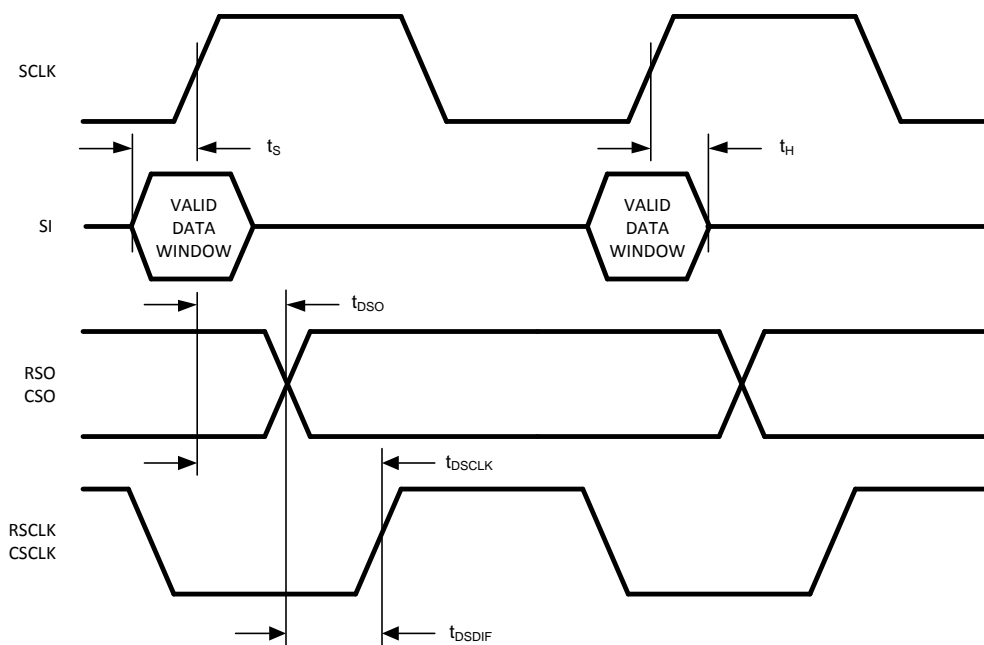


Figure 10. Serial Interface Propagation Delay and Input Timing Waveforms

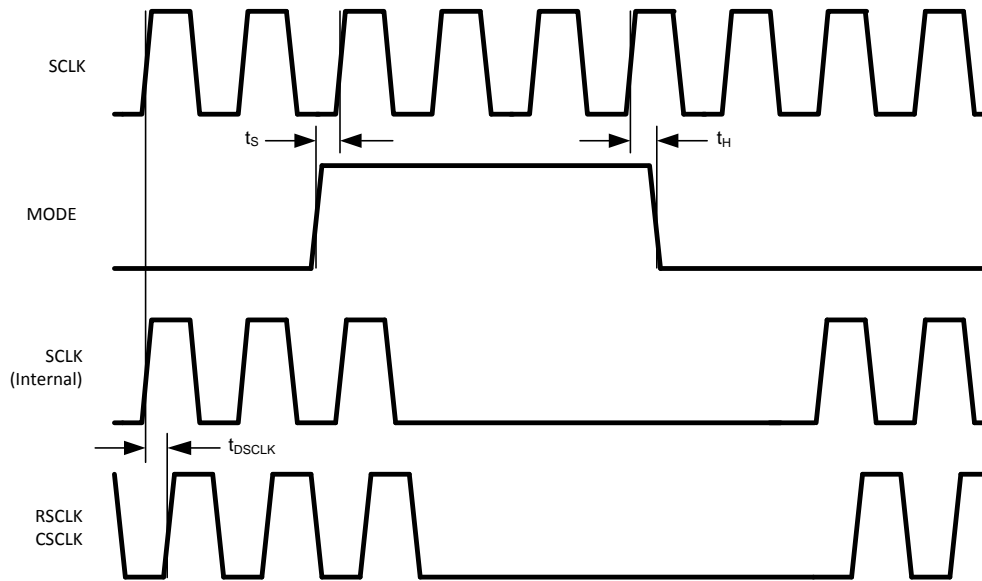


Figure 11. Serial Interface— MODE Timing and Functionality

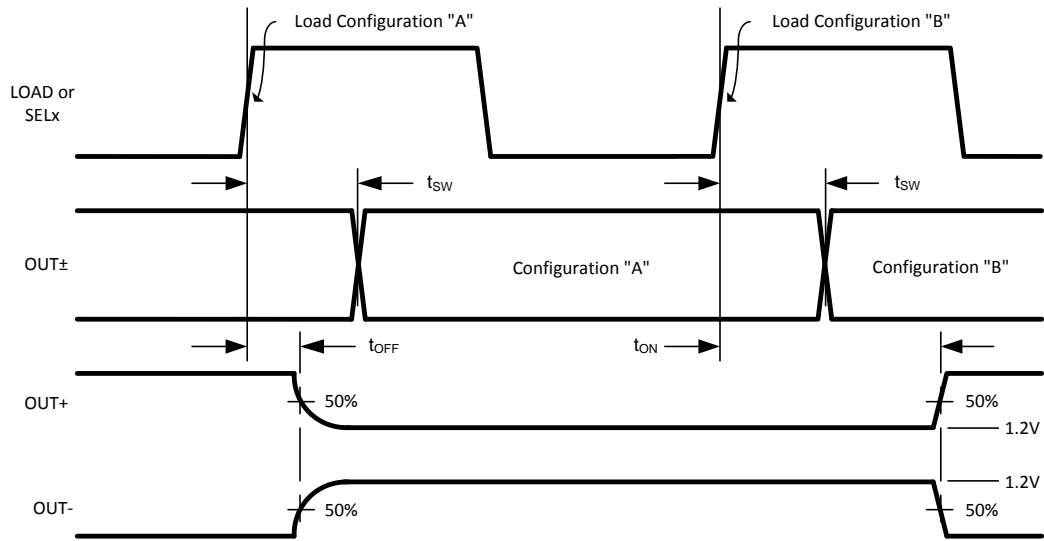


Figure 12. Configuration and Output Enable/Disable Timing

## FUNCTIONAL DESCRIPTIONS

### Programming with the Serial Interface

The configuration of the internal multiplexer is programmed through a simple serial interface consisting of serial clock SCLK and serial input data line SI. The serial interface is designed for easy expansion to larger switch array. A replicated output serial interface (RSCLK, RSO) is provided for propagating the control data to the downstream device in the row of an array of DS90CP04 devices in a matrix. A similar replicated serial interface (CSCLK, CSO) is provided for propagating the control data to the downstream devices in the first column of the device matrix. Through this scheme, user can program all the devices in the matrix through one serial control bus (SCLK and SI) with the use of the feed-through replicated control bus at RSCLK and RSO, CSCLK and CSO.

To program the configuration of the switch, a 30-bit control word is sent to the device. The first 6 bits shift the start frame into SI. The only two valid start frames are 1F'h for a configuration load and 1E'h for a configuration read. The start frame is followed by the row and column addresses of the device to be accessed, as well as the switch configuration of the four channels of the device. [Table 1](#) and [Table 2](#) are the bit definitions of the control word. D29 is the first bit that shifts into SI.

**Table 1. 30-Bit Control Word**

| Bit     | Bit Length | Descriptions   |
|---------|------------|--|
| D29–D24 | 6          | The start frame for control word synchronization (01 1111'b = LOAD).   |
| D23–D18 | 6          | Specify the row address of the device to be access. The serial interface can access up to 64 devices in the row.       |
| D17–D12 | 6          | Specify the column address of the device to be access. The serial interface can access up to 64 devices in the column. |
| D11–D9  | 3          | Specify the switch configuration for Output 1. See <a href="#">Table 2</a> .   |
| D8–D6   | 3          | Specify the switch configuration for Output 2. See <a href="#">Table 2</a> .   |
| D5–D3   | 3          | Specify the switch configuration for Output 3. See <a href="#">Table 2</a> .   |
| D2–D0   | 3          | Specify the switch configuration for Output 4. See <a href="#">Table 2</a> .   |

**Table 2. Switch Configuration Data**

| MSB |   | LSB | OUT1± Connects to  | OUT2± Connects to   | OUT3± Connects to   | OUT4± Connects to   |
|-----|---|-----|--|---------------------|---------------------|---------------------|
| 0   | 0 | 0   | Output 1 Tri-Stated  | Output 2 Tri-Stated | Output 3 Tri-Stated | Output 4 Tri-Stated |
| 0   | 0 | 1   | IN1±   | IN1±                | IN1±                | IN1±                |
| 0   | 1 | 0   | IN2±   | IN2±                | IN2±                | IN2±                |
| 0   | 1 | 1   | IN3±   | IN3±                | IN3±                | IN3±                |
| 1   | 0 | 0   | IN4±   | IN4±                | IN4±                | IN4±                |
| 1   | 0 | 1   | Invalid.   |                     |                     |                     |
| 1   | 1 | 0   | Use of these invalid combinations may cause loss of synchronization. |                     |                     |                     |
| 1   | 1 | 1   |  |                     |                     |                     |

### Row and Column Addressing

The upper left device in an array of NxN devices is assigned row address 0, and column address 0. The devices to its right have column addresses of 1 to N, whereas devices below it have row addresses of 1 to N. The Serial Control Interface (SCLK and SI) is connected to the first device with the row and column addresses of 0. The Serial Control Interface shifts in a control word containing the row and column address of the device it wants to access. When the control data propagates through each device, the control word's address is internally decremented by one before it is sent to the next row or column device. When the control data is sent out the column interface (CSO and CSCLK) the row address is decremented by one. Similarly, when the column address data is shifted out the row interface (RSO and RSCLK) the column address is decremented by one. By the time the control word reaches the device it has been intended to program, both the row and column addresses have been decremented to 0.

Each device constantly checks for the receipt of a frame start (D29–24=01 1111'b or 01 1110'b). When it detects the proper start frame string, and the row and column addresses it receives are both 0, the device responds by storing the switch configuration data of the 30-bit control word into its load register.

Each device in the array is sequentially programmed through the serial interface. When programming is completed for the entire array, LOAD is pulsed high and the load register's content is transferred to the configuration register of each device. The LOAD pulse must wait until the final bit of the control word has been placed into the "load" register. This timing is ensured to take place two clock cycles after programming has been completed.

Due to internal shift registers additional SCLK cycles will be necessary to complete array programming. It takes 7 clock (SCLK) positive edge transitions for the control data to appear at RSO and CSO for its near neighbor. Users must provide the correct number of clock transitions for the control data word to reach its destination in the array. [Table 3](#) shows an example of the control data words for a 4 device serial chain with connections (OUT1=IN1, OUT2=IN2, OUT16=IN16). To program the array, it requires four 30-bit control words to ripple through the serial chain and reach their destinations. In order to completely program the array in the 120 clock cycles associated with the 30-bit control words it is important to program the last device in the chain first. The following programming data pushes the initial data through the chain into the correct devices.

### Read-Back Switch Configuration

The DS90CP04 is put into read-back mode by sending a special "Read" start frame (01 1110'b). Upon receipt of the special read start frame the configuration register information is transferred into the shift register and output at both RSO and CSO in the OUT1 to OUT4 bit segments of the read control word. Each time the read-back data from a device passes through its downstream device, its default address (11 1111'b) is internally decremented by one. The "relative" column address emerges at RSO of the last device in the row and is used to determine (11 1111'b - N) the column of the sending device. Similarly, the row address emerges at CSO of the sending device. After inserting the channel configuration information in the "read" control word, the device will automatically revert to write mode, ready to accept a new control word at SI.

[Table 4](#) shows an example of reading back the configuration registers of 4 devices in the first row of a 4x4 device array. Again, due to internal shift registers additional SCLK cycles will be necessary to complete the array read. It takes 4x30 SCLK clock cycles to shift out 4 30-bit configuration registers plus 7 SCLK cycles per device to account for device latency making for a total SCLK count of 148. The serialized read data is sampled at RSO and synchronized with RSCLK of the last device in the row. The user is recommended to backfill with all 0's at SI after the four reads have been shifted in.

**Table 3. Example to Program a 4 Device Array**

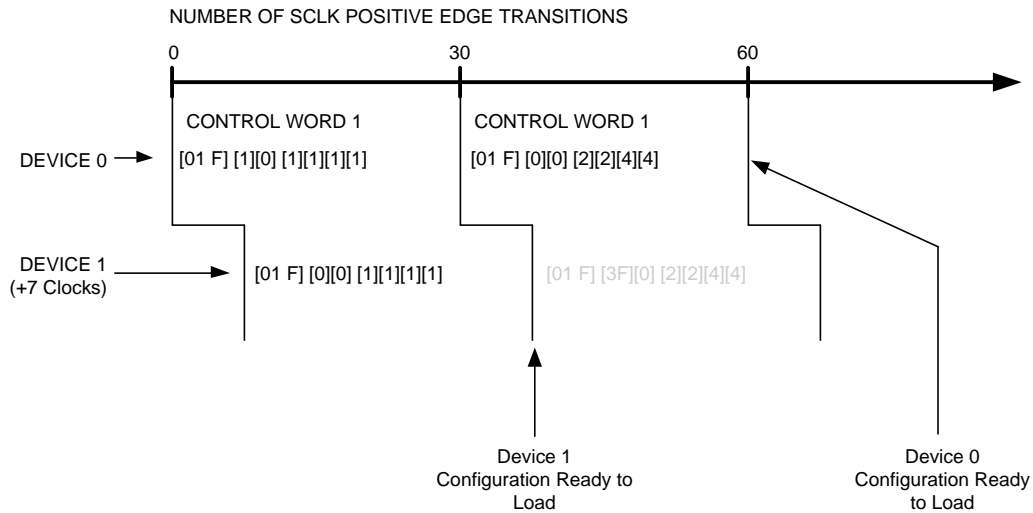
| Frame D29:D24  | Row Address D23:D18 | Column Address D17:D12 | OUT1 D11:D9 | OUT2 D8:D6 | OUT3 D5:D3 | OUT4 D2:D0 | Number of SCLK Cycles | Control Word Destination Device in Array Row, Column |
|--|---------------------|------------------------|-------------|------------|------------|------------|-----------------------|--|
| 01 1111  | 00 0000             | 00 0011                | 001         | 010        | 011        | 100        | 30                    | 0, 3   |
| 01 1111  | 00 0000             | 00 0010                | 001         | 010        | 011        | 100        | 30                    | 0, 2   |
| 01 1111  | 00 0000             | 00 0001                | 001         | 010        | 011        | 100        | 30                    | 0, 1   |
| 01 1111  | 00 0000             | 00 0000                | 001         | 010        | 011        | 100        | 30                    | 0, 0   |
| Shift in configuration information from device furthest from system SI input first to minimize array latency during the programming process. |                     |                        |             |            |            |            |                       |  |
| The 2 clock cycle delay ensures all channel information has reached the "load" register and all switches are ready to be configured.         |                     |                        |             |            |            |            | 2                     |  |

**Table 4. A Read-Back Example from a 4 Device Array**

| Frame D29:D24 | Row Address D23:D18 | Column Address D17:D12 | OUT1 D11:D9 | OUT2 D8:D6 | OUT3 D5:D3 | OUT4 D2:D0 | Number of SCLK Cycles | Descriptions         |
|---------------|---------------------|------------------------|-------------|------------|------------|------------|-----------------------|----------------------|
| 01 1110       | 00 0000             | 11 1111                | 000         | 000        | 000        | 000        | 30                    | Read-Back (R,C)=0, 3 |
| 01 1110       | 00 0000             | 11 1110                | 000         | 000        | 000        | 000        | 30                    | Read-Back (R,C)=0, 2 |
| 01 1110       | 00 0000             | 11 1101                | 000         | 000        | 000        | 000        | 30                    | Read-Back (R,C)=0, 1 |
| 01 1110       | 00 0000             | 11 1100                | 001         | 010        | 011        | 100        | 30                    | Read-Back (R,C)=0, 0 |

### Switch Expansion For Minimum Programming Latency

Programming data ripples through the array through RSO and RSCLK in the row and CSO and CSCLK in the first column. LOAD pins of all devices are electrically tied together and driven by the same “load” signal. To prevent excessive stub length in the array from affecting the signal quality of LOAD, it is recommended that the load signal is distributed to each row or column in large crosspoint array applications.



### Programming Example

#### CONFIGURATION WRITE

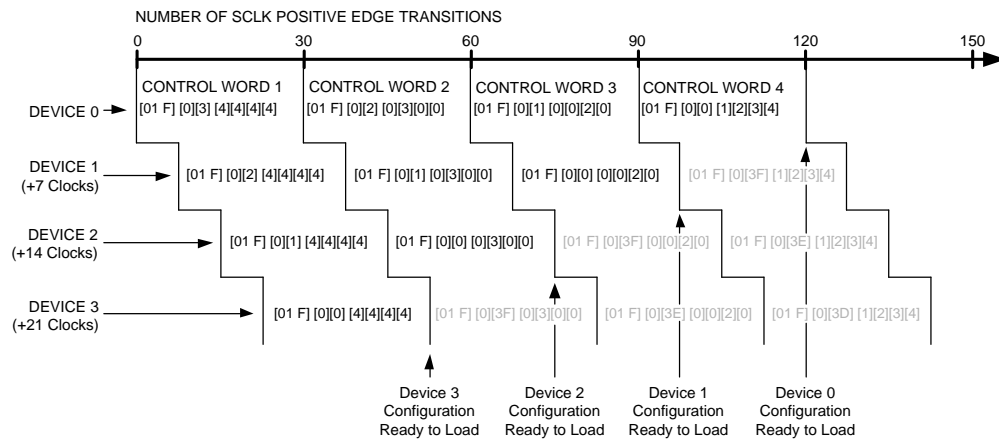
30 Bit Control Word: [WRITE FRAME] [ROW ADDRESS][COLUMN ADDRESS] [OUT1][OUT2][OUT3][OUT4]

#### ARRAY WRITE

[01 1111] [0][1] [1][1][1][1] */\*Array position 1, Broadcast IN1 \*/*

[01 1111] [0][0] [2][2][4][4] */\*Array position 0, Connect IN2 to OUT1 and 2, IN4 to OUT3 and OUT4 \*/*

LOAD = H and SCLK = LH



**DEVICE 0 WRITE PROGRAMMING SEQUENCE**

| SCLK Number | Event Description   |
|-------------|---|
| 6           | Device 0 (R=0, C=0) detects "WRITE" frame of first Control Word.  |
| 18          | Device 0 (R=0, C=0) sees Row = 1, Column = 0 of first Control Word. The Row address of the first Control Word is decremented by 1 (Row Address = 0) and sent out RSO.     |
| 36          | Device 0 (R=0, C=0) detects "WRITE" frame of second Control Word.   |
| 48          | Device 0 (R=0, C=0) sees Row = 0, Column = 0 of second Control Word. This is a valid configuration write address, Device 1 prepares to receive configuration information. |
| 60          | Device 0 (R=0, C=0) has received configuration information and is waiting for a LOAD.   |

**DEVICE 1 WRITE PROGRAMMING SEQUENCE**

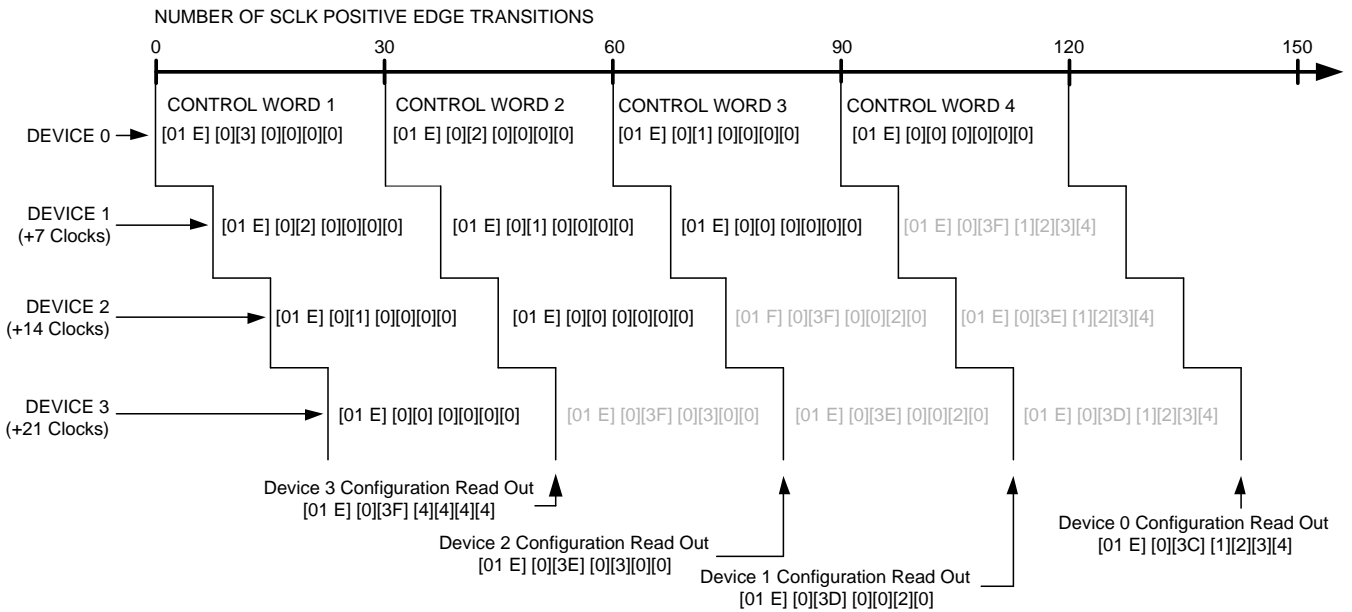
| SCLK Number | Event Description   |
|-------------|---|
| 13          | Device 1 (R=1, C=0) detects "WRITE" frame of first Control Word.  |
| 25          | Device 1 (R=1, C=0) sees Row = 0, Column = 0 of first Control Word. This is a valid configuration write address, Device 1 prepares to receive configuration information.  |
| 37          | Device 1 (R=1, C=0) has received configuration information and is waiting for a LOAD.   |
| 43          | Device 1 (R=1, C=0) detects "WRITE" frame of second Control Word.   |
| 55          | Device 1 (R=1, C=0) sees Row = 3F, Column = 0 of second Control Word. The Row address of the second Control Word is decremented by 1 (Row Address = 3E) and sent out RSO. |

**CONFIGURATION READ**

30 Bit Control Word: [READ FRAME] [ROW ADDRESS][COLUMN ADDRESS] [OUT1][OUT2][OUT3][OUT4]

**ARRAY WRITE**

[01 1110] [1][0] [0][0][0][0] /\*Array position 1, Return Configuration Information \*/  
 [01 1110] [0][0] [0][0][0][0] /\*Array position 0, Return Configuration Information \*/



**DEVICE 0 READ PROGRAMMING SEQUENCE**

| <b>SCLK Number</b> | <b>Event Description</b>   |
|--------------------|--|
| 6                  | Device 0 (R=0, C=0) detects "READ" frame of first Control Word.  |
| 18                 | Device 0 (R=0,C=0) sees Row = 1, Column = 0 of first Control Word. The Row address of the first Control Word is decremented by 1 (Row Address = 0) and sent out RSO.   |
| 36                 | Device 0 (R=0,C=0) detects "READ" frame of second Control Word.  |
| 48                 | Device 0 (R=0,C=0) sees Row = 0, Column = 0 of second Control Word. This is a valid configuration read address, Device 0 prepares to transmit configuration information. The Row address of the last Control Word is decremented by 1 (Row Address = 3F) and sent out RSO. |
| 60                 | Device 0 (R=0,C=0) has transmitted configuration information.  |
| 74                 | Finished transmitting configuration information at Array Output (RSO of Device 1).   |

**DEVICE 1 READ PROGRAMMING SEQUENCE**

| <b>SCLK Number</b> | <b>Event Description</b>  |
|--------------------|---|
| 13                 | Device 1 (R=1, C=0) detects "READ" frame of first Control Word.   |
| 25                 | Device 1 (R=1,C=0) sees Row = 0, Column = 0 of first Control Word. This is a valid configuration read address, Device 1 prepares to transmit configuration information. The Row address of the last Control Word is decremented by 1 (Row Address = 3F) and sent out RSO. |
| 37                 | Device 1 (R=1,C=0) has transmitted configuration information at Array Output (RSO of Device 1).   |

## REVISION HISTORY

| Changes from Revision H (April 2013) to Revision I         | Page |
|--|------|
| • Changed layout of National Data Sheet to TI format ..... | 17   |

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2)         | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|---------|
| DS90CP04TLQ      | NRND          | WQFN         | NJE             | 32   | 250         | TBD                     | Call TI                 | Call TI              | -40 to 85    | 90CP04T                 |         |
| DS90CP04TLQ/NOPB | ACTIVE        | WQFN         | NJE             | 32   | 250         | Green (RoHS & no Sb/Br) | CU SN                   | Level-3-260C-168 HR  | -40 to 85    | 90CP04T                 | Samples |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

| Device           | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------------|--------------|-----------------|------|-----|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| DS90CP04TLQ      | WQFN         | NJE             | 32   | 250 | 178.0              | 16.4               | 6.3     | 6.3     | 1.5     | 12.0    | 16.0   | Q1            |
| DS90CP04TLQ/NOPB | WQFN         | NJE             | 32   | 250 | 178.0              | 16.4               | 6.3     | 6.3     | 1.5     | 12.0    | 16.0   | Q1            |

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

| Device           | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|------------------|--------------|-----------------|------|-----|-------------|------------|-------------|
| DS90CP04TLQ      | WQFN         | NJE             | 32   | 250 | 213.0       | 191.0      | 55.0        |
| DS90CP04TLQ/NOPB | WQFN         | NJE             | 32   | 250 | 213.0       | 191.0      | 55.0        |



## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

### Products

|                              |  |
|------------------------------|--|
| Audio                        | <a href="http://www.ti.com/audio">www.ti.com/audio</a>                               |
| Amplifiers                   | <a href="http://amplifier.ti.com">amplifier.ti.com</a>                               |
| Data Converters              | <a href="http://dataconverter.ti.com">dataconverter.ti.com</a>                       |
| DLP® Products                | <a href="http://www.dlp.com">www.dlp.com</a>   |
| DSP                          | <a href="http://dsp.ti.com">dsp.ti.com</a>   |
| Clocks and Timers            | <a href="http://www.ti.com/clocks">www.ti.com/clocks</a>                             |
| Interface                    | <a href="http://interface.ti.com">interface.ti.com</a>                               |
| Logic                        | <a href="http://logic.ti.com">logic.ti.com</a>                                       |
| Power Mgmt                   | <a href="http://power.ti.com">power.ti.com</a>                                       |
| Microcontrollers             | <a href="http://microcontroller.ti.com">microcontroller.ti.com</a>                   |
| RFID                         | <a href="http://www.ti-rfid.com">www.ti-rfid.com</a>                                 |
| OMAP Applications Processors | <a href="http://www.ti.com/omap">www.ti.com/omap</a>                                 |
| Wireless Connectivity        | <a href="http://www.ti.com/wirelessconnectivity">www.ti.com/wirelessconnectivity</a> |

### Applications

|                               |  |
|-------------------------------|--|
| Automotive and Transportation | <a href="http://www.ti.com/automotive">www.ti.com/automotive</a>                         |
| Communications and Telecom    | <a href="http://www.ti.com/communications">www.ti.com/communications</a>                 |
| Computers and Peripherals     | <a href="http://www.ti.com/computers">www.ti.com/computers</a>                           |
| Consumer Electronics          | <a href="http://www.ti.com/consumer-apps">www.ti.com/consumer-apps</a>                   |
| Energy and Lighting           | <a href="http://www.ti.com/energy">www.ti.com/energy</a>                                 |
| Industrial                    | <a href="http://www.ti.com/industrial">www.ti.com/industrial</a>                         |
| Medical                       | <a href="http://www.ti.com/medical">www.ti.com/medical</a>                               |
| Security                      | <a href="http://www.ti.com/security">www.ti.com/security</a>                             |
| Space, Avionics and Defense   | <a href="http://www.ti.com/space-avionics-defense">www.ti.com/space-avionics-defense</a> |
| Video and Imaging             | <a href="http://www.ti.com/video">www.ti.com/video</a>                                   |

### TI E2E Community

[e2e.ti.com](http://e2e.ti.com)