



FSA2270T Low-Voltage, Dual-SPDT (0.4 Ω) Analog Switch with Negative Swing Audio Capability

Features

- 0.4 Ω Typical On Resistance (R_{ON}) for +3.0 V Supply
- 0.25 Ω Maximum R_{ON} Flatness for +3.0 V Supply
- -3 db Bandwidth: > 50 MHz
- Low- I_{CCT} Current Over Expanded Control Input Range
- Packaged in 10-Lead UMLP
- Power-Off Protection on Common Ports
- Broad V_{CC} Operating Range: 1.65 to 4.3 V
- Noise Immunity Termination Resistors
- Low Electrostatic Discharge (ESD)
 - Human Body Model (JEDEC: JESD22-A114)
 - Power to GND 16 kV
 - I/O to GND 11 kV
 - All other pins 8 kV
 - Charged Device Model (JEDEC: JESD22-A101)

Applications

- Cell Phone, PDA, Digital Camera, and Notebook
- LCD Monitor, TV, and Set-Top Box

IMPORTANT NOTE:

For additional information, please contact analogswitch@fairchildsemi.com.

Description

The FSA2270T is a high-performance, dual Single-Pole Double-Throw (SPDT) analog switch with negative swing audio capability. The FSA2270T features ultra-low R_{ON} of 0.4 Ω (typical) at 3.0 V V_{CC} . The FSA2270T operates over a wide V_{CC} range of 1.65 V to 4.3 V, is fabricated with sub-micron CMOS technology to achieve fast switching speeds, and is designed for break-before-make operation. The select input is TTL-level compatible.

The FSA2270T features very low quiescent current even when the control voltage is lower than the V_{CC} supply. This feature suits mobile handset applications by allowing direct interface with baseband processor general-purpose I/Os with minimal battery consumption.

The FSA2270T includes termination resistors that improve noise immunity during overshoot excursions, off-isolation coupling, or “pop-minimization.”

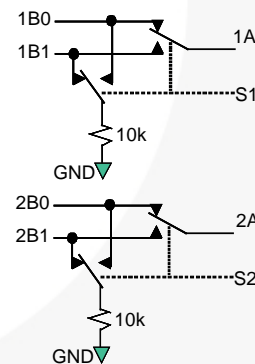


Figure 1. Analog Symbol

Ordering Information

Part Number	Top Mark	Package Description
FSA2270TUMX	HK	10-Lead, Quad Ultrathin Molded Leadless Package (UMLP), 1.4 x 1.8 mm, 0.4 mm Pitch

Pin Configuration

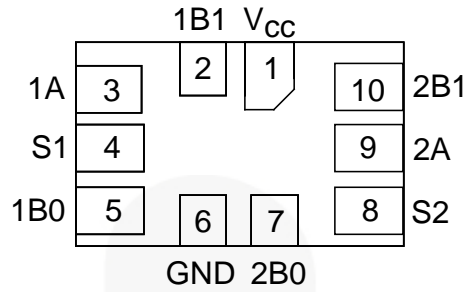


Figure 2. 10-Pin UMLP (Top Through View)

Pin Descriptions

Pin#	Name	Description
1	V _{CC}	Supply Voltage
3, 9	1A, 2A	Data Points
4, 8	S1, S2	Switch Select Pins
5, 7	1B0, 2B0	Data Ports
6	GND	Ground
2, 10	1B1, 2B1	Data Ports

Truth Table

Control Input, S _n	Function
LOW Logic Level	nB0 connected to nA; nB1 terminated to GND
HIGH Logic Level	nB1 connected to nA; nB0 terminated to GND

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. Functional operation above the recommended operating conditions is not implied. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. Absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Units	
V_{CC}	Supply Voltage	-0.5	5.5	V	
V_{SW}	Switch I/O Voltage ⁽¹⁾	1B0, 1B1, 2B0, 2B1, 1A, 2A Pins	$V_{CC} + 0.3$	V	
V_{CNTRL}	Control Input Voltage ⁽¹⁾	S1, S2	$V_{CC} + 0.3$		
I_{IK}	Input Clamp Diode Current		-50	mA	
I_{SW}	Switch I/O Current (Continuous)		350	mA	
I_{SWPEAK}	Peak Switch Current (Pulsed at 1 ms Duration, <10% Duty Cycle)		500	mA	
T_{STG}	Storage Temperature Range	-65	+150	°C	
T_J	Maximum Junction Temperature		+150	°C	
T_L	Lead Temperature Soldering, 10 Seconds		+260	°C	
ESD	Human Body Model, JEDEC: JESD22-A114	Power to GND		16	kV
		I/O to GND		11	kV
		All Other Pins		8	kV
	Charged Device Model, JEDEC: JESD22-C101			2	kV

Note:

- Input and output negative ratings may be exceeded if input and output diode current ratings are observed.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min.	Max.	Units
V_{CC}	Supply Voltage	1.65	4.30	V
$V_{S1, S2}$	Control Input Voltage	0	V_{CC}	V
V_{SW}	Switch I/O Voltage	$V_{CC} - 4.3$	V_{CC}	V
T_A	Operating Temperature	-40	+85	°C

DC Electrical Characteristics

All typical values are for $V_{CC}=3.3\text{ V}$ at $T_A=25^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A=+25^\circ\text{C}$			$T_A=-40$ to $+85^\circ\text{C}$		Units
				Min.	Typ.	Max.	Min.	Max.	
V_{IH}	Input Voltage High		3.60 to 4.30				1.7		V
			2.70 to 3.60				1.5		
			2.30 to 2.70				1.4		
			1.65 to 1.95				0.9		
V_{IL}	Input Voltage Low		3.60 to 4.30					0.7	V
			2.70 to 3.60					0.5	
			2.30 to 2.70					0.4	
			1.65 to 1.95					0.4	
I_{IN}	Control Input Leakage (S1, S2)	$V_{IN}=0$ to V_{CC}	1.65 to 4.30				-0.5	0.5	μA
$I_{A(ON)}$	On Leakage Current of Port nA	nA=0.5 V, $V_{CC}=0.5\text{ V}$ nB0 or nB1= $V_{CC}-0.5\text{ V}$, 0.5 V, or Floating Figure 5	1.95 to 4.30				-1	1	μA
I_{OFF}	Power-Off Leakage Current (Common Port Only 1A, 2A)	Common Port (1A, 2A), $V_{IN}=0\text{ V}$ to 4.3 V, $V_{CC}=0\text{ V}$ nB0, nB1=0 V or Floating	0				-45	45	μA
R_{ON}	Switch On Resistance ^(2,5)	$I_{ON}=100\text{ mA}$, nB0 or nB1=0.7 V, 3.6 V, 4.3 V Figure 3	4.30		0.30				Ω
		$I_{ON}=100\text{ mA}$, nB0 or nB1=0.7 V, 3.6 V, 4.3 V Figure 3	3.00		0.40			0.80	
		$I_{ON}=100\text{ mA}$, nB0 or nB1=0 V, 0.7 V, 1.6 V, 2.3 V Figure 3	2.30		0.52				
		$I_{ON}=100\text{ mA}$, nB0 or nB1=0 V, 0.7 V, 1.65 V Figure 3	1.65		1.00				
ΔR_{ON}	On Resistance Matching Between Channels ⁽³⁾	$I_{ON}=100\text{ mA}$, nB0 or nB1=0.7 V	4.30		0.04			0.13	Ω
			3.00		0.06			0.13	
			2.30		0.12				
			1.65		1.00				
$R_{FLAT(ON)}$	On Resistance Flatness ⁽⁴⁾	$I_{OUT}=100\text{ mA}$, nB0 or nB1=0 V to V_{CC}	4.30					0.25	Ω
			3.00					0.25	
			2.30		0.5				
			1.65		0.6				
R_{TERM}	Internal Termination Resistors ⁽⁵⁾				10			$\text{k}\Omega$	
I_{CC}	Quiescent Supply Current	$V_{IN}=0\text{ V}$ or V_{CC} , $I_{OUT}=0\text{ mA}$	4.30	-100		100	-500	500	nA
I_{CCT}	Increase in I_{CC} per Input	Input at 2.6 V	4.30		3.0			10.0	μA
		Input at 1.8 V			7.0			15.0	

Notes:

- On resistance is determined by the voltage drop between A and B pins at the indicated current through the switch.
- $\Delta R_{ON}=R_{ONmax} - R_{ONmin}$ measured at identical V_{CC} , temperature, and voltage.
- Flatness is defined as the difference between the maximum and minimum value of on resistance (R_{ON}) over the specified range of conditions.
- Guaranteed by characterization, not production tested.

AC Electrical Characteristics

All typical value are for $V_{CC}=3.3$ V at $T_A=25^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A=+25^\circ\text{C}$			$T_A=-40$ to $+85^\circ\text{C}$		Units	Figure
				Min.	Typ.	Max.	Min.	Max.		
t_{ON}	Turn-On Time	nB0 or nB1=1.5 V, $R_L=50 \Omega$, $C_L=35$ pF	3.60 to 4.30			60	15	65	ns	Figure 6 Figure 7
			2.70 to 3.60			65	15	70		
			2.30 to 2.70			80	15	85		
			1.65 to 1.95		100					
t_{OFF}	Turn-Off Time	nB0 or nB1=1.5 V, $R_L=50 \Omega$, $C_L=35$ pF	3.60 to 4.30			55	5	60	ns	Figure 6 Figure 7
			2.70 to 3.60			60	5	65		
			2.30 to 2.70			65	5	70		
			1.65 to 1.95		65					
t_{BBM}	Break-Before-Make Time	nB0 or nB1=1.5 V, $R_L=50 \Omega$, $C_L=35$ pF	3.60 to 4.30		3		1		ns	Figure 8
			2.70 to 3.60		5		2			
			2.30 to 2.70		10		2			
			1.65 to 1.95		15		2			
Q	Charge Injection	$C_L=1.0$ nF, $V_S=0$ V, $R_S=0 \Omega$	1.65 to 4.30		25				pC	Figure 12
OIRR	Off Isolation	$f=100$ kHz, $R_L=50 \Omega$, $C_L=0$ pF	1.65 to 4.30		-70				dB	Figure 10
Xtalk	Crosstalk	$f=100$ kHz, $R_L=50 \Omega$, $C_L=0$ pF	1.65 to 4.30		-70				dB	Figure 11
BW	-3 db Bandwidth	$R_L=50 \Omega$, $C_L=0$ pF	1.65 to 4.30		>50				MHz	Figure 9
THD	Total Harmonic Distortion	$f=20$ Hz to 20 kHz, $R_L=32 \Omega$, $V_{IN}=2$ V _{pp} $V_{BIAS}=0$ V	1.65 to 4.30		.06				%	Figure 15

Capacitance

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A=+25^\circ\text{C}$			Units	Figure
				Min.	Typ.	Max.		
C_{IN}	Control Pin Input Capacitance	$f=1$ MHz	0		2.5		pF	Figure 13
C_{OFF}	B Port Off Capacitance	$f=1$ MHz	3.3		30		pF	Figure 13
C_{ON}	A Port On Capacitance	$f=1$ MHz	3.3		120		pF	Figure 14

Test Diagrams

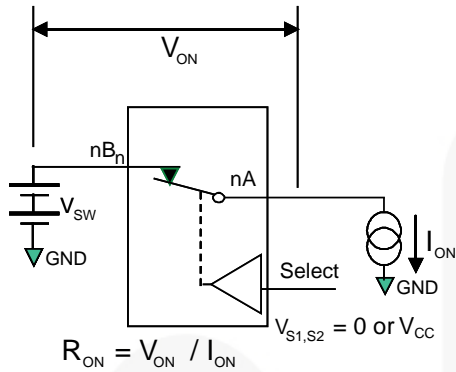
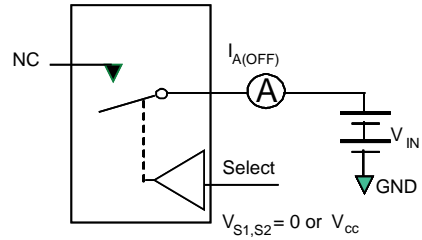


Figure 3. On Resistance



Each switch port is tested separately.

Figure 4. Off Leakage

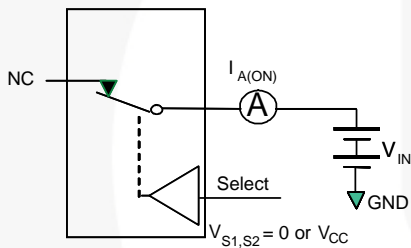
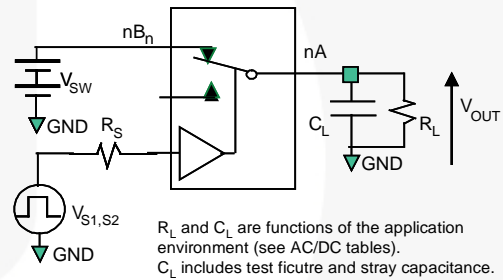


Figure 5. On Leakage



R_L and C_L are functions of the application environment (see AC/DC tables). C_L includes test fixture and stray capacitance.

Figure 6. Test Circuit Load

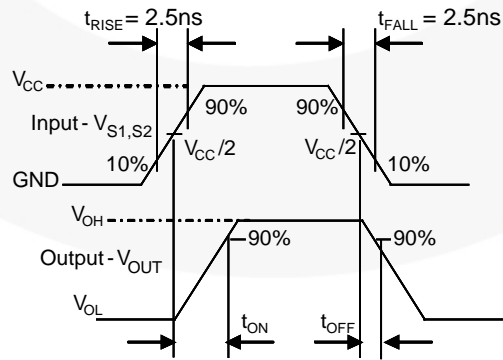


Figure 7. Turn-On / Turn-Off Waveforms

Test Diagrams (Continued)

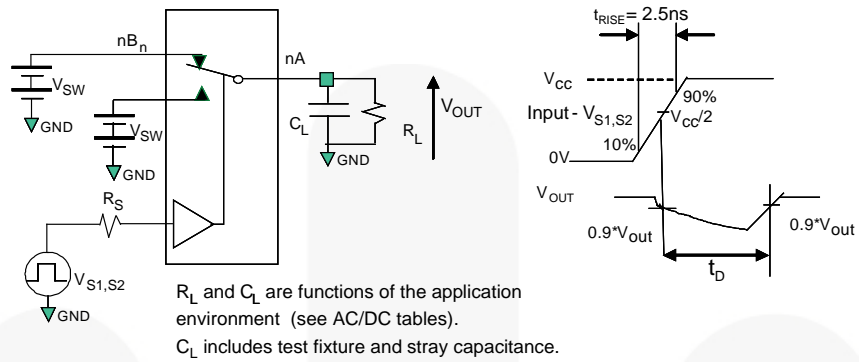


Figure 8. Break-Before-Make Interval Timing

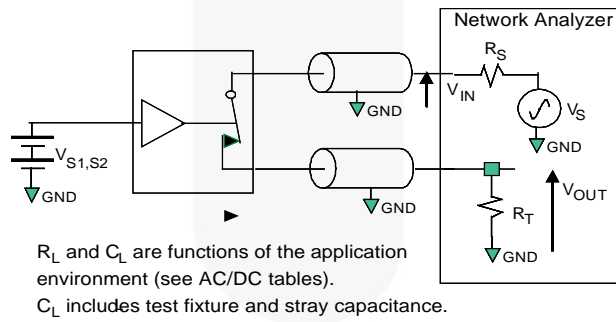


Figure 9. Bandwidth

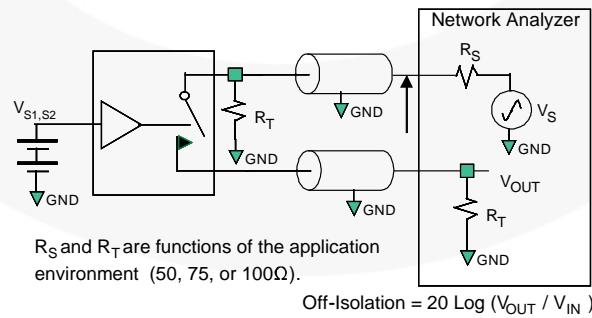


Figure 10. Channel Off Isolation

Test Diagrams (Continued)

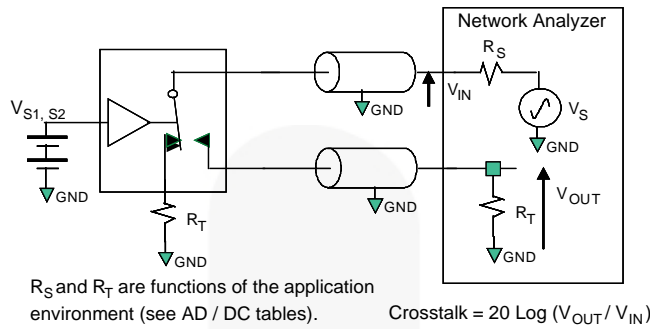


Figure 11. Adjacent Channel Crosstalk

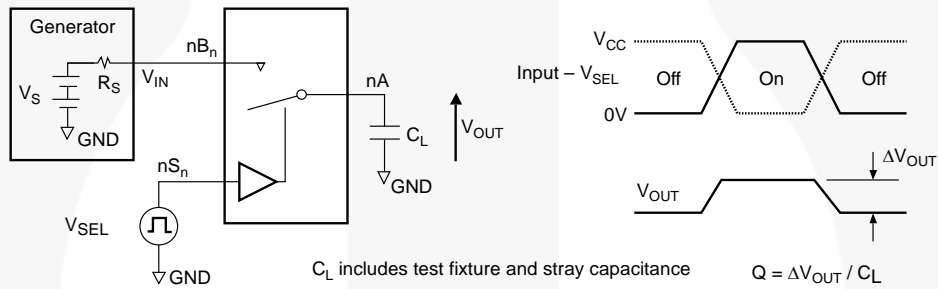


Figure 12. Charge Injection Test

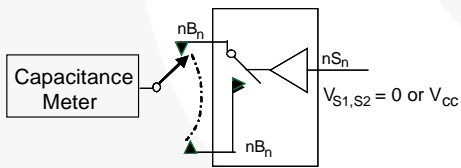


Figure 13. Channel Off Capacitance

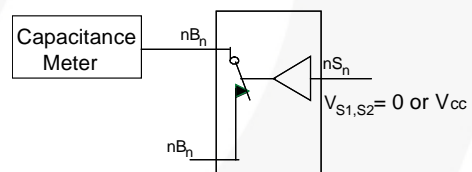


Figure 14. Channel On Capacitance

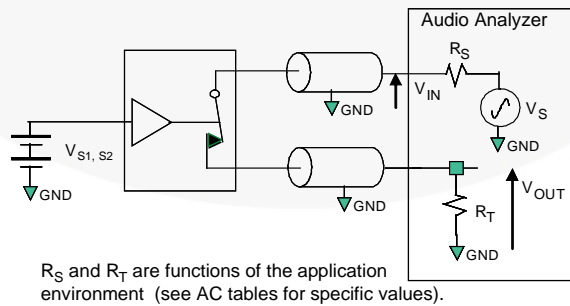


Figure 15. Total Harmonic Distortion

Physical Dimensions

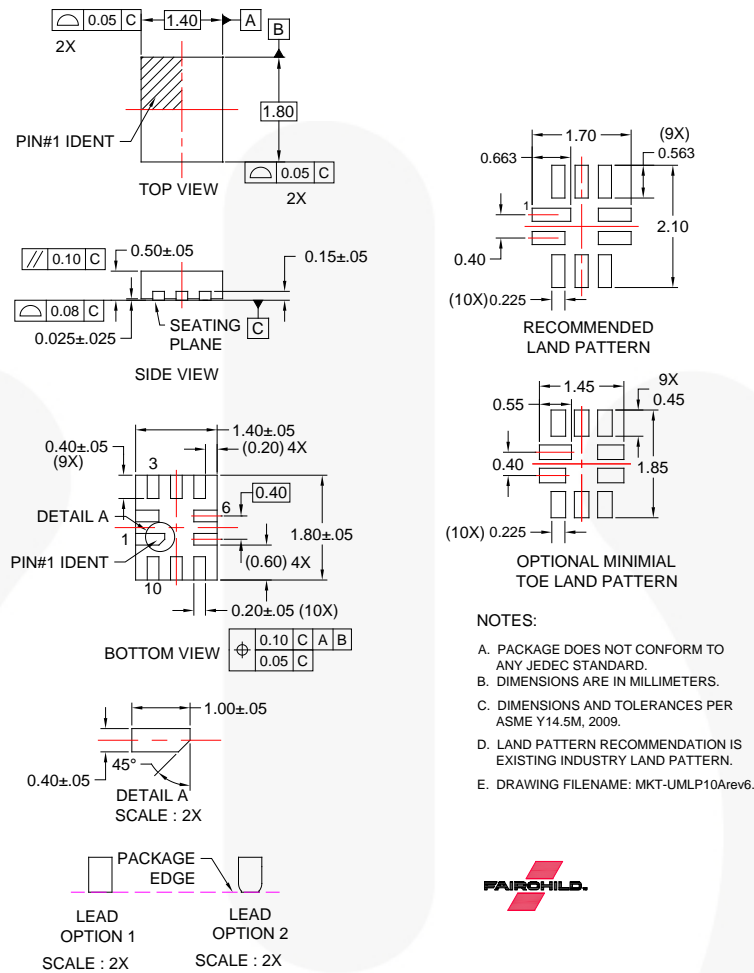


Figure 16. 10-Lead, Quad Ultrathin Molded Leadless Package (UMLP)

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Table 1. Nominal Values

JEDEC Symbol	Description	Nominal Values (mm)
A	Overall Height	0.5
A1	Package Standoff	0.026
A3	Lead Thickness	0.152
b	Lead Width	0.2
L	Lead Length	0.4
e	Lead Pitch	0.4
D	Body Length (Y)	1.8
E	Body Width (X)	1.4





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