ISO734x Robust EMC, Low Power, Quad-Channel Digital Isolators

1 Features

- Signaling Rate: 25 Mbps
- Integrated Noise Filter on the Inputs
- Default Output 'High' and 'Low' Options
- Low Power Consumption, Typical I_{CC} per Channel at 1 Mbps:
  - ISO7340: 0.9 mA (5 V Supplies), 0.7 mA (3.3 V Supplies)
  - ISO7341: 1.2 mA (5 V Supplies), 0.9 mA (3.3 V Supplies)
  - ISO7342: 1.3 mA (5 V Supplies), 0.9 mA (3.3 V Supplies)
- Low Propagation Delay: 31 ns Typical (5 V Supplies)
- 3.3 V and 5 V Level Translation
- Wide Temperature Range: –40°C to 125°C
- 70 KV/µs Transient Immunity, Typical (5 V Supplies)
- Robust Electromagnetic Compatibility (EMC)
  - System-level ESD, EFT, and Surge Immunity
  - Low Emissions
- Operates from 3.3 V and 5 V Supplies
- Wide Body SOIC-16 Package
- Safety and Regulatory Approvals:
  - 4242 V_{PK} Basic Isolation per DIN V VDE V 0884-10 and DIN EN 61010-1
  - 3 KV_{RMS} Isolation for 1 minute per UL 1577
  - CSA Component Acceptance Notice 5A, IEC 60950-1 and IEC 61010-1 End Equipment Standards
  - GB4943.1-2011 CQC Certification

2 Applications

- Optocoupler Replacement in:
  - Industrial Fieldbus
    - Profibus
    - Modbus
    - DeviceNet™ Data Buses
  - Servo Control Interface
  - Motor Control
  - Power Supplies
  - Battery Packs

3 Description

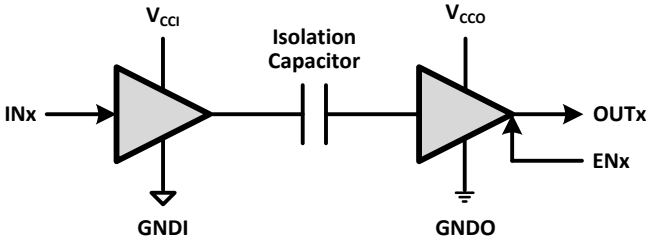
ISO734x provide galvanic isolation up to 3000 V_{RMS} for 1 minute per UL and 4242 V_{PK} per VDE. These devices have four isolated channels comprised of logic input and output buffers separated by a silicon dioxide (SiO_2) insulation barrier. ISO7340 has four channels in forward direction, ISO7341 has three forward and one reverse-direction channels; and ISO7342 has two forward and two reverse-direction channels. In case of input power or signal loss, default output is 'low' for devices with suffix 'F' and 'high' for devices without suffix 'F'. See *Device Functional Modes* for further details. Used in conjunction with isolated power supplies, these devices prevent noise currents on a data bus or other circuits from entering the local ground and interfering with or damaging sensitive circuitry. ISO734x has integrated noise filter for harsh industrial environment where short noise pulses may be present at the device input pins. ISO734x has TTL input thresholds and operates from 3 V to 5.5 V supply levels. Through innovative chip design and layout techniques, electromagnetic compatibility of ISO734x has been significantly enhanced to enable system-level ESD, EFT, Surge and Emissions compliance.

Device Information(1)

ORDER NUMBER	PACKAGE	BODY SIZE
ISO7340C	SOIC (16)	10.3mm x 7.50mm
ISO7340FC		
ISO7341C		
ISO7341FC		
ISO7342C		
ISO7342FC		

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic



(1) V_{CCI} and GNDI are supply and ground connections respectively for the input channels.

(2) V_{CCO} and GNDO are supply and ground connections respectively for the output.

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (March 2015) to Revision E — **Page**

- Deleted "(VDE V0884-10):2006-12" and "(VDE 0411-1:2011-07)" from the *Features Safety and Regulatory Approvals:* ... 1
- Deleted "(Approval Pending)" From the CSA Component Acceptance list item in the *Features* ... 1
- Changed From: V_{CC1} To: V_{CCI} in Figure 13 ... 13
- Changed From: V_{CC1} To: V_{CCI} and From: V_{CC2} To: V_{CCO} in Figure 16 ... 14
- Deleted IEC from the section title: *Insulation and Safety-Related Specifications for DW-16 Package* ... 16
- Changed the TEST Conditions of CTI in *Insulation and Safety-Related Specifications for DW-16 Package* ... 16
- Changed the Test Conditions of V_{ISO} in *Insulation Characteristics* ... 17
- Changed column CSA in the *Regulatory Information* table ... 17

Changes from Revision C (December 2014) to Revision D — **Page**

- Changed the DIN V VDE 0884-10 number in the *Features Safety and Regulatory Approvals:* ... 1
- Added "(Approval Pending)" to the CSA Component Acceptance list item in the *Features* ... 1
- Deleted "All Agencies Approvals Planned" from the *Features Safety and Regulatory Approvals:* ... 1
- Changed the Simplified Schematic: V_{CC1} To V_{CCI}, V_{CC2} to V_{CCO} and GND1 to GNDI, GND2 to GNDO. Added Notes 1 and 2 ... 1
- Added Note: "Maximum voltage must not exceed 6 V:" to *Absolute Maximum Ratings*(1) ... 5
- Changed MIN value for V_{OH} in the *Electrical Characteristics*From: V_{CCx} - 0.5 To: V_{CCO} - 0.5 ... 7
- Changed V_{CCx} To V_{CCO} in Note 1 of the *Electrical Characteristics* ... 7
- Changed MIN value for V_{OH} in the *Electrical Characteristics*From: V_{CCx} - 0.5 To: V_{CCO} - 0.5 ... 9
- Changed V_{CCx} To V_{CCO} in Note 1 of the *Electrical Characteristics* ... 9
- Added "DT1" to the Minimum internal gap in *Insulation and Safety-Related Specifications for DW-16 Package* ... 16
- Changed V_{IORM} "Maximum repetitive peak voltage" To: "Maximum repetitive peak isolation voltage per DIN V VDE V 0884-10" in *Insulation Characteristics* ... 17
- Changed V_{PR} From: "DIN V VDE 0884-10 " To: "DIN V VDE V 0884-10" in *Insulation Characteristics* ... 17

- Changed V_{IOTM} From: "DIN V VDE 0884-10 " To: "DIN V VDE V 0884-10" in *Insulation Characteristics* 17
- Changed V_{IOSM} "Maximum surge voltage per DIN V VDE 0884-10 " To: "Maximum surge isolation voltage per DIN V VDE V 0884-100" in *Insulation Characteristics* 17
- Changed V_{IOSM} Test Conditions in *Insulation Characteristics* 17
- Changed R_S Test Conditions in *Insulation Characteristics* From: T_S To: T_S = 150°C 17
- Changed the *Regulatory Information* table 17
- Changed title From: " IEC Safety Limiting Values" To: *Safety Limiting Values* 18
- Changed Table 2 Header information From: INPUT-SIDE V_{CC} To: VCC_I and OUTPUT-SIDE V_{CC} To: V_{CCO} 18
- Changed Figure 19 From: V_{CC} To: V_{CCI} on the inputs and V_{CCO} on Output and Enabled 19
- Moved Figure 21 to Figure 23 from the *Design Requirements* section to the *Detailed Design Procedure* section 21

Changes from Revision B (November 2014) to Revision C **Page**

- Changed the Handling Ratings table to ESD Ratings 5
- Changed the I_{CC2}, Supply current, DC to 1 Mbps TYP value From: 3 To 3.2 mA 7
- Changed the I_{CC2}, Supply current, 10 Mbps TYP value From: 5.1 To 5.6 mA 7
- Changed the I_{CC2}, Supply current, 25 Mbps TYP value From: 8.6 To 9.3 mA 7
- Changed the I_{CC1}, Supply current, 10 Mbps TYP value From: 0.8 To 0.9 mA 9
- Changed the I_{CC2}, Supply current, 10 Mbps TYP value From: 0.3.6 To 3.9 mA 9
- Changed the I_{CC2}, Supply current, 25 Mbps TYP value From: 5.9 To 6.3 mA 9
- Added Figure 1 and Figure 2 11
- Changed Figure 4 11
- Changed Minimum internal gap MIN value in *Insulation and Safety-Related Specifications for DW-16 Package* From: 0.014 mm To: 13.5 µm 16
- Changed Minimum internal gap MIN value in *Insulation and Safety-Related Specifications for DW-16 Package* From: 13.5 µm To: 13 µm 16
- Delete text "per DIN V VDE 0884-10" from V_{IORM} in the table in section *Insulation Characteristics* 17
- Changed From: V_{PEAK} To V_{PK} in the UNIT column of the table in section *Insulation Characteristics* 17
- Added V_{IOSM} to the table in section *Insulation Characteristics* 17
- Changed the table in *Regulatory Information* section - removed text "Certified according to", "Approved under", "Recognized under", changed "pending" To: "planned" 17
- Changed Maximum Repetitive Peak Voltage, 1414 V_{PK} To: Maximum surge voltage , 6000 V_{PK} in the VDE column of the table in section *Regulatory Information* 17

Changes from Revision A (Octoberr 2014) to Revision B **Page**

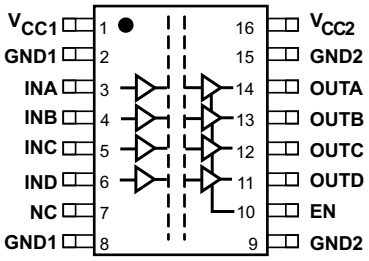
- Added Figure 3 and Figure 4 11
- Changed the R_{IO} Test Conditions in *Insulation and Safety-Related Specifications for DW-16 Package* : Added T_A = 25°C at MIN = 10^{12} 16
- Changed the R_{IO} Test Conditions in *Insulation and Safety-Related Specifications for DW-16 Package* : Added V_{IO} = 500 V, 100°C ≤ T_A ≤ 125°C at MIN = 10^{11} 16
- Added Test Condition to Table 1: Rated mains voltage ≤ 1000 V_{RMS} 17

Changes from Original (September 2014) to Revision A **Page**

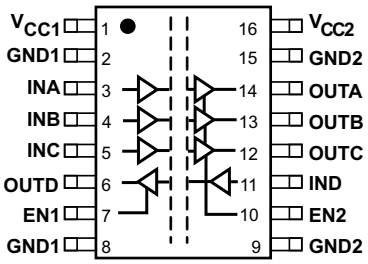
- Changed From a 1 page Product Preview to the full datasheet 1
- Changed the *Simplified Schematic*, added ground symbols 1

5 Pin Configuration and Functions

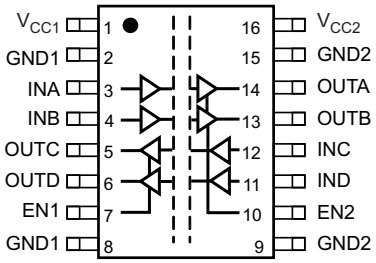
ISO7340
DW Package
Top View



ISO7341
DW Package
Top View



ISO7342
DW Package
Top View



Pin Functions

PIN				I/O	DESCRIPTION
NAME	ISO7340	ISO7341	ISO7342		
INA	3	3	3	I	Input, channel A
INB	4	4	4	I	Input, channel B
INC	5	5	12	I	Input, channel C
IND	6	11	11	I	Input, channel D
OUTA	14	14	14	O	Output, channel A
OUTB	13	13	13	O	Output, channel B
OUTC	12	12	5	O	Output, channel C
OUTD	11	6	6	O	Output, channel D
EN1	–	7	7	I	Output enable 1. Output pins on side-1 are enabled when EN1 is high or disconnected and disabled when EN1 is low.
EN2	–	10	10	I	Output enable 2. Output pins on side-2 are enabled when EN2 is high or disconnected and disabled when EN2 is low.
EN	10	–	–	I	Output enable. All output pins are enabled when EN is high or disconnected and disabled when EN is low.
V_{CC1}	1	1	1	–	Power supply, V_{CC1}
V_{CC2}	16	16	16	–	Power supply, V_{CC2}
GND1	2,8	2,8	2, 8	–	Ground connection for V_{CC1}
GND2	9,15	9,15	9, 15	–	Ground connection for V_{CC2}
NC	7	–	–	–	No Connect pins are floating with no internal connection

6 Specifications

6.1 Absolute Maximum Ratings(1)

		MIN	MAX	UNIT
Supply voltage(2)	V_{CC1}, V_{CC2}	–0.5	6	V
Voltage	INx, OUTx, ENx	–0.5	V_{CC} + 0.5(3)	V
Output Current, I_O			±15	mA
Maximum junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GND1 or GND2) and are peak voltage values.
(3) Maximum voltage must not exceed 6 V.

6.2 ESD Ratings

			VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	±4000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

PARAMETER		MIN	TYP	MAX	UNIT
V_{CC1}, V_{CC2}	Supply voltage	3		5.5	V
I_{OH}	High-level output current	-4			mA
I_{OL}	Low-level output current			4	mA
V_{IH}	High-level input voltage	2		5.5	V
V_{IL}	Low-level input voltage	0		0.8	V
t_{ui}	Input pulse duration	40			ns
1 / t_{ui}	Signaling rate	0		25	Mbps
T_J	Junction temperature(1)			136	°C
T_A	Ambient temperature	-40	25	125	°C

(1) To maintain the recommended operating conditions for T_J, see the *Thermal Information* table.

6.4 Thermal Information

THERMAL METRIC			DW (16 Pins)	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance		78.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance		41.0	
$R_{\theta JB}$	Junction-to-board thermal resistance		43.0	
ψ_{JT}	Junction-to-top characterization parameter		15.6	
ψ_{JB}	Junction-to-board characterization parameter		42.5	
$R_{\theta JC(bottom)}$	Junction-to-case(bottom) thermal resistance		n/a	
P_D	Maximum Power Dissipation by ISO7340	$V_{CC1} = V_{CC2} = 5.5V$, $T_J = 150°C$, $C_L = 15pF$, Input a 12.5 MHz 50% duty cycle square wave	92	mW
P_{D1}	Maximum Power Dissipation by Side-1 of ISO7340		24	
P_{D2}	Maximum Power Dissipation by Side-2 of ISO7340		68	
P_D	Maximum Power Dissipation by ISO7341	$V_{CC1} = V_{CC2} = 5.5V$, $T_J = 150°C$, $C_L = 15pF$, Input a 12.5 MHz 50% duty cycle square wave	102	mW
P_{D1}	Maximum Power Dissipation by Side-1 of ISO7341		42	
P_{D2}	Maximum Power Dissipation by Side-2 of ISO7341		60	
P_D	Maximum Power Dissipation by ISO7342	$V_{CC1} = V_{CC2} = 5.5V$, $T_J = 150°C$, $C_L = 15pF$, Input a 12.5 MHz 50% duty cycle square wave	111	mW
P_{D1}	Maximum Power Dissipation by Side-1 of ISO7342		55.5	
P_{D2}	Maximum Power Dissipation by Side-2 of ISO7342		55.5	

6.5 Electrical Characteristics

V_{CC1} and V_{CC2} at 5 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA; see Figure 13		V_{CCO} (1) – 0.5	4.7		V
		I_{OH} = –20 µA; see Figure 13		V_{CCO} (1) – 0.1	5		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; see Figure 13			0.2	0.4	V
		I_{OL} = 20 µA; see Figure 13			0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis				480		mV
I_{IH}	High-level input current	V_{IH} = V_{CC} at INx or ENx				10	µA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx or ENx		-10			
CMTI	Common-mode transient immunity	V_I = V_{CC} or 0 V; see Figure 16		25	70		kV/µs
Supply Current (All inputs switching with square wave clock signal for dynamic I_{CC} measurement)							
ISO7340							
I_{CC1}	Supply current	Disable	EN = 0 V		0.6	1.4	mA
I_{CC2}					0.4	0.8	
I_{CC1}		DC to 1 Mbps	DC Signal: V_I = V_{CC} or 0 V, AC Signal: All channels switching with square wave clock input; C_L = 15 pF		0.6	1.4	
I_{CC2}					3.2	4.8	
I_{CC1}		10 Mbps			1.4	2.3	
I_{CC2}					5.6	7.1	
I_{CC1}		25 Mbps			2.7	4	
I_{CC2}					9.3	12	
ISO7341							
I_{CC1}	Supply current	Disable	EN1 = EN2 = 0 V		0.8	1.8	mA
I_{CC2}					0.7	1.3	
I_{CC1}		DC to 1 Mbps	DC Signal: V_I = V_{CC} or 0 V, AC Signal: All channels switching with square wave clock input; C_L = 15 pF		2	3.2	
I_{CC2}					2.9	4.4	
I_{CC1}		10 Mbps			3.2	4.5	
I_{CC2}					4.9	6.5	
I_{CC1}		25 Mbps			5	7	
I_{CC2}					7.8	11	
ISO7342							
I_{CC1}, I_{CC2}	Supply current	Disable	EN1 = EN2 = 0 V		0.7	1.6	mA
I_{CC1}, I_{CC2}		DC to 1 Mbps	DC Signal: V_I = V_{CC} or 0 V, AC Signal: All channels switching with square wave clock input; C_L = 15 pF		2.5	4	
I_{CC1}, I_{CC2}		10 Mbps			4.1	5.6	
I_{CC1}, I_{CC2}		25 Mbps			6.4	9	

(1) V_{CCO} is supply voltage, V_{CC1} or V_{CC2}, for the output channel being measured.

6.6 Switching Characteristics

V_{CC1} and V_{CC2} at 5 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time		See Figure 13	20	31	58	ns
PWD (1)	Pulse width distortion $\lvert t_{PHL} - t_{PLH} \rvert$					4	
$t_{sk(o)}$ (2)	Channel-to-channel output skew time		Same-direction Channels			2.5	
			Opposite-direction Channels			17	
$t_{sk(pp)}$ (3)	Part-to-part skew time					23	
t_r	Output signal rise time		See Figure 13		2.1		ns
t_f	Output signal fall time				1.7		
t_{PHZ}	Disable Propagation Delay, high-to-high impedance output		See Figure 14		7	13	ns
t_{PLZ}	Disable Propagation Delay, low-to-high impedance output				7	13	
t_{PZH}	Enable Propagation Delay, high impedance-to-high output	ISO734xC			7	13	
		ISO734xFC			15000	23000 (4)	
t_{PZL}	Enable Propagation Delay, high impedance-to-low output	ISO734xC			15000	23000 (4)	
		ISO734xFC			7	13	
t_{fs}	Fail-safe output delay time from input power loss		See Figure 15		9.4		µs

(1) Also known as Pulse Skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.
(4) The enable signal rate should be ≤ 43 Kbps.

6.7 Electrical Characteristics

V_{CC1} and V_{CC2} at 3.3 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA; see Figure 13		V_{CCO} (1) – 0.5	3		V
		I_{OH} = –20 µA; see Figure 13		V_{CCO} (1) – 0.1	3.3		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; see Figure 13			0.2	0.4	V
		I_{OL} = 20 µA; see Figure 13			0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis				450		mV
I_{IH}	High-level input current	V_{IH} = V_{CC} at INx or ENx				10	µA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx or ENx		-10			
CMTI	Common-mode transient immunity	V_I = V_{CC} or 0 V; see Figure 16		25	50		kV/µs
Supply Current (All inputs switching with square wave clock signal for dynamic I_{CC} measurement)							
ISO7340							
I_{CC1}	Supply current	Disable	EN = 0 V		0.4	0.7	mA
I_{CC2}					0.3	0.6	
I_{CC1}		DC to 1 Mbps	DC Signal: V_I = V_{CC} or 0 V, AC Signal: All channels switching with square wave clock input; C_L = 15 pF		0.4	0.7	
I_{CC2}					2.3	3.6	
I_{CC1}		10 Mbps			0.9	1.3	
I_{CC2}					3.9	5.1	
I_{CC1}		25 Mbps			1.6	2.4	
I_{CC2}					6.3	8	
ISO7341							
I_{CC1}	Supply current	Disable	EN1 = EN2 = 0 V		0.6	1	mA
I_{CC2}					0.5	0.8	
I_{CC1}		DC to 1 Mbps	DC Signal: V_I = V_{CC} or 0 V, AC Signal: All channels switching with square wave clock input; C_L = 15 pF		1.4	2.3	
I_{CC2}					2.2	3.2	
I_{CC1}		10 Mbps			2.2	3	
I_{CC2}					3.4	4.5	
I_{CC1}		25 Mbps			3.3	4.7	
I_{CC2}					5.2	7.2	
ISO7342							
I_{CC1}, I_{CC2}	Supply current	Disable	EN1 = EN2 = 0 V		0.5	0.9	mA
I_{CC1}, I_{CC2}		DC to 1 Mbps	DC Signal: V_I = V_{CC} or 0 V, AC Signal: All channels switching with square wave clock input; C_L = 15 pF		1.8	2.8	
I_{CC1}, I_{CC2}		10 Mbps			2.8	4	
I_{CC1}, I_{CC2}		25 Mbps			4.3	5.8	

(1) V_{CCO} is supply voltage, V_{CC1} or V_{CC2}, for the output channel being measured.

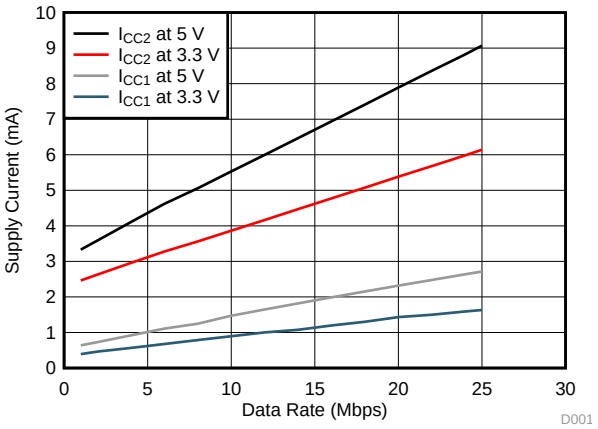
6.8 Switching Characteristics

V_{CC1} and V_{CC2} at 3.3 V ± 10% (over recommended operating conditions unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time		See Figure 13	22	35	66	ns
PWD (1)	Pulse width distortion $\lvert t_{PHL} - t_{PLH} \rvert$		See Figure 13			2.5	ns
$t_{sk(o)}$ (2)	Channel-to-channel output skew time		Same-direction Channels			3	ns
			Opposite-direction Channels			16	ns
$t_{sk(pp)}$ (3)	Part-to-part skew time		See Figure 13			28	ns
t_r	Output signal rise time		See Figure 13		2.8		ns
t_f	Output signal fall time		See Figure 13		2.1		ns
t_{PHZ}	Disable Propagation Delay, high-to-high impedance output		See Figure 14		9	18	ns
t_{PLZ}	Disable Propagation Delay, low-to-high impedance output		See Figure 14		9	18	ns
t_{PZH}	Enable Propagation Delay, high impedance-to-high output	ISO734xC	See Figure 14		9	18	ns
		ISO734xFC	See Figure 14		16	24000 (4)	ns
t_{PZL}	Enable Propagation Delay, high impedance-to-low output	ISO734xC	See Figure 14		16	24000 (4)	ns
		ISO734xFC	See Figure 14		9	18	ns
t_{fs}	Fail-safe output delay time from input power loss		See Figure 15		9.4		µs

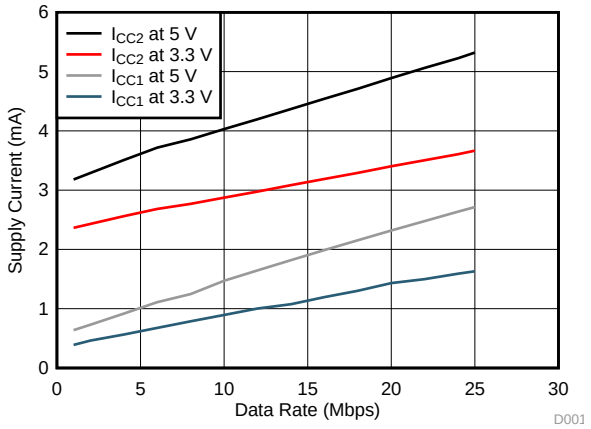
(1) Also known as Pulse Skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.
(4) The enable signal rate should be ≤ 45 Kbps.

6.9 Typical Characteristics



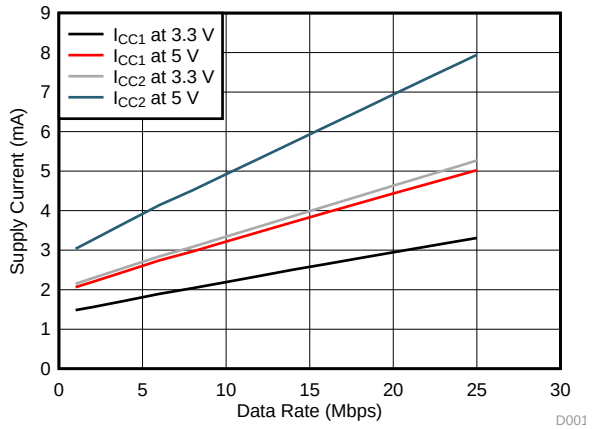
T_A = 25°C C_L = 15 pF

Figure 1. ISO7340 Supply Current vs Data Rate (15 pF Load)



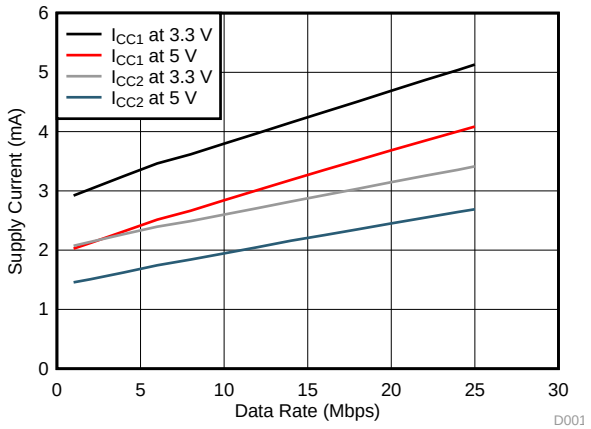
T_A = 25°C C_L = No Load

Figure 2. ISO7340 Supply Current vs Data Rate (No Load)



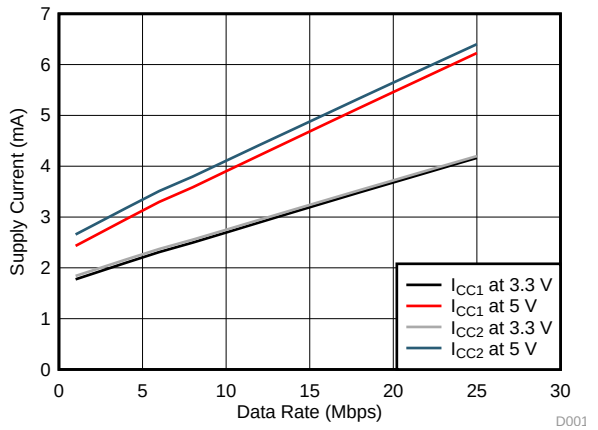
T_A = 25°C C_L = 15 pF

Figure 3. ISO7341 Supply Current vs Data Rate (15 pF Load)



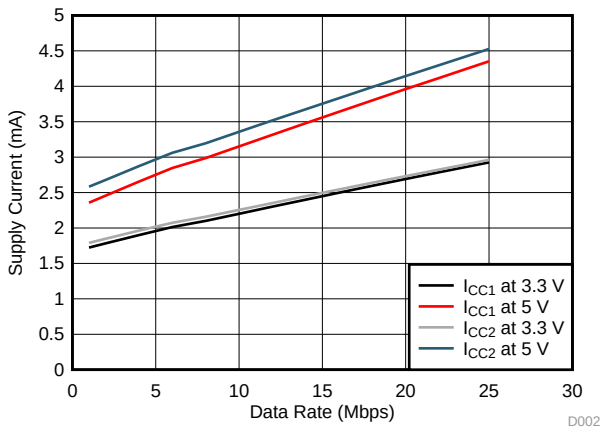
T_A = 25°C C_L = No Load

Figure 4. ISO7341 Supply Current vs Data Rate (No Load)



T_A = 25°C C_L = 15 pF

Figure 5. ISO7342 Supply Current vs Data Rate (15 pF Load)



T_A = 25°C C_L = No Load

Figure 6. ISO7342 Supply Current vs Data Rate (No Load)

Typical Characteristics (continued)

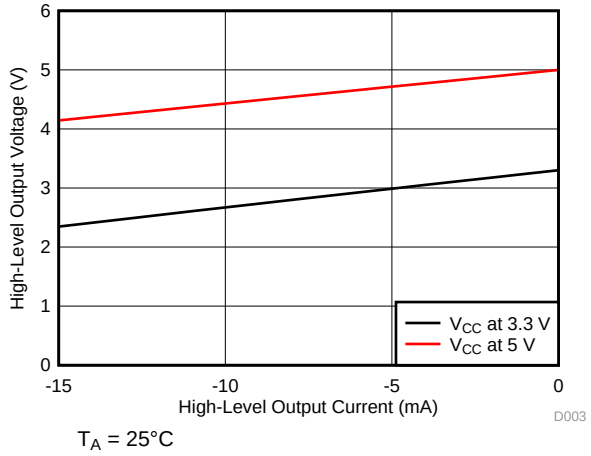


Figure 7. High-Level Output Voltage vs High-level Output Current

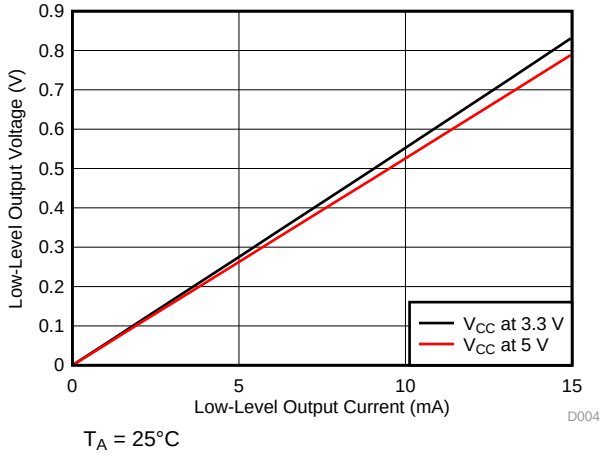


Figure 8. Low-Level Output Voltage vs Low-Level Output Current

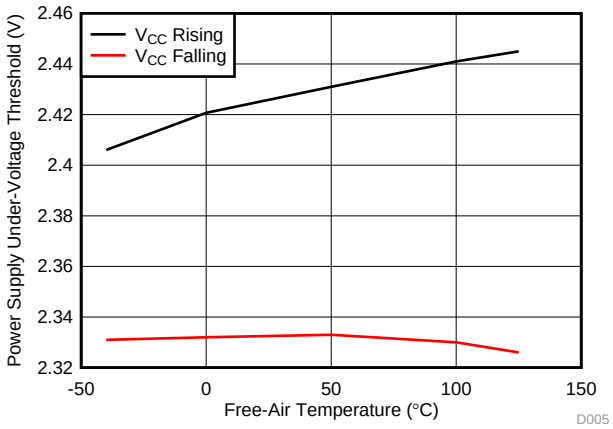


Figure 9. Power Supply Undervoltage Threshold vs Free-Air Temperature

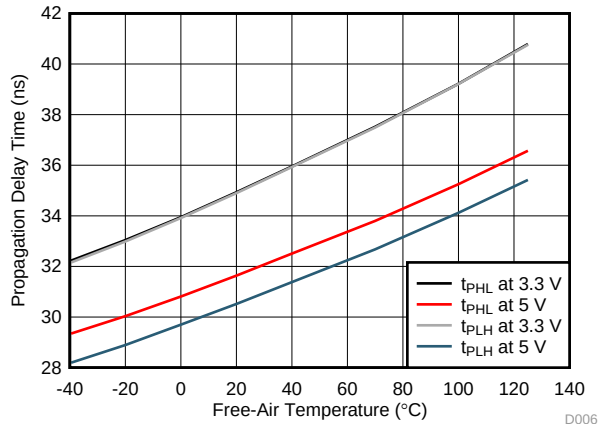


Figure 10. Propagation Delay Time vs Free-Air Temperature

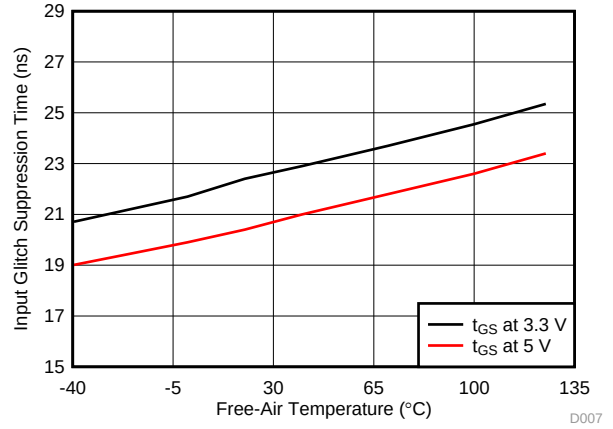


Figure 11. Input Glitch Suppression Time vs Free-Air Temperature

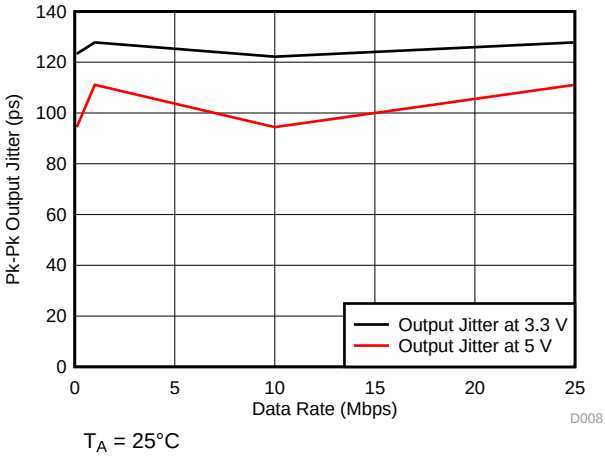
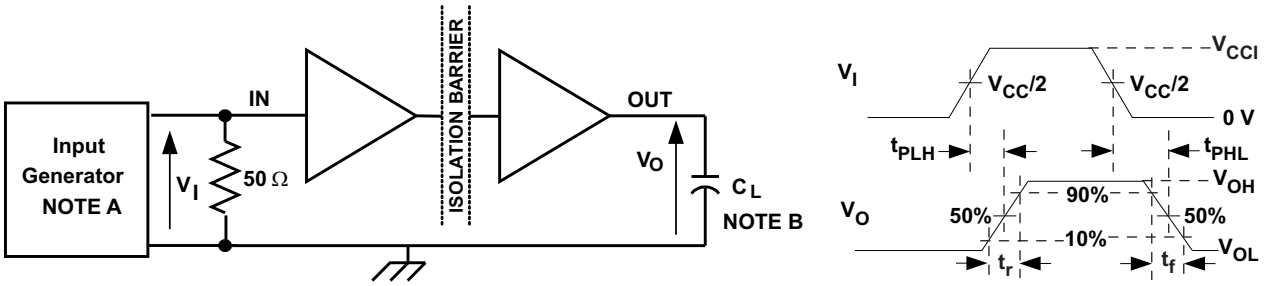


Figure 12. Output Jitter vs Data Rate

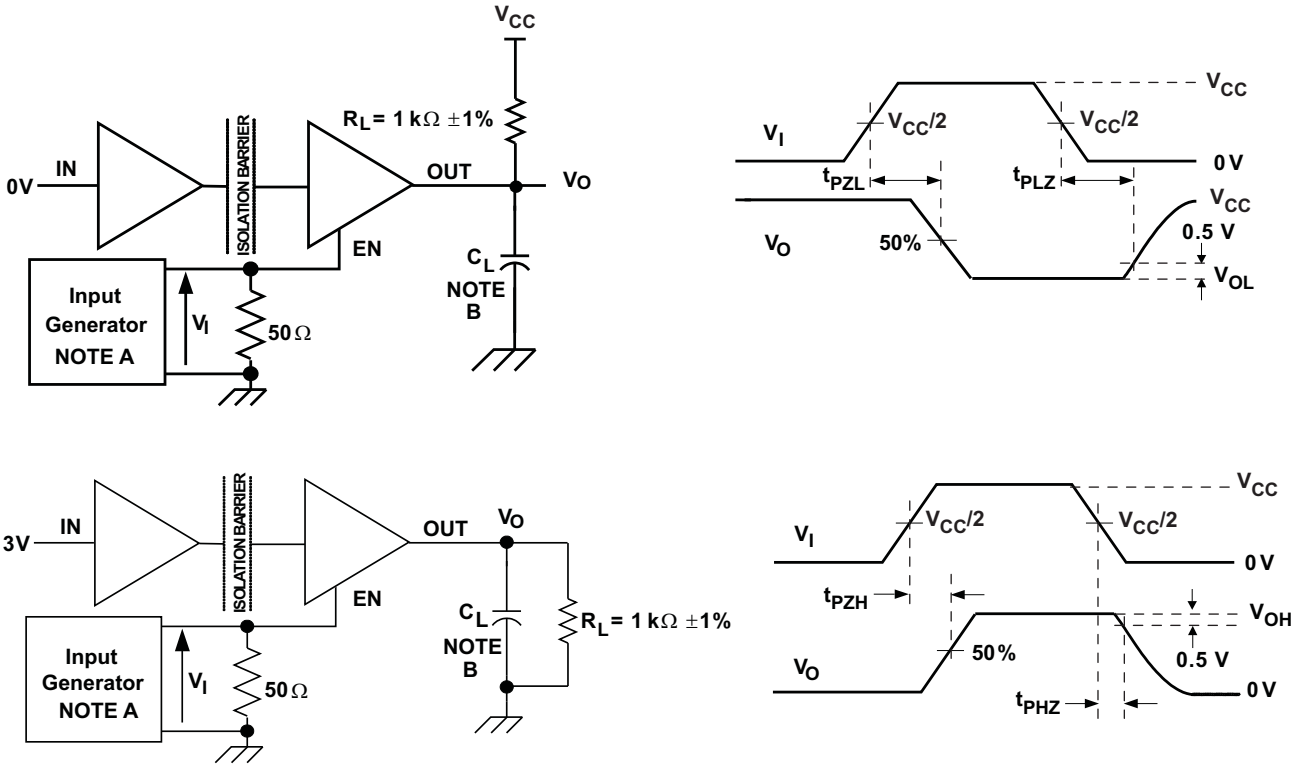
7 Parameter Measurement Information



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3ns, Z_O = 50 Ω. At the input, 50 Ω resistor is required to terminate Input Generator signal. It is not needed in actual application.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 13. Switching Characteristics Test Circuit and Voltage Waveforms

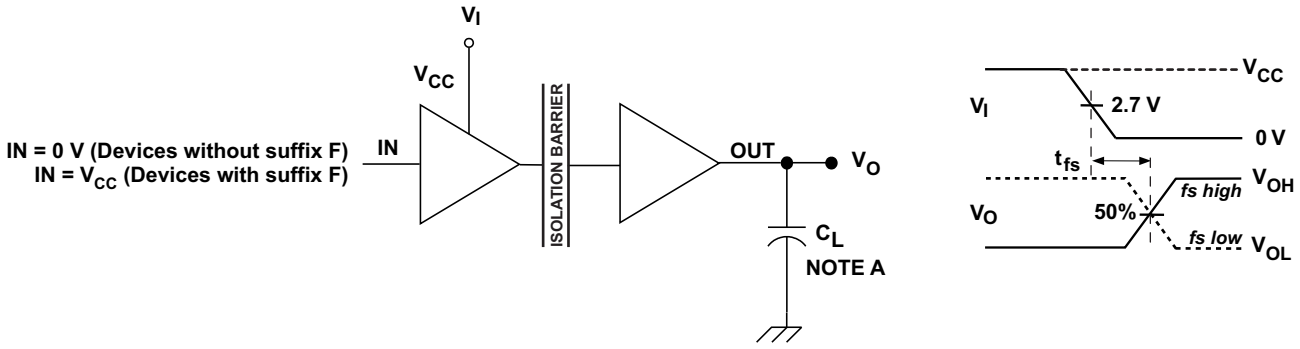


A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 10 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50 Ω.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

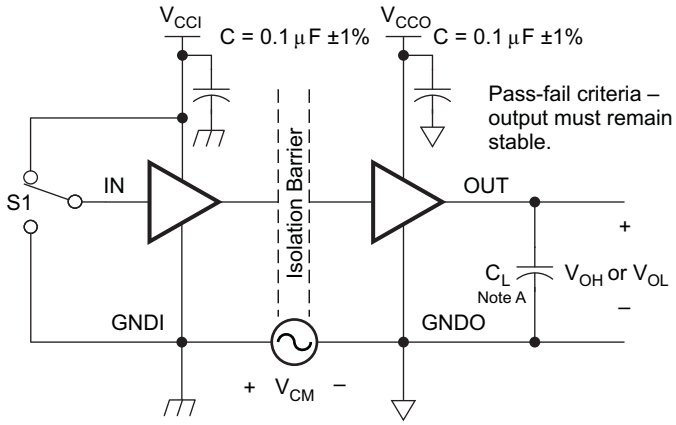
Figure 14. Enable/Disable Propagation Delay Time Test Circuit and Waveform

Parameter Measurement Information (continued)



A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 15. Failsafe Delay Time Test Circuit and Voltage Waveforms



A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 16. Common-Mode Transient Immunity Test Circuit

8 Detailed Description

8.1 Overview

The isolator in Figure 17 is based on a capacitive isolation barrier technique. The I/O channel of the device consists of two internal data channels, a high-frequency (HF) channel with a bandwidth from 100 kbps up to 25 Mbps, and a low-frequency (LF) channel covering the range from 100 kbps down to DC.

In principle, a single-ended input signal entering the HF channel is split into a differential signal via the inverter gate at the input. The following capacitor-resistor networks differentiate the signal into transient pulses, which then are converted into CMOS levels by a comparator. The transient pulses at the input of the comparator can be either above or below the common mode voltage VREF depending on whether the input bit transitioned from 0 to 1 or 1 to 0. The comparator threshold is adjusted based on the expected bit transition. A decision logic (DCL) at the output of the HF channel comparator measures the durations between signal transients. If the duration between two consecutive transients exceeds a certain time limit, (as in the case of a low-frequency signal), the DCL forces the output-multiplexer to switch from the high-frequency to the low-frequency channel.

Because low-frequency input signals require the internal capacitors to assume prohibitively large values, these signals are pulse-width modulated (PWM) with the carrier frequency of an internal oscillator, thus creating a sufficiently high frequency, capable of passing the capacitive barrier. As the input is modulated, a low-pass filter (LPF) is needed to remove the high-frequency carrier from the actual data before passing it on to the output multiplexer.

8.2 Functional Block Diagram

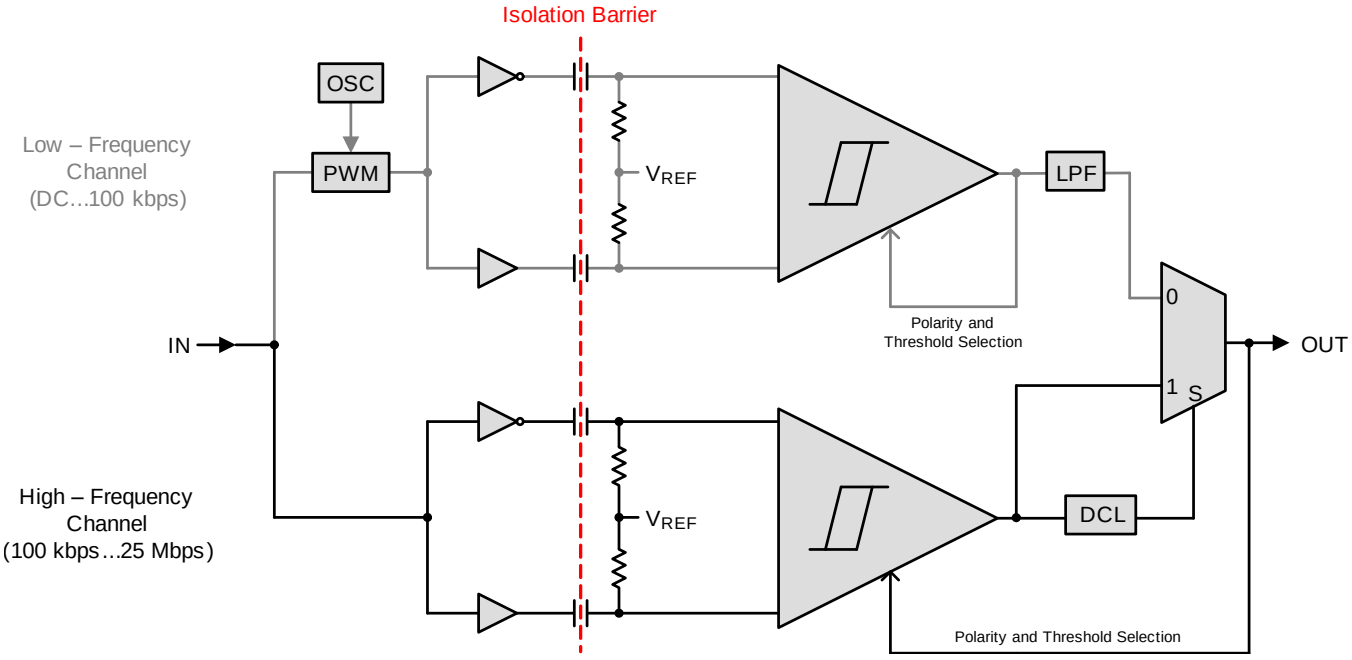


Figure 17. Conceptual Block Diagram of a Digital Capacitive Isolator

8.3 Feature Description

ISO734x are available in multiple channel configurations and default output state options to enable wide variety of application uses.

PRODUCT	CHANNEL DIRECTION	RATED ISOLATION	MAX DATA RATE	DEFAULT OUTPUT
ISO7340C	4 Forward, 0 Reverse	3000 V_{RMS} / 4242 V_{PK} (1)	25 Mbps	High
ISO7340FC				Low
ISO7341C	3 Forward, 1 Reverse			High
ISO7341FC				Low
ISO7342C	2 Forward, 2 Reverse			High
ISO7342FC				Low

(1) See the *Regulatory Information* section for detailed isolation ratings.

8.3.1 High Voltage Feature Description

8.3.1.1 Insulation and Safety-Related Specifications for DW-16 Package

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
L(I01)	Minimum air gap (clearance)	Shortest terminal-to-terminal distance through air	8			mm
L(I02)	Minimum external tracking (creepage)	Shortest terminal-to-terminal distance across the package surface	8			mm
CTI	Tracking resistance (comparative tracking index)	DIN EN 60112 (VDE 0303-11); IEC 60112	400			V
DTI	Minimum internal gap (internal clearance)	Distance through the insulation	13			µm
R_{IO}	Isolation resistance, input to output(1)	V_{IO} = 500 V, T_A = 25°C	10^{12}			Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125°C	10^{11}			
C_{IO}	Isolation capacitance, input to output(1)	V_{IO} = 0.4 sin (2πft), f = 1 MHz		2.4		pF
C_I	Input capacitance(2)	V_I = V_{CC}/2 + 0.4 sin (2πft), f = 1 MHz, V_{CC} = 5 V		3.4		pF

(1) All pins on each side of the barrier tied together creating a two-terminal device.
(2) Measured from input pin to ground.

NOTE

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.

8.3.1.2 Insulation Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER(1)		TEST CONDITIONS	SPECIFICATION	UNIT
V_{IOWM}	Maximum isolation working voltage		1000	V_{RMS}
V_{IORM}	Maximum repetitive peak isolation voltage per DIN V VDE V 0884-10		1414	V_{PK}
V_{PR}	Input-to-output test voltage per DIN V VDE V 0884-10	After Input/Output safety test subgroup 2/3, V_{PR} = V_{IORM} x 1.2, t = 10 s, Partial discharge < 5 pC	1697	V_{PK}
		Method a, After environmental tests subgroup 1, V_{PR} = V_{IORM} x 1.6, t = 10 s, Partial Discharge < 5 pC	2262	
		Method b1, V_{PR} = V_{IORM} x 1.875, t = 1 s (100% Production test) Partial discharge < 5 pC	2651	
V_{IOTM}	Maximum transient overvoltage per DIN V VDE V 0884-10	V_{TEST} = V_{IOTM} t = 60 sec (qualification) t = 1 sec (100% production)	4242	V_{PK}
V_{IOSM}	Maximum surge isolation voltage per DIN V VDE V 0884-10	Test method per IEC 60065, 1.2/50 µs waveform, V_{TEST} = 1.3 x V_{IOSM} = 7800 V_{PK} (qualification)	6000	V_{PK}
V_{ISO}	Withstand isolation voltage per UL 1577	V_{TEST} = V_{ISO} = 3000 V_{RMS}, t = 60 sec (qualification) V_{TEST} = 1.2 x V_{ISO} = 3600 V_{RMS}, t = 1 sec (100% production)	3000	V_{RMS}
R_S	Insulation resistance	V_{IO} = 500 V at T_S = 150°C	>10^9	Ω
	Pollution degree		2	

(1) Climatic Classification 40/125/21

Table 1. IEC 60664-1 Ratings Table

PARAMETER	TEST CONDITIONS	SPECIFICATION
Basic isolation group	Material group	II
Installation classification	Rated mains voltage ≤ 300 V_{RMS}	I–IV
	Rated mains voltage ≤ 600 V_{RMS}	I–III
	Rated mains voltage ≤ 1000 V_{RMS}	I-II

8.3.1.3 Regulatory Information

VDE	CSA	UL	CQC
Certified according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 and DIN EN 61010-1 (VDE 0411-1):2011-07	Approved under CSA Component Acceptance Notice 5A, IEC 60950-1, and IEC 61010-1	Recognized under UL 1577 Component Recognition Program	Certified according to GB4943.1-2011
Basic Insulation; Maximum Transient Overvoltage, 4242 V_{PK}; Maximum Surge Isolation Voltage , 6000 V_{PK}; Maximum Repetitive Peak Isolation Voltage, 1414 V_{PK}	800 V_{RMS} Basic Insulation and 400 V_{RMS} Reinforced Insulation working voltage per CSA 60950-1-07+A1+A2 and IEC 60950-1 2nd Ed.+A1+A2; 300 V_{RMS} Basic Insulation working voltage per CSA 61010-1-12 and IEC 61010-1 3rd Ed.	Single protection, 3000 V_{RMS} (1)	Reinforced Insulation, Altitude ≤ 5000 m, Tropical Climate, 250 V_{RMS} maximum working voltage
Certificate number: 40016131	Master contract number: 220991	File number: E181974	Certificate number: CQC15001121716

(1) Production tested ≥ 3600 V_{RMS} for 1 second in accordance with UL 1577.

8.3.1.4 Safety Limiting Values

Safety limiting intends to prevent potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier, potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 78.4 °C/W, V_I = 5.5 V, T_J = 150°C, T_A = 25°C			290	mA
		$R_{\theta JA}$ = 78.4 °C/W, V_I = 3.6 V, T_J = 150°C, T_A = 25°C			443	
T_S	Maximum case temperature				150	°C

The safety-limiting constraint is the absolute-maximum junction temperature specified in the *Absolut Maximun Ratings* table. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the *Thermal Information* table is that of a device installed on a High-K Test Board for Leaded Surface-Mount Packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

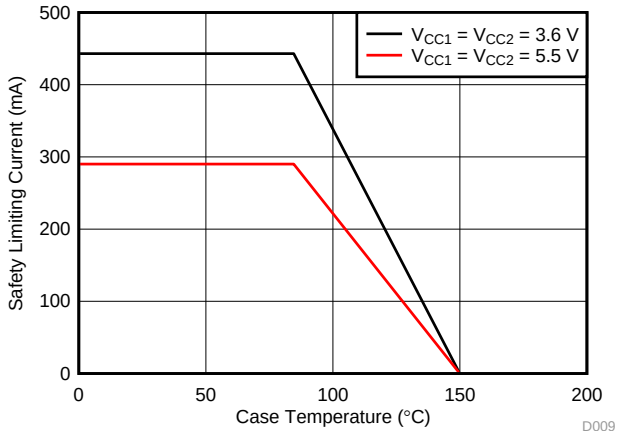


Figure 18. θ_{JC} Thermal Derating Curve per DIN V VDE 0884-10

8.4 Device Functional Modes

ISO734x functional modes are shown in Table 2.

Table 2. Function Table(1)

V_{CCI}	V_{CCO}	INPUT (INx)	OUTPUT ENABLE (ENx)	OUTPUT (OUTx)	
				ISO734xC	ISO734xFC
PU	PU	H	H or Open	H	H
		L	H or Open	L	L
		X	L	Z	Z
		Open	H or Open	H(2)	L(3)
PD	PU	X	H or Open	H(2)	L(3)
X	PU	X	L	Z	Z
X	PD	X	X	Undetermined	Undetermined

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}; PU = Powered up (V_{CC} ≥ 3 V); PD = Powered down (V_{CC} ≤ 2.1 V); X = Irrelevant; H = High level; L = Low level ; Z = High Impedance
(2) In fail-safe condition, output defaults to high level
(3) In fail-safe condition, output defaults to low level

8.4.1 Device I/O Schematics

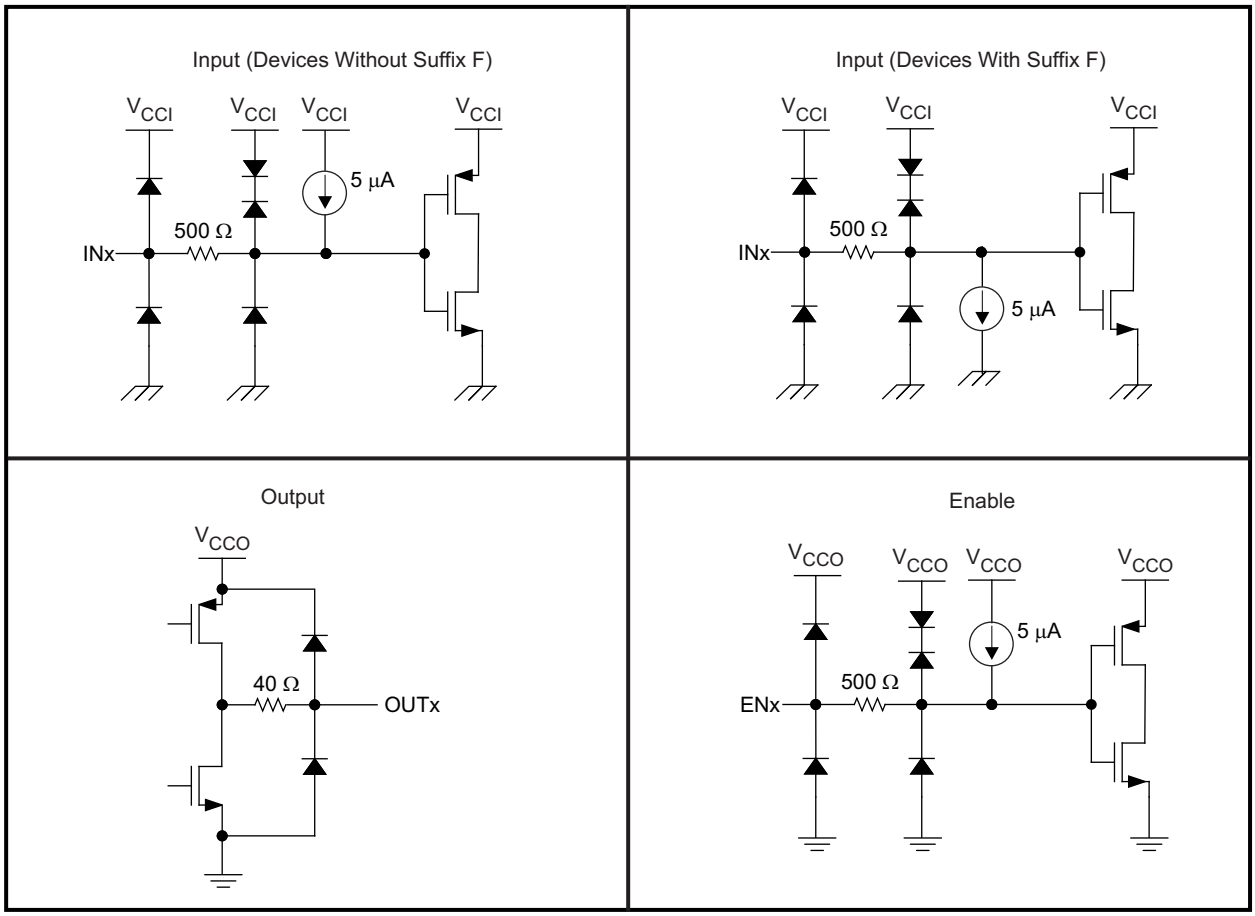


Figure 19. Device I/O Schematics

9 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

ISO734x use single-ended TTL-logic switching technology. Its supply voltage range is from 3 V to 5.5 V for both supplies, V_{CC1} and V_{CC2}. When designing with digital isolators, it is important to note that due to the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended CMOS or TTL digital signal lines. The isolator is typically placed between the data controller (that is, µC or UART), and a data converter or a line transceiver, regardless of the interface type or standard.

9.2 Typical Application

9.2.1 Isolated Data Acquisition System for Process Control

ISO734x combined with Texas Instruments' precision analog-to-digital converter and mixed signal micro-controller can create an advanced isolated data acquisition system as shown in Figure 20.

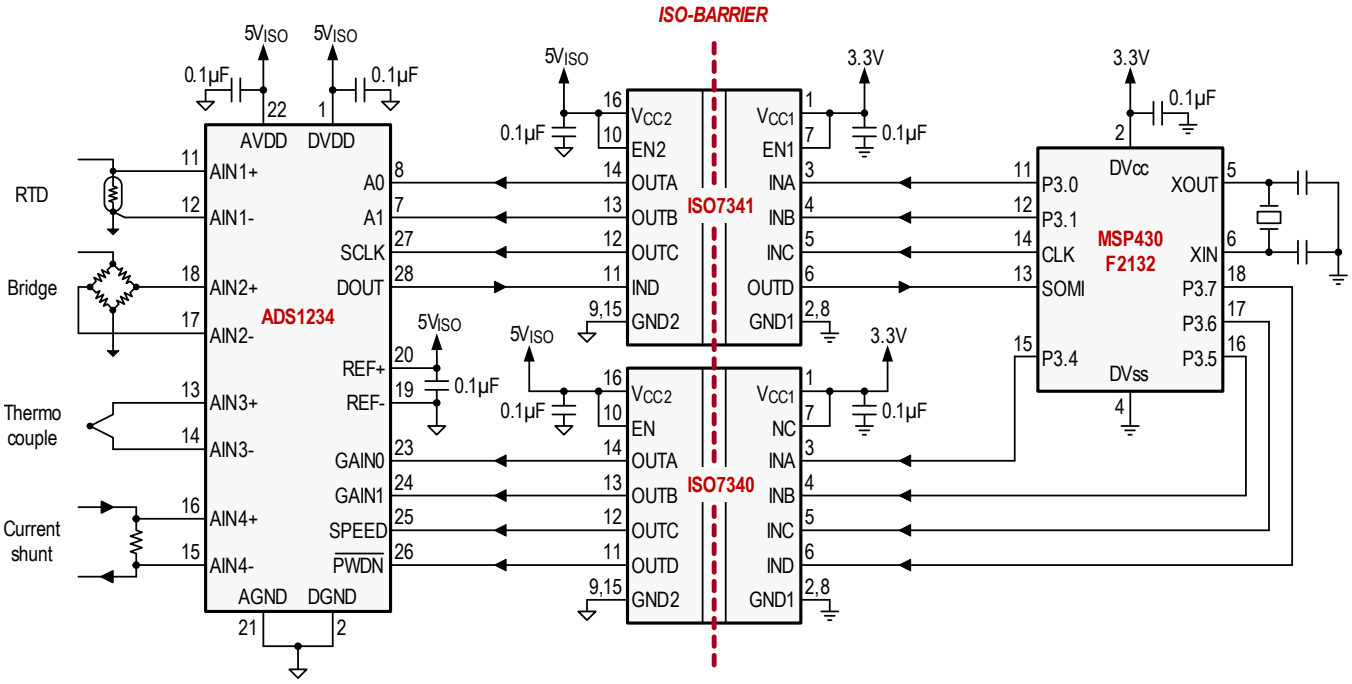


Figure 20. Isolated Data Acquisition System for Process Control

Typical Application (continued)

9.2.1.1 Design Requirements

9.2.1.1.1 Typical Supply Current Equations

9.2.1.1.1.1 ISO7340

At $V_{CC1} = V_{CC2} = 5$ V

$$I_{CC1} = 0.54366 + (0.0873 \times f) \quad (1)$$

$$I_{CC2} = 2.74567 + (0.08433 \times f) + (0.01 \times f \times C_L) \quad (2)$$

At $V_{CC1} = V_{CC2} = 3.3$ V

$$I_{CC1} = 0.3437 + (0.04922 \times f) \quad (3)$$

$$I_{CC2} = 2.1068 + (0.04374 \times f) + (0.007045 \times f \times C_L) \quad (4)$$

9.2.1.1.1.2 ISO7341

At $V_{CC1} = V_{CC2} = 5$ V

$$I_{CC1} = 1.7403 + (0.1006 \times f) + (0.001711 \times f \times C_L) \quad (5)$$

$$I_{CC2} = 2.502 + (0.09629 \times f) + (0.00687 \times f \times C_L) \quad (6)$$

At $V_{CC1} = V_{CC2} = 3.3$ V

$$I_{CC1} = 1.2915 + (0.046 \times f) + (0.00185 \times f \times C_L) \quad (7)$$

$$I_{CC2} = 1.8833 + (0.0566 \times f) + (0.004514 \times f \times C_L) \quad (8)$$

9.2.1.1.1.3 ISO7342

At $V_{CC1} = V_{CC2} = 5$ V

$$I_{CC1}, I_{CC2} = 2.1254 + (0.08694 \times f) + (0.004868 \times f \times C_L) \quad (9)$$

At $V_{CC1} = V_{CC2} = 3.3$ V

$$I_{CC1}, I_{CC2} = 1.5912 + (0.0410 \times f) + (0.003785 \times f \times C_L) \quad (10)$$

I_{CC1} and I_{CC2} are typical supply currents measured in mA, f is data rate measured in Mbps, C_L is the capacitive load measured in pF.

9.2.1.2 Detailed Design Procedure

Unlike optocouplers, which need external components to improve performance, provide bias, or limit current, ISO734x only needs two external bypass capacitors to operate.

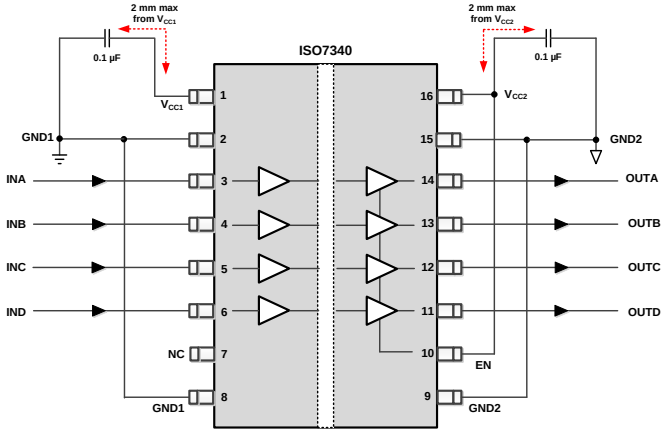


Figure 21. Typical ISO7340 Circuit Hook-up

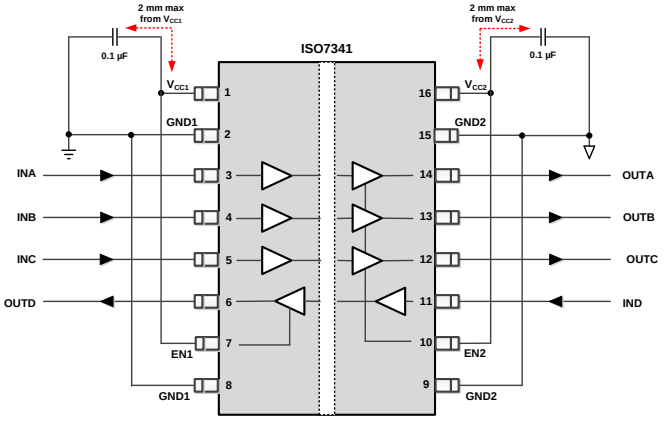


Figure 22. Typical ISO7341 Circuit Hook-up

Typical Application (continued)

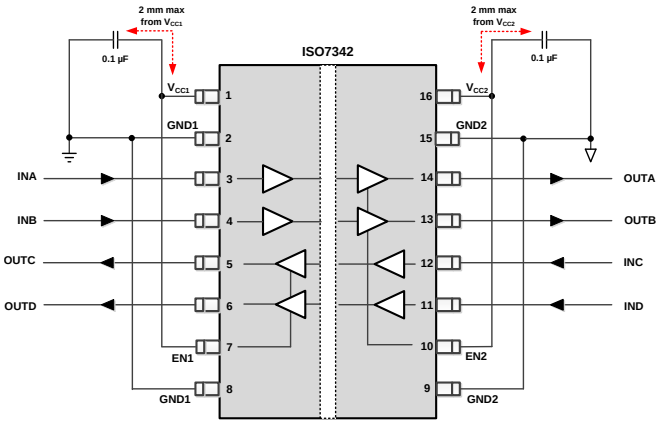


Figure 23. Typical ISO7342 Circuit Hook-up

9.2.1.2.1 Electromagnetic Compatibility (EMC) Considerations

Many applications in harsh industrial environment are sensitive to disturbances such as electrostatic discharge (ESD), electrical fast transient (EFT), surge and electromagnetic emissions. These electromagnetic disturbances are regulated by international standards such as IEC 61000-4-x and CISPR 22. Although system-level performance and reliability depends, to a large extent, on the application board design and layout, the ISO734x incorporate many chip-level design improvements for overall system robustness. Some of these improvements include:

- Robust ESD protection cells for input and output signal pins and inter-chip bond pads.
- Low-resistance connectivity of ESD cells to supply and ground pins.
- Enhanced performance of high voltage isolation capacitor for better tolerance of ESD, EFT and surge events.
- Bigger on-chip decoupling capacitors to bypass undesirable high energy signals through a low impedance path.
- PMOS and NMOS devices isolated from each other by using guard rings to avoid triggering of parasitic SCRs.
- Reduced common mode currents across the isolation barrier by ensuring purely differential internal operation.

9.2.1.3 Application Performance Curves

Typical eye diagrams of ISO734x indicate low jitter and wide open eye at the maximum data rate of 25 Mbps.

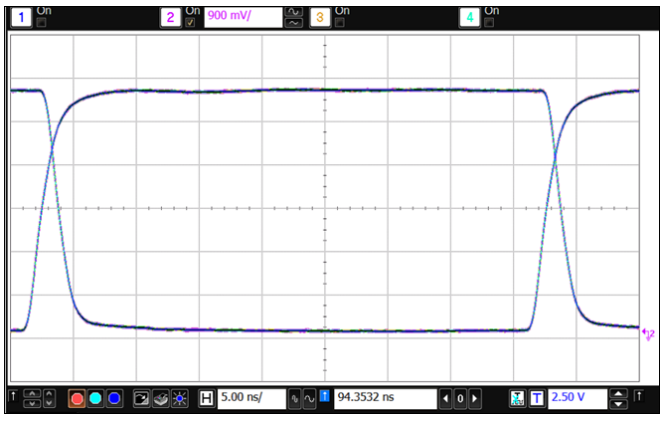


Figure 24. Eye Diagram at 25 Mbps, 5 V and 25°C

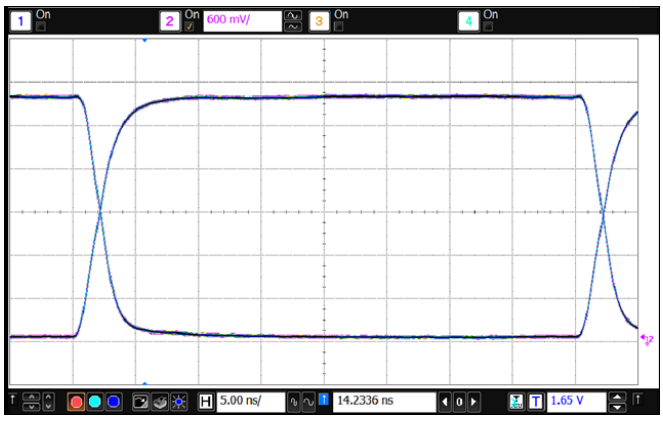


Figure 25. Eye Diagram at 25 Mbps, 3.3 V and 25°C

Typical Application (continued)

9.2.2 Typical Application for Module with 16 Inputs

ISO7341 and several other components from Texas Instruments can be used to create an isolated SPI interface for input module with 16 inputs.

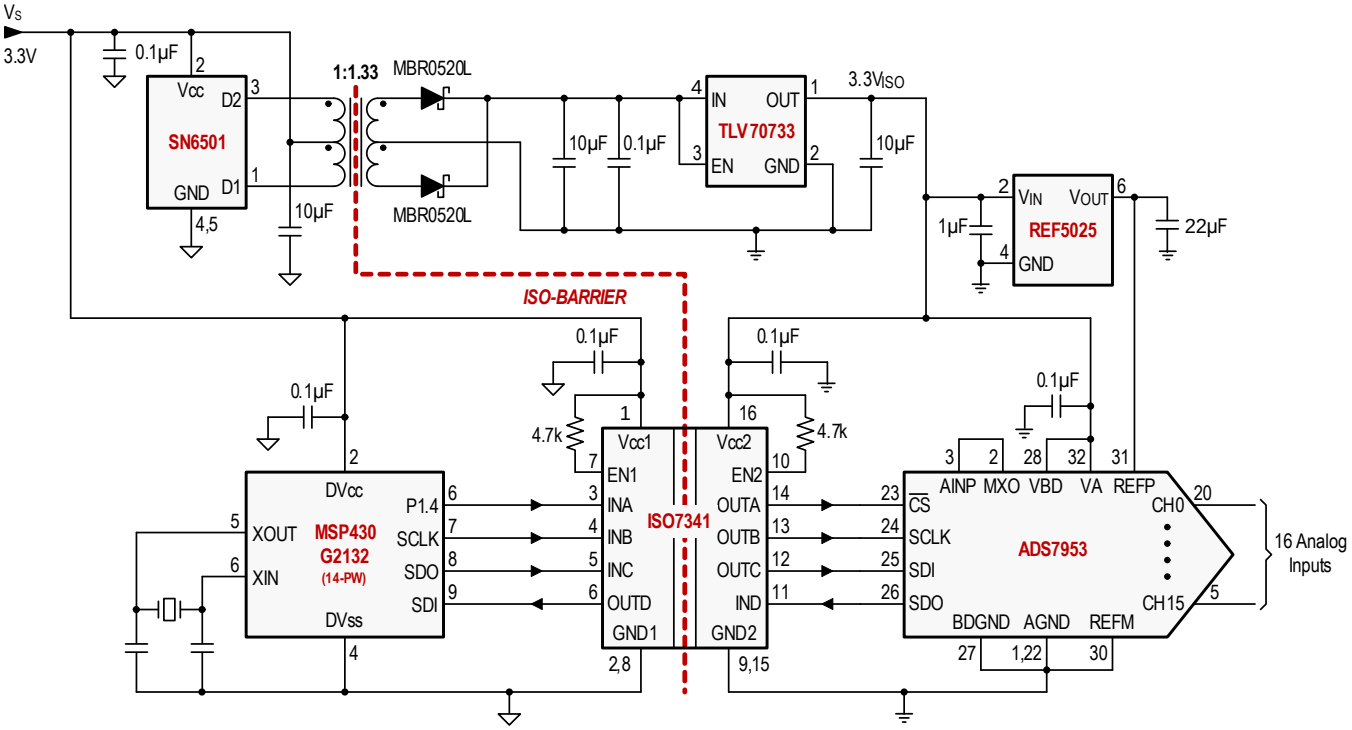


Figure 26. Isolated SPI Interface for an Analog Input Module With 16 Inputs

9.2.2.1 Design Requirements

Refer to *Isolated Data Acquisition System for Process Control* for the design requirements.

9.2.2.2 Detailed Design Procedure

Refer to *Isolated Data Acquisition System for Process Control* for the detailed design procedures.

9.2.2.3 Application Performance Curves

Refer to *Isolated Data Acquisition System for Process Control* for the application performance curves.

Typical Application (continued)

9.2.3 Typical Application for RS-232 Interface

Typical isolated RS-232 interface implementation is shown in Figure 27.

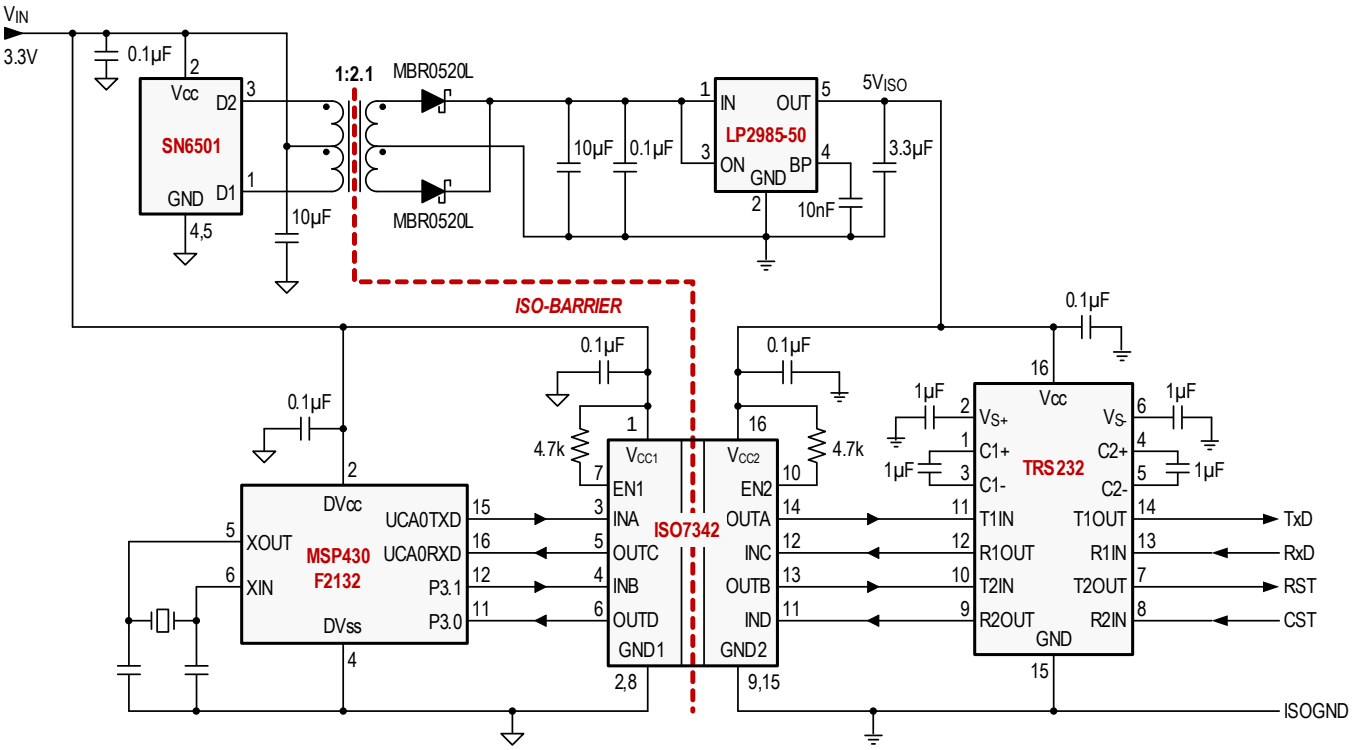


Figure 27. Isolated RS-232 Interface

9.2.3.1 Design Requirements

Refer to *Isolated Data Acquisition System for Process Control* for the design requirements.

9.2.3.2 Detailed Design Procedure

Refer to *Isolated Data Acquisition System for Process Control* for the detailed design procedures.

9.2.3.3 Application Performance Curves

Refer to *Isolated Data Acquisition System for Process Control* for the application performance curves.

10 Power Supply Recommendations

To ensure reliable operation at all data rates and supply voltages, a 0.1 µF bypass capacitor is recommended at input and output supply pins (V_{CC1} and V_{CC2}). The capacitors should be placed as close to the supply pins as possible. If only a single primary-side power supply is available in an application, isolated power can be generated for the secondary-side with the help of a transformer driver such as Texas Instruments' SN6501. For such applications, detailed power supply design and transformer selection recommendations are available in SN6501 datasheet (SLLSEA0) .

11 Layout

11.1 PCB Material

For digital circuit boards operating below 150 Mbps, (or rise and fall times higher than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 epoxy-glass as PCB material. FR-4 (Flame Retardant 4) meets the requirements of Underwriters Laboratories UL94-V0, and is preferred over cheaper alternatives due to its lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and its self-extinguishing flammability-characteristics.

11.2 Layout Guidelines

A minimum of four layers is required to accomplish a low EMI PCB design (see Figure 28). Layer stacking should be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100pF/in^2.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.

If an additional supply voltage plane or signal layer is needed, add a second power / ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

For detailed layout recommendations, see Application Note SLLA284, *Digital Isolator Design Guide*.

11.3 Layout Example

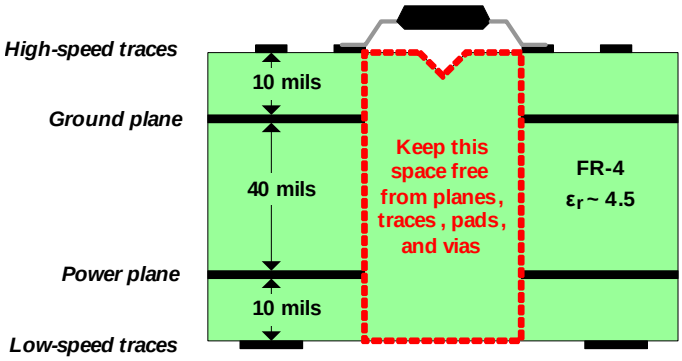


Figure 28. Recommended Layer Stack

12 Device and Documentation Support

12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 3. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
ISO7340C	Click here	Click here	Click here	Click here	Click here
ISO7340FC	Click here	Click here	Click here	Click here	Click here
ISO7341C	Click here	Click here	Click here	Click here	Click here
ISO7341FC	Click here	Click here	Click here	Click here	Click here
ISO7342C	Click here	Click here	Click here	Click here	Click here
ISO7342FC	Click here	Click here	Click here	Click here	Click here

12.2 Trademarks

All trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

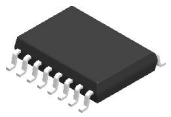
SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

Isolation Glossary, SLLS353

13 Mechanical, Packaging, and Orderable Information

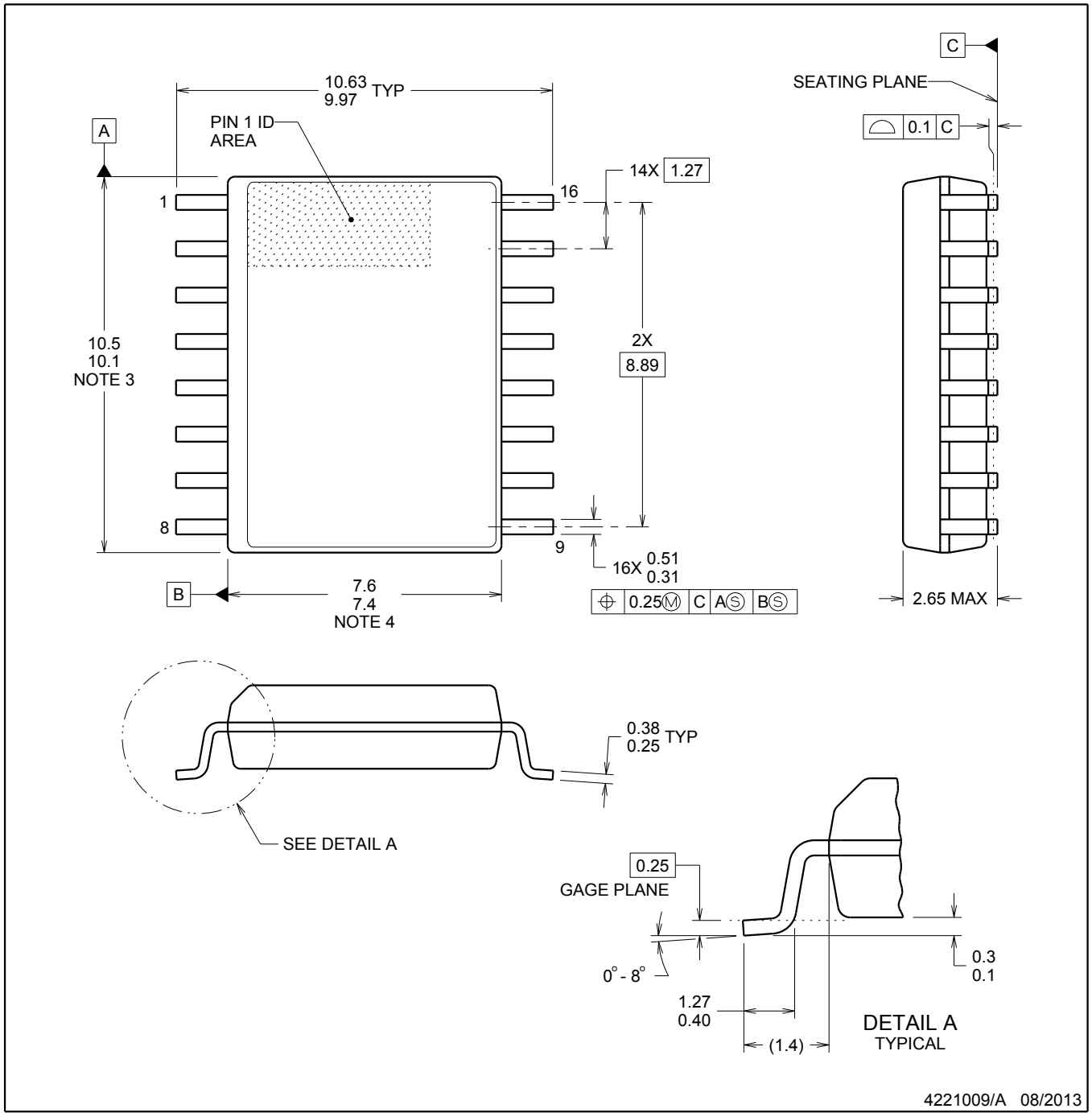
The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.



DW0016B

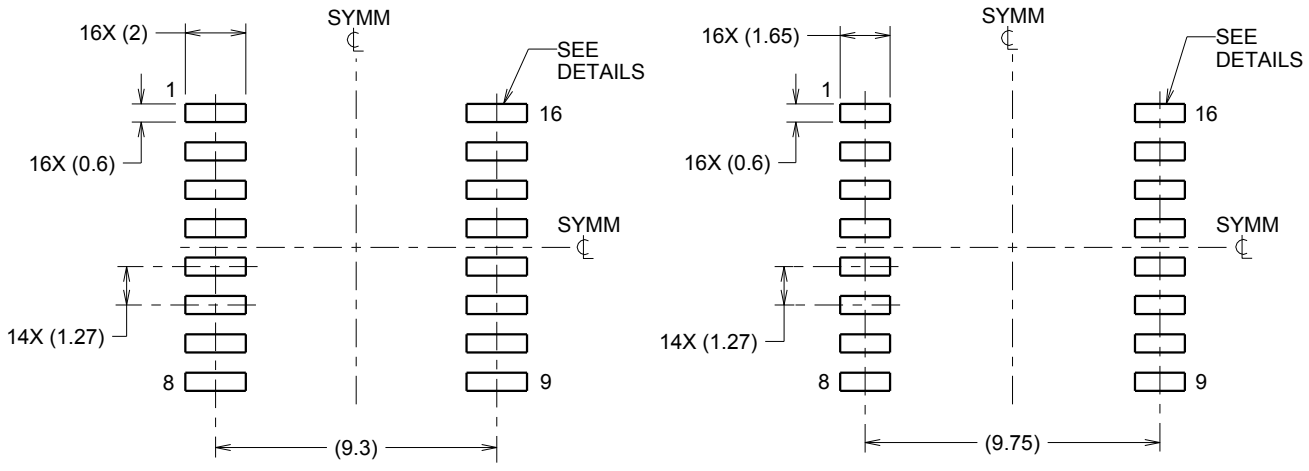
SOIC - 2.65 mm max height

SOIC



NOTES:

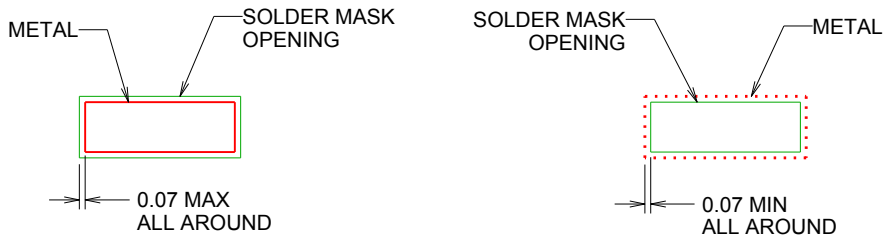
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MO-013, variation AA.



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

LAND PATTERN EXAMPLE
SCALE:4X



NON SOLDER MASK DEFINED

SOLDER MASK DEFINED

SOLDER MASK DETAILS

4221009/A 08/2013

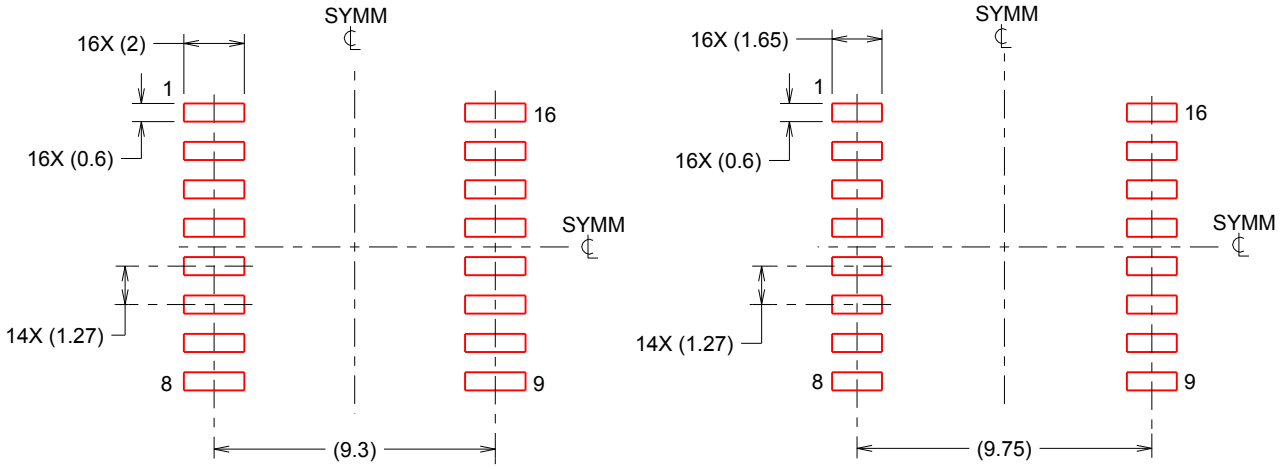
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

DW0016B

SOIC - 2.65 mm max height

SOIC



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

4221009/A 08/2013

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ISO7340CDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7340C	Samples
ISO7340CDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7340C	Samples
ISO7340FCDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7340FC	Samples
ISO7340FCDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7340FC	Samples
ISO7341CDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7341C	Samples
ISO7341CDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7341C	Samples
ISO7341FCDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7341FC	Samples
ISO7341FCDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7341FC	Samples
ISO7342CDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7342C	Samples
ISO7342CDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7342C	Samples
ISO7342FCDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7342FC	Samples
ISO7342FCDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7342FC	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

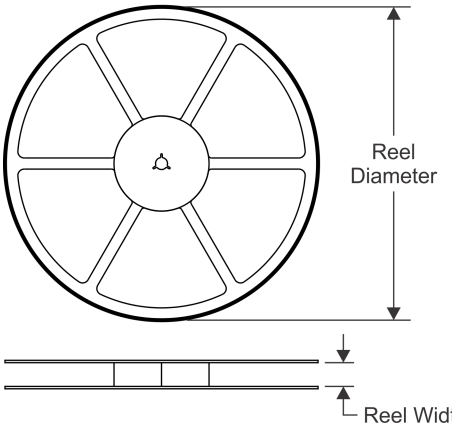
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

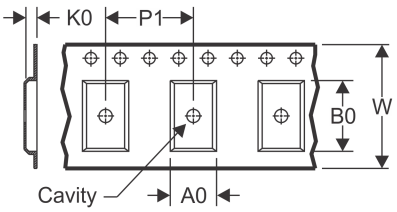
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

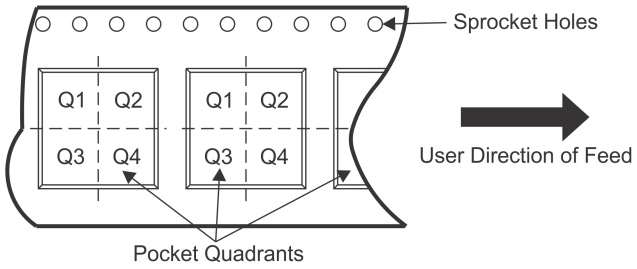


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

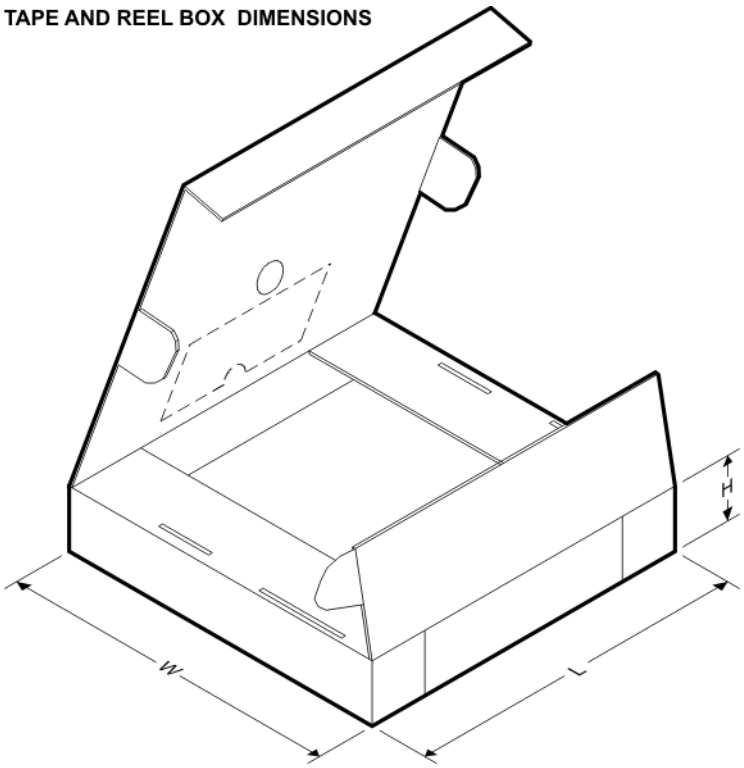
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO7340CDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7340FCDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7341CDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7341FCDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7342CDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7342FCDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO7340CDWR	SOIC	DW	16	2000	367.0	367.0	38.0
ISO7340FCDWR	SOIC	DW	16	2000	367.0	367.0	38.0
ISO7341CDWR	SOIC	DW	16	2000	367.0	367.0	38.0
ISO7341FCDWR	SOIC	DW	16	2000	367.0	367.0	38.0
ISO7342CDWR	SOIC	DW	16	2000	367.0	367.0	38.0
ISO7342FCDWR	SOIC	DW	16	2000	367.0	367.0	38.0

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