LM3704/LM3705 Microprocessor Supervisory Circuits with Power Fail Input, Low Line Output and Manual Reset

Check for Samples: LM3704, LM3705

FEATURES

- **Standard Reset Threshold Voltage: 3.08V**
- **Custom Reset Threshold Voltages: For Other Voltages Between 2.2V and 5.0V in 10mV Increments, Contact Texas Instruments.**
- **No External Components Required**
- **Manual-Reset Input**
- **$\overline{\text{RESET}}$ (LM3704) or RESET (LM3705) Outputs**
- **Precision Supply Voltage Monitor**
- **Factory Programmable Reset Timeout Delay**
- **Separate Power Fail Comparator**
- **Available in DSBGA Package for Minimum Footprint**
- **±0.5% Reset Threshold Accuracy at Room Temperature**
- **±2% Reset Threshold Accuracy Over Temperature Extremes**
- **Reset Assertion Down to 1V V_{CC} ($\overline{\text{RESET}}$ Option Only)**
- **28 µA V_{CC} Supply Current**

APPLICATIONS

- **Embedded Controllers and Processors**
- **Intelligent Instruments**
- **Automotive Systems**
- **Critical µP Power Monitoring**

DESCRIPTION

The LM3704/LM3705 series of microprocessor supervisory circuits provide the maximum flexibility for monitoring power supplies and battery controlled functions in systems without backup batteries. The LM3704/LM3705 series are available in VSSOP-10 and 9-bump DSBGA packages.

Built-in features include the following:

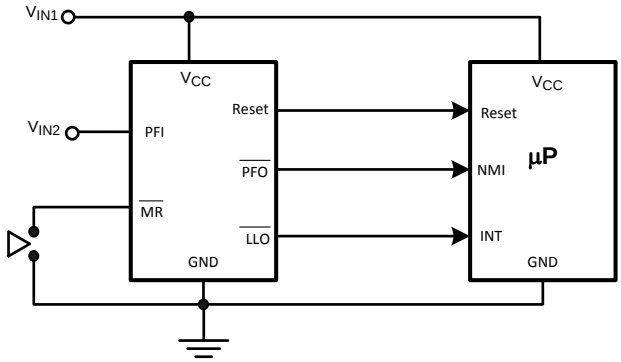
Reset: Reset is asserted during power-up, power-down, and brownout conditions. $\overline{\text{RESET}}$ is ensured down to V_{CC} of 1.0V.

Manual Reset Input: An input that asserts reset when pulled low.

Power-Fail Input: A 1.225V threshold detector for power fail warning, or to monitor a power supply other than V_{CC}.

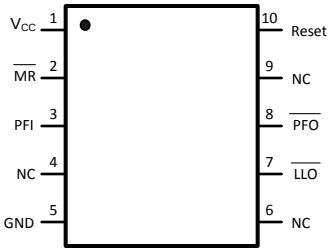
Low Line Output: This early power failure warning indicator goes low when the supply voltage drops to a value which is 2% higher than the reset threshold voltage.

Typical Application

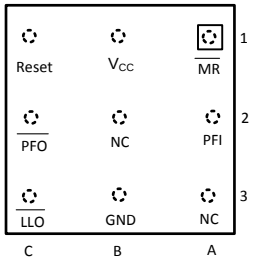


Connection Diagram

VSSOP-10



DSBGA 9 Bump Package
Top View
(looking from the coating side)



PIN DESCRIPTION

Pin No.		Name	Function
DSBGA	VSSOP		
A1	2	$\overline{MR}$	Manual-Reset input. When $\overline{MR}$ is less than V_{MRT} (Manual Reset Threshold) $\overline{RESET}$/RESET is engaged.
B1	1	V_{CC}	Power Supply input.
C1	10	$\overline{RESET}$	Reset Logic Output. Pulses low for t_{RP} (Reset Timeout Period) when triggered, and stays low whenever V_{CC} is below the reset threshold or when $\overline{MR}$ is below V_{MRT}. It remains low for t_{RP} after either V_{CC} rises above the reset threshold, or after $\overline{MR}$ input rises above V_{MRT} (LM3704 only).
		RESET	Reset Logic Output. RESET is the inverse of $\overline{RESET}$ (LM3705 only).
C2	8	$\overline{PFO}$	Power-Fail Logic Output. When PFI is below V_{PFT}, $\overline{PFO}$ goes low; otherwise, $\overline{PFO}$ remains high.
C3	7	$\overline{LLO}$	Low-Line Logic Output. Early Power-Fail warning output. Low when V_{CC} falls below V_{LLOT} (Low-Line Output Threshold). This output can be used to generate an NMI (Non-Maskable Interrupt) to provide an early warning of imminent power-failure.
B3	5	GND	Ground reference for all signals.
A3	4, 6	NC	No Connect.
A2	3	PFI	Power-Fail Comparator Input. When PFI is less than V_{PFT} (Power-Fail Reset Threshold), the $\overline{PFO}$ goes low; otherwise, $\overline{PFO}$ remains high.
B2	9	NC	No Connect. Test input used at factory only. Leave floating.

Block Diagram

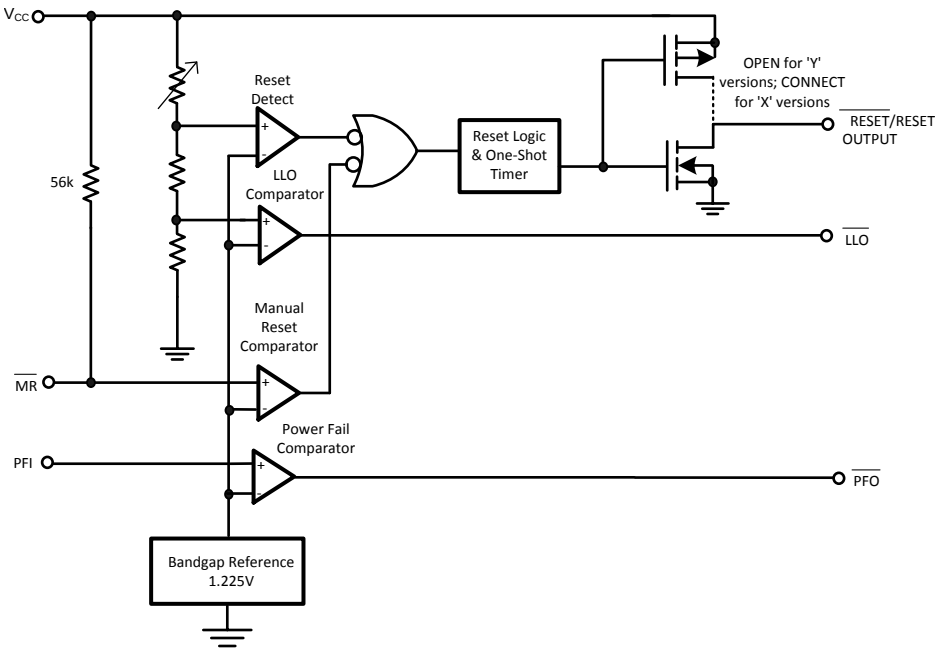


Figure 1. Block Diagram

Table 1. Table of Functions

Part Number	Active Low Reset	Active High Reset	Output (X = totem-pole) (Y = open-drain)	Reset Timeout Period	Manual Reset	Power Fail Comparator	Low Line Output
LM3704	x		X, Y*(1)	Customized	x	x	x
LM3705		x	X	Customized	x	x	x

(1) * = available upon request. Contact TI

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[1][2]

Supply Voltage (V_{CC})		−0.3V to 6.0V
All Other Inputs		−0.3V to V_{CC} + 0.3V
ESD Ratings[3]	Human Body Model	1.5kV
	Machine Model	150V
Power Dissipation		See[4]

(1) **Absolute Maximum Ratings** indicate limits beyond which damage to the device may occur. **Operating Ratings** indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed conditions.

(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

(3) The Human Body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. The machine model is a 200pF capacitor discharged directly into each pin.

(4) The maximum allowable power dissipation is a function of the maximum junction temperature, $T_J(MAX)$, the junction-to-ambient thermal resistance, θ_{J-A}, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperture is calculated using:

$$P(MAX) = \frac{T_J(MAX) - T_A}{\theta_{J-A}}$$

Where the value of θ_{J-A} for the VSSOP-10 package is 195°C/W in a typical PC board mounting and the DSBGA package is 220°C/W.

Operating Ratings[1]

Temperature Range	−40°C ≤ T_J ≤ 85°C

(1) **Absolute Maximum Ratings** indicate limits beyond which damage to the device may occur. **Operating Ratings** indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed conditions.

LM3704/LM3705 Series Electrical Characteristics

Limits in the standard typeface are for T_J = 25°C and limits in **boldface type** apply over full operating range. Unless otherwise specified: V_{CC} = +2.2V to 5.5V.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
POWER SUPPLY						
V_{CC}	Operating Voltage Range: V_{CC}	LM3704	**1.0**		**5.5**	V
		LM3705	**1.2**		**5.5**	
I_{CC}	V_{CC} Supply Current	All inputs = V_{CC}; all outputs floating		28	**50**	µA
RESET THRESHOLD						
V_{RST}	Reset Threshold	V_{CC} falling	−0.5 **−2**	V_{RST}	+0.5 **+2**	%
		V_{CC} falling: T_A = 0°C to 70°C	**−1.5**		**+1.5**	
V_{RSTH}	Reset Threshold Hysteresis			0.0032•V_{RST}		mV
t_{RP}	Reset Timeout Period	Reset Timeout Period = A Reset Timeout Period = B Reset Timeout Period = C Reset Timeout Period = D	**1** **20** **140** **1120**	1.4 28 200 1600	**2** **40** **280** **2240**	ms
t_{RD}	V_{CC} to Reset Delay	V_{CC} falling at 1mV/µs		20		µs
RESET (LM3705)						
V_{OL}	RESET	V_{CC} > 2.25V, I_{SINK} = 900µA			**0.3**	V
		V_{CC} > 2.7V, I_{SINK} = 1.2mA			**0.3**	
		V_{CC} > 4.5V, I_{SINK} = 3.2mA			**0.4**	
V_{OH}	RESET	V_{CC} > 1.2V, I_{SOURCE} = 50µA	**0.8 V_{CC}**			V
		V_{CC} > 1.8V, I_{SOURCE} = 150µA	**0.8 V_{CC}**			
		V_{CC} > 2.25V, I_{SOURCE} = 300µA	**0.8 V_{CC}**			
		V_{CC} > 2.7V, I_{SOURCE} = 500µA	**0.8 V_{CC}**			
		V_{CC} > 4.5V, I_{SOURCE} = 800µA	**V_{CC} − 1.5V**			

LM3704/LM3705 Series Electrical Characteristics (continued)

Limits in the standard typeface are for T_J = 25°C and limits in **boldface type** apply over full operating range. Unless otherwise specified: V_{CC} = +2.2V to 5.5V.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LKG}	Output Leakage Current	V_{RESET} = 5.5V			**1.0**	µA
$\overline{\text{RESET}}$ (LM3704)						
V_{OL}	$\overline{\text{RESET}}$	V_{CC} > 1.0V, I_{SINK} = 50µA			**0.3**	V
		V_{CC} > 1.2V, I_{SINK} = 100µA			**0.3**	
		V_{CC} > 2.25V, I_{SINK} = 900µA			**0.3**	
		V_{CC} > 2.7V, I_{SINK} = 1.2mA			**0.3**	
		V_{CC} > 4.5V, I_{SINK} = 3.2mA			**0.4**	
V_{OH}	$\overline{\text{RESET}}$	V_{CC} > 2.25V, I_{SOURCE} = 300µA	**0.8 V_{CC}**			
		V_{CC} > 2.7V, I_{SOURCE} = 500µA	**0.8 V_{CC}**			
		V_{CC} > 4.5V, I_{SOURCE} = 800µA	**V_{CC} − 1.5V**			
PFI/$\overline{\text{MR}}$						
V_{PFT}	PFI Input Threshold		**1.200**	1.225	**1.250**	V
V_{MRT}	$\overline{\text{MR}}$ Input Threshold	$\overline{\text{MR}}$, Low			**0.8**	V
		$\overline{\text{MR}}$, High	**2.0**			
V_{PFTH}/ V_{MRTH}	PFI/$\overline{\text{MR}}$ Threshold Hysteresis	PFI/$\overline{\text{MR}}$ falling: V_{CC} = $V_{RST\ MAX}$ to 5.5V		0.0032•V_{RST}		mV
I_{PFI}	Input Current (PFI only)		**−75**		**75**	nA
R_{MR}	$\overline{\text{MR}}$ Pull-up Resistance		**35**	56	**75**	kΩ
t_{MD}	$\overline{\text{MR}}$ to Reset Delay			12		µS
t_{MR}	$\overline{\text{MR}}$ Pulse Width		**25**			µS
$\overline{\text{PFO}}$, $\overline{\text{LLO}}$						
V_{OL}	$\overline{\text{PFO}}$, $\overline{\text{LLO}}$ Output Voltage	V_{CC} > 2.25V, I_{SINK} = 900µA			**0.3**	V
		V_{CC} > 2.7V, I_{SINK} = 1.2mA			**0.3**	
		V_{CC} > 4.5V, I_{SINK} = 3.2mA			**0.4**	
V_{OH}		V_{CC} > 2.25V, I_{SOURCE} = 300µA	**0.8 V_{CC}**			
		V_{CC} > 2.7V, I_{SOURCE} = 500µA	**0.8 V_{CC}**			
		V_{CC} > 4.5V, I_{SOURCE} = 800µA	**V_{CC} − 1.5V**			
$\overline{\text{LLO}}$ OUTPUT						
V_{LLOT}	$\overline{\text{LLO}}$ Output Threshold ($V_{\overline{LLO}}$ − V_{RST}, V_{CC} falling)		**1.01•V_{RST}**	1.02•V_{RST}	**1.03•V_{RST}**	V
V_{LLOTH}	Low-Line Comparator Hysteresis			0.0032•V_{RST}		mV
t_{CD}	Low-Line Comparator Delay	V_{CC} falling at 1mV/µs		20		µs

Typical Performance Characteristics

Supply Current vs Supply Voltage

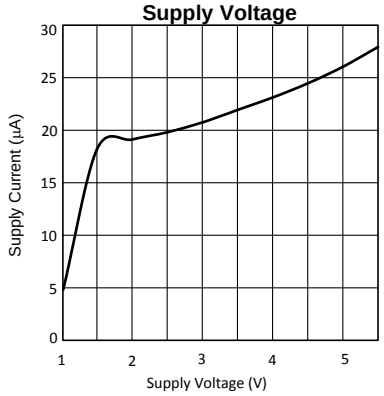


Figure 2.

3.3V Supply Current vs Temperature

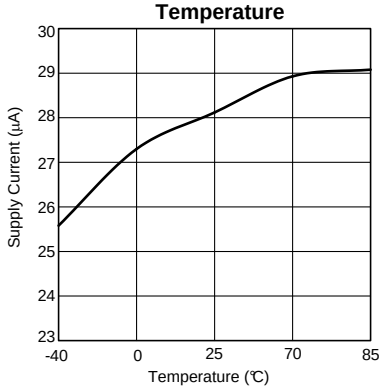


Figure 3.

Normalized Reset Threshold Voltage vs Temperature

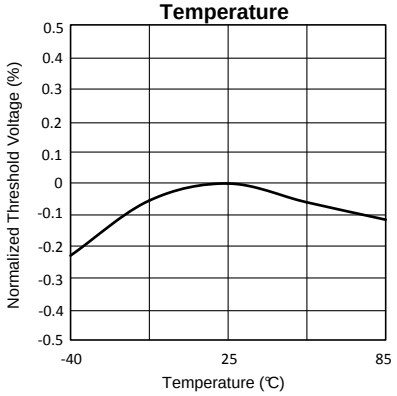


Figure 4.

Reset Timeout Period vs V_{CC}

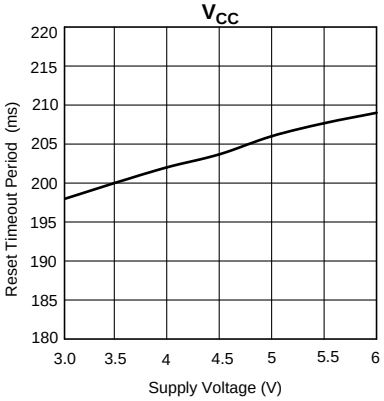


Figure 5.

Reset Timeout Period vs Temperature

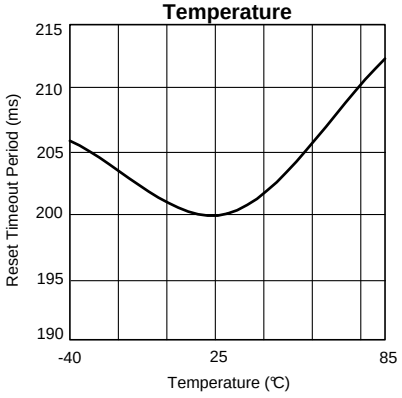


Figure 6.

Max. Transient Duration vs Reset Comparator Overdrive (V_{CC} = 3.3V)

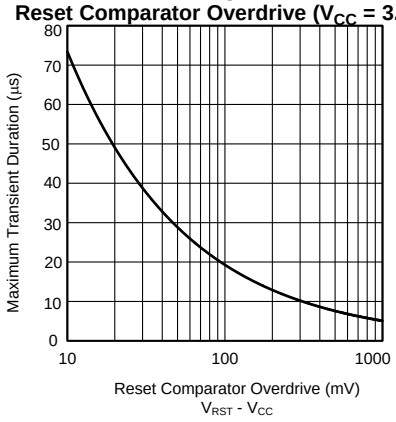


Figure 7.

Typical Performance Characteristics (continued)

Low-Line Comparator Propagation Delay vs Temperature

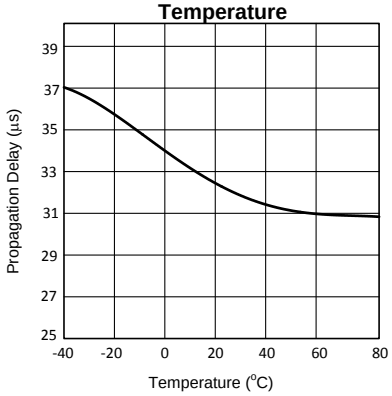


Figure 8.

CIRCUIT INFORMATION

RESET OUTPUT

The Reset input of a µP initializes the device into a known state. The LM3704/LM3705 microprocessor supervisory circuits assert a forced reset output to prevent code execution errors during power-up, power-down, and brownout conditions.

$\overline{\text{RESET}}$ is ensured valid for V_{CC} > 1V. Once V_{CC} exceeds the reset threshold, an internal timer maintains the output for the reset timeout period. After this interval, reset goes high. The LM3704 offers an active-low $\overline{\text{RESET}}$; The LM3705 offers an active-high RESET.

Any time V_{CC} drops below the reset threshold (such as during a brownout), the reset activates. When V_{CC} again rises above the reset threshold, the internal timer starts. Reset holds until V_{CC} exceeds the reset threshold for longer than the reset timeout period. After this time, reset releases.

The Manual Reset input ($\overline{\text{MR}}$) will initiate a forced reset also. See the MANUAL RESET INPUT ($\overline{\text{MR}}$) section.

RESET THRESHOLD

The LM3704/LM3705 family is available with a reset voltage of 3.08V. Other reset thresholds in the 2.20V to 5.0V range, in steps of 10 mV, are available; contact Texas Instruments for details.

MANUAL RESET INPUT ($\overline{\text{MR}}$)

Many µP-based products require a manual reset capability, allowing the operator to initiate a reset. The $\overline{\text{MR}}$ input is fully debounced and provides an internal 56 kΩ pull-up. When the $\overline{\text{MR}}$ input is pulled below V_{MRT} (1.225V) for more than 25 µs, reset is asserted after a typical delay of 12 µs. Reset remains active as long as $\overline{\text{MR}}$ is held low, and releases after the reset timeout period expires after $\overline{\text{MR}}$ rises above V_{MRT}. Use $\overline{\text{MR}}$ with digital logic to assert or to daisy chain supervisory circuits. It may be used as another low-line comparator by adding a buffer.

POWER-FAIL COMPARATOR (PFI/$\overline{\text{PFO}}$)

The PFI is compared to a 1.225V internal reference, V_{PFT}. If PFI is less than V_{PFT}, the Power Fail Output $\overline{\text{PFO}}$ drops low. The power-fail comparator signals a falling power supply, and is driven typically by an external voltage divider that senses either the unregulated supply or another system supply voltage. The voltage divider generally is chosen so the voltage at PFI drops below V_{PFT} several milliseconds before the main supply voltage drops below the reset threshold, providing advanced warning of a brownout.

The voltage threshold is set by R_1 and R_2 and is calculated as follows:

$$V_{PFT} = \left(\frac{R1 + R2}{R2}\right) \times 1.225V$$

Note this comparator is completely separate from the rest of the circuitry, and may be employed for other functions as needed.

LOW-LINE OUTPUT ($\overline{\text{LLO}}$)

The low-line output comparator is typically used to provide a non-maskable interrupt to a µP when V_{CC} begins falling. $\overline{\text{LLO}}$ monitors V_{CC} and goes low when V_{CC} falls below V_{LLOT} (typically 1.02 • V_{RST}) with hysteresis of 0.0032 • V_{RST}.

SPECIAL PRECAUTIONS FOR THE DSBGA PACKAGE

As with most integrated circuits, the LM3704 and LM3705 are sensitive to exposure from visible and infrared (IR) light radiation. Unlike a plastic encapsulated IC, the DSBGA package has very limited shielding from light, and some sensitivity to light reflected from the surface of the PC board or long wavelength IR entering the die from the side may be experienced. This light could have an unpredictable affect on the electrical performance of the IC. Care should be taken to shield the device from direct exposure to bright visible or IR light during operation.

DSBGA MOUNTING

The DSBGA package requires specific mounting techniques which are detailed in Texas Instruments Application Note AN-1112 (SNVA009). Referring to the section ***Surface Mount Technology (SMT) Assembly Considerations***, it should be noted that the pad style which must be used with the 9-pin package is the NSMD (non-solder mask defined) type.

For best results during assembly, alignment ordinals on the PC board may be used to facilitate placement of the DSBGA device.

TEST CIRCUIT DIAGRAMS

Timing Diagrams

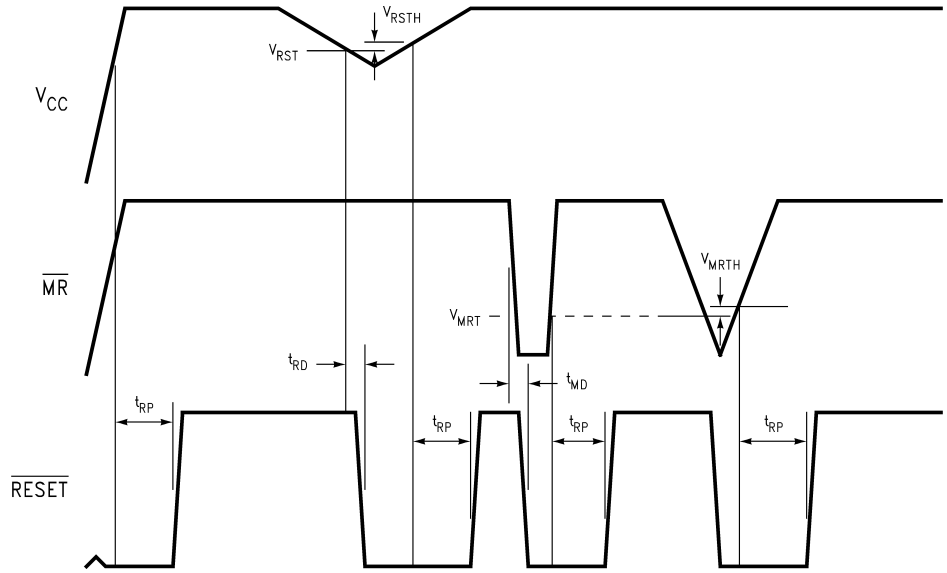


Figure 9. LM3704 Reset Time with $\overline{MR}$

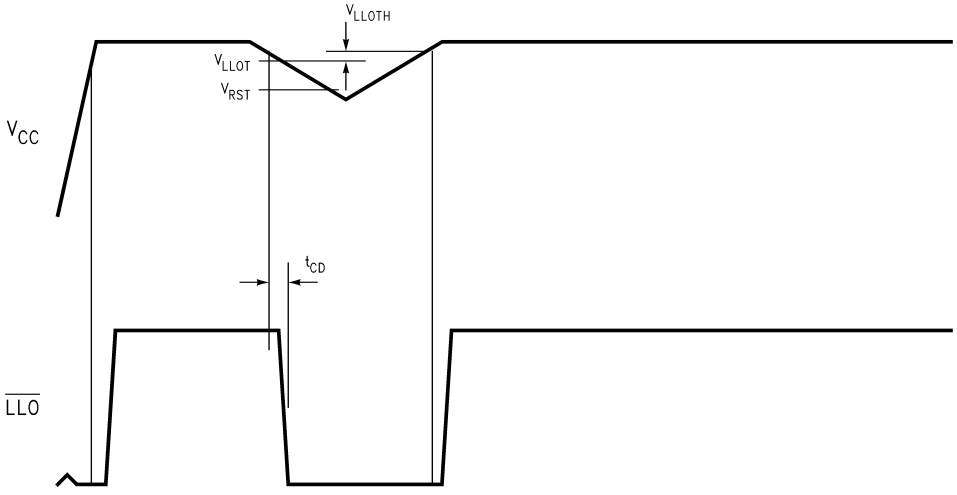


Figure 10. $\overline{LLO}$ Output

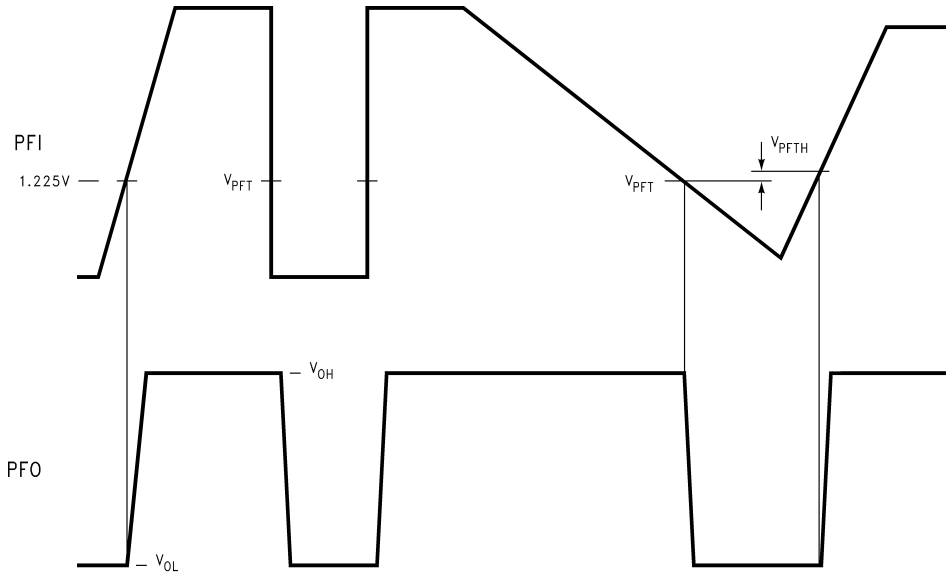
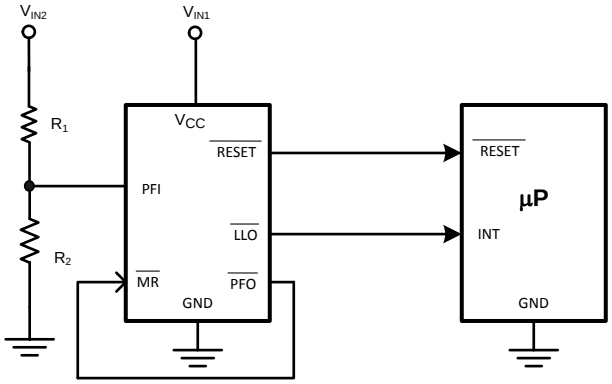


Figure 11. PFI Comparator Timing Diagram

Typical Application Circuits



Power-Fail Reset Threshold, $V_{PFT} = 1.225 \cdot \left(\frac{R_1}{R_2} + 1\right)$

Figure 12. Monitoring Two Critical Supplies

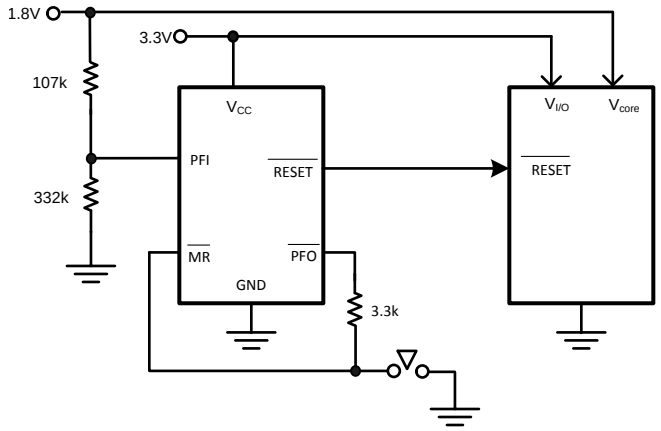


Figure 13. Monitoring Two Supplies plus Manual Reset

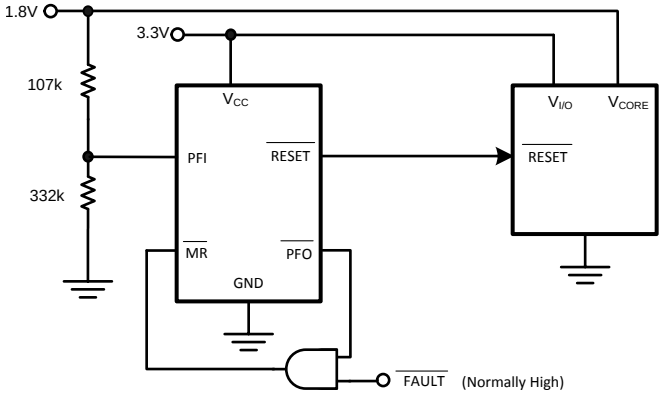
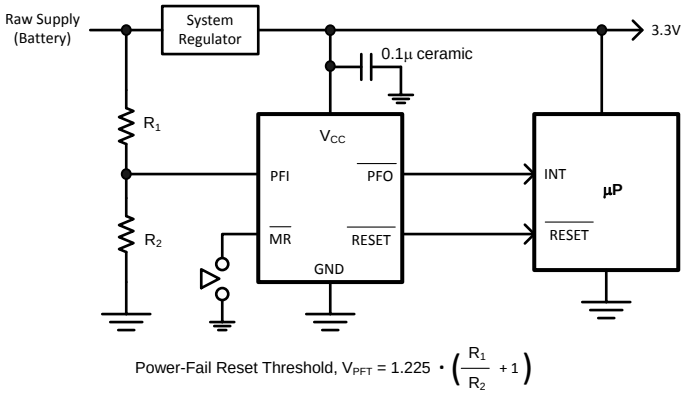


Figure 14. Monitoring Dual Supplies plus External Fault Input



$\overline{MR}$ input with its 1.225V nominal threshold, may monitor an additional supply voltage. An internal 56 kΩ pull-up resistor is included on this input.

Figure 15. Microprocessor Supervisor with Early Warning Detector

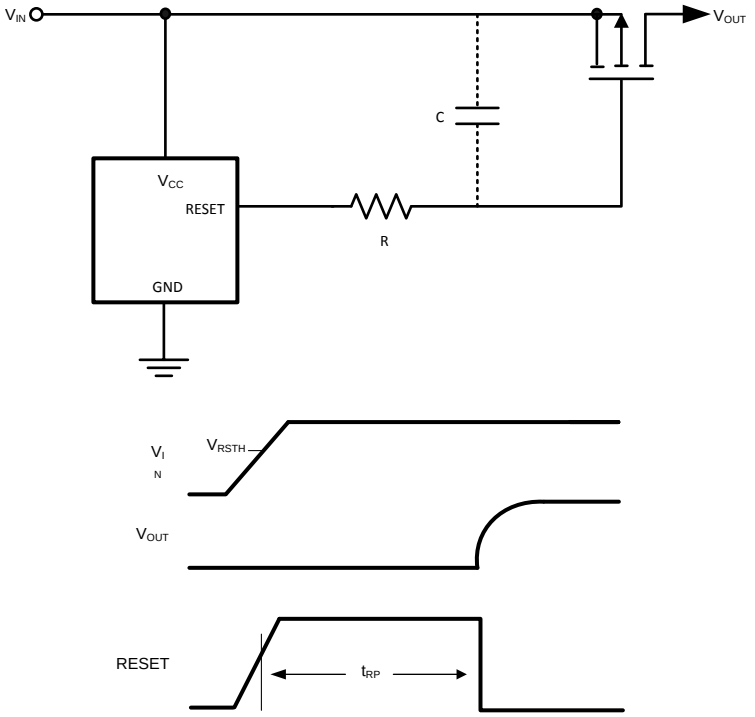


Figure 16. LM3705 Power-On Delay

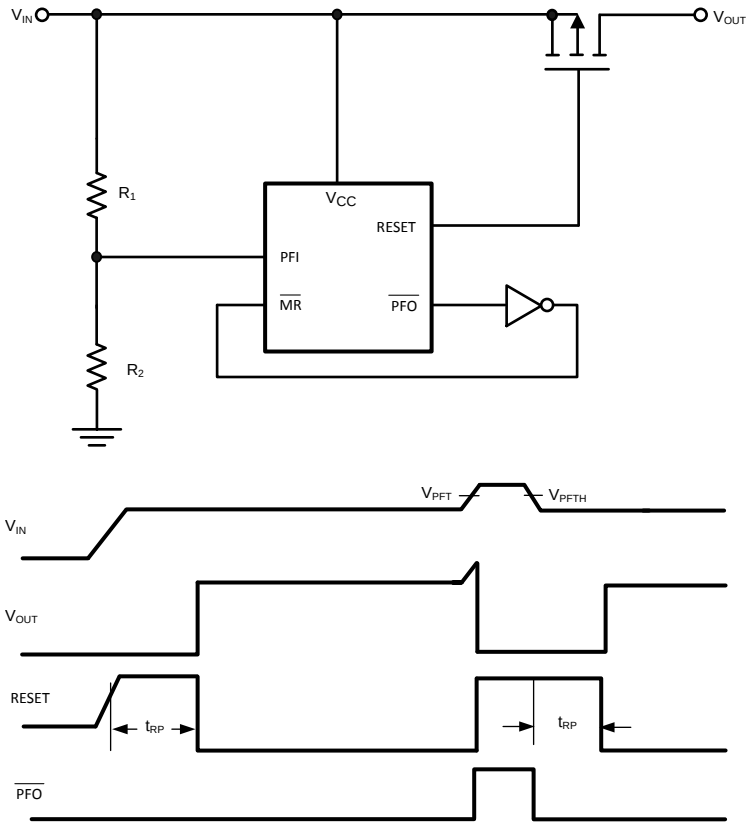


Figure 17. LM3705 Power-On Delay with Overvoltage Protection

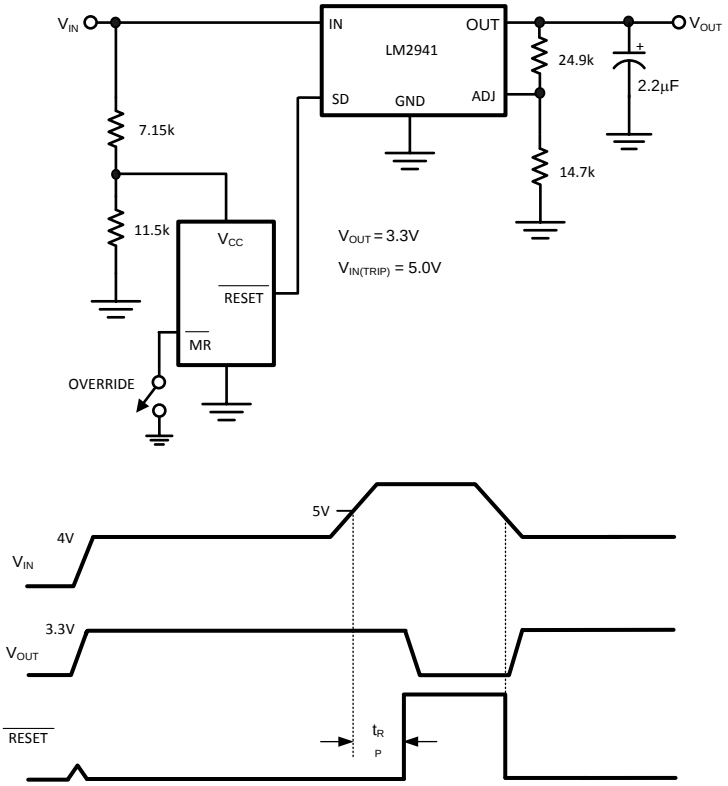


Figure 18. Regulator/Switch with Long-Term Overvoltage Lockout Prevents Overdissipation in Linear Regulator

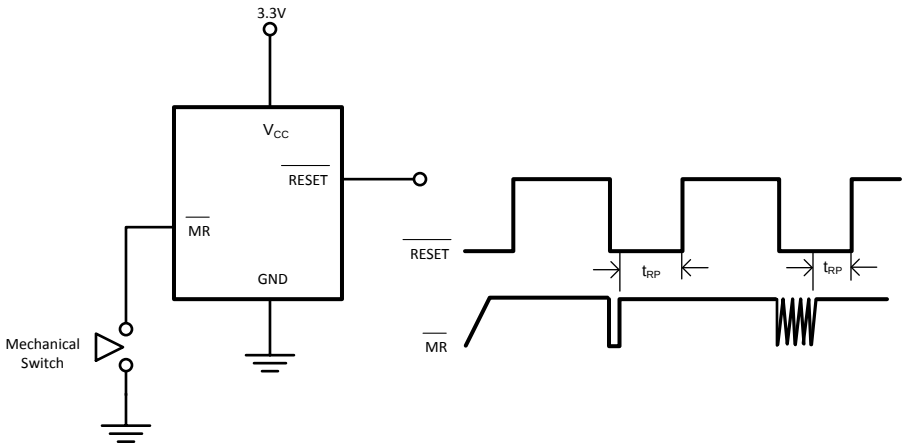


Figure 19. Switch Debouncer

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM3704XCMM-308/NOPB	ACTIVE	VSSOP	DGS	10	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	R35B	Samples
LM3704YCMM-232/NOPB	ACTIVE	VSSOP	DGS	10	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM		R76B	Samples
LM3704YCMM-308/NOPB	ACTIVE	VSSOP	DGS	10	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	R48B	Samples
LM3704YCMMX-308/NOPB	ACTIVE	VSSOP	DGS	10	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	R48B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

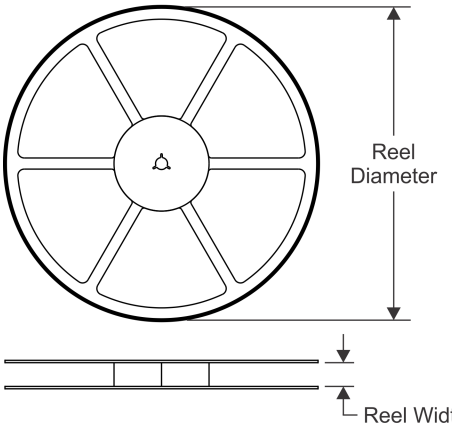
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

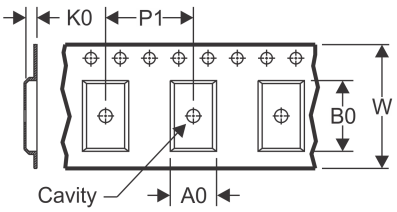
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

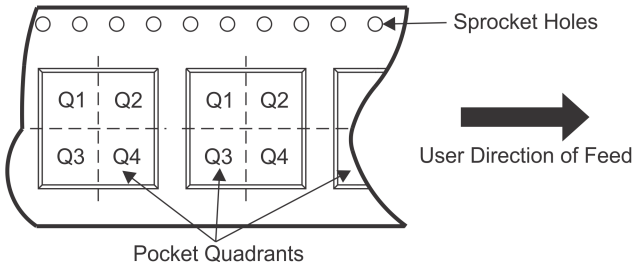


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

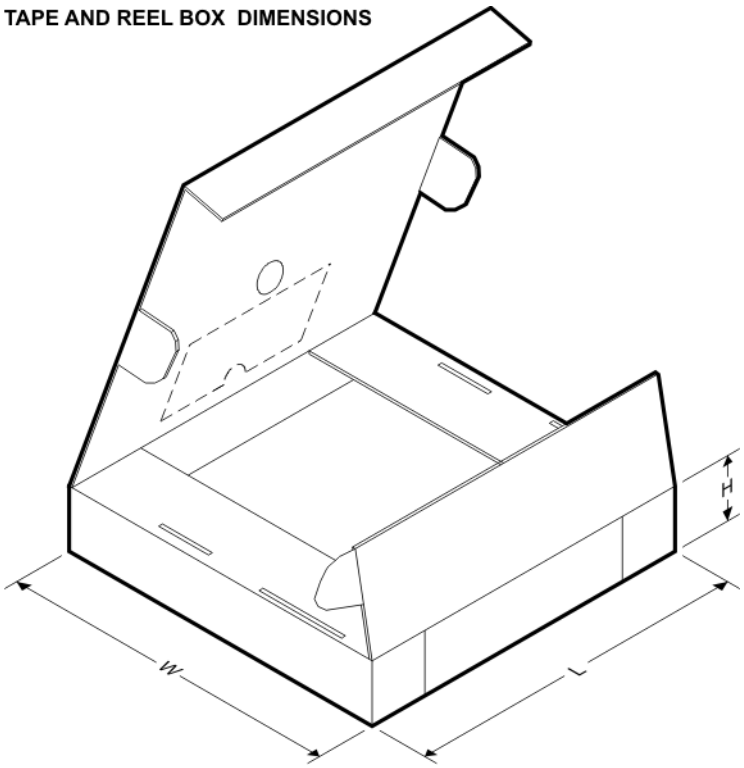
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM3704XCMM-308/NOPB	VSSOP	DGS	10	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM3704YCMM-232/NOPB	VSSOP	DGS	10	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM3704YCMM-308/NOPB	VSSOP	DGS	10	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM3704YCMMX-308/NOPB	VSSOP	DGS	10	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

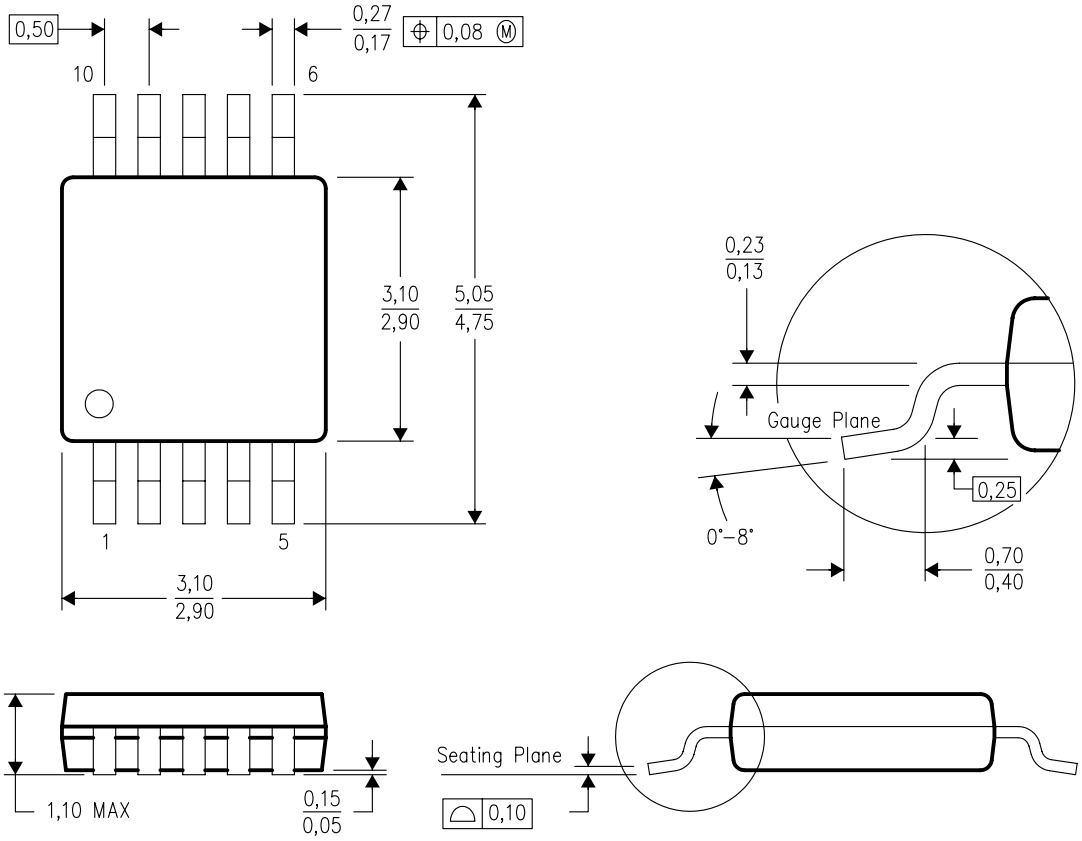
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM3704XCMM-308/NOPB	VSSOP	DGS	10	1000	210.0	185.0	35.0
LM3704YCMM-232/NOPB	VSSOP	DGS	10	1000	210.0	185.0	35.0
LM3704YCMM-308/NOPB	VSSOP	DGS	10	1000	210.0	185.0	35.0
LM3704YCMMX-308/NOPB	VSSOP	DGS	10	3500	367.0	367.0	35.0

DGS (S–PDSO–G10) PLASTIC SMALL–OUTLINE PACKAGE



4073272/C 02/04

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–187 variation BA.

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