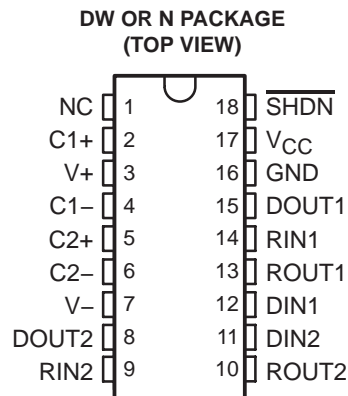


# MAX222

## 5-V DUAL RS-232 LINE DRIVER/RECEIVER WITH $\pm 15$ -kV ESD PROTECTION

SLLS590D – SEPTEMBER 2003 – REVISED AUGUST 2004

- ESD Protection for RS-232 Bus Pins
  - $\pm 15$ -kV Human-Body Model
- Meets or Exceeds the Requirements of TIA/EIA-232-F and ITU v.28 Standards
- Operates at 5-V  $V_{CC}$  Supply
- Operates Up To 200 kbit/s
- Low Supply Current in Shutdown Mode . . . 2  $\mu$ A Typical
- External Capacitors . . .  $4 \times 0.1 \mu$ F
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- Applications
  - Battery-Powered Systems, PDAs, Notebooks, Laptops, Palmtop PCs, and Hand-Held Equipment



### description/ordering information

The MAX222 consists of two line drivers, two line receivers, and a dual charge-pump circuit with  $\pm 15$ -kV ESD protection pin to pin (serial-port connection pins, including GND). This device meets the requirements of TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 5-V supply. This device operates at data signaling rates up to 200 kbit/s and a maximum of 30-V/ $\mu$ s driver output slew rate. By using  $\overline{\text{SHDN}}$ , all receivers can be disabled.

### ORDERING INFORMATION

$T_A$	PACKAGE†	ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP (N)	Tube of 20	MAX222CN
	SOIC (DW)	Tube of 20	MAX222CDW
		Reel of 1000	MAX222CDWR
–40°C to 85°C	PDIP (N)	Tube of 20	MAX222IN
	SOIC (DW)	Tube of 20	MAX222IDW
		Reel of 1000	MAX222IDWR

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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**MAX222**  
**5-V DUAL RS-232 LINE DRIVER/RECEIVER**  
**WITH ±15-kV ESD PROTECTION**

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**Function Tables**

**EACH DRIVER**

INPUT D <sub>IN</sub>	OUTPUT D <sub>OUT</sub>
L	H
H	L

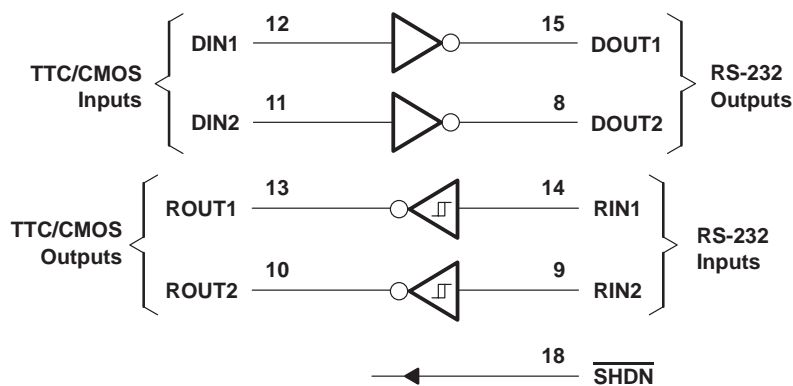
H = high level, L = low level

**EACH RECEIVER**

INPUT R <sub>IN</sub>	OUTPUT R <sub>OUT</sub>
L	H
H	L
Open	H

H = high level, L = low level, Open = input disconnected or connected driver off

**logic diagram (positive logic)**



# MAX222

## 5-V DUAL RS-232 LINE DRIVER/RECEIVER WITH $\pm 15$ -kV ESD PROTECTION

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### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ (see Note 1)	–0.3 V to 6 V
Input voltage range, $V_I$ : Drivers	–0.3 V to $V_{CC} - 0.3$ V
Receivers	±30 V
Output voltage range, $V_O$ : Drivers	±15 V
Receivers	–0.3 V to $V_{CC} + 0.3$ V
Short-circuit duration, $D_{OUT}$	Continuous
Package thermal impedance, $\theta_{JA}$ (see Notes 2 and 3): DW package	TBD°C/W
N package	TBD°C/W
Operating virtual junction temperature, $T_J$	150°C
Storage temperature range, $T_{stg}$	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. All voltages are with respect to network GND.
  2. Maximum power dissipation is a function of  $T_{J(max)}$ ,  $\theta_{JA}$ , and  $T_A$ . The maximum allowable power dissipation at any allowable ambient temperature is  $P_D = (T_{J(max)} - T_A)/\theta_{JA}$ . Operating at the absolute maximum  $T_J$  of 150°C can affect reliability.
  3. The package thermal impedance is calculated in accordance with JESD 51-7.

### recommended operating conditions (see Note 4 and Figure 4)

			MIN	NOM	MAX	UNIT
$V_{CC}$	Supply voltage		4.5	5	5.5	V
$V_{IH}$	Driver high-level input voltage	$D_{IN}$	2			V
	Shutdown high-level input voltage	$\overline{SHDN}$	2			V
$V_{IL}$	Driver low-level input voltage	$D_{IN}$			0.8	V
	Shutdown low-level input voltage	$\overline{SHDN}$			0.8	V
$V_I$	Driver input voltage	$D_{IN}$	0		5.5	V
	Receiver input voltage		–30		30	
$T_A$	Operating free-air temperature	MAX222C	0		70	°C
		MAX222I	–40		85	

NOTE 4: Test conditions are C1–C4 = 0.1  $\mu$ F at  $V_{CC} = 5$  V  $\pm$  0.5 V.

### electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 4)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
$I_{CC}$	Supply current	$V_{CC} = 5$ V	$\overline{SHDN} = V_{CC}$	No load		4	10	mA
				3 k $\Omega$ on both inputs		15		
	Shutdown supply current					2	50	$\mu$ A
$\overline{SHDN}$	Shutdown input leakage current						±1	$\mu$ A

NOTE 4: Test conditions are C1–C4 = 0.1  $\mu$ F at  $V_{CC} = 5$  V  $\pm$  0.5 V.



**MAX222**  
**5-V DUAL RS-232 LINE DRIVER/RECEIVER**  
**WITH ±15-kV ESD PROTECTION**

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**DRIVER SECTION**

**electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 4)**

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V <sub>OH</sub>	High-level output voltage	DOUT at R <sub>L</sub> = 3 kΩ to GND, D <sub>IN</sub> = GND	5	8		V
V <sub>OL</sub>	Low-level output voltage	DOUT at R <sub>L</sub> = 3 kΩ to GND, D <sub>IN</sub> = V <sub>CC</sub>	-5	-8		V
I <sub>IH</sub>	Driver high-level input current	DIN = V <sub>CC</sub>		5	40	μA
	Control high-level input current	SHDN = V <sub>CC</sub>		0.01	1	
I <sub>IL</sub>	Driver low-level input current	DIN = 0 V		-5	-40	μA
	Control low-level input current	SHDN = 0 V		-0.01	-1	
I <sub>OS</sub> ‡	Short-circuit output current	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 0 V	±7	±22		mA
I <sub>off</sub>	Output leakage current	V <sub>CC</sub> = 5.5 V, SHDN = GND, V <sub>O</sub> = ±10 V		±0.01	±10	μA
r <sub>o</sub>	Output resistance	V <sub>CC</sub> , V+, and V- = 0 V, V <sub>O</sub> = ±2 V	300	10 M		Ω

† All typical values are at V<sub>CC</sub> = 5 V, and T<sub>A</sub> = 25°C.

‡ Short-circuit durations should be controlled to prevent exceeding the device absolute power-dissipation ratings, and not more than one output should be shorted at a time.

NOTE 4: Test conditions are C1–C4 = 0.1 μF at V<sub>CC</sub> = 5 V ± 0.5 V.

**switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 4)**

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
	Data rate	C <sub>L</sub> = 1000 pF, R <sub>L</sub> = 3 kΩ, One DOUT switching, See Figure 1	200			kbit/s
t <sub>PLH</sub> (D)	Propagation delay time, low- to high-level output	See Figure 1		1.5	3.5	μs
t <sub>PHL</sub> (D)	Propagation delay time, high- to low-level output	See Figure 1		1.3	3.5	μs
t <sub>PHL</sub> (D) – t <sub>PLH</sub> (D)	Driver (+ to –) propagation delay difference			300		ns
t <sub>sk(p)</sub>	Pulse skew§	C <sub>L</sub> = 150 pF to 2500 pF, R <sub>L</sub> = 3 kΩ to 7 kΩ, See Figure 2		300		ns
SR(tr)	Slew rate, transition region (see Figure 1)	R <sub>L</sub> = 3 kΩ to 7 kΩ, V <sub>CC</sub> = 5 V, C <sub>L</sub> = 50 pF to 2500 pF	6	12	30	V/μs
t <sub>ET</sub>	Driver output enable time (after SHDN goes high)			250		μs
t <sub>DT</sub>	Driver output disable time (after SHDN goes low)			300		ns

† All typical values are at V<sub>CC</sub> = 5 V and T<sub>A</sub> = 25°C.

§ Pulse skew is defined as |t<sub>PLH</sub> – t<sub>PHL</sub>| of each channel of the same device.

NOTE 4: Test conditions are C1–C4 = 0.1 μF at V<sub>CC</sub> = 5 V ± 0.5 V.



**MAX222**  
**5-V DUAL RS-232 LINE DRIVER/RECEIVER**  
**WITH ±15-kV ESD PROTECTION**

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**RECEIVER SECTION**

**electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 4)**

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V <sub>OH</sub>	High-level output voltage	I <sub>OH</sub> = -1 mA	3.5	V <sub>CC</sub> - 0.2 V		V
V <sub>OL</sub>	Low-level output voltage	I <sub>OL</sub> = 3.2 mA			0.4	V
V <sub>IT+</sub>	Positive-going input threshold voltage	V <sub>CC</sub> = 5 V		1.7	2.4	V
V <sub>IT-</sub>	Negative-going input threshold voltage	V <sub>CC</sub> = 5 V	0.8	1.3		V
V <sub>hys</sub>	Input hysteresis (V <sub>IT+</sub> - V <sub>IT-</sub> )		0.2	0.5	1	V
r <sub>i</sub>	Input resistance	V <sub>I</sub> = ±3 V to ±25 V	3	5	7	kΩ

† All typical values are at V<sub>CC</sub> = 5 V, and T<sub>A</sub> = 25°C.

NOTE 4: Test conditions are C1–C4 = 0.1 μF at V<sub>CC</sub> = 5 V ± 0.5 V.

**switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 3)**

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t <sub>PLH</sub> (R)	Propagation delay time, low- to high-level output	C <sub>L</sub> = 150 pF		0.6	1	μs
t <sub>PHL</sub> (R)	Propagation delay time, high- to low-level output	C <sub>L</sub> = 150 pF		0.5	1	μs
t <sub>PHL</sub> (R) - t <sub>PLH</sub> (R)	Receiver (+ to -) propagation delay difference			100		ns
t <sub>sk(p)</sub>	Pulse skew‡			100		ns

† All typical values are at V<sub>CC</sub> = 5 V and T<sub>A</sub> = 25°C.

‡ Pulse skew is defined as |t<sub>PLH</sub> - t<sub>PHL</sub>| of each channel of the same device.

NOTE 4: Test conditions are C1–C4 = 0.1 μF, at V<sub>CC</sub> = 5 V ± 0.5 V.

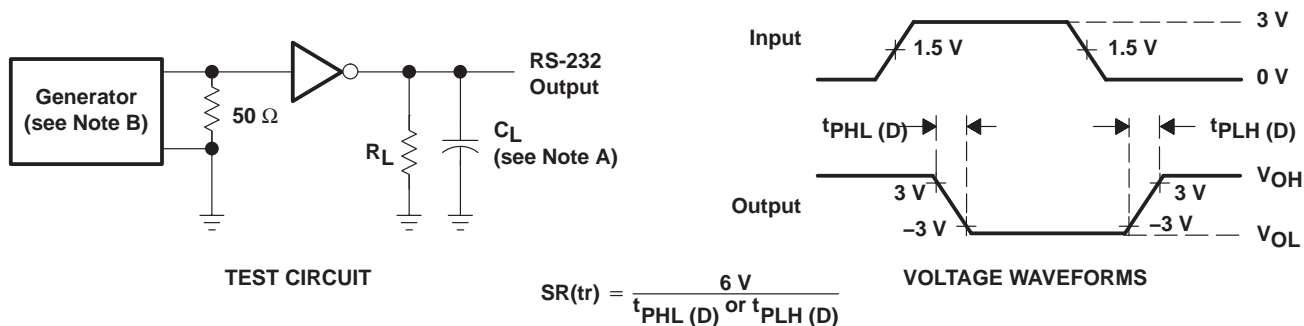
**ESD protection**

PIN	TEST CONDITIONS	TYP	UNIT
D <sub>OUT</sub> , R <sub>IN</sub>	Human-Body Model	±15	kV

**MAX222**  
**5-V DUAL RS-232 LINE DRIVER/RECEIVER**  
**WITH ±15-kV ESD PROTECTION**

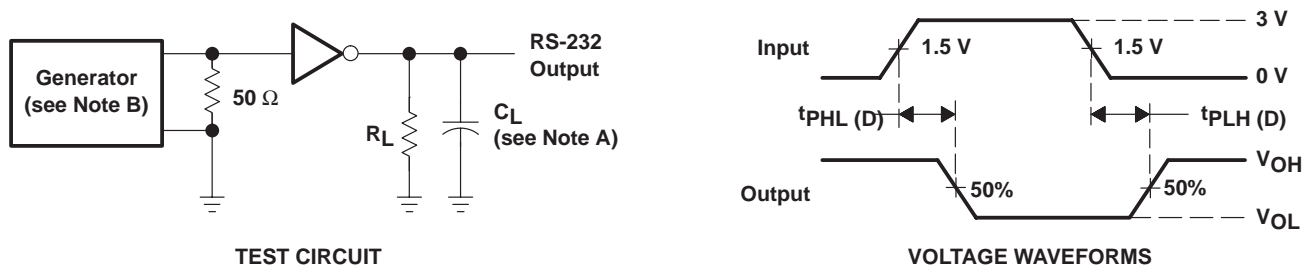
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**PARAMETER MEASUREMENT INFORMATION**



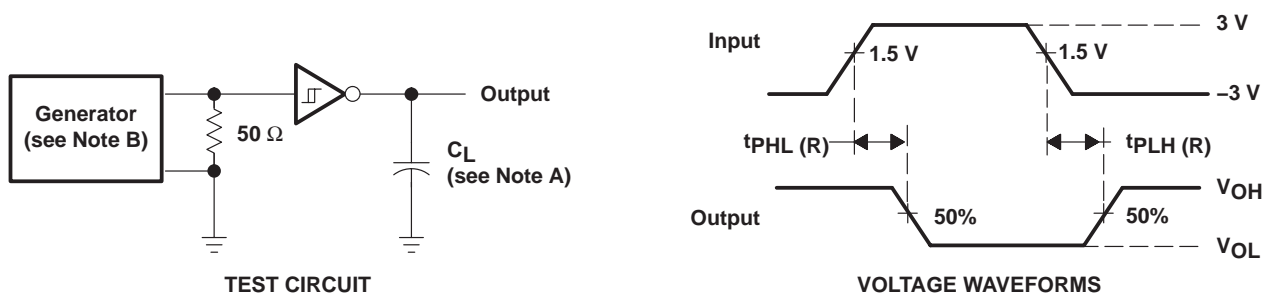
NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. The pulse generator has the following characteristics: PRR = 250 kbit/s,  $Z_O = 50\ \Omega$ , 50% duty cycle,  $t_r \leq 10\text{ ns}$ ,  $t_f \leq 10\text{ ns}$ .

**Figure 1. Driver Slew Rate**



NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. The pulse generator has the following characteristics: PRR = 250 kbit/s,  $Z_O = 50\ \Omega$ , 50% duty cycle,  $t_r \leq 10\text{ ns}$ ,  $t_f \leq 10\text{ ns}$ .

**Figure 2. Driver Pulse Skew**



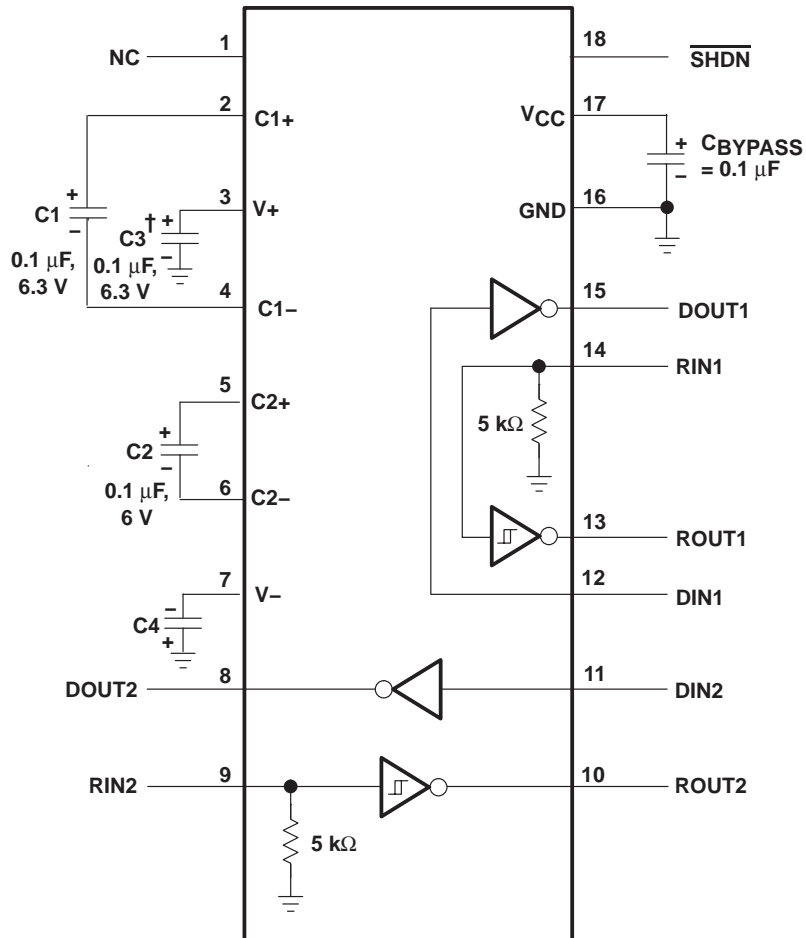
NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. The pulse generator has the following characteristics:  $Z_O = 50\ \Omega$ , 50% duty cycle,  $t_r \leq 10\text{ ns}$ ,  $t_f \leq 10\text{ ns}$ .

**Figure 3. Receiver Propagation Delay Times**

**MAX222**  
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**APPLICATION INFORMATION**



† C3 can be connected to  $V_{CC}$  or GND.

NOTES: A. Resistor values shown are nominal.

B. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown.

**Figure 4. Typical Operating Circuit and Capacitor Values**

# MAX222

## 5-V DUAL RS-232 LINE DRIVER/RECEIVER

### WITH $\pm 15$ -kV ESD PROTECTION

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## APPLICATION INFORMATION

### capacitor selection

The capacitor type used for C1–C4 is not critical for proper operation. The MAX222 requires 0.1- $\mu\text{F}$  capacitors, although capacitors up to 10  $\mu\text{F}$  can be used without harm. Ceramic dielectrics are suggested for the 0.1- $\mu\text{F}$  capacitors. When using the minimum recommended capacitor values, ensure that the capacitance value does not degrade excessively as the operating temperature varies. If in doubt, use capacitors with a larger (e.g., 2 $\times$ ) nominal value. The capacitors' effective series resistance (ESR), which usually rises at low temperatures, influences the amount of ripple on  $V_+$  and  $V_-$ .

Use larger capacitors (up to 10  $\mu\text{F}$ ) to reduce the output impedance at  $V_+$  and  $V_-$ .

Bypass  $V_{CC}$  to ground with at least 0.1  $\mu\text{F}$ . In applications sensitive to power-supply noise generated by the charge pumps, decouple  $V_{CC}$  to ground with a capacitor the same size as (or larger than) the charge-pump capacitors (C1–C4).

### ESD protection

TI MAX222 devices have standard ESD protection structures incorporated on the pins to protect against electrostatic discharges encountered during assembly and handling. In addition, the RS232 bus pins (driver outputs and receiver inputs) of these devices have an extra level of ESD protection. Advanced ESD structures were designed to successfully protect these bus pins against ESD discharge of  $\pm 15$ -kV when powered down.

### ESD test conditions

ESD testing stringently is performed by TI, based on various conditions and procedures. Contact TI for a reliability report that documents test setup, methodology, and results.

### Human-Body Model

The Human-Body Model (HBM) of ESD testing is shown in Figure 5, while Figure 6 shows the current waveform that is generated during a discharge into a low impedance. The model consists of a 100-pF capacitor, charged to the ESD voltage of concern, and subsequently discharged into the DUT through a 1.5-k $\Omega$  resistor.

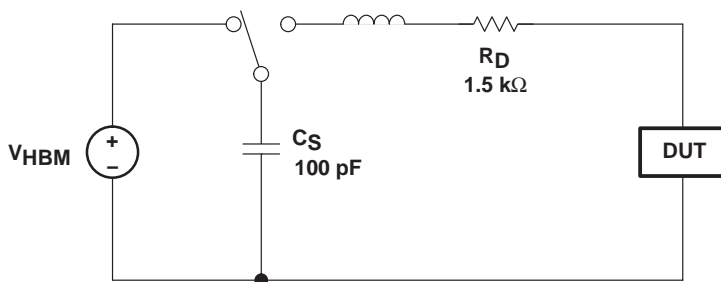


Figure 5. HBM ESD Test Circuit

APPLICATION INFORMATION

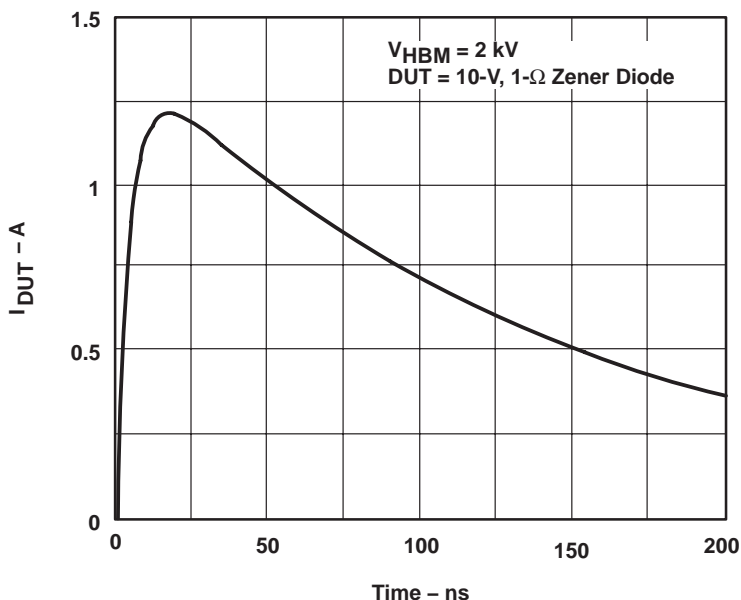


Figure 6. Typical HBM Current Waveform

Machine Model

The Machine Model (MM) ESD test applies to all pins using a 200-pF capacitor with no discharge resistance. The purpose of the MM test is to simulate possible ESD conditions that can occur during the handling and assembly processes of manufacturing. In this case, ESD protection is required for all pins, not just RS-232 pins. However, after PC board assembly, the MM test no longer is as pertinent to the RS-232 pins.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MAX222CDW	ACTIVE	SOIC	DW	18	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	MAX222C	<a href="#">Samples</a>
MAX222CDWG4	ACTIVE	SOIC	DW	18	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	MAX222C	<a href="#">Samples</a>
MAX222CDWR	ACTIVE	SOIC	DW	18	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	MAX222C	<a href="#">Samples</a>
MAX222CDWRG4	ACTIVE	SOIC	DW	18	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	MAX222C	<a href="#">Samples</a>
MAX222IDW	ACTIVE	SOIC	DW	18	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	MAX222I	<a href="#">Samples</a>
MAX222IDWG4	ACTIVE	SOIC	DW	18	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	MAX222I	<a href="#">Samples</a>
MAX222IDWR	ACTIVE	SOIC	DW	18	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	MAX222I	<a href="#">Samples</a>
MAX222IDWRG4	ACTIVE	SOIC	DW	18	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	MAX222I	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MAX222CDWR	SOIC	DW	18	2000	330.0	24.4	10.9	12.0	2.7	12.0	24.0	Q1
MAX222IDWR	SOIC	DW	18	2000	330.0	24.4	10.9	12.0	2.7	12.0	24.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MAX222CDWR	SOIC	DW	18	2000	370.0	355.0	55.0
MAX222IDWR	SOIC	DW	18	2000	370.0	355.0	55.0

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN

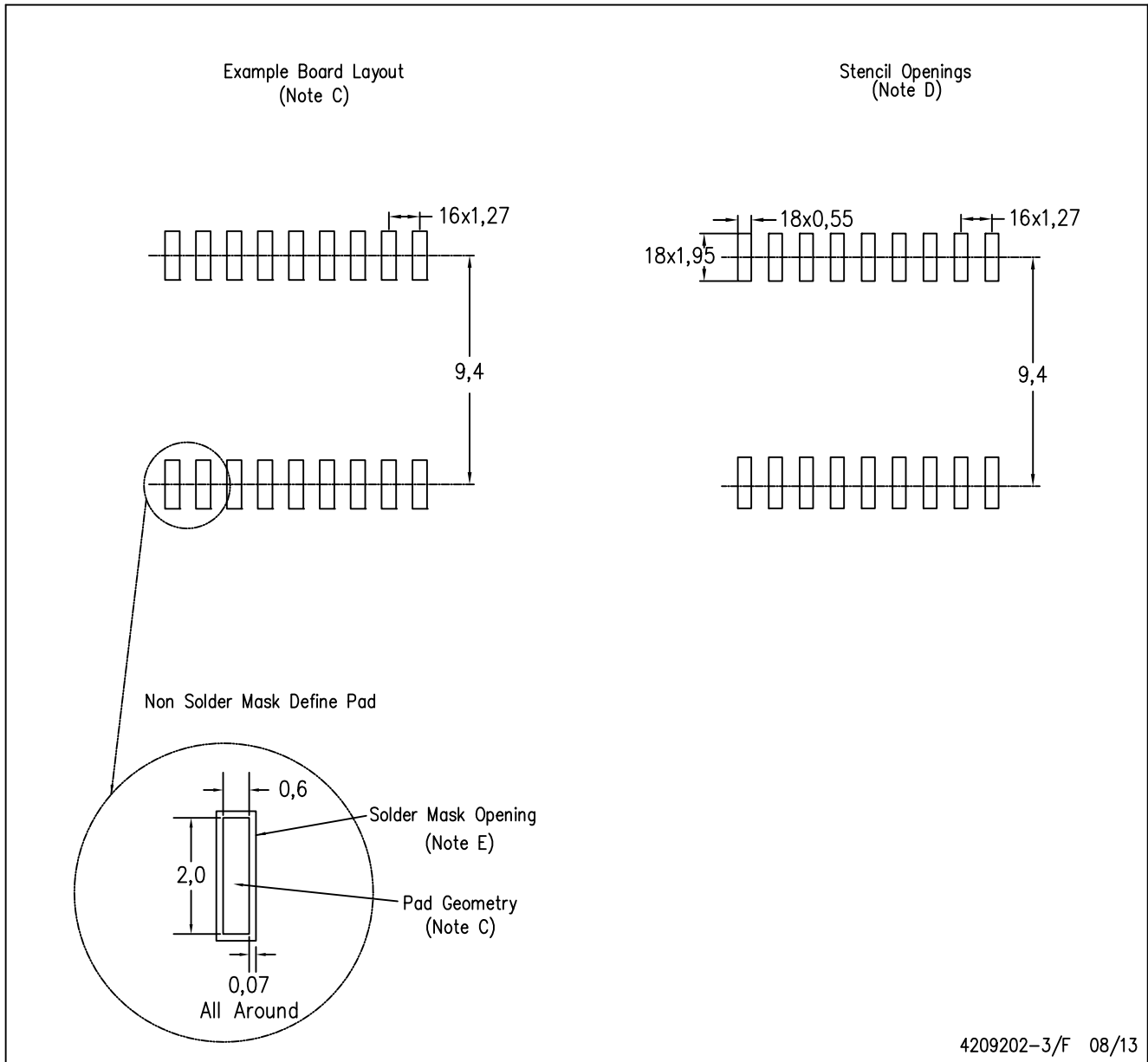


- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - D The 20 pin end lead shoulder width is a vendor option, either half or full width.



DW (R-PDSO-G18)

PLASTIC SMALL OUTLINE



4209202-3/F 08/13

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Refer to IPC7351 for alternate board design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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