

**Nuvoton**  
**1.6 Times Linear Fan Driver**  
**NCT3940S/ NCT3940S-A**

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## 1. GENERAL DESCRIPTION

The NCT3940S/ NCT3940S-A is a simply linear fan driver. It is designed for noise-sensitive or power-sensitive applications that require system cooling. The NCT3940S/ NCT3940S-A is a low quiescent current, low dropout linear regulator which is designed with a P-channel MOSFET to power a DC fan and delivers output current up to 500mA. The output voltage follows the 1.6 times on the voltage of  $V_{SET}$  pin to dynamic adjust the DC fan speed. NCT3940S supports enable pin to control the output voltage. NCT3940S-A is power-on by the VSET pin voltage threshold and supports fully turn-on function. The internal power MOSFET can be fully turned on directly when FON# is at low level. NCT3940S/ NCT3940S-A is available in SOP-8 package.

## 2. FEATURES

### 2.1. General

- VOUT Follows 1.6 Times of VSET
- 150mV Dropout @ 0.5A Output Current
- 5uA Quiescent Current in Shutdown Mode
- UVLO Function
- Full On Function
- Over Current, Short Circuit and Over Temperature Protections
- Low External Component Count
- Low Cost and Easy to Use

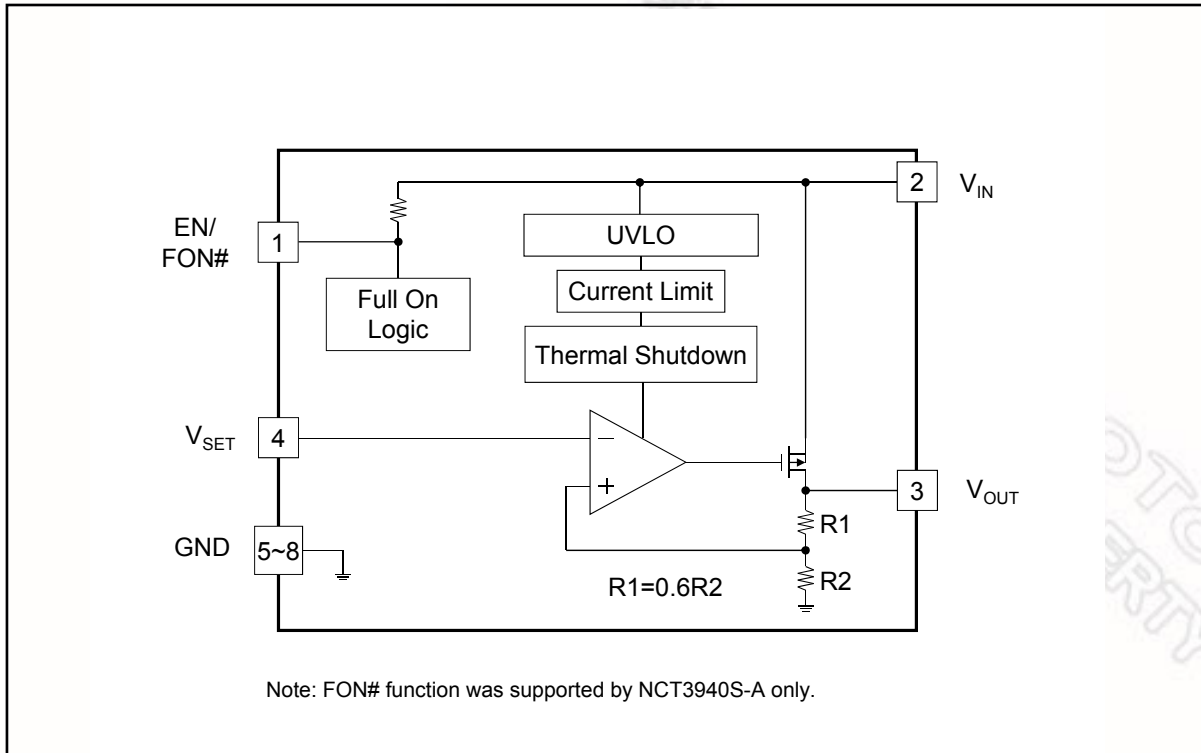
### 2.2. Package

- SOP-8 150mil with Exposed Pad Package
- Lead Free (ROHS Compliant) and Halogen Free

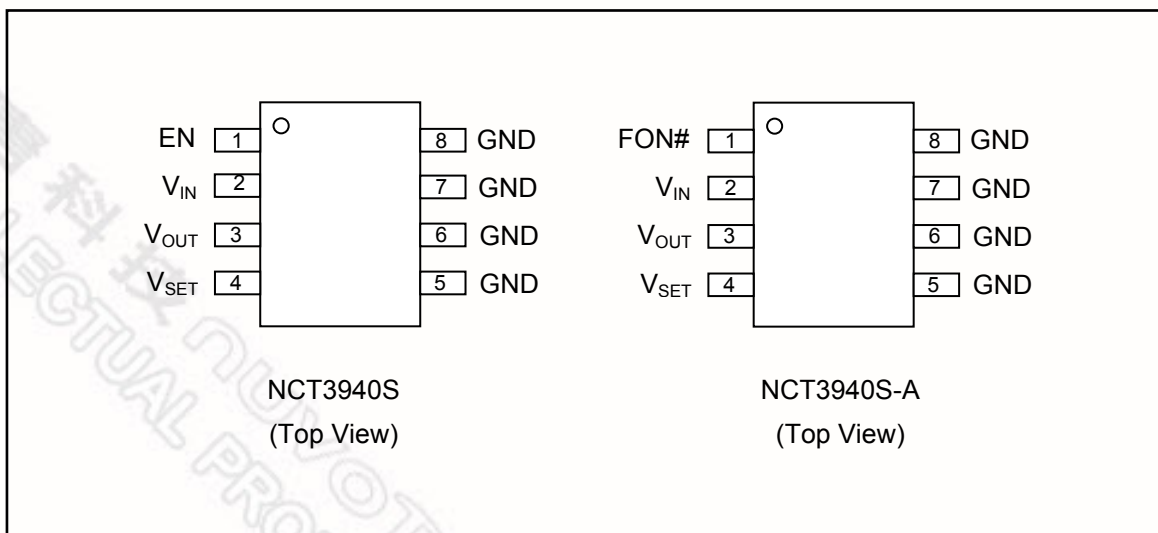
### 2.3. Application

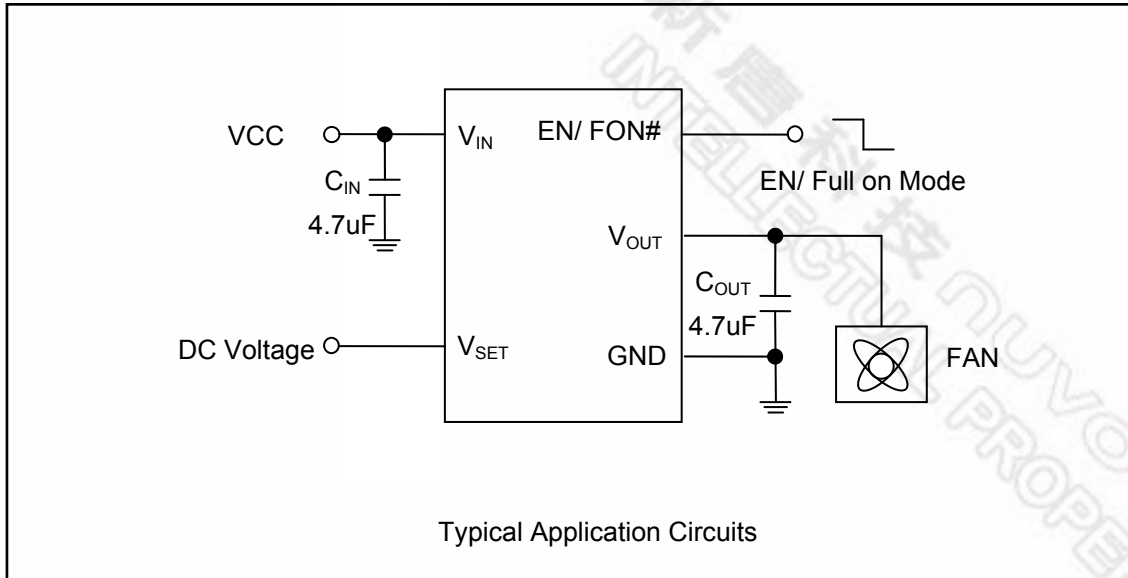
- Notebook/ Netbook Fan Driver
- Peripheral Add-in Cards
- Motherboards
- Battery Powered Systems

### 3. BLOCK DIAGRAM



### 4. PIN CONFIGURATION AND TYPICAL APPLICATION CIRCUIT





## 5. PIN DESCRIPTION

| PIN NAME  | NO       |            | PIN TYPE | DESCRIPTION                                                                                                                                                                                                                                                             |
|-----------|----------|------------|----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|           | NCT3940S | NCT3940S-A |          |                                                                                                                                                                                                                                                                         |
| FON#      | N/A      | 1          | I        | Only for NCT3940S-A device.<br>Full On mode selection pin. Output voltage follows 1.6 times of $V_{SET}$ pin voltage when FON# pin at high level. The internal power MOSFET full turns on when FON# pin at low level. Internal pull up resistor connected to $V_{IN}$ . |
| EN        | 1        | N/A        | I        | Only for NCT3940S device.<br>Enable pin. Output voltage follows 1.6 times of $V_{SET}$ pin voltage when Enable pin at high level.                                                                                                                                       |
| $V_{IN}$  | 2        |            | POWER    | DC power supply input. Connect a bypass capacitor (4.7uF, typically) is recommended.                                                                                                                                                                                    |
| $V_{OUT}$ | 3        |            | AO       | Voltage output pin. Connect a low ESR ceramic capacitor (4.7uF, typically) to ground to assure stability.                                                                                                                                                               |
| $V_{SET}$ | 4        |            | AIN      | Output voltage setting pin. The inputs could be DC voltage. The input voltage must be larger than 1V.                                                                                                                                                                   |

| GND      | 5~8                         | GROUND | Power supply ground. |
|----------|-----------------------------|--------|----------------------|
| PIN TYPE | PIN Attribute               |        |                      |
| AO       | Output pin (Analog)         |        |                      |
| AIN      | Input pin (Analog)          |        |                      |
| I        | Input pin (Digital)         |        |                      |
| POWER    | Positive power supply input |        |                      |
| GROUND   | Power supply ground         |        |                      |

## 6. FUNCTIONAL DESCRIPTION

### 6.1 General Description

The NCT3940S/ NCT3940S-A is a low quiescent current, low dropout linear regulator which is designed with a P-channel MOSFET to power a DC fan. It can deliver output current up to 500mA. The output voltage follows the 1.6 times on the voltage of  $V_{SET}$  pin to dynamic adjust the DC fan speed. NCT3940S supports enable pin to control the output voltage. NCT3940S-A is power-on by the VSET pin and supports fully turn-on function.

### 6.2 Under Voltage Lockout, UVLO

The NCT3940S/ NCT3940S-A was built-in a UVLO protection to keep the output off until the internal circuitry is operating properly. Typical UVLO threshold is 2.5V with 0.15V hysteresis.

### 6.3 Full On Function

The function is for NCT3940S-A only. The input voltage level of FON# can control the internal regulator fully turn on or following 1.6 times of  $V_{SET}$  voltage. When pulling this pin below 0.4V, the regulator will be fully turned on. When pulling this pin above 1.6V, the output voltage will follow 1.6 times of  $V_{SET}$  voltage.

### 6.4 VSET Setting

The output voltage is 1.6 times of  $V_{SET}$  pin voltage. If the input voltage of  $V_{SET}$  is under 1V, the internal regulator will be turned off. When the  $V_{SET}$  voltage exceeds 1V, the output voltage will follow 1.6 times of  $V_{SET}$  voltage.

### 6.5 Current Limit

The NCT3940S/ NCT3940S-A provides a current limit circuitry, which monitors the output current and controls PMOS gate voltage to limit the output current at a specific value.

#### **6.6 Thermal Shutdown**

The NCT3940S/ NCT3940S-A has a thermal shutdown circuitry to limit the junction temperature. When the junction temperature exceeds 150° C, the thermal shutdown circuits disable the output, allowing the device to cool down. The output circuitry is enabled again after the junction temperature cools down by 30° C, resulting in a pulsed output during continuous thermal overload conditions. The thermal protection is designed to protect the IC in the event of over temperature conditions. For reliable operation, the junction temperature cannot exceed 125° C.

#### **6.7 VIN Decoupling**

To achieve the best results when using the NCT3940S/ NCT3940S-A, decouple the power supply with a 4.7uF capacitor. Use a high quality ceramic surface mount capacitor if possible. Surface mount components minimize lead inductance, which improves performance, and ceramic capacitors tend to have adequate high frequency response for decoupling applications.

#### **6.8 VOUT Stability**

To maintain circuit stability and improve transient response over temperature and current, the NCT3940S/ NCT3940S-A needs a suitable output capacitor. In order to insure the circuit stability, the suitable output capacitor should be larger than 4.7uF.

## 7. ELECTRICAL CHARACTERISTIC

### 7.1 Absolute Maximum Ratings

| PARAMETER             |                 | RATING                                     | UNIT |
|-----------------------|-----------------|--------------------------------------------|------|
| Power Supply Voltage  |                 | -0.3 to 7V                                 | V    |
| Voltage on Other Pins |                 | -0.3 to 7V                                 | V    |
| Storage Temperature   |                 | -50 to 150                                 | °C   |
| Soldering Temperature |                 | Refer to IPC/JEDEC J-STD-020 Specification |      |
| ESD Protection        | Human Body Mode | 2                                          | kV   |
|                       | Machine Mode    | 200                                        | V    |
|                       | Latch-up        | 100                                        | mA   |

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

### 7.2 Thermal Information

| ITEM                                                | RATING           | UNIT |
|-----------------------------------------------------|------------------|------|
| Power Dissipation, $P_D$ @ $T_A=25^{\circ}\text{C}$ | Internal Limited | W    |
| Package Thermal Resistance, SOP8, $\theta_{JA}$     | 160              | °C/W |

### 7.3 Recommended operating conditions

| PARAMETER             | RATING       | UNIT |
|-----------------------|--------------|------|
| Operating Temperature | 0 to 70      | °C   |
| Junction Temperature  | -40 to 125   | °C   |
| Supply Voltage, VCC   | $5 \pm 10\%$ | V    |

#### 7.4 Electrical CHARACTERISTICS

$V_{IN}=5V$ ,  $V_{SET}=2V$ ,  $C_{IN}=C_{OUT}=2.2\mu F$ ,  $T_a=25^\circ C$

| PARAMETER                             | SYM.        | MIN.  | TYP. | MAX.  | UNIT       | CONDITIONS                               |
|---------------------------------------|-------------|-------|------|-------|------------|------------------------------------------|
| <b>Supply Input Voltage</b>           |             |       |      |       |            |                                          |
| Supply Input Voltage                  | $V_{IN}$    | 4.5   |      | 5.5   | V          |                                          |
| <b>Under Voltage Lockout (UVLO)</b>   |             |       |      |       |            |                                          |
| $V_{IN}$ UVLO Threshold               |             | 2.1   | 2.5  | 2.9   | V          | $V_{IN}$ rising                          |
| $V_{IN}$ UVLO Hysteresis              |             |       | 0.15 |       | V          |                                          |
| <b>EN Pin</b>                         |             |       |      |       |            |                                          |
| EN Voltage High                       |             | 2.0   |      |       | V          |                                          |
| EN Voltage Low                        |             |       |      | 0.4   | V          |                                          |
| EN Pin Bias Current                   |             |       | 1.5  | 10    | $\mu A$    | EN=0V                                    |
| <b>FON# Pin</b>                       |             |       |      |       |            |                                          |
| Low Voltage                           | $V_{IL}$    |       |      | 0.4   | V          |                                          |
| High Voltage                          | $V_{IH}$    | 1.6   |      |       | V          |                                          |
| FON# Pin Bias Current                 | $I_{FON\#}$ |       | 1.5  | 10    | $\mu A$    | FON#=0V                                  |
| <b>Supply Input Current</b>           |             |       |      |       |            |                                          |
| Quiescent Current                     | $I_Q$       |       | 0.5  | 1     | mA         | $V_{OUT} = 5V$                           |
| <b>Output Voltage</b>                 |             |       |      |       |            |                                          |
| $V_{OUT}$ Voltage / $V_{SET}$ Voltage |             | 1.552 | 1.6  | 1.648 | V/V        | $V_{IN}=5.5V$ ,<br>$V_{SET}=1V\sim 3.2V$ |
| Load Regulation                       |             |       | 30   | 40    | mV         | $10mA \leq I_{OUT} \leq 500mA$           |
| Line Regulation                       |             |       | 0.2  | 0.5   | %          | $V_{IN}=4.5V$ to $5.5V$                  |
| Output Resistance                     |             |       | 0.3  | 0.4   | $\Omega$   | $I_{OUT}=500mA$ ,<br>$V_{SET}=3.4V$      |
| Output Leakage                        |             |       | 0    | 1     | $\mu A$    | $V_{SET} < 1V$                           |
| <b><math>V_{SET}</math> Pin</b>       |             |       |      |       |            |                                          |
| Minimum $V_{SET}$ Voltage             |             |       | 1    |       | V          |                                          |
| <b>Current Limit Protection</b>       |             |       |      |       |            |                                          |
| Current Limit                         | $I_{LIMIT}$ | 0.7   | 1.0  |       | A          |                                          |
| <b>Over Temperature Protection</b>    |             |       |      |       |            |                                          |
| Thermal Shutdown Temperature          |             | 145   | 150  | 160   | $^\circ C$ |                                          |
| Thermal Shutdown Hysteresis           |             | 20    | 30   | 40    | $^\circ C$ |                                          |

## 8. TYPICAL OPERATING WAVEFORMS

$V_{SET} = 2V$ ,  $V_{EN}=V_{IN}$ ,  $V_{IN} = 5V$ ,  $I_O = 0.5A$ ,  $C_{IN} = C_{OUT} = 4.7\mu F$ ,  $T_A = T_J = 25^\circ C$ , unless otherwise specified

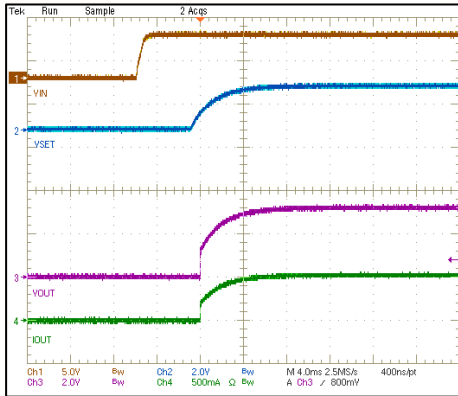


Figure 01. Power on

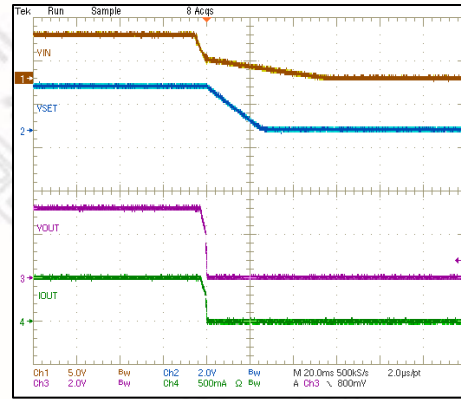


Figure 02. Power off

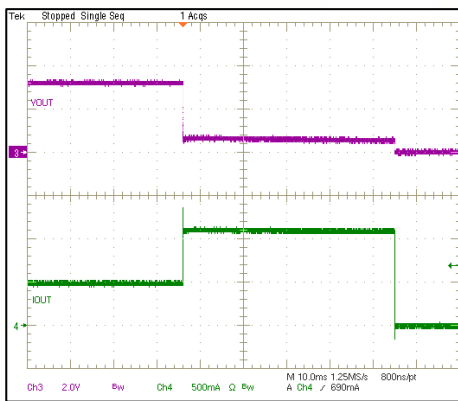


Figure 03. Current Limit, OTP

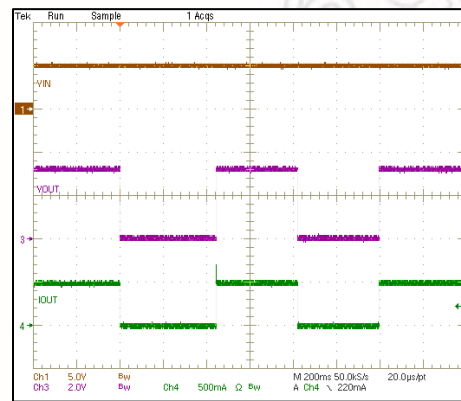


Figure 04. OTP

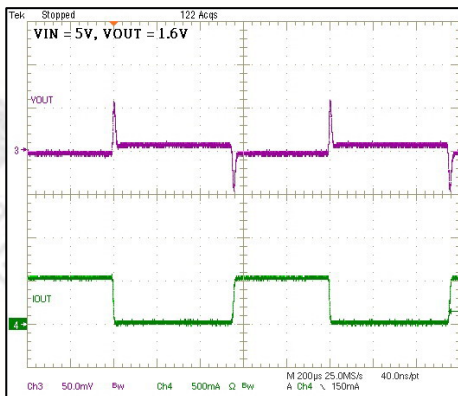


Figure 05. Load Transient

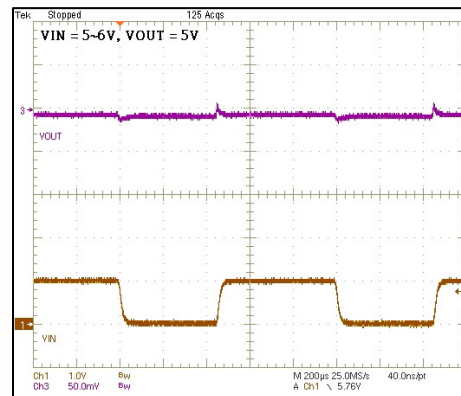


Figure 06. Line Transient

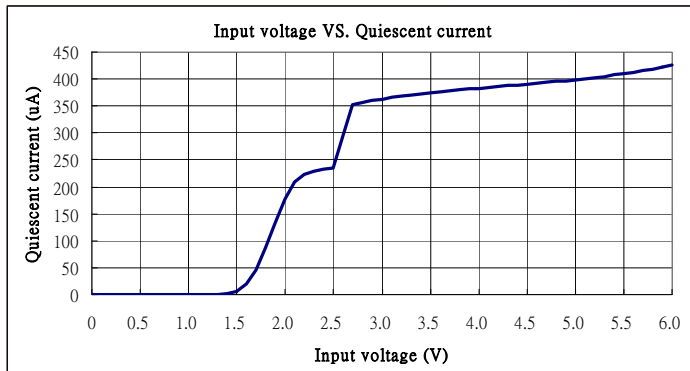


Figure 07. Input Voltage vs. Quiescent Current

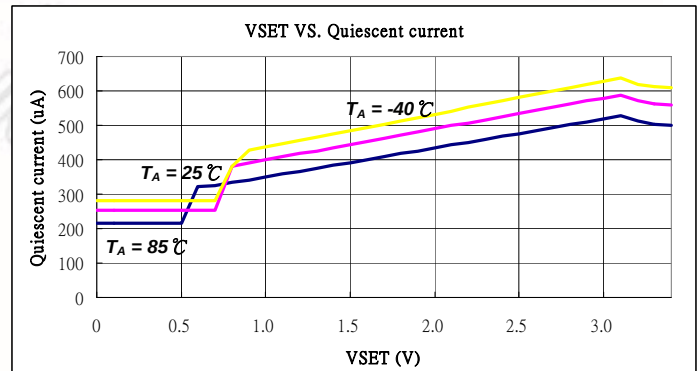
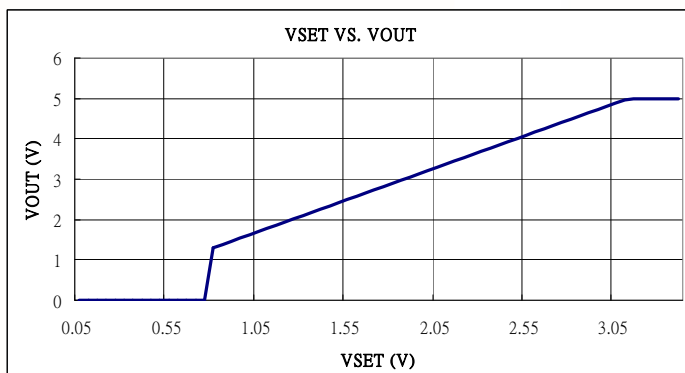
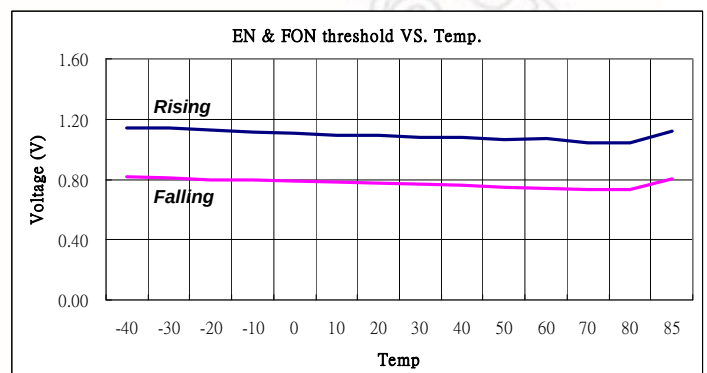
Figure 08.  $V_{SET}$  vs. Quiescent CurrentFigure 09.  $V_{SET}$  vs.  $V_{OUT}$ 

Figure 10. EN &amp; FON Threshold vs. Temperature

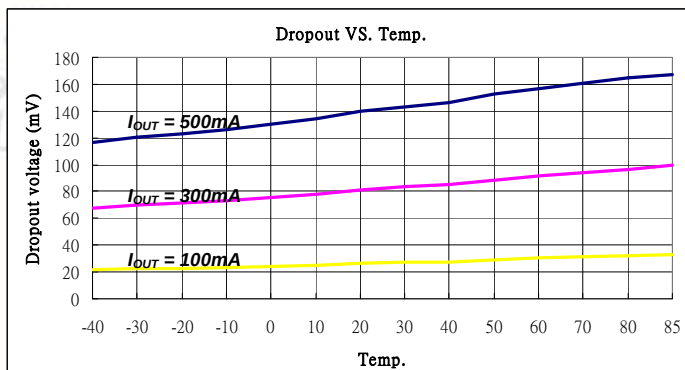
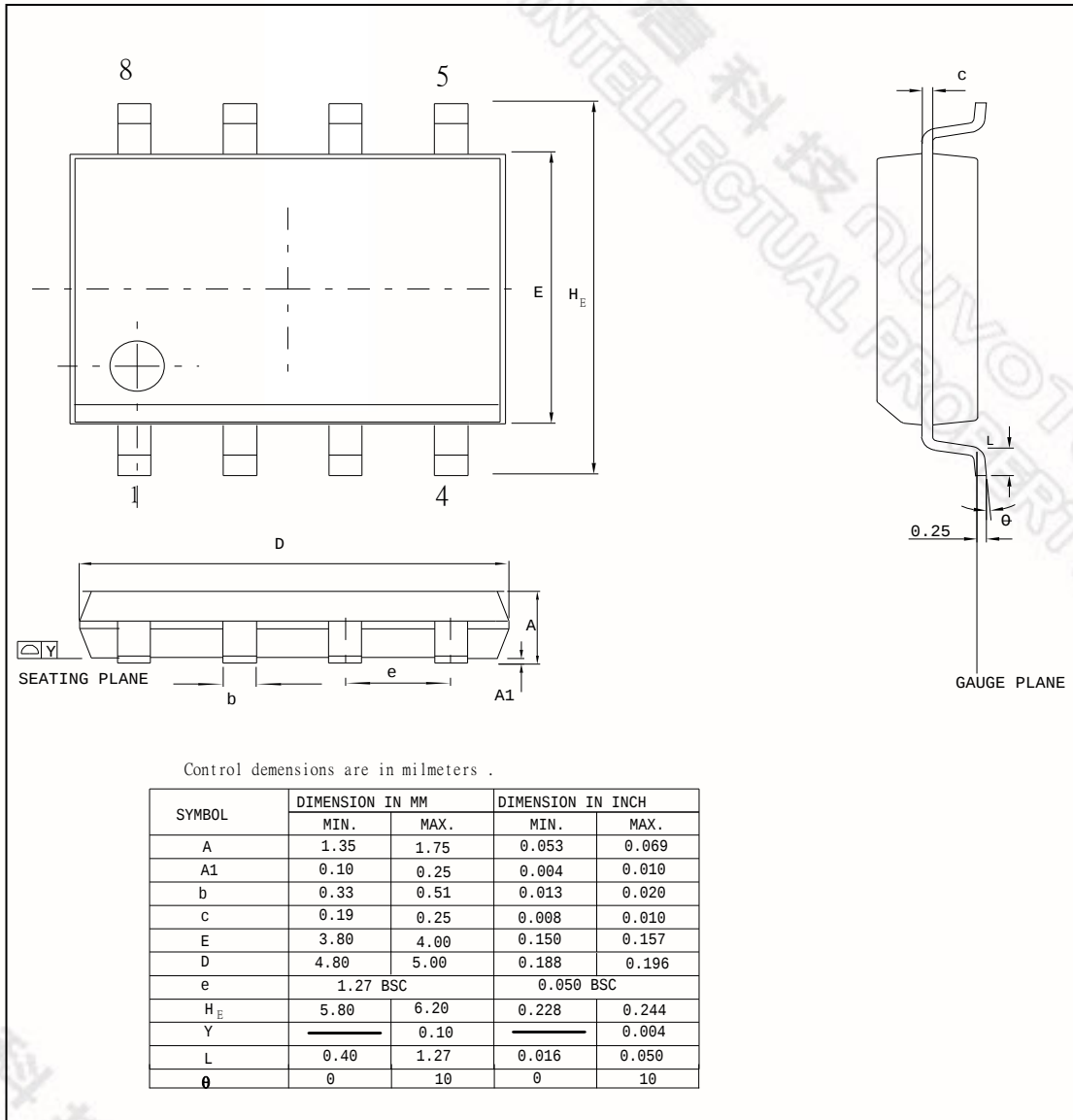


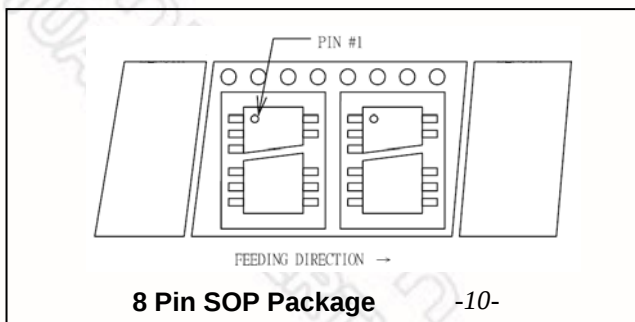
Figure 11. Dropout Voltage vs. Temperature

## 9. PACKAGE DIMENSION

SOP-8 (150mil)



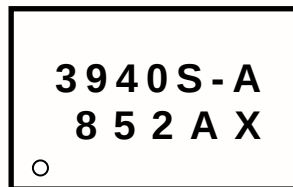
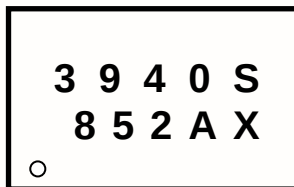
### 9.1 Taping Specification



## 10. ORDERING INFORMATION

| Part Number | Package Type             | Supplied as                                         | Production Flow          |
|-------------|--------------------------|-----------------------------------------------------|--------------------------|
| NCT3940S    | 8PIN SOP (Green Package) | E Shape: 100 units/Tube<br>T Shape: 2,500 units/T&R | Commercial, 0°C to +70°C |
| NCT3940S-A  |                          |                                                     |                          |

## 11. TOP MARKING SPECIFICATION



1<sup>st</sup> Line: 3940S/ 3940S-A

2<sup>nd</sup> Line: Tracking code

- 852: packages assembled in Year 2008, week 52
- A: assembly house ID.
- X: IC version. (A means A; B means B and C means C...etc.)

## 12. REVISION HISTORY

| VERSION | DATE       | PAGE   | DESCRIPTION                             |
|---------|------------|--------|-----------------------------------------|
| A1      | 11/28/2008 | All    | New Create                              |
| A2      | 11/28/2008 | P8, P9 | Added waveforms, fixed some description |
| A3      | 03/07/2011 | All    | Fixed some description                  |

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