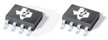


OPA1652
OPA1654

SoundPlus™ Low Noise and Distortion, General-Purpose, FET-Input AUDIO OPERATIONAL AMPLIFIERS

Check for Samples: OPA1652, OPA1654

FEATURES

- **Low Noise: 4.5 nV/$\sqrt{\text{Hz}}$ at 1 kHz**
- **Low Distortion: 0.00005% at 1 kHz**
- **Low Quiescent Current:**
  2 mA Per Channel
- **Low Input Bias Current: 10 pA**
- **Slew Rate: 10 V/µs**
- **Wide Gain Bandwidth: 18 MHz (G = +1)**
- **Unity Gain Stable**
- **Rail-to-Rail Output**
- **Wide Supply Range:**
  ±2.25 V to ±18 V, or +4.5 V to +36 V
- **Dual and Quad Versions Available**
- **Small Package Sizes:**
  DUAL: SO-8 and MSOP-8
  QUAD: SO-14 and TSSOP-14

APPLICATIONS

- **Analog and Digital Mixers**
- **Audio Effects Processors**
- **Musical Instruments**
- **A/V Receivers**
- **DVD and Blu-Ray™ Players**
- **Car Audio Systems**

DESCRIPTION

The OPA1652 (dual) and OPA1654 (quad) FET-input operational amplifiers achieve a low 4.5 nV/$\sqrt{\text{Hz}}$ noise density with an ultralow distortion of 0.00005% at 1 kHz. The OPA1652 and OPA1654 op amps offer rail-to-rail output swing to within 800 mV with 2-kΩ load, which increases headroom and maximizes dynamic range. These devices also have a high output drive capability of ±30 mA.

These devices operate over a very wide supply range of ±2.25 V to ±18 V, or +4.5 V to +36 V, on only 2 mA of supply current per channel. The OPA1652 and OPA1654 op amps are unity-gain stable and provide excellent dynamic behavior over a wide range of load conditions.

These devices also feature completely independent circuitry for lowest crosstalk and freedom from interactions between channels, even when overdriven or overloaded.

The OPA1652 and OPA1654 temperature ranges are specified from –40°C to +85°C.

SoundPlus is a trademark of Texas Instruments Incorporated.
Blu-Ray is a trademark of Blu-Ray Disc Association.
All other trademarks are the property of their respective owners.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	PACKAGE MARKING
OPA1652	SO-8	D	OP1652
	MSOP-8	DGK	OUPI
OPA1654	SO-14	D	OP1654
	TSSOP-14	PW	OP1654

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

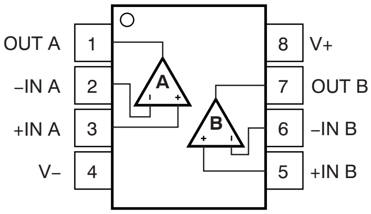
Over operating free-air temperature range (unless otherwise noted).

		OPA1652, OPA1654	UNIT
Supply Voltage	V_S = (V+) – (V–)	40	V
Input Voltage		(V–) – 0.5 to (V+) + 0.5	V
Input Current (All pins except power-supply pins)		±10	mA
Output Short-Circuit(2)		Continuous	
Operating Temperature		–55 to +125	°C
Storage Temperature		–65 to +150	°C
Junction Temperature		200	°C
ESD Ratings	Human Body Model (HBM)	2	kV
	Charged Device Model (CDM)	1	kV
	Machine Model (MM)	200	V

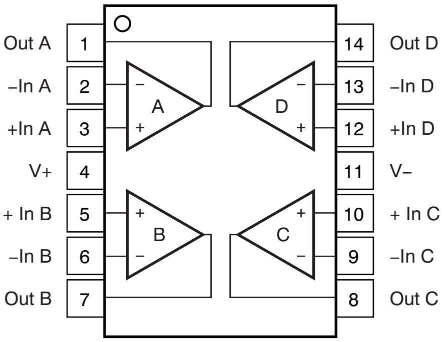
(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.
(2) Short-circuit to $V_S/2$ (ground in symmetrical dual supply setups), one amplifier per package.

PIN CONFIGURATIONS

OPA1652: D AND DGK PACKAGES
SO-8 AND MSOP-8
(TOP VIEW)



OPA1654: D AND PW PACAKGES
SO-14 AND TSSOP-14
(TOP VIEW)



ELECTRICAL CHARACTERISTICS: $V_S = \pm 15$ V

At $T_A = +25°C$, $R_L = 2\ k\Omega$, and $V_{CM} = V_{OUT}$ = midsupply, unless otherwise noted.

PARAMETER		TEST CONDITIONS		OPA1652, OPA1654			UNIT
				MIN	TYP	MAX	
AUDIO PERFORMANCE							
THD+N	Total harmonic distortion + noise				0.00005		%
		G = +1, f = 1 kHz, $V_O = 3\ V_{RMS}$			–126		dB
IMD	Intermodulation distortion	G = +1, $V_O = 3\ V_{RMS}$	SMPTE/DIN Two-Tone, 4:1 (60 Hz and 7 kHz)		0.00005		%
					–126		dB
			DIM 30 (3-kHz square wave and 15-kHz sine wave)		0.00005		%
					–126		dB
			CCIF Twin-Tone (19 kHz and 20 kHz)		0.00005		%
					–126		dB
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product	G = +1			18		MHz
SR	Slew rate	G = –1			10		V/μs
	Full power bandwidth(1)	$V_O = 1\ V_P$			1.6		MHz
	Overload recovery time	G = –10			1		μs
	Channel separation (dual and quad)	f = 1 kHz			–120		dB
NOISE							
e_n	Input voltage noise	f = 20 Hz to 20 kHz			5.4		μV_{PP}
	Input voltage noise density	f = 1 kHz			4.5		nV/√Hz
I_n	Input current noise density	f = 1 kHz			0.5		pA/√Hz
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	V_S = ±2.25 V to ±18 V			±0.5	±1.5	mV
		V_S = ±2.25 V to ±18 V, T_A = –40°C to +85°C(2)			2	8	μV/°C
PSRR	Power-supply rejection ratio	V_S = ±2..25 V to ±18 V			3	8	μV/V
INPUT BIAS CURRENT							
I_B	Input bias current	V_{CM} = 0 V			±10	±100	pA
I_{OS}	Input offset current	V_{CM} = 0 V			±10	±100	pA
INPUT VOLTAGE RANGE							
V_{CM}	Common-mode voltage range			(V–) + 0.5		(V+) – 2	V
CMRR	Common-mode rejection ratio			100	110		dB
INPUT IMPEDANCE							
	Differential				100 || 6		MΩ || pF
	Common-mode				6000 || 2		GΩ || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	$(V–) + 0.8\ V \le V_O \le (V+) – 0.8\ V$, $R_L = 2\ k\Omega$		106	114		dB
OUTPUT							
V_{OUT}	Voltage output	$R_L = 2\ k\Omega$		(V–) + 0.8		(V+) – 0.8	V
I_{OUT}	Output current				See Typical Characteristics		mA
Z_O	Open-loop output impedance	f = 1 MHz			See Typical Characteristics		Ω
I_{SC}	Short-circuit current(3)				±50		mA
C_{LOAD}	Capacitive load drive				100		pF
POWER SUPPLY							
V_S	Specified voltage			±2.25		±18	V
I_Q	Quiescent current (per channel)	I_{OUT} = 0 A			2.0	2.5	mA
		I_{OUT} = 0 A, T_A = –40°C to +85°C(2)				2.8	mA

(1) Full-power bandwidth = SR/(2π × V_P), where SR = slew rate.
(2) Specified by design and characterization.
(3) One channel at a time.

ELECTRICAL CHARACTERISTICS: V_S = ±15 V (continued)

At T_A = +25°C, R_L = 2 kΩ, and V_{CM} = V_{OUT} = midsupply, unless otherwise noted.

PARAMETER	TEST CONDITIONS	OPA1652, OPA1654 MIN	TYP	MAX	UNIT
TEMPERATURE					
Specified range		–40		+85	°C
Operating range		–55		+125	°C

THERMAL INFORMATION: OPA1652

THERMAL METRIC[1]		OPA1652 D (SO) 8 PINS	OPA1652 DGK (MSOP) 8 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	143.6	218.9	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	76.9	78.6	
θ_{JB}	Junction-to-board thermal resistance	61.8	103.7	
ψ_{JT}	Junction-to-top characterization parameter	27.8	14.6	
ψ_{JB}	Junction-to-board characterization parameter	61.3	101.8	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	N/A	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

THERMAL INFORMATION: OPA1654

THERMAL METRIC[1]		OPA1654 D (SO) 14 PINS	OPA1654 PW (TSSOP) 14 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	90.1	126.9	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	54.8	46.6	
θ_{JB}	Junction-to-board thermal resistance	44.4	58.6	
ψ_{JT}	Junction-to-top characterization parameter	19.9	5.5	
ψ_{JB}	Junction-to-board characterization parameter	44.2	57.8	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	N/A	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

TYPICAL CHARACTERISTICS

At $T_A = +25°C$, $V_S = ±15\ V$, and $R_L = 2\ kΩ$, unless otherwise noted.

INPUT VOLTAGE NOISE DENSITY vs FREQUENCY

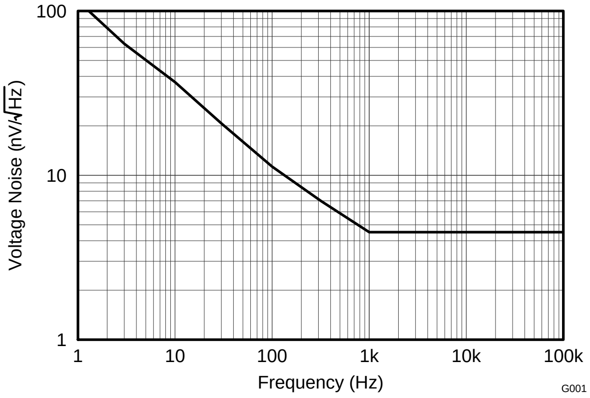


Figure 1.

0.1Hz TO 10Hz NOISE

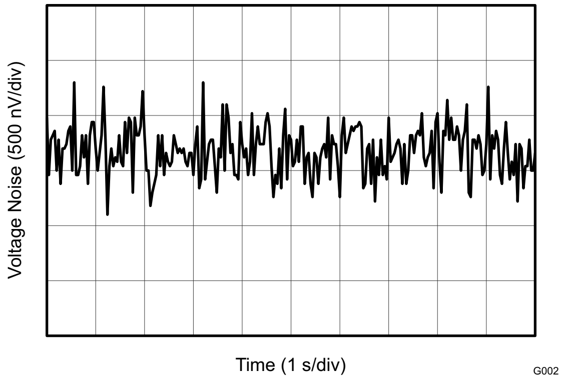


Figure 2.

VOLTAGE NOISE vs SOURCE RESISTANCE

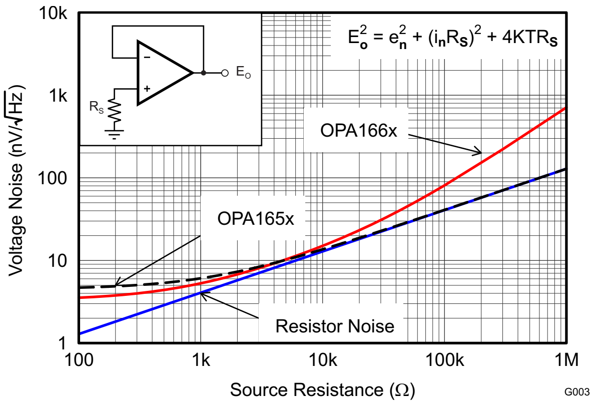


Figure 3.

MAXIMUM OUTPUT VOLTAGE vs FREQUENCY

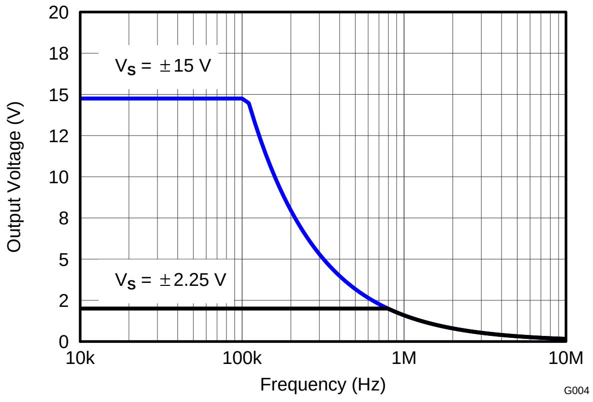


Figure 4.

GAIN AND PHASE vs FREQUENCY

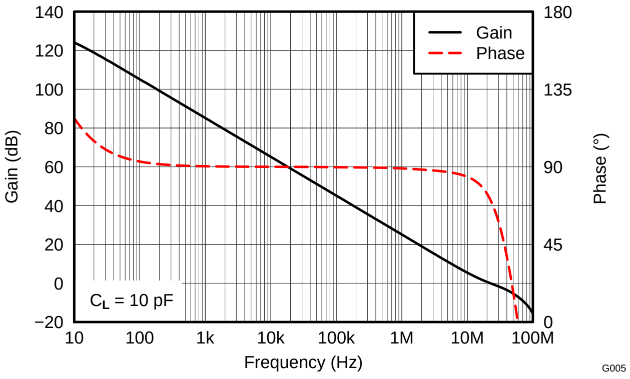


Figure 5.

CLOSED-LOOP GAIN vs FREQUENCY

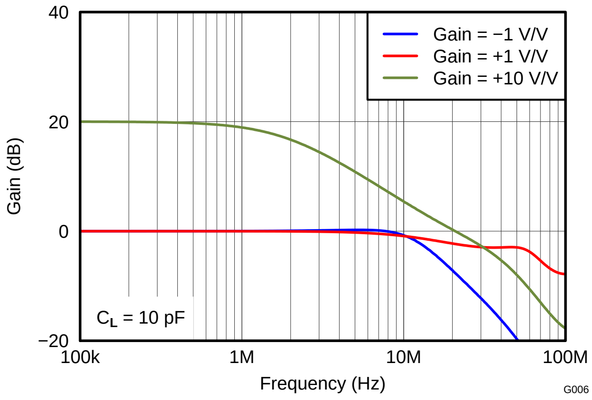


Figure 6.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = ±15 V, and R_L = 2 kΩ, unless otherwise noted.

THD+N RATIO vs FREQUENCY

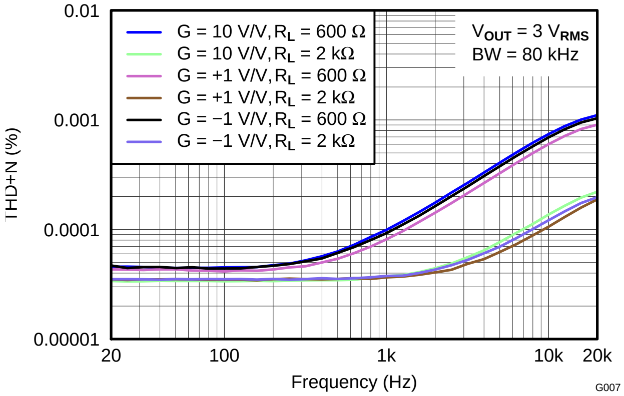


Figure 7.

THD+N RATIO vs FREQUENCY

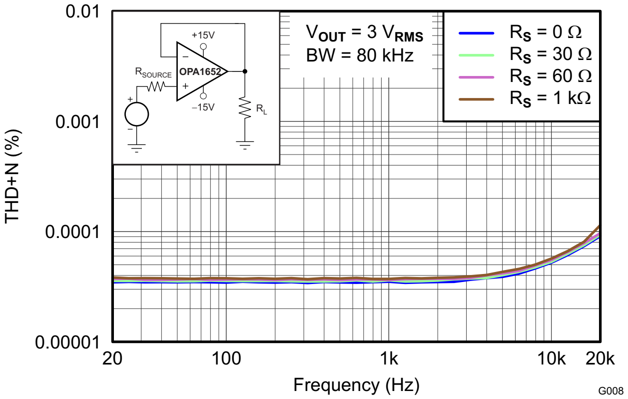


Figure 8.

THD+N RATIO vs FREQUENCY

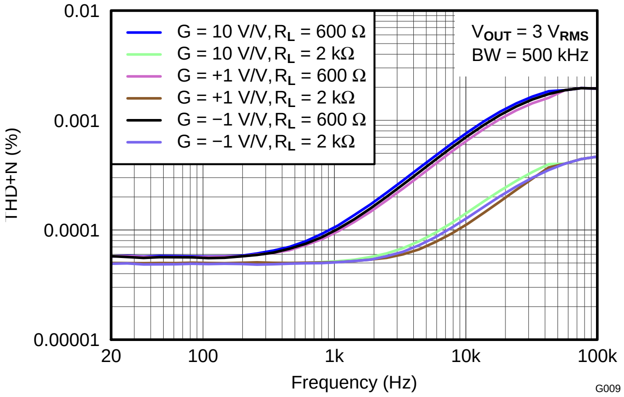


Figure 9.

THD+N RATIO vs FREQUENCY

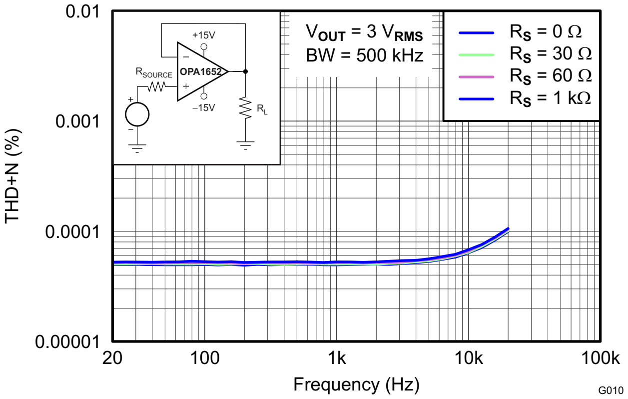


Figure 10.

THD+N RATIO vs OUTPUT AMPLITUDE

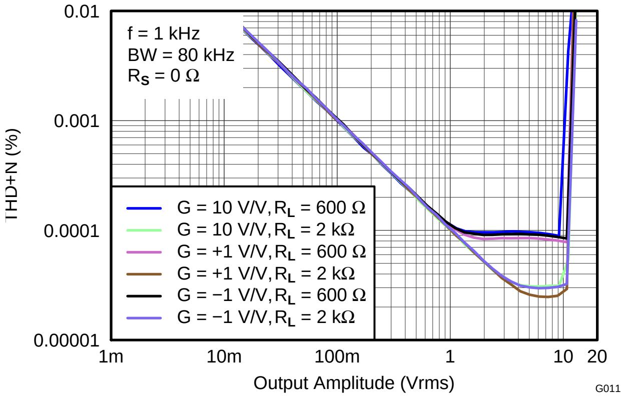


Figure 11.

INTERMODULATION DISTORTION vs OUTPUT AMPLITUDE

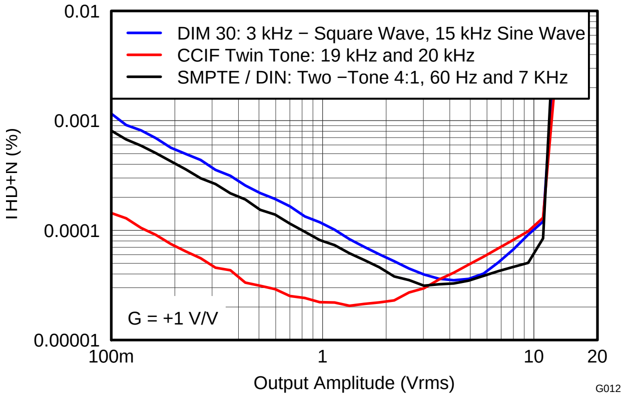


Figure 12.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = ±15 V, and R_L = 2 kΩ, unless otherwise noted.

CHANNEL SEPARATION vs FREQUENCY

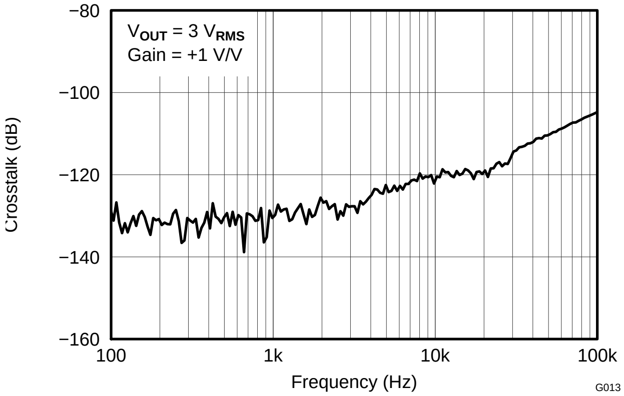


Figure 13.

CMRR AND PSRR vs FREQUENCY (Referred to Input)

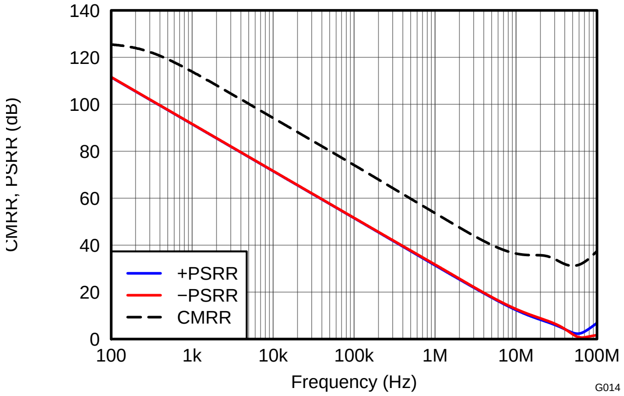


Figure 14.

SMALL-SIGNAL STEP RESPONSE (100mV)

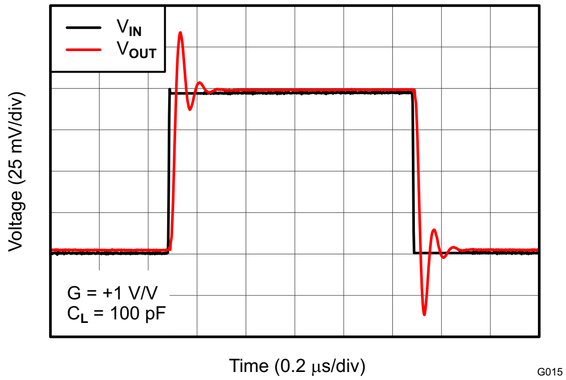


Figure 15.

SMALL-SIGNAL STEP RESPONSE (100mV)

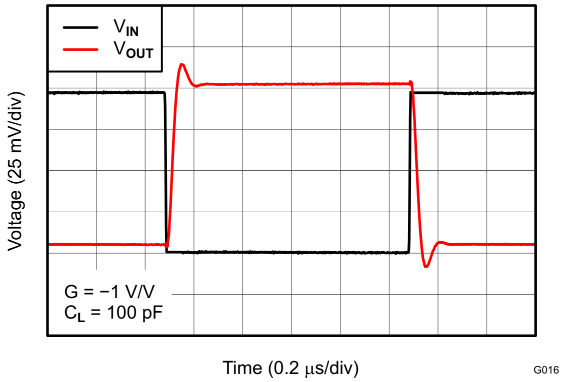


Figure 16.

LARGE-SIGNAL STEP RESPONSE

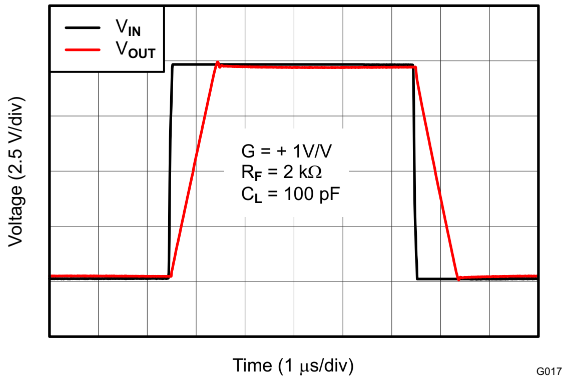


Figure 17.

LARGE-SIGNAL STEP RESPONSE

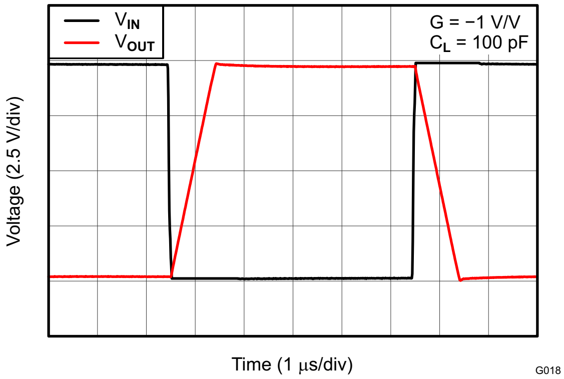


Figure 18.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = ±15 V, and R_L = 2 kΩ, unless otherwise noted.

SMALL-SIGNAL OVERSHOOT vs CAPACITIVE LOAD

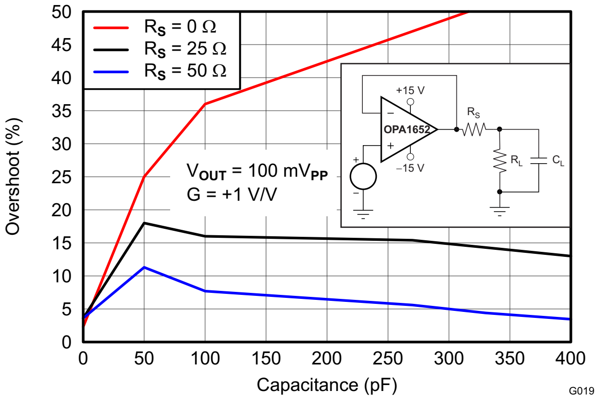


Figure 19.

SMALL-SIGNAL OVERSHOOT vs CAPACITIVE LOAD

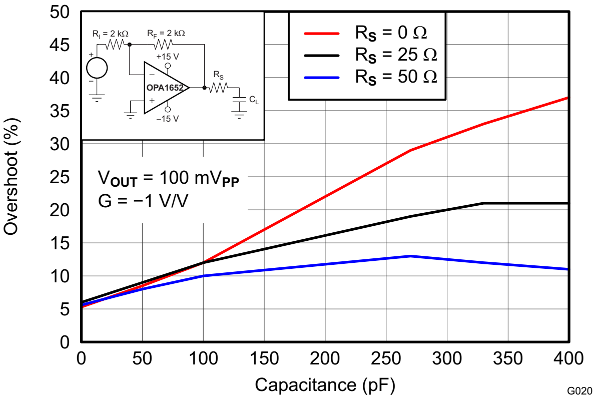


Figure 20.

SMALL-SIGNAL OVERSHOOT vs FEEDBACK CAPACITOR (100mV Output Step)

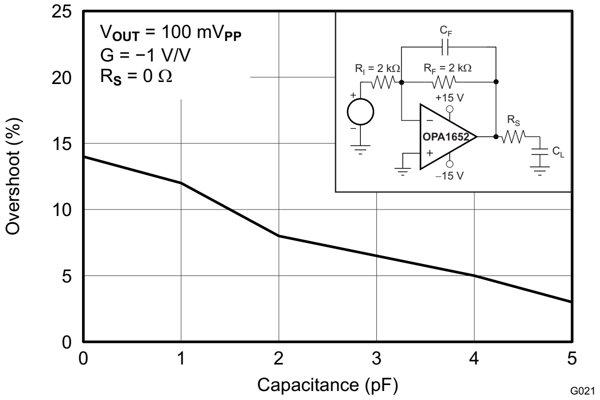


Figure 21.

OPEN-LOOP GAIN vs TEMPERATURE

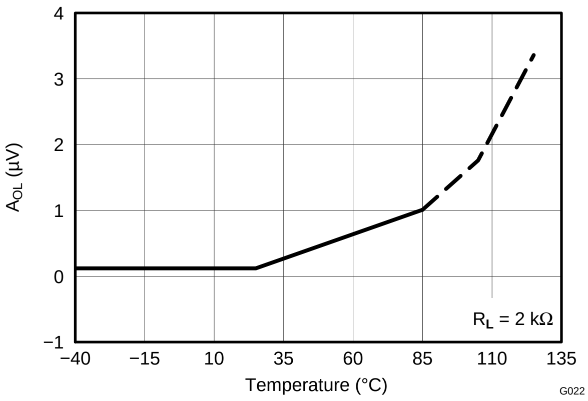


Figure 22.

I_B AND I_{OS} vs TEMPERATURE

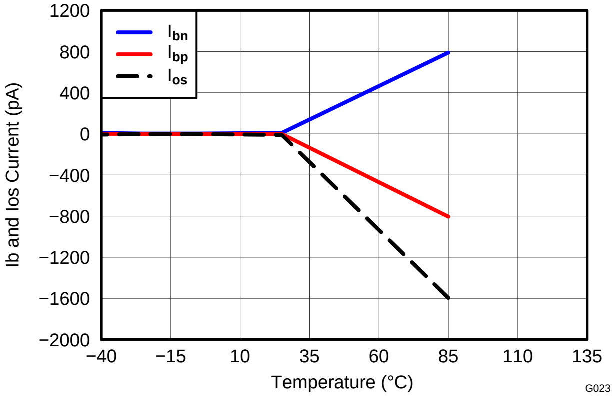


Figure 23.

I_B AND I_{OS} vs COMMON-MODE VOLTAGE

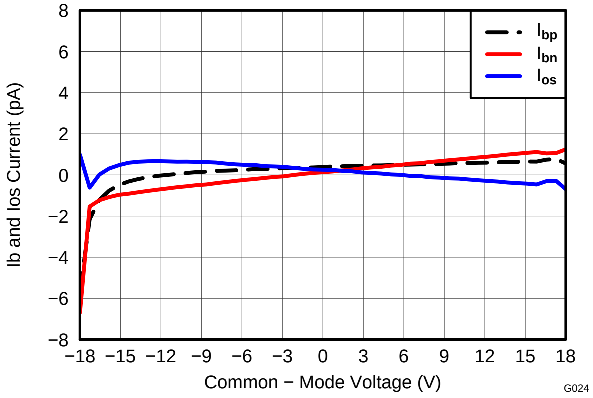


Figure 24.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = ±15 V, and R_L = 2 kΩ, unless otherwise noted.

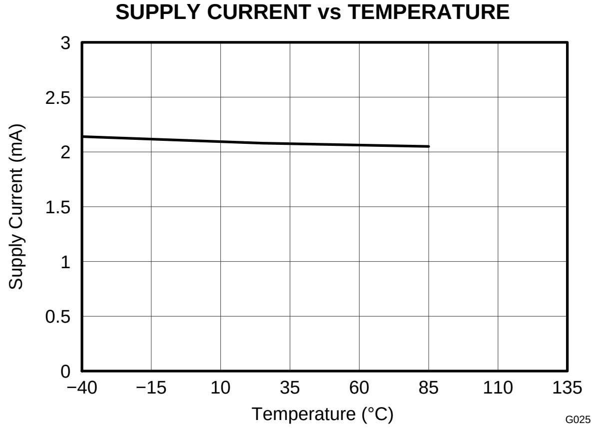

SUPPLY CURRENT vs TEMPERATURE

Figure 25.

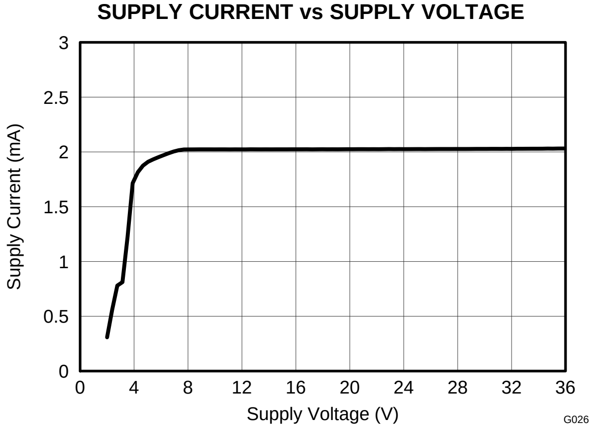

SUPPLY CURRENT vs SUPPLY VOLTAGE

Figure 26.

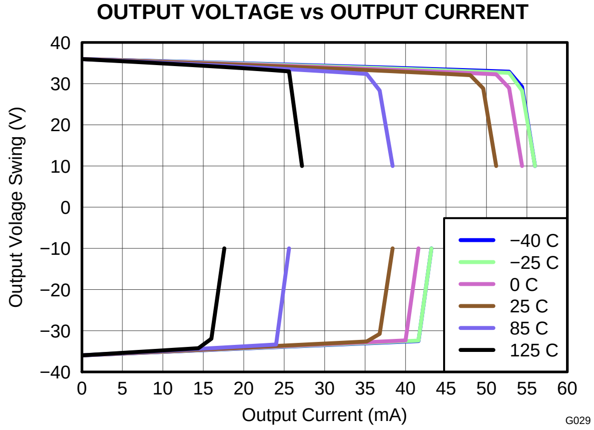

OUTPUT VOLTAGE vs OUTPUT CURRENT

Figure 27.

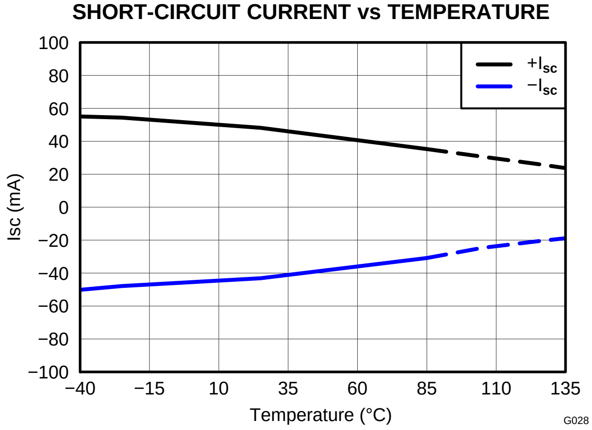

SHORT-CIRCUIT CURRENT vs TEMPERATURE

Figure 28.

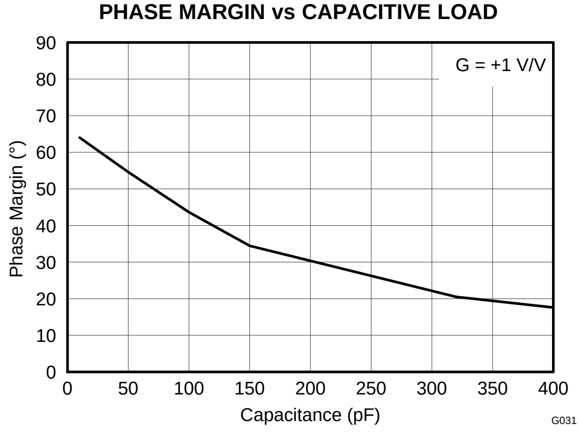

PHASE MARGIN vs CAPACITIVE LOAD

Figure 29.

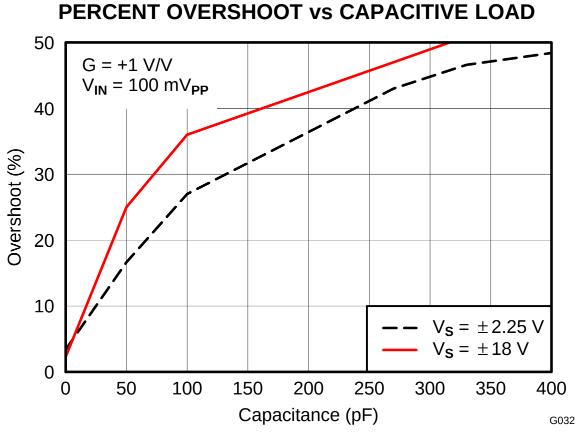

PERCENT OVERSHOOT vs CAPACITIVE LOAD

Figure 30.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = ±15 V, and R_L = 2 kΩ, unless otherwise noted.

NEGATIVE OVERLOAD RECOVERY

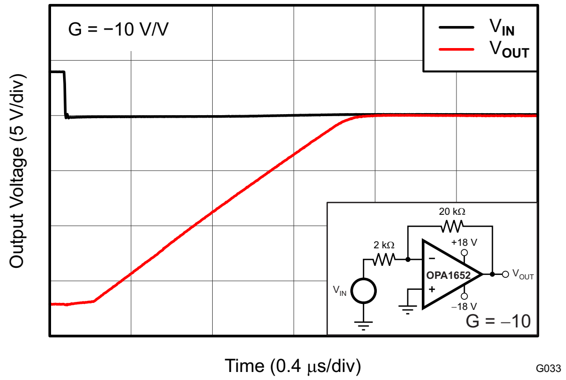


Figure 31.

POSITIVE OVERLOAD RECOVERY

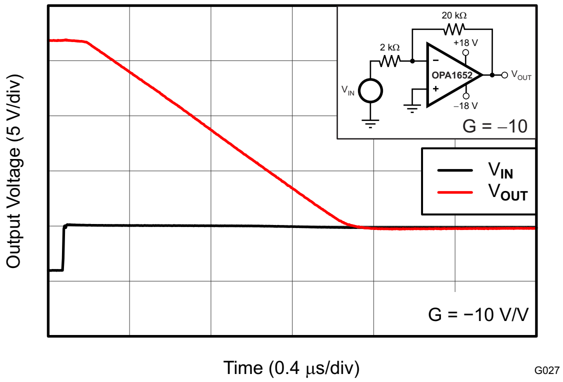


Figure 32.

OPEN-LOOP OUTPUT IMPEDANCE vs FREQUENCY

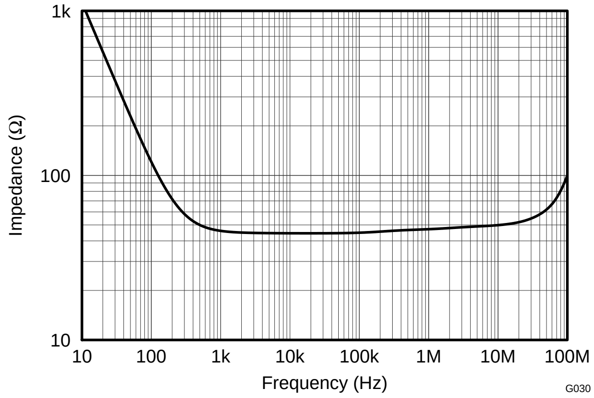


Figure 33.

NO PHASE REVERSAL

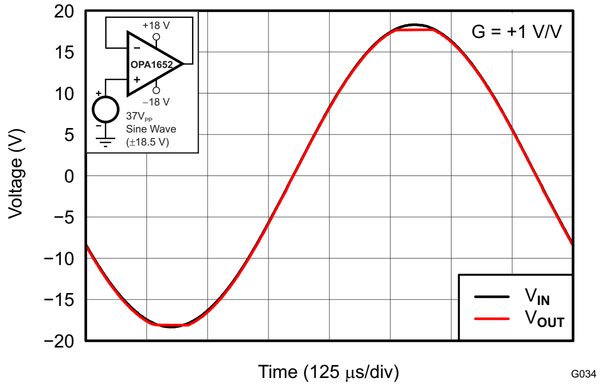


Figure 34.

APPLICATION INFORMATION

The OPA1652 and OPA1654 are unity-gain stable, precision dual and quad op amps with very low noise. Applications with noisy or high-impedance power supplies require decoupling capacitors close to the device pins. In most cases, 0.1-μF capacitors are adequate. Figure 35 shows a simplified schematic of the OPA165x (one channel shown).

OPERATING VOLTAGE

The OPA165x series op amps operate from ±2.25 V to ±18 V supplies while maintaining excellent performance. The OPA165x series can operate with as little as +4.5V between the supplies and with up to +36 V between the supplies. However, some applications do not require equal positive and negative output voltage swing. With the OPA165x series, power-supply voltages do not need to be equal. For example, the positive supply could be set to +25 V with the negative supply at –5 V.

In all cases, the common-mode voltage must be maintained within the specified range. In addition, key parameters are assured over the specified temperature range of T_A = –40°C to +85°C. Parameters that vary significantly with operating voltage or temperature are shown in the Typical Characteristics.

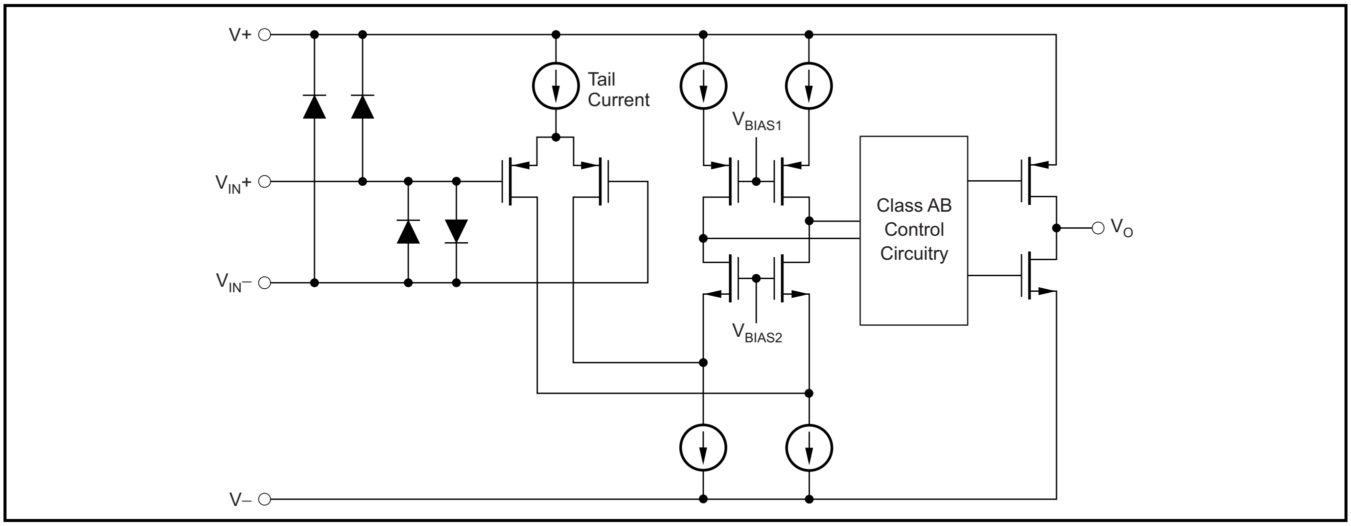


Figure 35. OPA165x Simplified Schematic

INPUT PROTECTION

The input terminals of the OPA1652 and OPA1654 are protected from excessive differential voltage with back-to-back diodes, as Figure 36 illustrates. In most circuit applications, the input protection circuitry has no consequence. However, in low-gain or G = +1 circuits, fast ramping input signals can forward bias these diodes because the output of the amplifier cannot respond rapidly enough to the input ramp. If the input signal is fast enough to create this forward bias condition, the input signal current must be limited to 10 mA or less. If the input signal current is not inherently limited, an input series resistor (R_I) and/or a feedback resistor (R_F) can be used to limit the signal input current. This resistor degrades the low-noise performance of the OPA165x and is examined in the following *Noise Performance* section. Figure 36 shows an example configuration when both current-limiting input and feeback resistors are used.

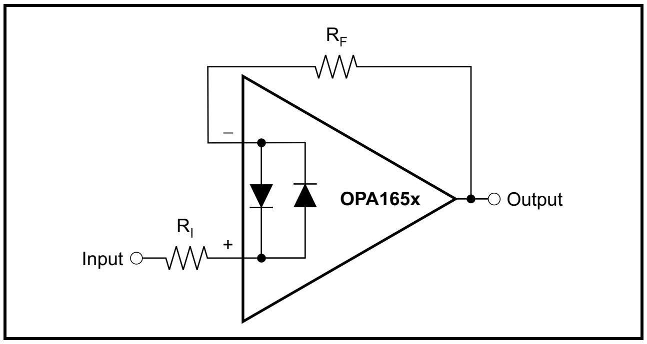


Figure 36. Pulsed Operation

NOISE PERFORMANCE

Figure 37 shows the total circuit noise for varying source impedances with the op amp in a unity-gain configuration (no feedback resistor network, and therefore no additional noise contributions).

The OPA165x (GBW = 18 MHz, G = +1) is shown with total circuit noise calculated. The op amp itself contributes both a voltage noise component and a current noise component. The voltage noise is commonly modeled as a time-varying component of the offset voltage. The current noise is modeled as the time-varying component of the input bias current and reacts with the source resistance to create a voltage component of noise. Therefore, the lowest noise op amp for a given application depends on the source impedance. For low source impedance, current noise is negligible, and voltage noise generally dominates. The voltage noise of the OPA165x series op amps makes them a better choice for source impedances greater than or equal to 1 kΩ.

The equation in Figure 37 shows the calculation of the total circuit noise, with these parameters:

- e_n = Voltage noise
- i_n = Current noise
- R_S = Source impedance
- k = Boltzmann's constant = 1.38×10^{-23} J/K
- T = Temperature in Kelvins (K)

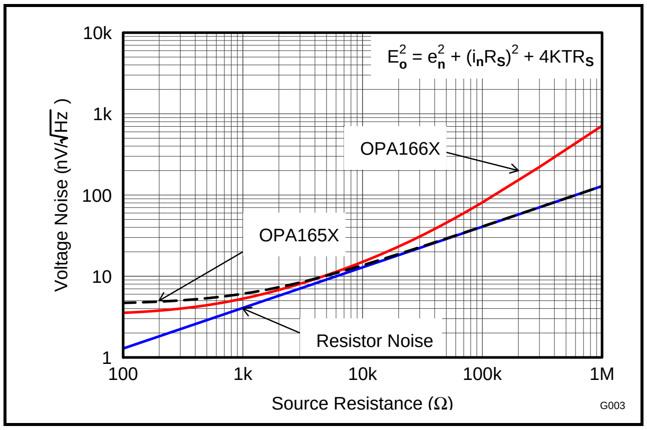


Figure 37. Noise Performance of the OPA165x in Unity-Gain Buffer Configuration

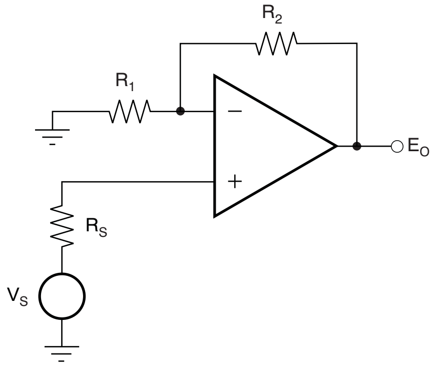
BASIC NOISE CALCULATIONS

Design of low-noise op amp circuits requires careful consideration of a variety of possible noise contributors: noise from the signal source, noise generated in the op amp, and noise from the feedback network resistors. The total noise of the circuit is the root-sum-square combination of all noise components.

The resistive portion of the source impedance produces thermal noise proportional to the square root of the resistance. Figure 37 plots this equation. The source impedance is usually fixed; consequently, select the op amp and the feedback resistors to minimize the respective contributions to the total noise.

Figure 38 illustrates both inverting and noninverting op amp circuit configurations with gain. In circuit configurations with gain, the feedback network resistors also contribute noise. The current noise of the op amp reacts with the feedback resistors to create additional noise components. The feedback resistor values can generally be chosen to make these noise sources negligible. The equations for total noise are shown for both configurations.

A) Noise in Noninverting Gain Configuration



Noise at the output:

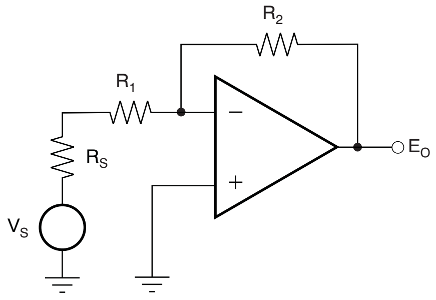
$$E_O^2 = \left[1 + \frac{R_2}{R_1}\right]^2 e_n^2 + \left[\frac{R_2}{R_1}\right]^2 e_1^2 + e_2^2 + \left[1 + \frac{R_2}{R_1}\right]^2 e_s^2$$

Where $e_S = \sqrt{4kTR_S}$ = thermal noise of R_S

$e_1 = \sqrt{4kTR_1}$ = thermal noise of R_1

$e_2 = \sqrt{4kTR_2}$ = thermal noise of R_2

B) Noise in Inverting Gain Configuration



Noise at the output:

$$E_O^2 = \left[1 + \frac{R_2}{R_1 + R_S}\right]^2 e_n^2 + \left[\frac{R_2}{R_1 + R_S}\right]^2 e_1^2 + e_2^2 + \left[\frac{R_2}{R_1 + R_S}\right]^2 e_s^2$$

Where $e_S = \sqrt{4kTR_S}$ = thermal noise of R_S

$e_1 = \sqrt{4kTR_1}$ = thermal noise of R_1

$e_2 = \sqrt{4kTR_2}$ = thermal noise of R_2

Note: For the OPA165x series of op amps at 1kHz, $e_n = 4.5\text{nV}/\sqrt{\text{Hz}}$.

Figure 38. Noise Calculation in Gain Configurations

TOTAL HARMONIC DISTORTION MEASUREMENTS

The OPA165x series op amps have excellent distortion characteristics. THD + noise is below 0.0002% (G = +1, V_O = 3 V_{RMS}, BW = 80 kHz) throughout the audio frequency range, 20 Hz to 20 kHz, with a 2-kΩ load (see Figure 7 for characteristic performance).

The distortion produced by the OPA165x series op amps is below the measurement limit of many commercially available distortion analyzers. However, a special test circuit (such as Figure 39 shows) can be used to extend the measurement capabilities.

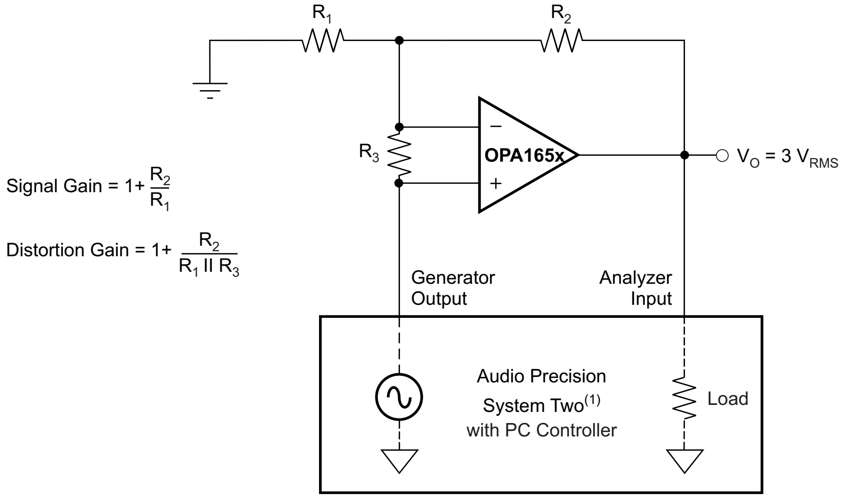
Op amp distortion can be considered an internal error source that can be referred to the input. Figure 39 shows a circuit that causes the op amp distortion to be gained up (refer to the table in Figure 39 for the distortion gain factor for various signal gains). The addition of R_3 to the otherwise standard noninverting amplifier configuration alters the feedback factor or noise gain of the circuit. The closed-loop gain is unchanged, but the feedback available for error correction is reduced by the distortion gain factor, thus extending the resolution by the same amount. Note that the input signal and load applied to the op amp are the same as with conventional feedback without R_3. The value of R_3 should be kept small to minimize its effect on the distortion measurements.

The validity of this technique can be verified by duplicating measurements at high gain and/or high frequency where the distortion is within the measurement capability of the test equipment. Measurements for this data sheet were made with an Audio Precision System Two distortion/noise analyzer, which greatly simplifies such repetitive measurements. The measurement technique can, however, be performed with manual distortion measurement instruments.

CAPACITIVE LOADS

The dynamic characteristics of the OPA1652 and OPA1654 have been optimized for commonly encountered gains, loads, and operating conditions. The combination of low closed-loop gain and high capacitive loads decreases the phase margin of the amplifier and can lead to gain peaking or oscillations. As a result, heavier capacitive loads must be isolated from the output. The simplest way to achieve this isolation is to add a small resistor (R_S equal to 50 Ω, for example) in series with the output.

This small series resistor also prevents excess power dissipation if the output of the device becomes shorted. Figure 19 illustrates a graph of *Small-Signal Overshoot vs Capacitive Load* for several values of R_S. Also, refer to Applications Bulletin AB-028 (literature number SBOA015, available for download from the TI web site) for details of analysis techniques and application circuits.



SIGNAL GAIN	DISTORTION GAIN	R_1	R_2	R_3
+1	101	∞	1 kΩ	10 Ω
–1	101	4.99 kΩ	4.99 kΩ	49.9 Ω
+10	110	549 Ω	4.99 kΩ	49.9 Ω

(1) For measurement bandwidth, see Figure 7 through Figure 12.

Figure 39. Distortion Test Circuit

POWER DISSIPATION

The OPA1652 and OPA1654 series op amps are capable of driving 2-kΩ loads with a power-supply voltage up to ±18V and full operating temperature range. Internal power dissipation increases when operating at high supply voltages. Copper leadframe construction used in the OPA165x series op amps improves heat dissipation compared to conventional materials. Circuit board layout can also help minimize junction temperature rise. Wide copper traces help dissipate the heat by acting as an additional heat sink. Temperature rise can be further minimized by soldering the devices to the circuit board rather than using a socket.

ELECTRICAL OVERSTRESS

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

These ESD protection diodes also provide in-circuit, input overdrive protection, as long as the current is limited to 10 mA as stated in the Absolute Maximum Ratings. Figure 40 shows how a series input resistor may be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and its value should be kept to a minimum in noise-sensitive applications.

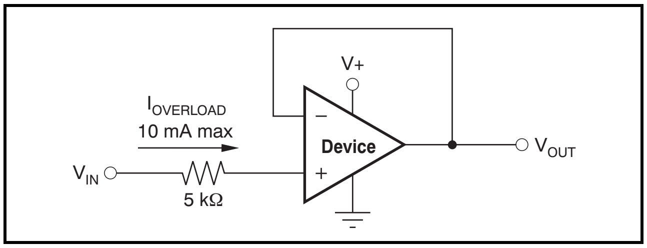


Figure 40. Input Current Protection

An ESD event produces a short duration, high-voltage pulse that is transformed into a short duration, high-current pulse as it discharges through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent it from being damaged. The energy absorbed by the protection circuitry is then dissipated as heat.

When the operational amplifier connects into a circuit, the ESD protection components are intended to remain inactive and not become involved in the application circuit operation. However, circumstances may arise where an applied voltage exceeds the operating voltage range of a given pin. Should this condition occur, there is a risk that some of the internal ESD protection circuits may be biased on, and conduct current. Any such current flow occurs through ESD cells and rarely involves the absorption device.

If there is an uncertainty about the ability of the supply to absorb this current, external zener diodes may be added to the supply pins. The zener voltage must be selected such that the diode does not turn on during normal operation.

However, its zener voltage should be low enough so that the zener diode conducts if the supply pin begins to rise above the safe operating supply voltage level.

APPLICATION CIRCUIT

An additional application idea is shown in Figure 41.

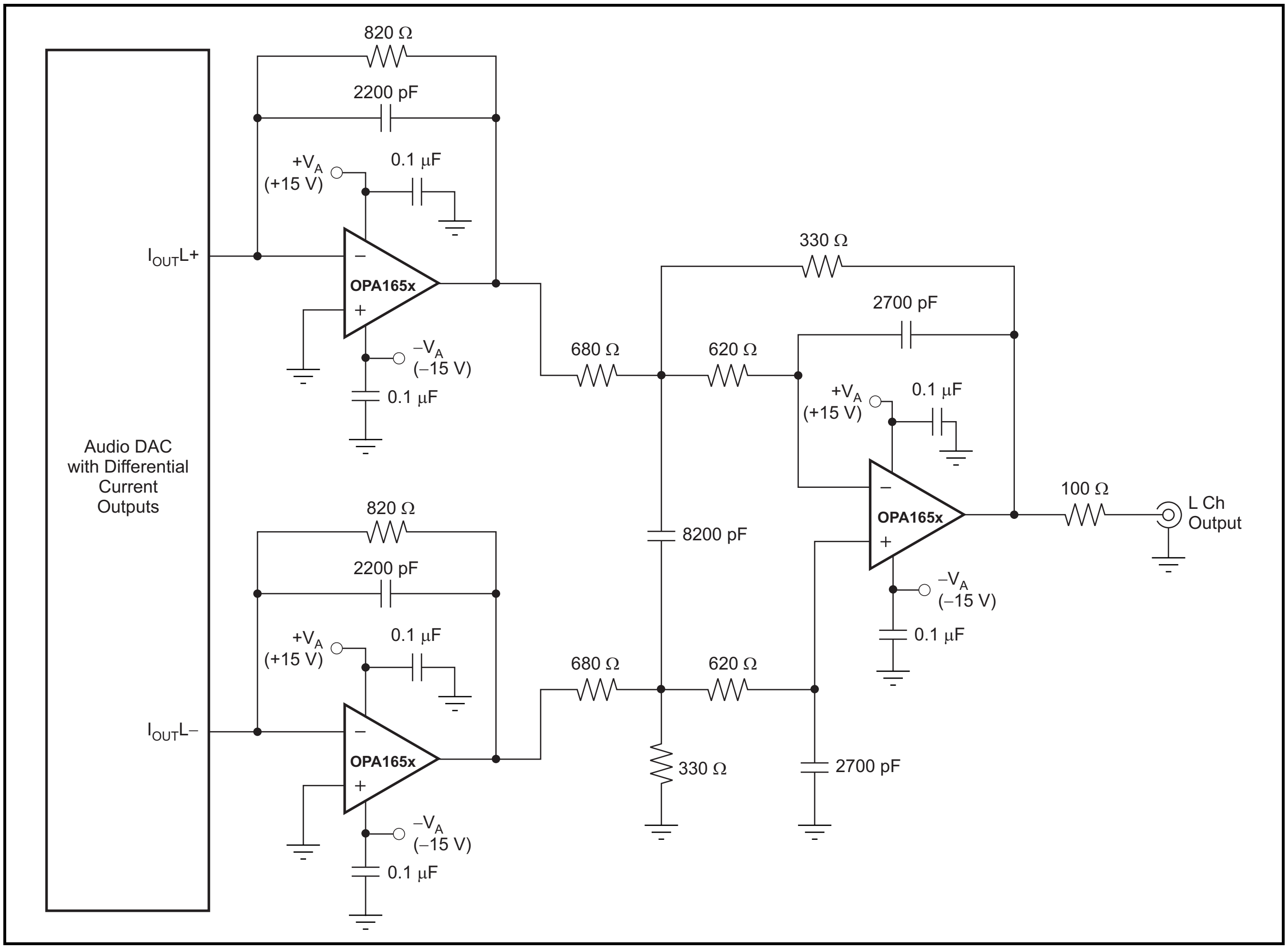


Figure 41. Audio DAC I/V Converter and Output Filter

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
OPA1652AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OP1652	Samples
OPA1652AIDGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	OUPI	Samples
OPA1652AIDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	OUPI	Samples
OPA1652AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OP1652	Samples
OPA1654AID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA1654	Samples
OPA1654AIDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA1654	Samples
OPA1654AIPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA1654	Samples
OPA1654AIPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA1654	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

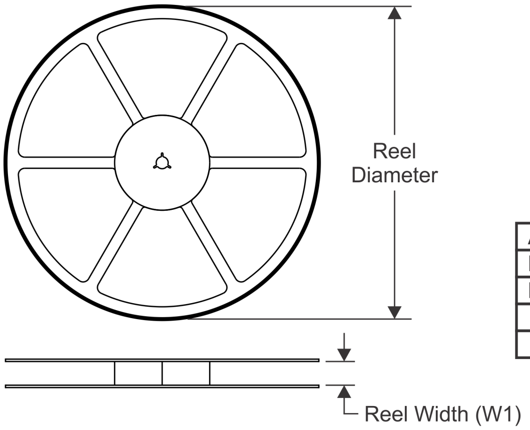
[4] Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

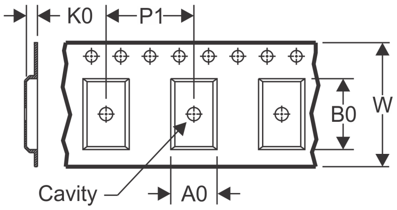
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

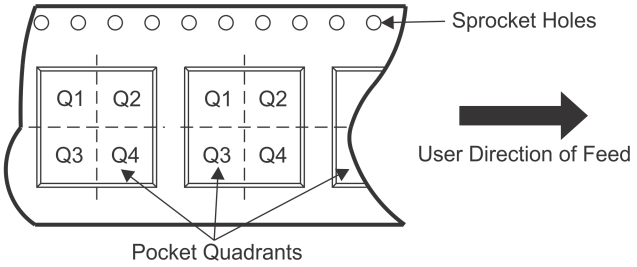


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

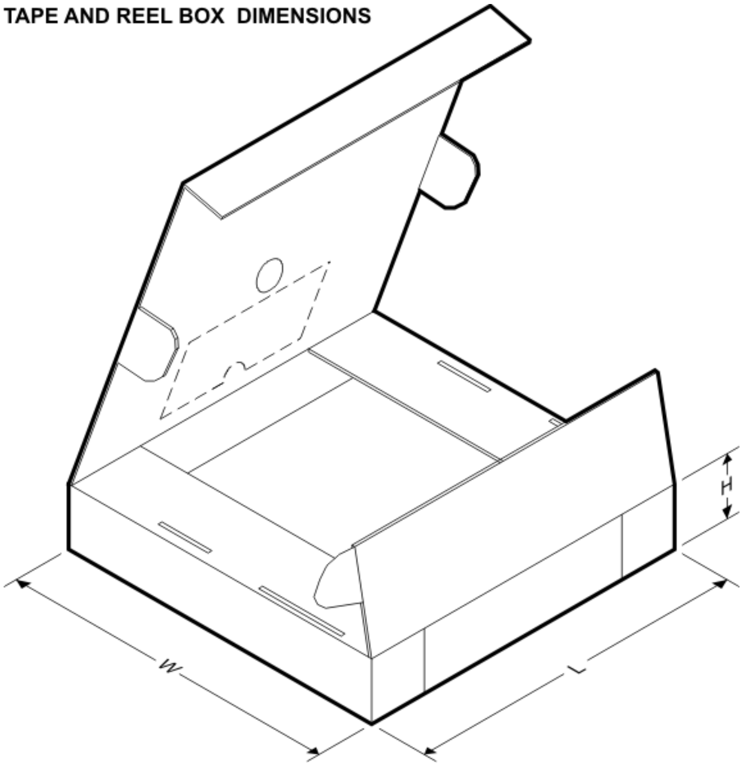
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA1652AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA1652AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA1654AIDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
OPA1654AIPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

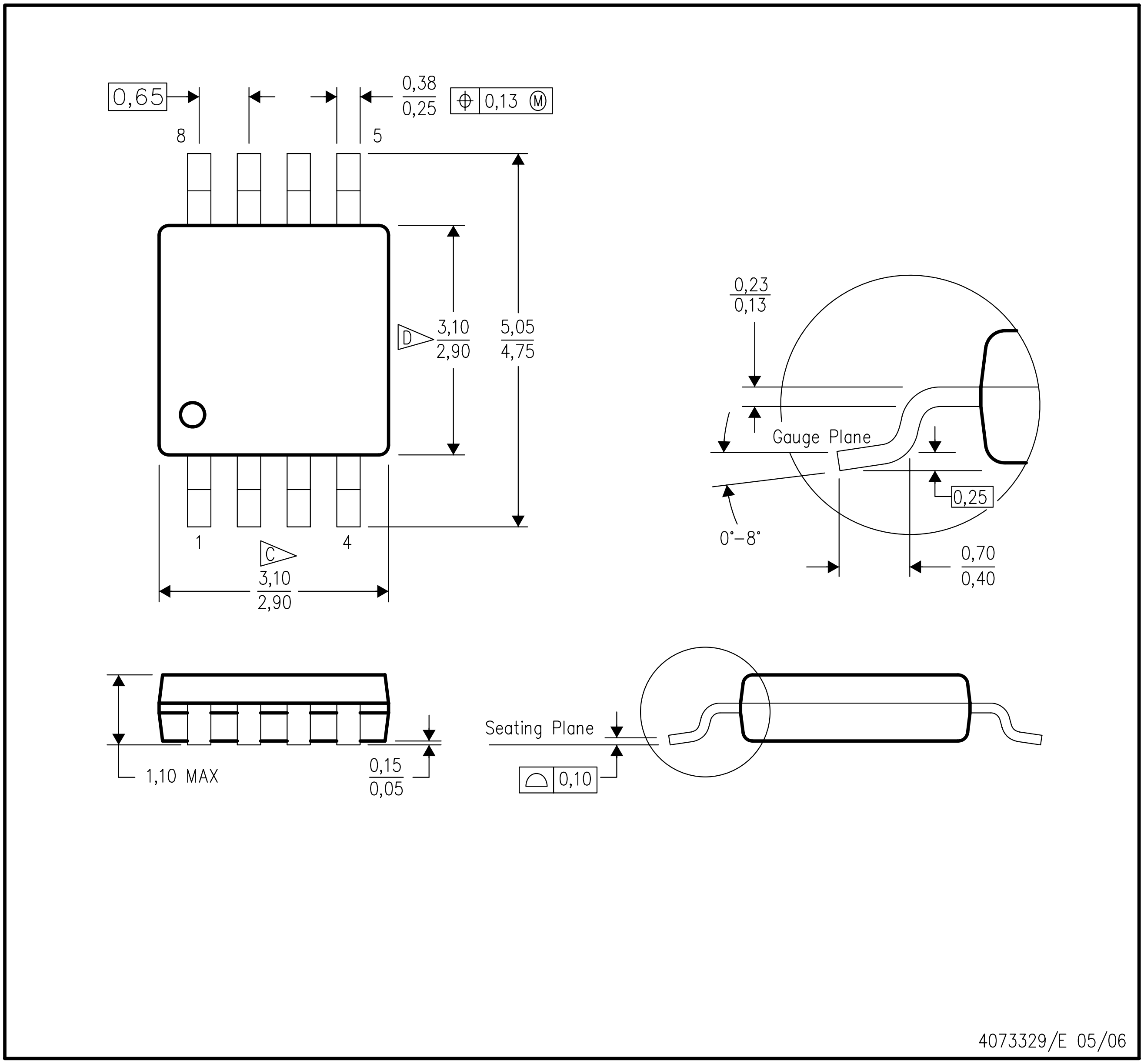
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA1652AIDGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0
OPA1652AIDR	SOIC	D	8	2500	367.0	367.0	35.0
OPA1654AIDR	SOIC	D	14	2500	367.0	367.0	38.0
OPA1654AIPWR	TSSOP	PW	14	2000	367.0	367.0	35.0

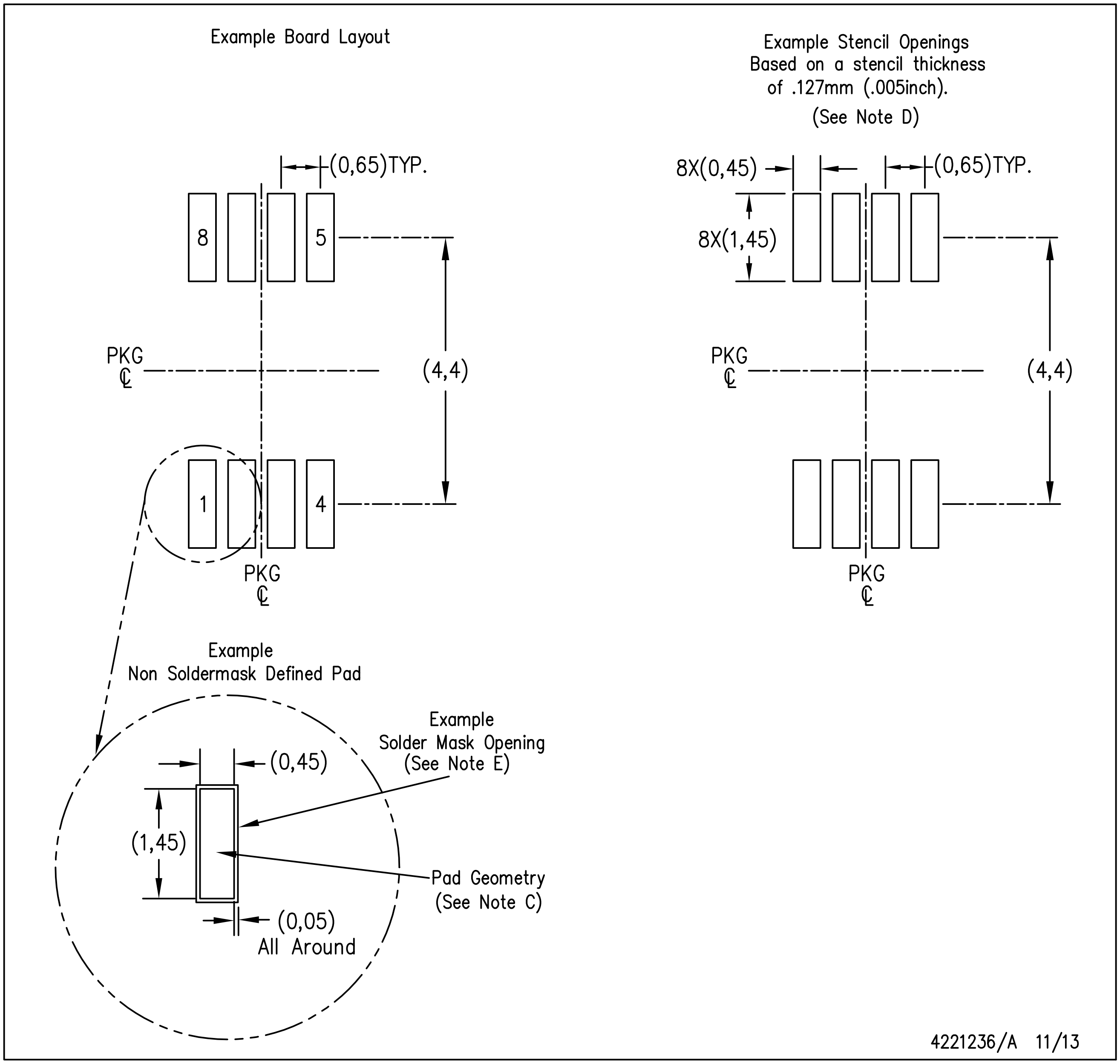
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

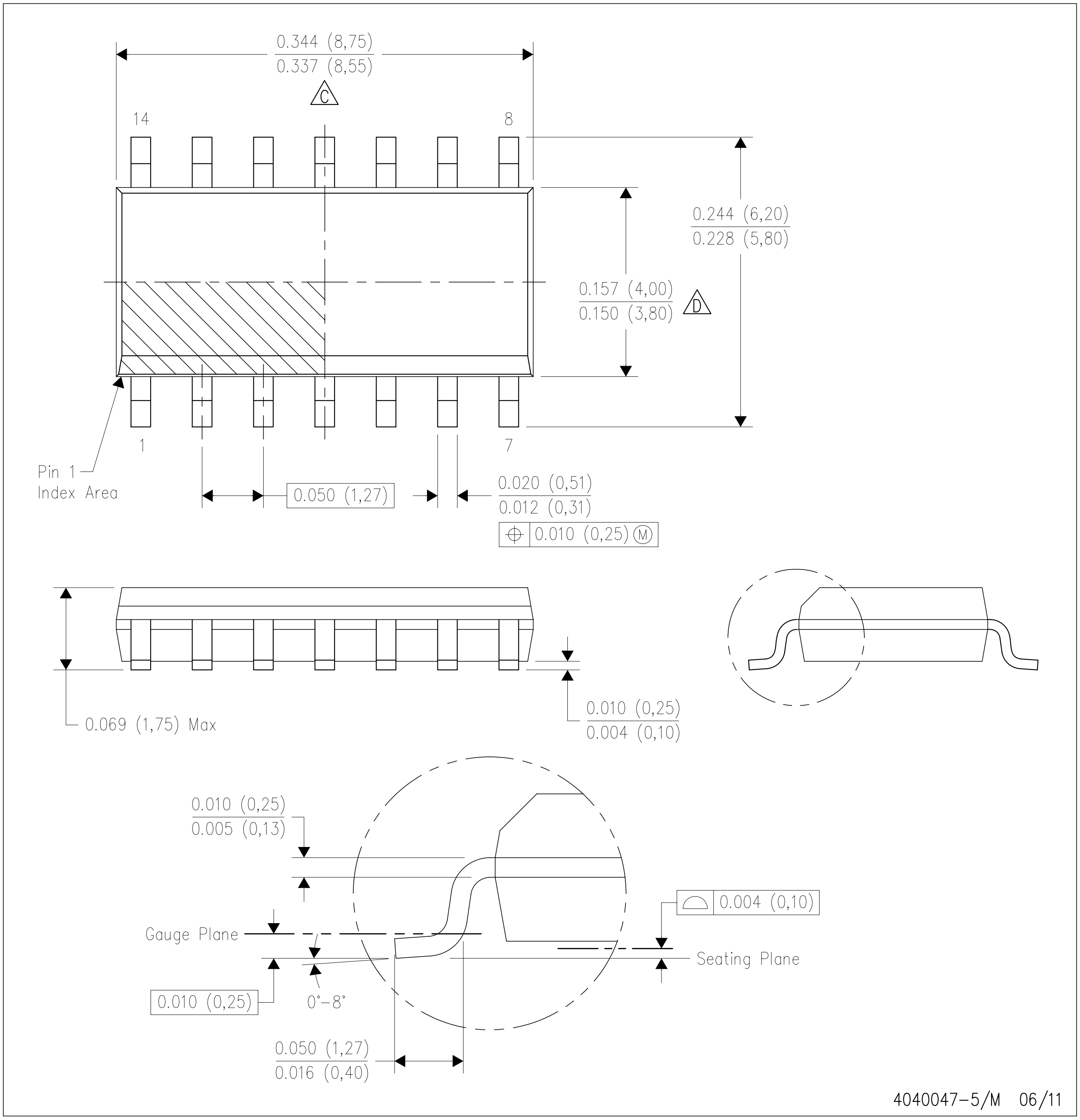
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



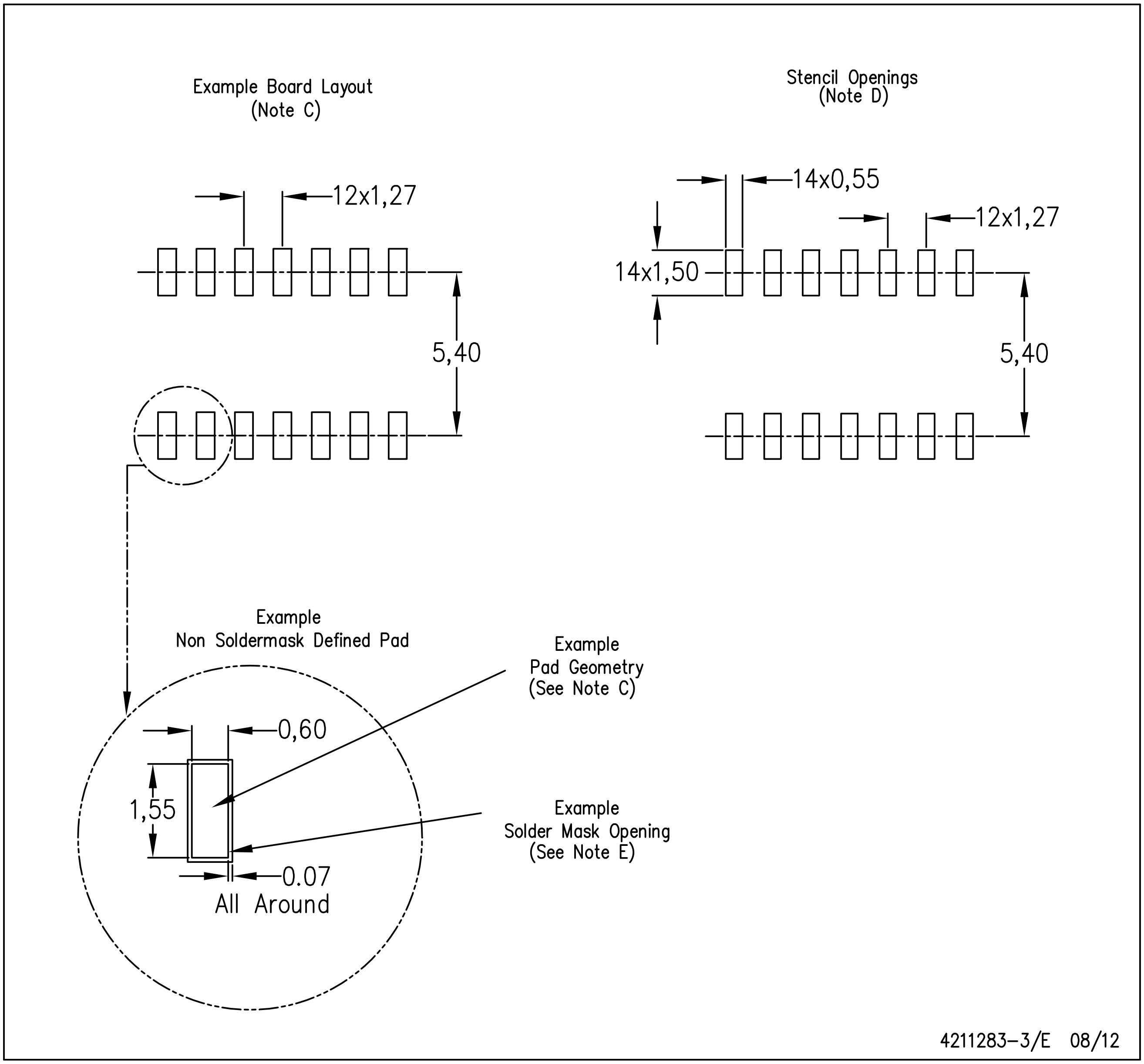
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



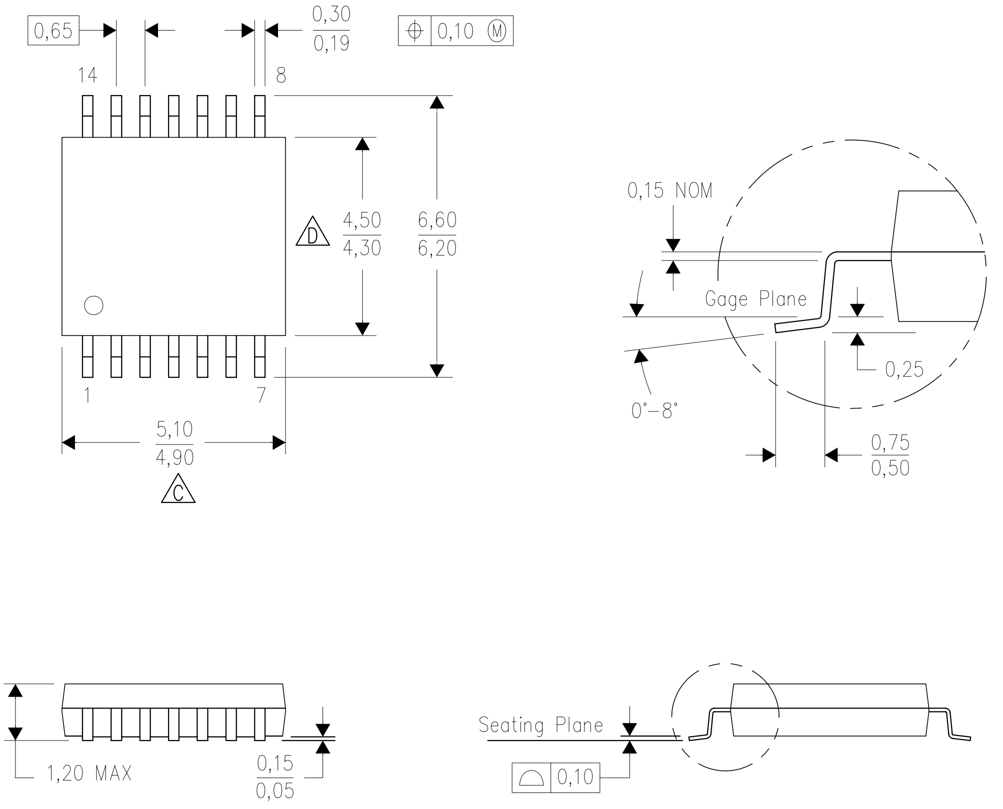
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS–012 variation AB.

D (R-PDSO-G14) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

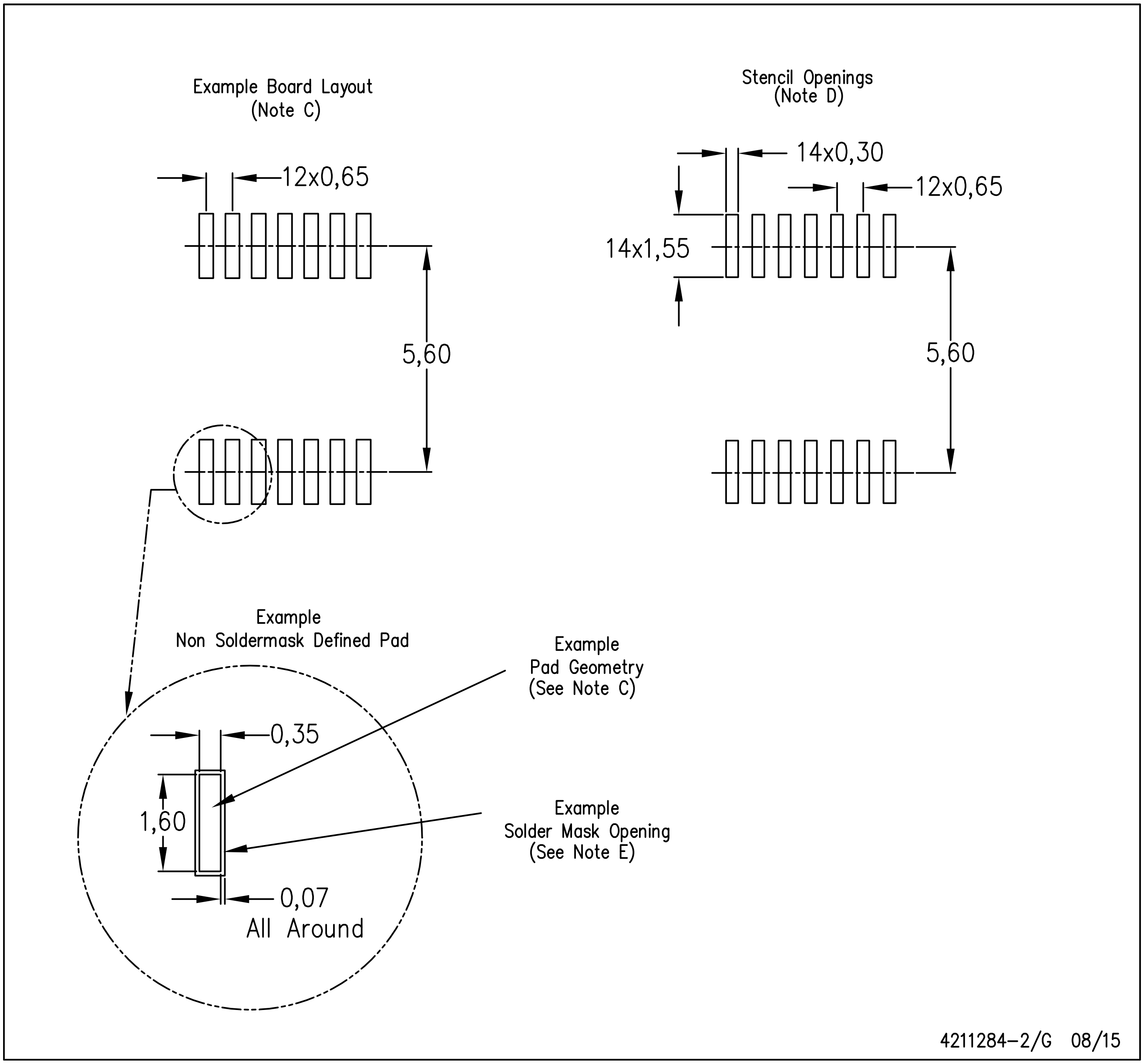
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

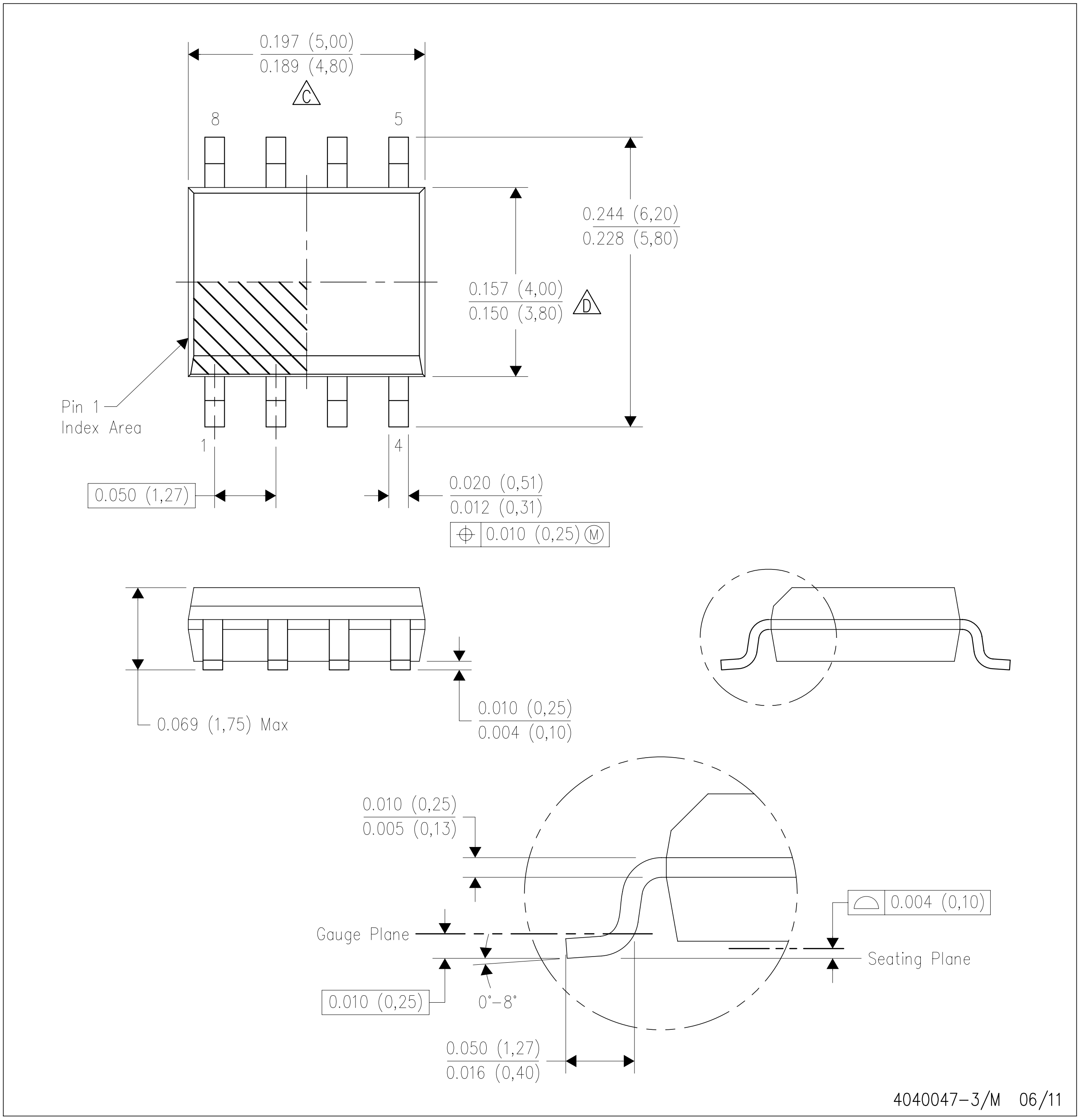
NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- D Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



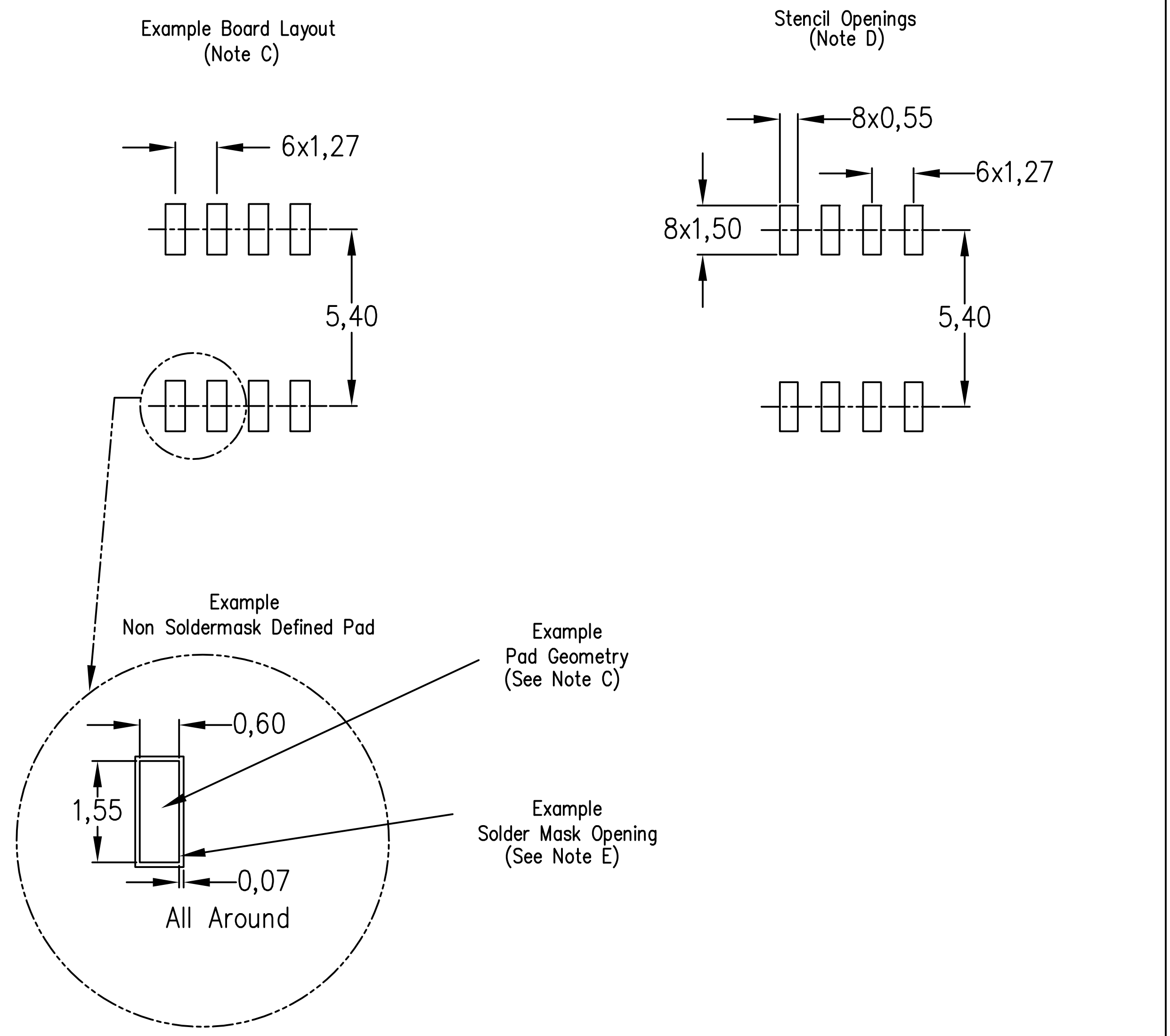
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R-PDSO-G8) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



4211283–2/E 08/12

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265