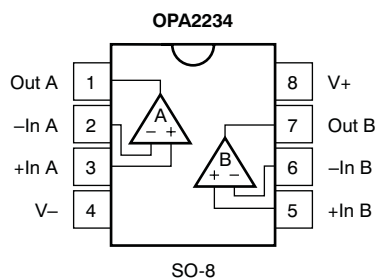


LOW-POWER, PRECISION SINGLE-SUPPLY OPERATIONAL AMPLIFIERS

Check for Samples: [OPA2234M](#)

FEATURES

- **Wide Supply Range:**
 - **Single Supply:** $V_S = 2.7\text{ V to }36\text{ V}$
 - **Dual Supply:** $V_S = \pm 1.35\text{ V to } \pm 18\text{ V}$
- **Specified Performance:**
 - **2.7 V, 5 V, and $\pm 15\text{ V}$**
- **Low Quiescent Current: 250 $\mu\text{A}/\text{amp}$**
- **Low Input Bias Current: 35 nA Max**
- **Low Offset Voltage: 100 μV Typ**
- **High CMRR, PSRR, and A_{OL}**
- **Dual Versions**



DESCRIPTION

The OPA2234 series low-cost op amps are ideal for single-supply, low-voltage, low-power applications. The series provides lower quiescent current than older “1013”-type products and comes in current industry-standard packages and pinouts. The combination of low offset voltage, high common-mode rejection, high power-supply rejection, and a wide supply range provides excellent accuracy and versatility. Dual versions have identical specifications for maximum design flexibility. These general-purpose op amps are ideal for portable and battery-powered applications.

The OPA2234 series op amps operate from either single or dual supplies. In single-supply operation, the input common-mode range extends below ground and the output can swing to within 50mV of ground. Excellent phase margin makes the OPA2234 series ideal for demanding applications, including high load capacitance. Dual design features completely independent circuitry for lowest crosstalk and freedom from interaction.

Single and dual packages are in an SO-8 surface-mount and are specified for -55°C to 125°C operation.

ORDERING INFORMATION⁽¹⁾

PRODUCT	PACKAGE	PACKAGE MARKING
OPA2234MDR	SO-8 Surface-Mount	2234M

(1) For the most current package and ordering information, see the Package Option Addendum located at the end of this data sheet.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT
Supply Voltage, V+ to V–			
Input Voltage		(V–) – 0.7 to (V+) + 0.7	V
Output Short-Circuit ⁽¹⁾		Continuous	
Operating Temperature		–55 to 125	°C
Storage Temperature		–55 to 125	°C
Junction Temperature	T _{JA}	150	°C/W
	T _{JC}	39	
Lead Temperature (soldering, 10 s)		300	°C

(1) Short-circuit to ground, one amplifier per package.

ELECTRICAL CHARACTERISTICS: $V_S = 5\text{ V}$

At $T_A = -55^\circ\text{C}$ to 125°C , $V_S = 5\text{ V}$, $R_L = 10\text{ k}\Omega$ connected to $V_S/2$, and $V_{OUT} = V_S/2$, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
OFFSET VOLTAGE						
Input Offset Voltage	V_{OS}	$T_A = 25^\circ\text{C}$, $V_{CM} = 2.5\text{ V}$		± 40	± 100	μV
		$V_{CM} = 2.5\text{ V}$			± 600	
vs Temperature ⁽¹⁾	dV_{OS}/dT	Operating Temperature Range		± 3		$\mu\text{V}/^\circ\text{C}$
vs Power Supply	PSRR	$V_S = 2.7\text{ V}$ to 30 V , $V_{CM} = 1.7\text{ V}$		3	20	$\mu\text{V}/\text{V}$
vs Time				0.2		$\mu\text{V}/\text{mo}$
Channel Separation (Dual)				0.3		$\mu\text{V}/\text{V}$
INPUT BIAS CURRENT						
Input Bias Current ⁽²⁾	I_B	$V_{CM} = 2.5\text{ V}$		-15	-35	nA
Input Offset Current	I_{OS}	$V_{CM} = 2.5\text{ V}$		± 1	± 12	nA
NOISE						
		$f = 1\text{ kHz}$				
Input Voltage Noise Density	V_n			25		$\text{nV}/\sqrt{\text{Hz}}$
Current Noise Density	I_n			80		$\text{fA}/\sqrt{\text{Hz}}$
INPUT VOLTAGE RANGE						
Common-Mode Voltage Range				0.5	$(V+) - 1$	V
Common-Mode Rejection	CMRR	$V_{CM} = 0.5\text{ V}$ to 4 V		86	106	dB
INPUT IMPEDANCE						
Differential				$10^7 \parallel 5$		$\Omega \parallel \text{pF}$
Common-Mode		$V_{CM} = 2.5\text{ V}$		$10^{10} \parallel 6$		$\Omega \parallel \text{pF}$
OPEN-LOOP GAIN						
Open-Loop Voltage Gain	A_{OL}	$R_L = 10\text{ k}\Omega$, $V_O = 0.25\text{ V}$ to 4 V		78	120	dB
		$R_L = 2\text{ k}\Omega$, $V_O = 0.5\text{ V}$ to 4 V		75	96	dB
FREQUENCY RESPONSE						
Gain-Bandwidth Product	GBW	$C_L = 100\text{ pF}$		0.35		MHz
Slew Rate	SR			0.2		$\text{V}/\mu\text{s}$
Settling Time:						
0.1%		$G = 1$, 3 V Step , $C_L = 100\text{ pF}$		15		μs
0.01%		$G = 1$, 3 V Step , $C_L = 100\text{ pF}$		25		μs
Overload Recovery Time		(V_{IN}) (Gain) = V_S		16		μs
OUTPUT						
Voltage Output:						
Positive		$R_L = 10\text{ k}\Omega$ to $V_S/2$		$(V+) - 1$	$(V+) - 0.65$	V
Negative		$R_L = 10\text{ k}\Omega$ to $V_S/2$		0.25	0.05	V
Positive		$R_L = 10\text{ k}\Omega$ to Ground		$(V+) - 1$	$(V+) - 0.65$	V
Negative		$R_L = 10\text{ k}\Omega$ to Ground		0.1	0.05	V
Short-Circuit Current	I_{SC}			± 11		mA
Capacitive Load Drive (Stable Operation) ⁽³⁾		$G = 1$		1000		pF
POWER SUPPLY						
Specified Operating Voltage				5		V
Operating Voltage Range				2.7	36	V
Quiescent Current (per amplifier)	I_Q	$I_O = 0$		250	550	μA

(1) Wafer-level tested to 95% confidence level.

(2) Positive conventional current flows into the input terminals.

(3) See *Small-Signal Overshoot vs Load Capacitance* typical curve.

ELECTRICAL CHARACTERISTICS: $V_S = 5\text{ V}$ (continued)

At $T_A = -55^\circ\text{C}$ to 125°C , $V_S = 5\text{ V}$, $R_L = 10\text{ k}\Omega$ connected to $V_S/2$, and $V_{OUT} = V_S/2$, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
TEMPERATURE RANGE					
Specified Range		-55		125	$^\circ\text{C}$
Operating Range		-55		125	$^\circ\text{C}$
Storage		-55		125	$^\circ\text{C}$
Thermal Resistance θ_{JA}			150		$^\circ\text{C}/\text{W}$

ELECTRICAL CHARACTERISTICS: $V_S = 2.7\text{ V}$

At $T_A = -55^\circ\text{C}$ to 125°C , $V_S = 2.7\text{ V}$, $R_L = 10\text{ k}\Omega$ connected to $V_S/2$, and $V_{OUT} = V_S/2$, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
Input Offset Voltage	V_{OS}	$T_A = 25^\circ\text{C}$, $V_{CM} = 1.35\text{ V}$		± 40	± 100	μV
		$V_{CM} = 1.35\text{ V}$			± 600	
vs Temperature ⁽¹⁾	dV_{OS}/dT	Operating Temperature Range		± 3		$\mu\text{V}/^\circ\text{C}$
vs Power Supply	PSRR	$V_S = 2.7\text{ V}$ to 30 V , $V_{CM} = 1.7\text{ V}$		3	20	$\mu\text{V}/\text{V}$
vs Time				0.2		$\mu\text{V}/\text{mo}$
Channel Separation (Dual)				0.3		$\mu\text{V}/\text{V}$
INPUT BIAS CURRENT						
Input Bias Current ⁽²⁾	I_B	$V_{CM} = 1.35\text{ V}$		-15	-35	nA
Input Offset Current	I_{OS}	$V_{CM} = 1.35\text{ V}$		± 1	± 12	nA
NOISE						
		$f = 1\text{ kHz}$				
Input Voltage Noise Density	V_n			25		$\text{nV}/\sqrt{\text{Hz}}$
Current Noise Density	I_n			80		$\text{fA}/\sqrt{\text{Hz}}$
INPUT VOLTAGE RANGE						
Common-Mode Voltage Range			0.5		$(V+) - 1.1$	V
Common-Mode Rejection	CMRR	$V_{CM} = 0.5\text{ V}$ to 1.6 V	86	106		dB
INPUT IMPEDANCE						
Differential				$10^7 \parallel 5$		$\Omega \parallel \text{pF}$
Common-Mode		$V_{CM} = 1.35\text{ V}$		$10^{10} \parallel 6$		$\Omega \parallel \text{pF}$
OPEN-LOOP GAIN						
Open-Loop Voltage Gain	A_{OL}	$R_L = 10\text{ k}\Omega$, $V_O = 0.25\text{ V}$ to 1.7 V	78	125		dB
		$R_L = 2\text{ k}\Omega$, $V_O = 0.5\text{ V}$ to 1.7 V	69	96		dB
FREQUENCY RESPONSE						
Gain-Bandwidth Product	GBW	$C_L = 100\text{ pF}$		0.35		MHz
Slew Rate	SR			0.2		$\text{V}/\mu\text{s}$
Settling Time:						
0.1%		$G = 1$, 1 V Step, $C_L = 100\text{ pF}$		6		μs
0.01%		$G = 1$, 1 V Step, $C_L = 100\text{ pF}$		16		μs
Overload Recovery Time		(V_{IN}) (Gain) = V_S		8		μs
OUTPUT						
Voltage Output:						
Positive		$R_L = 10\text{ k}\Omega$ to $V_S/2$	$(V+) - 1$	$(V+) - 0.6$		V
Negative		$R_L = 10\text{ k}\Omega$ to $V_S/2$	0.25	0.05		V
Positive		$R_L = 10\text{ k}\Omega$ to Ground	$(V+) - 1$	$(V+) - 0.65$		V
Negative		$R_L = 10\text{ k}\Omega$ to Ground	0.1	0.05		V
Short-Circuit Current	I_{SC}			± 8		mA
Capacitive Load Drive (Stable Operation) ⁽³⁾		$G = 1$		1000		pF
POWER SUPPLY						
Specified Operating Voltage				2.7		V
Operating Voltage Range			2.7		36	V
Quiescent Current (per amplifier)	I_Q	$I_O = 0$		250	550	μA

(1) Wafer-level tested to 95% confidence level.

(2) Positive conventional current flows into the input terminals.

(3) See *Small-Signal Overshoot vs Load Capacitance* typical curve.

ELECTRICAL CHARACTERISTICS: $V_S = 2.7\text{ V}$ (continued)

At $T_A = -55^\circ\text{C}$ to 125°C , $V_S = 2.7\text{ V}$, $R_L = 10\text{ k}\Omega$ connected to $V_S/2$, and $V_{OUT} = V_S/2$, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
TEMPERATURE RANGE					
Specified Range		-55		125	$^\circ\text{C}$
Operating Range		-55		125	$^\circ\text{C}$
Storage		-55		125	$^\circ\text{C}$
Thermal Resistance	θ_{JA}		150		$^\circ\text{C/W}$

ELECTRICAL CHARACTERISTICS: $V_S = \pm 15\text{ V}$

At $T_A = -55^\circ\text{C}$ to 125°C , $V_S = \pm 15\text{ V}$, $R_L = 10\text{ k}\Omega$ connected to $V_S/2$, and $V_{OUT} = V_S/2$, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
Input Offset Voltage	V_{OS}	$T_A = 25^\circ\text{C}$, $V_{CM} = 0\text{ V}$		± 70	± 250	μV
		$V_{CM} = 0\text{ V}$			± 750	
vs Temperature ⁽¹⁾	dV_{OS}/dT	Operating Temperature Range		± 3		$\mu\text{V}/^\circ\text{C}$
vs Power Supply	PSRR	$V_S = \pm 1.35\text{ V}$ to $\pm 18\text{ V}$, $V_{CM} = 0\text{ V}$		3	20	$\mu\text{V}/\text{V}$
vs Time				0.2		$\mu\text{V}/\text{mo}$
Channel Separation (Dual)				0.3		$\mu\text{V}/\text{V}$
INPUT BIAS CURRENT						
Input Bias Current ⁽²⁾	I_B	$V_{CM} = 0\text{ V}$		-12	-30	nA
Input Offset Current	I_{OS}	$V_{CM} = 0\text{ V}$		± 1	± 12	nA
NOISE						
		$f = 1\text{ kHz}$				
Input Voltage Noise Density	V_n			25		$\text{nV}/\sqrt{\text{Hz}}$
Current Noise Density	I_n			80		$\text{fA}/\sqrt{\text{Hz}}$
INPUT VOLTAGE RANGE						
Common-Mode Voltage Range			$(V_-) + 1$		$(V_+) - 1$	V
Common-Mode Rejection	CMRR	$V_{CM} = -14\text{ V}$ to 14 V	86	106		dB
INPUT IMPEDANCE						
Differential				$10^7 \parallel 5$		$\Omega \parallel \text{pF}$
Common-Mode		$V_{CM} = 0\text{ V}$		$10^{10} \parallel 6$		$\Omega \parallel \text{pF}$
OPEN-LOOP GAIN						
Open-Loop Voltage Gain	A_{OL}	$V_O = -13.5\text{ V}$ to 13 V	87	120		dB
FREQUENCY RESPONSE						
Gain-Bandwidth Product	GBW	$C_L = 100\text{ pF}$		0.35		MHz
Slew Rate	SR			0.2		$\text{V}/\mu\text{s}$
Settling Time:						
0.1%		$G = 1$, 10 V Step, $C_L = 100\text{ pF}$		41		μs
0.01%		$G = 1$, 10 V Step, $C_L = 100\text{ pF}$		47		μs
Overload Recovery Time		(V_{IN}) (Gain) = V_S		22		μs
OUTPUT						
Voltage Output:						
Positive			$(V_+) - 2$	$(V_+) - 0.7$		V
Negative			$(V_-) + 1.5$	$(V_-) + 0.15$		V
Short-Circuit Current	I_{SC}			± 22		mA
Capacitive Load Drive (Stable Operation) ⁽³⁾		$G = 1$		1000		pF
POWER SUPPLY						
Specified Operating Voltage				± 15		V
Operating Voltage Range			± 1.35		± 18	V
Quiescent Current (per amplifier)	I_Q	$I_O = 0$		± 275	± 550	μA

(1) Wafer-level tested to 95% confidence level.

(2) Positive conventional current flows into the input terminals.

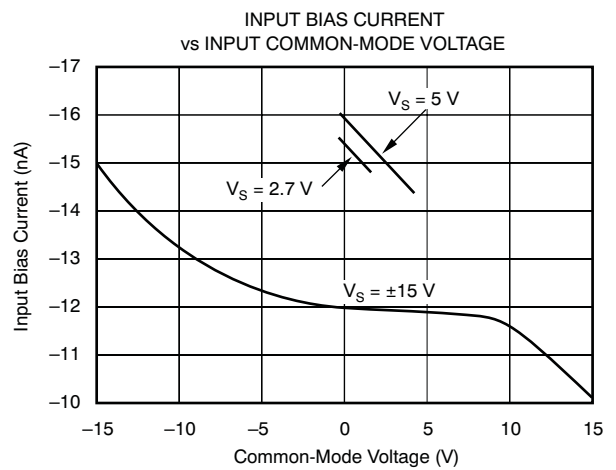
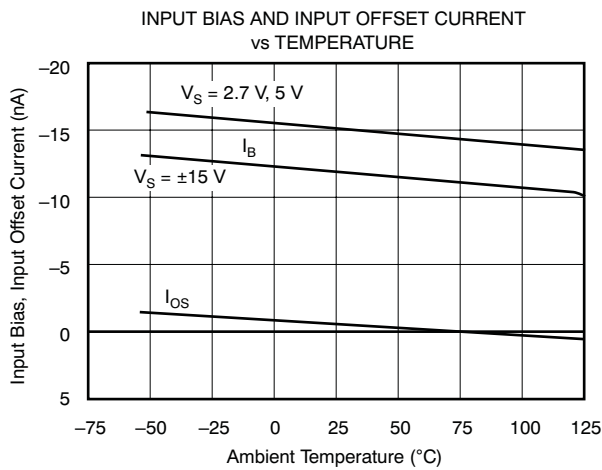
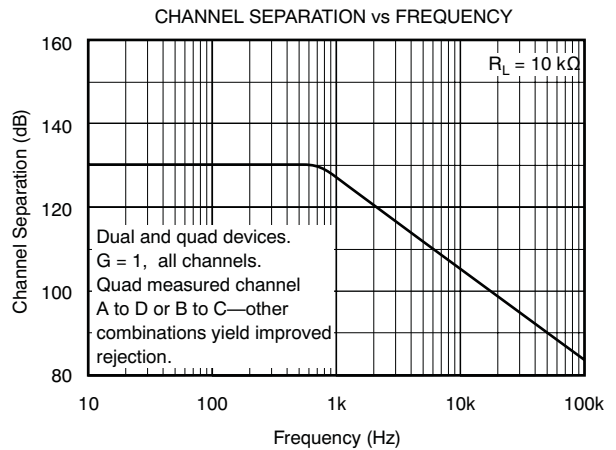
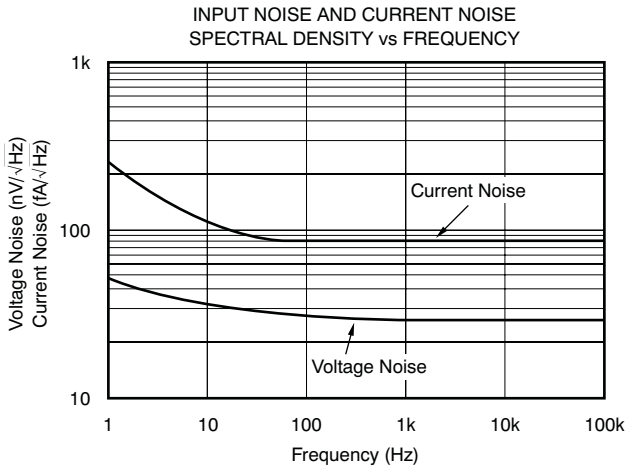
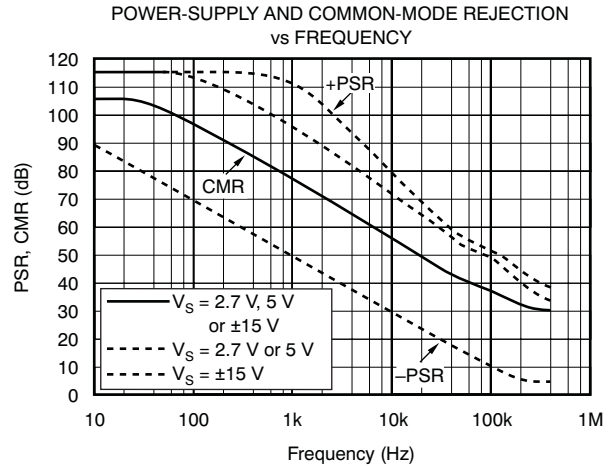
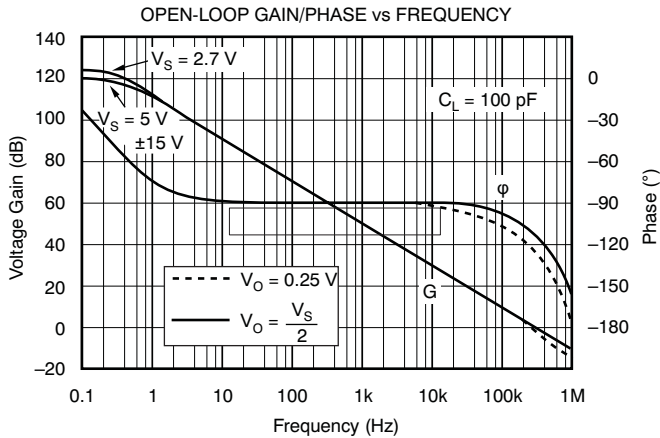
(3) See *Small-Signal Overshoot vs Load Capacitance* typical curve.

ELECTRICAL CHARACTERISTICS: $V_S = \pm 15\text{ V}$ (continued)

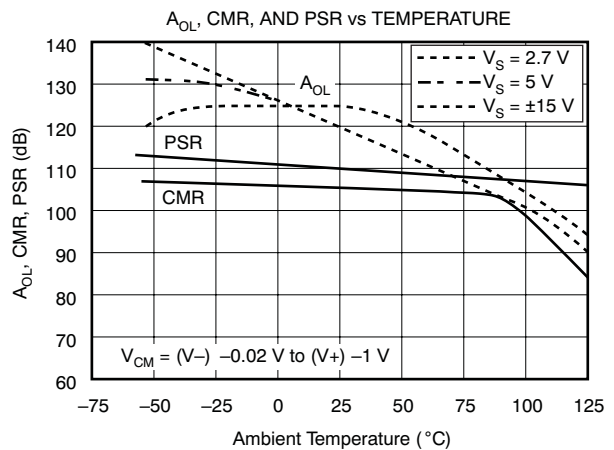
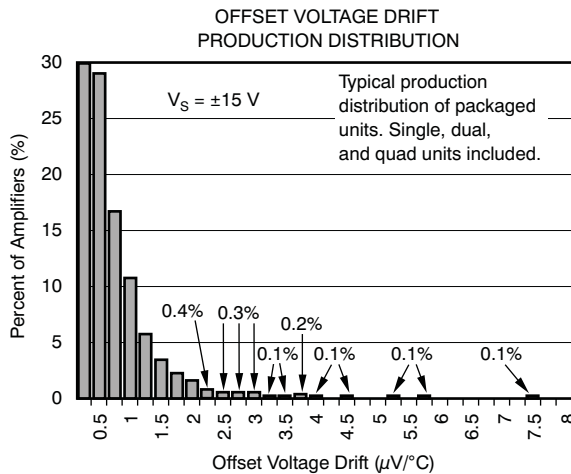
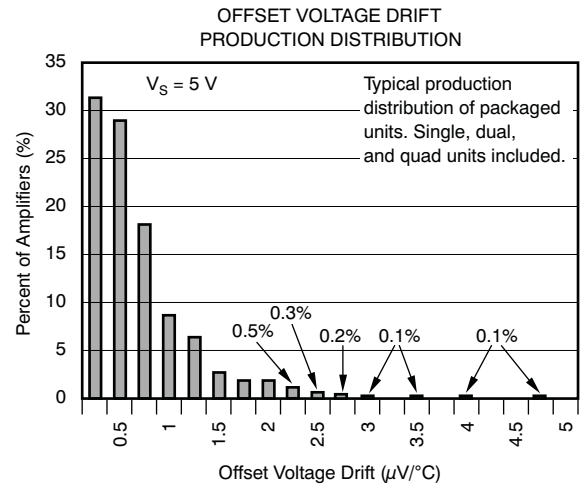
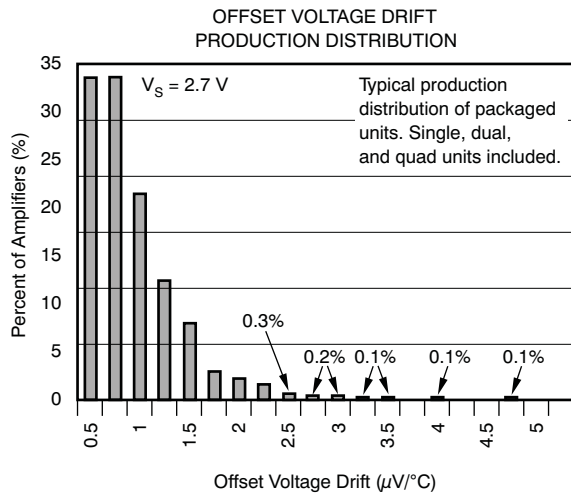
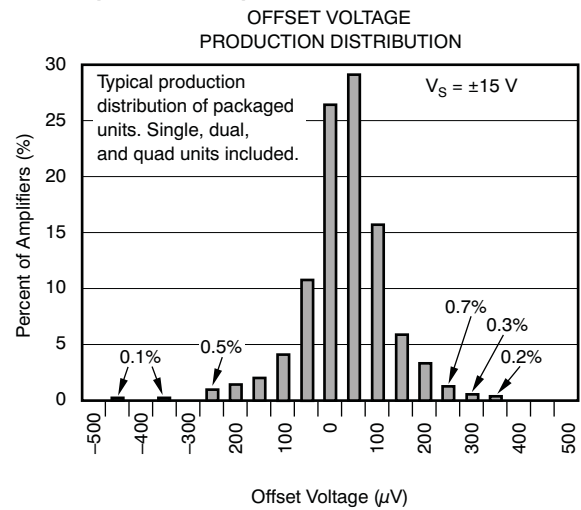
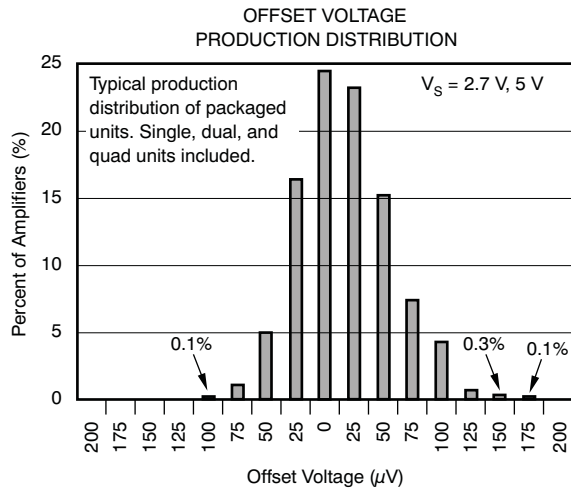
At $T_A = -55^\circ\text{C}$ to 125°C , $V_S = \pm 15\text{ V}$, $R_L = 10\text{ k}\Omega$ connected to $V_S/2$, and $V_{OUT} = V_S/2$, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
TEMPERATURE RANGE					
Specified Range		-55		125	$^\circ\text{C}$
Operating Range		-55		125	$^\circ\text{C}$
Storage		-55		125	$^\circ\text{C}$
Thermal Resistance	θ_{JA}		150		$^\circ\text{C/W}$

TYPICAL CHARACTERISTICS

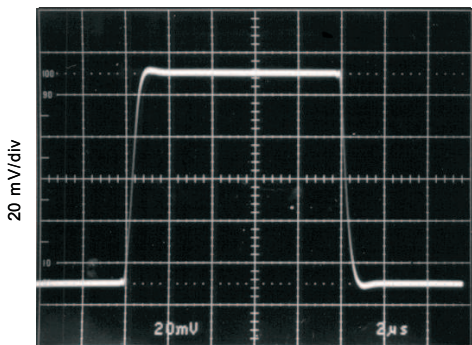


TYPICAL CHARACTERISTICS (continued)



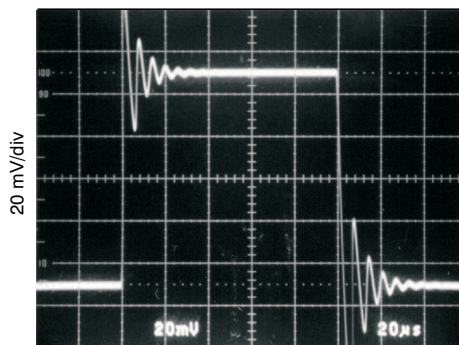
TYPICAL CHARACTERISTICS (continued)

SMALL-SIGNAL STEP RESPONSE
 $G = 1, C_L = 100 \text{ pF}, V_S = 5 \text{ V}$



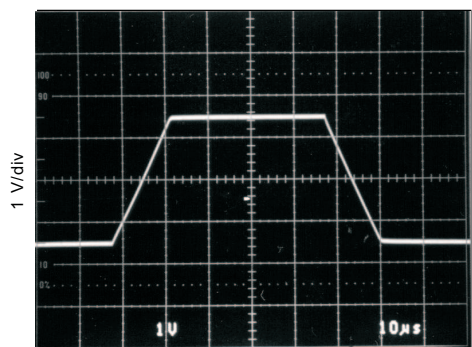
2 μs/div

SMALL-SIGNAL STEP RESPONSE
 $G = 1, C_L = 10,000 \text{ pF}, V_S = 5 \text{ V}$



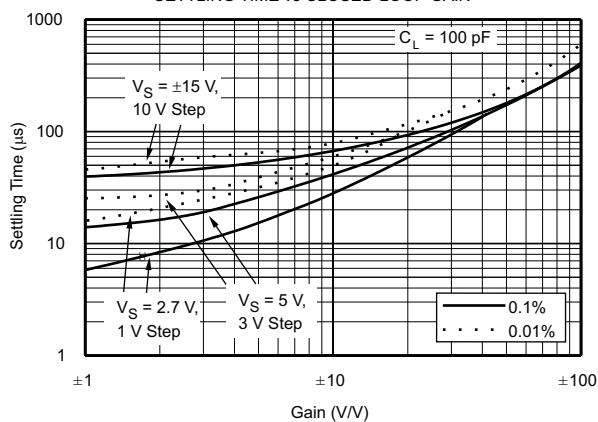
20 μs/div

LARGE-SIGNAL STEP RESPONSE
 $G = 1, C_L = 100 \text{ pF}, V_S = 5 \text{ V}$

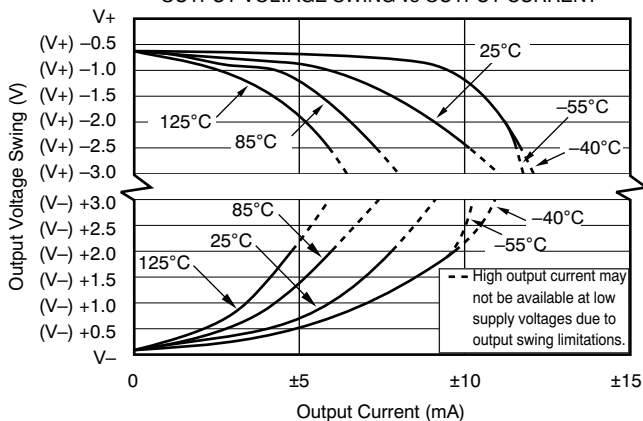


10 μs/div

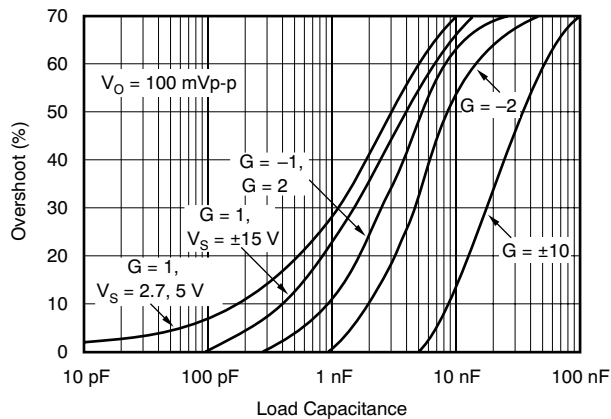
SETTLING TIME vs CLOSED-LOOP GAIN



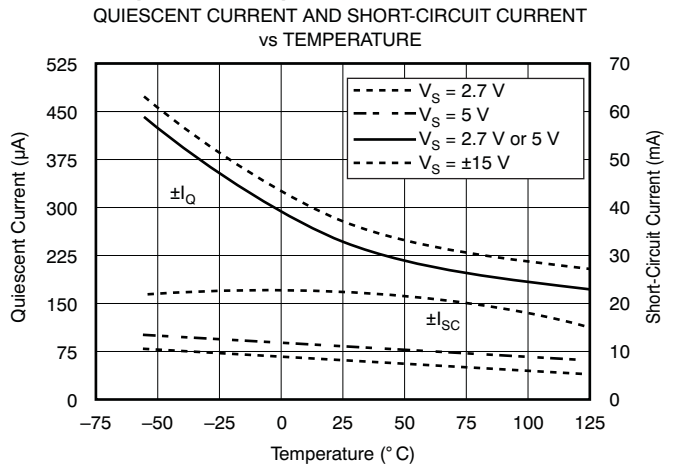
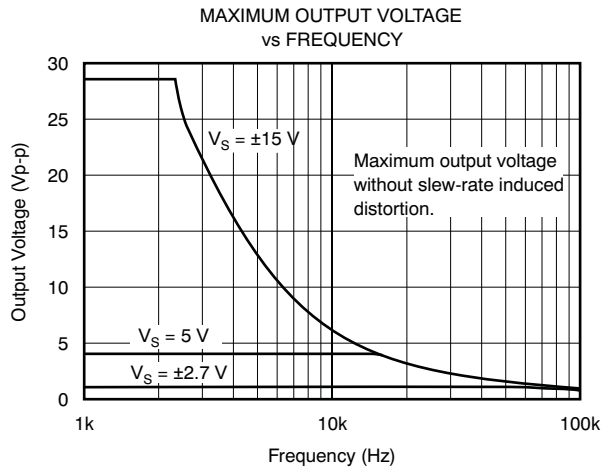
OUTPUT VOLTAGE SWING vs OUTPUT CURRENT



SMALL-SIGNAL OVERSHOOT vs LOAD CAPACITANCE



TYPICAL CHARACTERISTICS (continued)



APPLICATION INFORMATION

The OPA2234 series op amps are unity-gain stable and suitable for a wide range of general-purpose applications. Power-supply pins should be bypassed with 10 nF ceramic capacitors.

OPERATING VOLTAGE

The OPA2234 series op amps operate from single (2.7 V to 36 V) or dual (± 1.35 V to ± 18 V) supplies with excellent performance. Specifications are production tested with 2.7 V, 5 V, and ± 15 V supplies. Most behavior remains unchanged throughout the full operating voltage range. Parameters which vary significantly with operating voltage are shown in the Typical Characteristic curves.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2234MDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR	-55 to 125	2234M	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF OPA2234M :

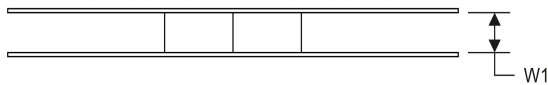
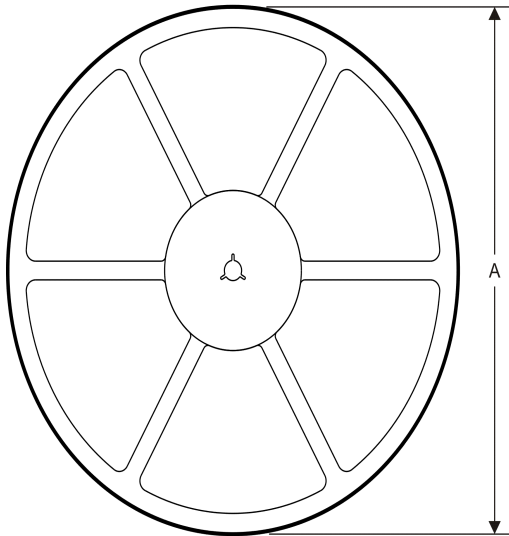
- Catalog: [OPA2234](#)

NOTE: Qualified Version Definitions:

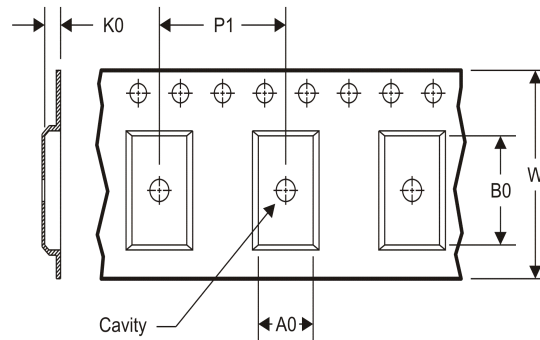
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2234MDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

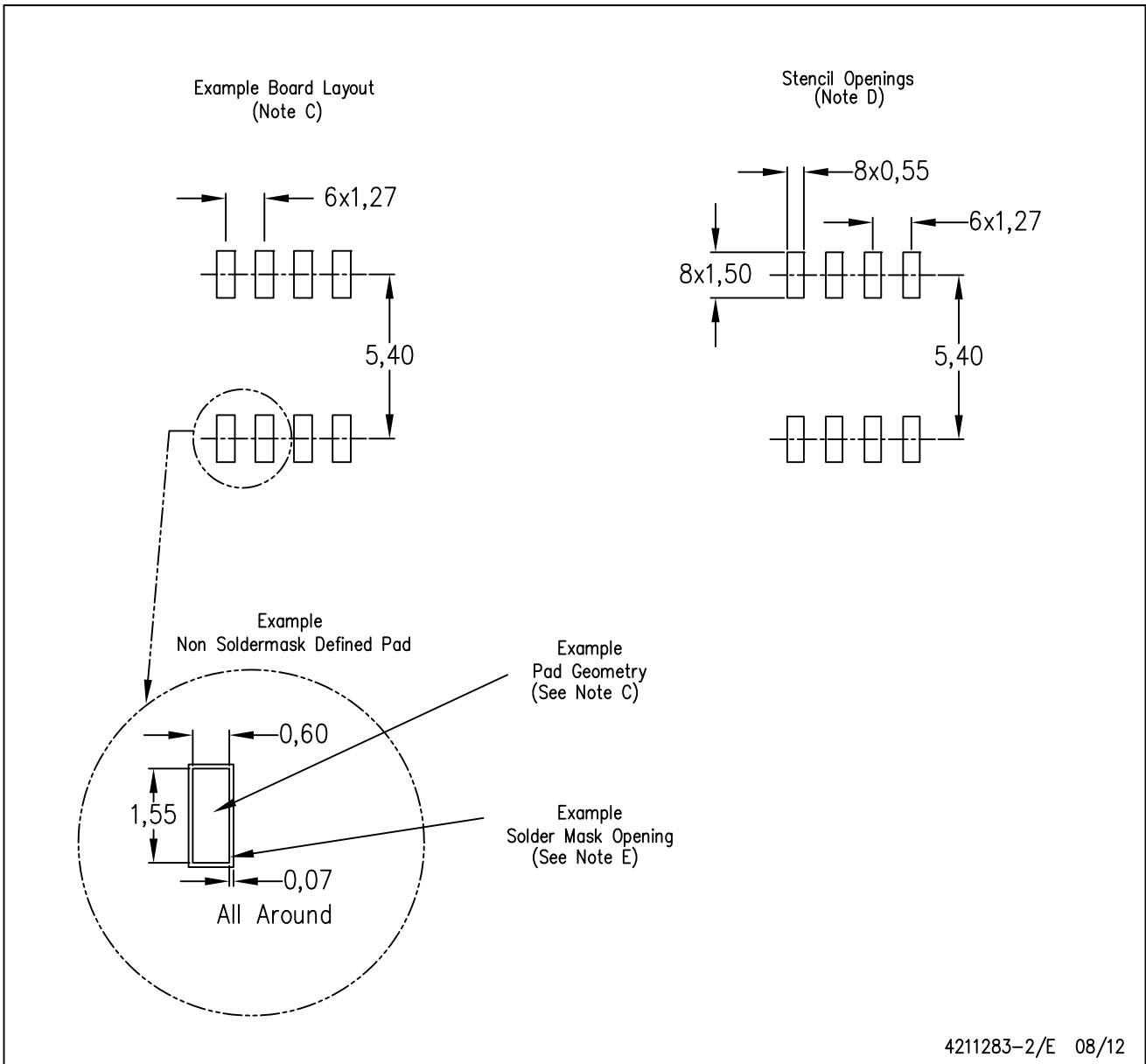


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2234MDR	SOIC	D	8	2500	367.0	367.0	35.0

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



4211283-2/E 08/12

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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