PIC32MX534/564/664/764

PIC32MX534/564/664/764 Family
Silicon Errata and Data Sheet Clarification

The PIC32MX534/564/664/764 family devices that you have received conform functionally to the current Device Data Sheet (DS60001156**H**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC32MX534/564/664/764 silicon.

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A2**).

Data Sheet clarifications and corrections start on page 9, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
   a) For MPLAB IDE 8, select *Programmer > Reconnect*.
   b) For MPLAB X IDE, select *Window > Dashboard*, and then click the **Refresh Debug Tool Status** icon ( ).
5. Depending on the development tool used, the part number and the Device and Revision ID values appear in the **Output** window.

Note:	If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The Device and Revision ID values for the various PIC32MX534/564/664/764 silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision(2)		
		A0	A1	A2
PIC32MX534F064H	0x4400053	0x0	0x1	0x2
PIC32MX564F064H	0x4401053			
PIC32MX564F128H	0x4403053			
PIC32MX664F064H	0x4405053			
PIC32MX664F128H	0x4407053			
PIC32MX764F128H	0x440B053			
PIC32MX534F064L	0x440C053			
PIC32MX564F064L	0x440D053			
PIC32MX564F128L	0x440F053			
PIC32MX664F064L	0x4411053			
PIC32MX664F128L	0x4413053			
PIC32MX764F128L	0x4417053			

Note 1: The Device and Revision IDs (DEVID and DEVREV) are located at the last two implemented addresses in program memory.

2: Refer to the *"PIC32MX Flash Programming Specification"* (DS61145) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item #	Issue Summary	Affected Revisions(1)		
				A0	A1	A2
JTAG	—	1.	On 64-pin devices the TMS pin requires an external pull-up.	X	X	X
CAN	—	2.	The TXBAT bit status may be incorrect after an abort.	X	X	X
SPI	Slave Mode	3.	The SPIBUSY status is incorrect after an aborted transfer.	X	X	X
SPI	Slave Mode	4.	A wake-up interrupt may not be clearable.	X	X	X
SPI	Frame Mode	5.	Recovery from an underrun requires multiple SPI clock periods.	X	X	X
SPI	—	6.	Byte writes to the SPISTAT register are not decoded correctly.	X	X	X
UART	—	7.	The TRMT bit is asserted before the transmission is complete.	X	X	X
UART	IrDA® with BCLK	8.	TX data is corrupted when BRG values greater than 0x200 are used.	X	X	X
UART	IrDA	9.	The IrDA minimum bit time is not detected at all baud rates.	X	X	X
UART	UART Receive Buffer Overrun Error Status	10.	OERR bit does not get cleared on a module Reset.	X	X	X
ADC	Conversion Trigger from INT0 Interrupt	11.	The ADC module conversion triggers occur on the rising edge of the INT0 signal even when INT0 is configured to generate an interrupt on the falling edge.	X	X	X
JTAG	Boundary Scan	12.	Pin 100 on 100-pin packages and pin A1 on 121-pin packages do not respond to boundary scan commands.	X	X	X
Oscillator	Clock Switch	13.	Clock switch may not work if Cache is disabled and Prefetch is enabled.	X	X	X
DMA	Suspend Status	14.	The DMABUSY status bit may not reflect the correct status if the DMA module is suspended.	X	X	X
Voltage Regulator	BOR	15.	Device may not exit BOR state if BOR event occurs.	X	X	
USB	OTG Mode	16.	When the USB model is configured for OTG operation, it may not properly recognize all required OTG voltage levels on VBUS pin.	X	X	X
Oscillator	Clock Switch	17.	If a Fail-Safe Clock Monitor (FSCM) event occurs when Primary Oscillator (POSC) mode is used, firmware clock switch requests to switch from FRC mode will fail.	X	X	X
I2C™	Slave Mode	18.	The I2C module does not respond to address 0x78 when the STRICT and A10M bits are cleared in the I2CxCON register.	X	X	X
USB	UIDLE Interrupt	19.	UIDLE interrupts cease if the UIDLE interrupt flag is cleared.	X	X	X
CPU	Constant Data Access from Flash	20.	A Data Bus Exception (DBE) may occur if an interrupt is encountered by the CPU while it is accessing constant data from Flash memory.	X	X	X
CPU	Data Write to a Peripheral	21.	A data write operation by the CPU to a peripheral may be repeated if an interrupt occurs during initial write operation.	X	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

TABLE 2: SILICON ISSUE SUMMARY (CONTINUED)

Module	Feature	Item #	Issue Summary	Affected Revisions(1)		
				A0	A1	A2
Oscillator	Clock Out	22.	A clock signal is present on the CLKO pin, regardless of the clock source and setting of the CLKO Enable Configuration bit, during a Power-on Reset (POR) condition.	X	X	X
Input Capture	Idle Mode and Sleep Mode	23.	All input capture modes selectable by ICM<2:0>, with the exception of Interrupt-only mode, will not work when the CPU enters Idle mode or Sleep mode.	X	X	X
USB	Host	24.	The USB bus might not be returned to the J-state following an acknowledgment packet when running low-speed through a hub.	X	X	X
Non-5V Tolerant Pins	Pull-ups	25.	Internal pull-up resistors may not guarantee a logical ‘1’ on non-5V tolerant pins when they are configured as digital inputs.	X	X	X
5V Tolerant Pins	Pull-ups	26.	Internal pull-up resistors may not guarantee a logical ‘1’ on 5V tolerant pins when they are configured as digital inputs.	X	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A2**).

1. Module: JTAG

On 64-pin devices, an external pull-up resistor is required on the TMS pin for proper JTAG.

Work around

Connect a 100k-200k pull-up to the TMS pin.

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

2. Module: CAN

When an abort request occurs concurrently with a successful message transmission, and additional messages remain in the FIFO, these remaining messages are not transmitted and the TXBAT bit does not reflect the abort.

Work around

The actual FIFO status can be determined by the FIFO pointers CFIFOCI and CFIFOUA.

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

3. Module: SPI

In Slave mode with Chip Select (CS) enabled, if the Master deasserts CS before the SPI clock has returned to the Idle state, the SPIBUSY bit will remain set until the next SPI data transfer is completed. The other SPI status bits will reflect the actual status.

Work around

None.

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

4. Module: SPI

In Slave mode when entering Sleep mode after a SPI transfer with SPI interrupts enabled, a false interrupt may be generated waking the device. This interrupt can be cleared; however, entering Sleep may cause the condition to occur again.

Work around

Do not use SPI in Slave mode as a wake-up source from Sleep mode.

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

5. Module: SPI

In Frame mode the module is not immediately ready for further transfers after clearing the SPITUR bit. The SPITUR bit will be cleared by hardware before the SPI state machine is prepared for the next operation.

Work around

Firmware must wait at least four bit times before writing to the SPI registers after clearing the SPITUR bit.

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

6. Module: SPI

Byte writes to the SPISTAT register are not decoded correctly. A byte write to byte zero of SPISTAT is actually performed on both byte zero and byte one. A byte write to byte one of SPISTAT is ignored.

Work around

Only perform word operations on the SPISTAT register.

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

7. Module: UART

The TRMT bit is asserted during the STOP bit generation not after the STOP bit has been sent.

Work around

If firmware needs to be aware when the transmission is complete, firmware should add a half bit time delay after the TRMT bit is asserted.

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

8. Module: UART

In IrDA mode with baud clock output enabled, the UART TX data is corrupted when the BRG value is greater than 0x200.

Work around

Use the Peripheral Bus (PB) divisor to lower the PB frequency such that the required UART BRG value is less than 0x201.

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

9. Module: UART

The UART module is not fully IrDA compliant. The module does not detect the 1.6 µs minimum bit width at all baud rates as defined in the IrDA specification. The module does detect the 3/16 bit width at all baud rates.

Work around

None.

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

10. Module: UART

The OERR bit does not get cleared on a module reset. If the OERR bit is set and the module is disabled, the OERR bit retains its status even after the UART module is reinitialized.

Work around

The user software must check this bit in the UART module initialization routine and clear it if it is set.

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

11. Module: ADC

When the ADC module is configured to start conversion on an external interrupt (SSRC<2:0> = 001), the start of conversion always occurs on a rising edge detected at the INT0 pin, even when the INT0 pin has been configured to generate an interrupt on a falling edge (INT0EP = 0).

Work around

Generate ADC conversion triggers on the rising edge of the INT0 signal.

Alternatively, use external circuitry to invert the signal appearing at the INT0 pin, so that a falling edge of the input signal is detected as a rising edge by the INT0 pin.

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

12. Module: JTAG

Pin 100 on 100-pin packages and pin A1 on 121-pin packages do not respond to boundary scan commands.

Work around

None.

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

13. Module: Oscillator

Clock switch may not work if Cache is disabled (DCSZ<1:0> = 00 in the CHECON register) and Prefetch is enabled (PREFEN<1:0> not equal '00' in the CHECON register).

Work around

Set wait states to a value of 7 (PFMWS<2:0> = 111 in the CHECON register), perform a clock switch, and then set waits states to the desired value.

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

14. Module: DMA

If the DMA module is suspended by setting the DMA Suspend bit (SUSPEND) in the DMA Controller Control register (DMACON), the DMA Module Busy Bit (DMABUSY) in the DMACON register may continue to show a Busy status, when the DMA module completes transaction.

Work around

Use the Channel Busy bit (CHBUSY) in the DMA Channel Control Register (DCHxCON) to check the status of the DMA channel.

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

15. Module: Voltage Regulator

Device may not exit BOR state if BOR event occurs.

Work arounds

Work around 1:

VDD must remain within published specification (see Parameter DC10 of the device data sheet).

Work around 2:

Reset device by providing POR condition.

Affected Silicon Revisions

A0	A1	A2					
X	X						

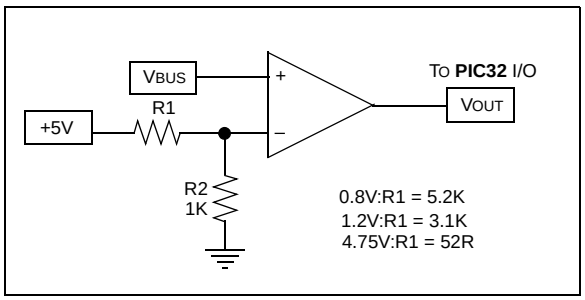
16. Module: USB

When the USB model is configured for OTG operation, it may not recognize all required OTG voltage levels on VBUS pin.

Work around

Use external comparator circuit to detect OTG specific voltage levels on VBUS pin.

FIGURE 1: EXTERNAL COMPARATOR SCHEMATIC EXAMPLE



Affected Silicon Revisions

A0	A1	A2					
X	X	X					

17. Module: Oscillator

If the Primary Oscillator (POSC) mode is implemented and a Fail-Safe Clock Monitor (FSCM) event occurs (failure of the external primary clock), the internal clock source will switch to the FRC oscillator. Subsequent firmware clock switch requests from the FRC oscillator to other clock sources will fail and the device will continue to execute on the FRC oscillator. Upon repair of the external clock source and a power-on state, the device will resume operation with the primary oscillator clock source.

Work around

None.

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

18. Module: I²C™

The slave address, 0x78, is one of a group of reserved addresses. It is used as the upper byte of a 10-bit address when 10-bit addressing is enabled. The I²C module control register allows the programmer to enable both 10-bit addressing and strict enforcement of reserved addressing, with the A10M and STRICT bits, respectively. When both bits are cleared, the device should respond to the reserved address 0x78, but it does not.

Work around

None.

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

19. Module: USB

If the bus has been idle for more than 3 ms, the UIDLE interrupt flag is set. If software clears the interrupt flag, and the bus remains idle, the UIDLE interrupt flag will not be set again.

Work around

Software can leave the UIDLE bit set until it has received some indication of bus resumption. (Resume, Reset, SOF, or Error).

Note: Resume and Reset are the only interrupts that should be following UIDLE assertion. If the UIDLE bit is set, it should be okay to suspend the USB module (as long as this code is protected by the GUARD and/or ACTPEND logic). This will require software to clear the UIDLE interrupt enable bit to exit the USB ISR (if using interrupt driven code).

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

20. Module: CPU

When both prefetch and instruction cache are enabled, a Data Bus Exception (DBE) may occur if an interrupt is encountered by the CPU while it is accessing constant data (not instructions) from Flash memory.

Work around

To avoid a DBE, use one of the following two solutions:

1. Structure application code, such that interrupts are not used while the CPU is accessing data from Flash memory.
2. Disable either the Prefetch module or CPU cache functionality as follows (by default both are disabled on a Power-on Reset (POR)):
   a) To disable the Prefetch module, set the Predictive Prefetch Enable bits, PREFEN<1:0>, in the Cache Control Register, CHECON<6:5>, to '00'.
   b) To disable CPU cache, set the Kseg0 bits, K0<2:0>, in the CP0 Configuration Register, Config<2:0>, to '010'.

Note: Disabling either the cache or Prefetch module will have minimum performance degradation, with a typical application realizing 10 percent or less performance impact.

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

21. Module: CPU

During normal operation, if a CPU write operation is interrupted by an incoming interrupt, it should be aborted (not completed) and resumed after the interrupt is serviced. However, some of these write operations may not be aborted, resulting in a double write to peripherals by the CPU (the first write during the interrupt and the second write after the interrupt is serviced).

Work around

Most peripherals are not affected by this issue, as a double write will not have a negative impact. However, the following communication peripherals will double-send data if their respective transmit buffers are written twice: SPI, I²C, UART and PMP. To avoid double transmission of data, utilize DMA to transfer data to these peripherals or disable interrupts while writing to these peripherals.

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

22. Module: Oscillator

A clock signal is present on the CLKO pin, regardless of the clock source and setting of the CLKO Enable Configuration bit, OSCIOFNC (DEVCFG1<10>), during a Power-on Reset (POR) condition.

Work around

Do not connect the CLKO pin to a device that would be adversely affected by rapid pin toggling or a frequency other than that defined by the oscillator configuration. Do not use the CLKO pin as an input if the device connected to the CLKO pin would be adversely affected by the pin driving a signal out.

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

23. Module: Input Capture

All input capture modes selectable by ICM<2:0>, with the exception of Interrupt-only mode, will not work when the CPU enters Idle or Sleep mode.

Work around

Configure the Input Capture module for Interrupt-only mode (ICM<2:0> = 111) when the CPU is in Sleep or Idle mode.

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

24. Module: USB

While operating in Host mode and attached to a low-speed device through a full-speed USB hub, the host may persistently drive the bus to an SE0 state (both D+/D- as '0'), which would be interpreted as a bus Reset condition by the hub; or the host may persistently drive the bus to a J state, which would make the hub detach condition undetectable by the host.

Work around

Connect low-speed devices directly to the Host USB port and not through a USB hub.

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

25. Module: Non-5V Tolerant Pins

When internal pull-ups are enabled on non-5V tolerant pins, the level as measured on the pin and available to external device inputs, may not exceed the minimum value of V_{IH}, and therefore, qualify as a logic "high". However, with respect to PIC32 devices, as long as the load does not exceed -50 µA, the internal pull-ups are guaranteed to be recognized as a logic "high" internally to the PIC32 device.

Work around

It is recommend to only use external pull-ups:

- To guarantee a logic "high" for external logic input circuits outside of the PIC32 device
- For PIC32 device inputs, if the external load exceeds -50 µA

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

26. Module: 5V Tolerant Pins

When internal pull-ups are enabled on 5V tolerant pins, the level as measured on the pin and available to external device inputs, may not exceed the minimum value of V_{IH}, and therefore, qualify as a logic "high". However, with respect to PIC32 devices, as long as the load does not exceed -50 µA, the internal pull-ups are guaranteed to be recognized as a logic "high" internally to the PIC32 device.

Work around

It is recommend to only use external pull-ups:

- To guarantee a logic "high" for external logic input circuits outside of the PIC32 device
- For PIC32 device inputs, if the external load exceeds -50 µA

Affected Silicon Revisions

A0	A1	A2					
X	X	X					

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS60001156**H**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. Module: DC Characteristics: I/O Pin Input Specifications

In the current version of the data sheet, the revision history for changes to **Table 31-8: DC Characteristics: I/O Pin Input Specifications** was omitted.

The text in bold in the following table shows the updates that were made.

TABLE 31-8: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param. No.	Symbol	Characteristics	Min.	Typical(1)	Max.	Units	Conditions
	VIH	Input High Voltage					
DI20		I/O Pins not 5V-tolerant(5)	**0.65 VDD**	—	VDD	V	(Note 4,**6**)
		I/O Pins 5V-tolerant with PMP(5)	0.25 VDD + 0.8V	—	5.5	V	(Note 4,**6**)
		I/O Pins 5V-tolerant(5)	**0.65 VDD**	—	5.5	V	
DI28		SDAx, SCLx	**0.65 VDD**	—	5.5	V	SMBus disabled (Note 4,**6**)
DI29		SDAx, SCLx	2.1	—	5.5	V	SMBus enabled, 2.3V ≤ VPIN ≤ 5.5 (Note 4,**6**)
DI30	ICNPU	Change Notification Pull-up Current	—	—	**-50**	μA	VDD = 3.3V, VPIN = VSS (Note 3,6)

Note 1: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: The leakage current on the $\overline{\text{MCLR}}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as current sourced by the pin.

4: This parameter is characterized, but not tested in manufacturing.

5: See the "Pin Diagrams" section for the 5V-tolerant pins.

6: The VIH specification is only in relation to externally applied inputs and not with respect to the user-selectable pull-ups. Externally applied high impedance or open drain input signals utilizing the PIC32 internal pull-ups are guaranteed to be recognized as a logic "high" internally to the PIC32 device, provided that the external load does not exceed the maximum value of ICNPU.

7: VIL source < (VSS - 0.3). Characterized but not tested.

8: VIH source > (VDD + 0.3) for non-5V tolerant pins only.

9: Digital 5V tolerant pins do not have an internal high side diode to VDD, and therefore, cannot tolerate any "positive" input injection current.

10: Injection currents > | 0 | can affect the ADC results by approximately 4 to 6 counts (i.e., VIH Source > (VDD + 0.3) or VIL source < (VSS - 0.3)).

11: Any number and/or combination of I/O pins not excluded under IICL or IICH conditions are permitted provided the "absolute instantaneous" sum of the input injection currents from all pins do not exceed the specified limit. If Note 7, IICL = (((Vss - 0.3) - VIL source) / Rs). If Note 8, IICH = ((IICH source - (VDD + 0.3)) / RS). RS = Resistance between input source voltage and device pin. If (VSS - 0.3) ≤ VSOURCE ≤ (VDD + 0.3), injection current = 0.

TABLE 31-8: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS (CONTINUED)

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param. No.	Symbol	Characteristics	Min.	Typical(1)	Max.	Units	Conditions
DI60a	IICL	Input Low Injection Current	0	—	-5(7,10)	mA	This parameter applies to all pins, with the exception of RB10. Maximum IICH current for this exception is 0 mA.
DI60b	IICH	Input High Injection Current	0	—	+5(8,9,10)	mA	This parameter applies to all pins, with the exception of all 5V tolerant pins, SOSCI, and RB10. Maximum IICH current for these exceptions is 0 mA.
DI60c	∑IICT	Total Input Injection Current (sum of all I/O and control pins)	-20(11)	—	+20(11)	mA	Absolute instantaneous sum of all ± input injection currents from all I/O pins (| IICL + | IICH |) ≤ ∑IICT

Note 1: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: The leakage current on the $\overline{\text{MCLR}}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as current sourced by the pin.

4: This parameter is characterized, but not tested in manufacturing.

5: See the "Pin Diagrams" section for the 5V-tolerant pins.

6: The VIH specification is only in relation to externally applied inputs and not with respect to the user-selectable pull-ups. Externally applied high impedance or open drain input signals utilizing the PIC32 internal pull-ups are guaranteed to be recognized as a logic "high" internally to the PIC32 device, provided that the external load does not exceed the maximum value of ICNPU.

7: VIL source < (VSS - 0.3). Characterized but not tested.

8: VIH source > (VDD + 0.3) for non-5V tolerant pins only.

9: Digital 5V tolerant pins do not have an internal high side diode to VDD, and therefore, cannot tolerate any "positive" input injection current.

10: Injection currents > | 0 | can affect the ADC results by approximately 4 to 6 counts (i.e., VIH Source > (VDD + 0.3) or VIL source < (VSS - 0.3)).

11: Any number and/or combination of I/O pins not excluded under IICL or IICH conditions are permitted provided the "absolute instantaneous" sum of the input injection currents from all pins do not exceed the specified limit. If Note 7, IICL = (((Vss - 0.3) - VIL source) / Rs). If Note 8, IICH = ((IICH source - (VDD + 0.3)) / RS). RS = Resistance between input source voltage and device pin. If (VSS - 0.3) ≤ VSOURCE ≤ (VDD + 0.3), injection current = 0.

2. Module: DC Characteristics: Program Memory

Certain specifications in Table 31-11 were stated incorrectly in the data sheet. The correct values are shown in bold type in the following table.

TABLE 31-11: DC CHARACTERISTICS: PROGRAM MEMORY

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param. No.	Symbol	Characteristics	Min.	Typical(1)	Max.	Units	Conditions
		Program Flash Memory(3)					
D130	EP	Cell Endurance	1000	—	—	E/W	—
D130a	EP	Cell Endurance	20,000	—	—	E/W	See Note 4
D131	VPR	VDD for Read	2.3	—	3.6	V	—
D132	VPEW	VDD for Erase or Write	3.0	—	3.6	V	—
D132a	VPEW	VDD for Erase or Write	2.3	—	3.6	V	See Note 4
D134	TRETD	Characteristic Retention	20	—	—	Year	Provided no other specifications are violated
D135	IDDP	Supply Current during Programming	—	10	—	mA	—
	TWW	Word Write Cycle Time	**—**	**411**	**—**	**FRC Cycles**	**See Note 4**
D136	TRW	Row Write Cycle Time(2)	**—**	**26067**	**—**	**FRC Cycles**	**See Note 4**
D137	TPE	Page Erase Cycle Time	**—**	**201060**	**—**	**FRC Cycles**	**See Note 4**
	TCE	Chip Erase Cycle Time	**—**	**804652**	**—**	**FRC Cycles**	**See Note 4**

Note 1: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated.

2: The minimum SYSCLK for row programming is 4 MHz. Care should be taken to minimize bus activities during row programming, such as suspending any memory-to-memory DMA operations. If heavy bus loads are expected, selecting Bus Matrix Arbitration mode 2 (rotating priority) may be necessary. The default Arbitration mode is mode 1 (CPU has lowest priority).

3: Refer to *"PIC32 Flash Programming Specification"* (DS60001145) for operating conditions during programming and erase cycles.

4: This parameter depends on the FRC accuracy (see Table 31-19) and the FRC tuning values (see Register 8-2).

3. Module: DC Characteristics: Operating Current (IDD)

Note 4 in Table 31-5 was stated incorrectly in the data sheet. The correct information is shown in **bold** type in the following table.

Note:	All previous **(Note 4)** references listed in the Conditions column were removed.

TABLE 31-5: DC CHARACTERISTICS: OPERATING CURRENT (IDD)

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param. No.	Typical(3)	Max.	Units	Conditions			
Operating Current (IDD)(1,2,4) for PIC32MX575/675/695/775/795 Family Devices							
DC20	6	9	mA	Code executing from Flash	-40ºC, +25ºC, +85ºC	—	4 MHz
DC20b	7	10			+105ºC		
DC20a	4	—		Code executing from SRAM	—		
DC21	37	40	mA	Code executing from Flash	—	—	25 MHz
DC21a	25	—		Code executing from SRAM			
DC22	64	70	mA	Code executing from Flash	—	—	60 MHz
DC22a	61	—		Code executing from SRAM			
DC23	85	98	mA	Code executing from Flash	-40ºC, +25ºC, +85ºC	—	80 MHz
DC23b	90	120			+105ºC		
DC23a	85	—		Code executing from SRAM	—		
DC25a	125	150	µA	—	+25°C	3.3V	LPRC (31 kHz)

Note 1: A device's IDD supply current is mainly a function of the operating voltage and frequency. Other factors, such as PBCLK (Peripheral Bus Clock) frequency, number of peripheral modules enabled, internal code execution pattern, execution from Program Flash memory vs. SRAM, I/O pin loading and switching rate, oscillator type, as well as temperature, can have an impact on the current consumption.

2: The test conditions for IDD measurements are as follows:

- Oscillator mode is EC (for 8 MHz and below) and EC+PLL (for above 8 MHz) with OSC1 driven by external square wave from rail-to-rail, (OSC1 input clock input over/undershoot < 100 mV required)
- OSC2/CLKO is configured as an I/O input pin
- USB PLL oscillator is disabled if the USB module is implemented, PBCLK divisor = 1:8
- CPU, program Flash, and SRAM data memory are operational, program Flash memory Wait states = 111, Program Cache and Prefetch are disabled and SRAM data memory Wait states = 1
- No peripheral modules are operating, (ON bit = 0)
- WDT, Clock Switching, Fail-Safe Clock Monitor, and Secondary Oscillator are disabled
- All I/O pins are configured as inputs and pulled to VSS
- $\overline{MCLR}$ = VDD
- CPU executing while(1) statement from Flash
- RTCC and JTAG are disabled

3: Data in "Typical" column is at 3.3V, 25°C at specified operating frequency unless otherwise stated. Parameters are for design guidance only and are not tested.

4: All parameters are characterized, but only those parameters listed for 4 MHz and 80 MHz are tested at 3.3V in manufacturing.

TABLE 31-5: DC CHARACTERISTICS: OPERATING CURRENT (IDD) (CONTINUED)

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp				
Param. No.	Typical(3)	Max.	Units	Conditions			
Operating Current (IDD)(1,2,4) for PIC32MX534/564/664/764 Family Devices							
DC20c	6	9	mA	Code executing from Flash	-40ºC, +25ºC, +85ºC	—	4 MHz
DC20d	7	10			+105ºC		
DC20e	2	—		Code executing from SRAM	—		
DC21b	19	32	mA	Code executing from Flash	—	—	25 MHz
DC21c	14	—		Code executing from SRAM			
DC22b	31	50	mA	Code executing from Flash	—	—	60 MHz
DC22c	29	—		Code executing from SRAM			
DC23c	39	65	mA	Code executing from Flash	-40ºC, +25ºC, +85ºC	—	80 MHz
DC23d	49	70			+105ºC		
DC23e	39	—		Code executing from SRAM	—		
DC25b	100	150	µA	—	+25°C	3.3V	LPRC (31 kHz)

Note 1: A device's IDD supply current is mainly a function of the operating voltage and frequency. Other factors, such as PBCLK (Peripheral Bus Clock) frequency, number of peripheral modules enabled, internal code execution pattern, execution from Program Flash memory vs. SRAM, I/O pin loading and switching rate, oscillator type, as well as temperature, can have an impact on the current consumption.

2: The test conditions for IDD measurements are as follows:

- Oscillator mode is EC (for 8 MHz and below) and EC+PLL (for above 8 MHz) with OSC1 driven by external square wave from rail-to-rail, (OSC1 input clock input over/undershoot < 100 mV required)
- OSC2/CLKO is configured as an I/O input pin
- USB PLL oscillator is disabled if the USB module is implemented, PBCLK divisor = 1:8
- CPU, program Flash, and SRAM data memory are operational, program Flash memory Wait states = 111, Program Cache and Prefetch are disabled and SRAM data memory Wait states = 1
- No peripheral modules are operating, (ON bit = 0)
- WDT, Clock Switching, Fail-Safe Clock Monitor, and Secondary Oscillator are disabled
- All I/O pins are configured as inputs and pulled to VSS
- $\overline{MCLR}$ = VDD
- CPU executing `while(1)` statement from Flash
- RTCC and JTAG are disabled

3: Data in "Typical" column is at 3.3V, 25°C at specified operating frequency unless otherwise stated. Parameters are for design guidance only and are not tested.

4: All parameters are characterized, but only those parameters listed for 4 MHz and 80 MHz are tested at 3.3V in manufacturing.

4. Module: DC Characteristics: Operating Current (I_{IDLE})

Note 3 in Table 31-6 was stated incorrectly in the data sheet. The correct references are shown in **bold** type in the following table.

Note:	All previous **(Note 3)** references listed in the Conditions column were removed.

TABLE 31-6: DC CHARACTERISTICS: IDLE CURRENT (I_{IDLE})

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp			
Parameter No.	Typical(2)	Max.	Units	Conditions		
Idle Current (I_{IDLE})(1,3) for PIC32MX575/675/695/775/795 Family Devices						
DC30	4.5	6.5	mA	-40ºC, +25ºC, +85ºC	—	4 MHz
DC30b	5	7		+105°C		
DC31	13	15	mA	-40ºC, +25ºC, +85ºC	—	25 MHz
DC32	28	30	mA	-40ºC, +25ºC, +85ºC	—	60 MHz
DC33	36	42	mA	-40ºC, +25ºC, +85ºC	—	80 MHz
DC33b	39	45	mA	+105°C		
DC34	—	40	µA	-40°C	2.3V	LPRC (31 kHz)
DC34a		75		+25°C		
DC34b		800		+85°C		
DC34c		1000		+105°C		
DC35	35	—	µA	-40°C	3.3V	
DC35a	65			+25°C		
DC35b	600			+85°C		
DC35c	800			+105°C		
DC36	—	43	µA	-40°C	3.6V	
DC36a		106		+25°C		
DC36b		800		+85°C		
DC36c		1000		+105°C		

Note 1: The test conditions for I_{IDLE} current measurements are as follows:

- Oscillator mode is EC (for 8 MHz and below) and EC+PLL (for above 8 MHz) with OSC1 driven by external square wave from rail-to-rail, (OSC1 input clock input over/undershoot < 100 mV required)
- OSC2/CLKO is configured as an I/O input pin
- USB PLL oscillator is disabled if the USB module is implemented, PBCLK divisor = 1:8
- CPU is in Idle mode, program Flash memory Wait states = 111, Program Cache and Prefetch are disabled and SRAM data memory Wait states = 1
- No peripheral modules are operating, (ON bit = 0)
- WDT, Clock Switching, Fail-Safe Clock Monitor, and Secondary Oscillator are disabled
- All I/O pins are configured as inputs and pulled to VSS
- $\overline{MCLR}$ = VDD
- RTCC and JTAG are disabled

2: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: All parameters are characterized, but only those parameters listed for 4 MHz and 80 MHz are tested at 3.3V in manufacturing.

TABLE 31-6: DC CHARACTERISTICS: IDLE CURRENT (IIDLE) (CONTINUED)

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp			
Parameter No.	Typical(2)	Max.	Units	Conditions		
Idle Current (IIDLE)(1,3) for PIC32MX534/564/664/764 Family Devices						
DC30a	1.5	5	mA	-40ºC, +25ºC, +85ºC	—	4 MHz
DC30c	3.5	6		+105ºC		
DC31a	7	11		-40ºC, +25ºC, +85ºC	—	25 MHz
DC32a	13	20	mA	-40ºC, +25ºC, +85ºC	—	60 MHz
DC33a	17	25	mA	-40ºC, +25ºC, +85ºC	—	80 MHz
DC33c	20	27		+105ºC		
DC34c	—	40	µA	-40°C	2.3V	LPRC (31 kHz)
DC34d		75		+25°C		
DC34e		800		+85°C		
DC34f		1000		+105ºC		
DC35c	30	—	µA	-40°C	3.3V	
DC35d	55			+25°C		
DC35e	230			+85°C		
DC35f	800			+105ºC		
DC36c	—	43	µA	-40°C	3.6V	
DC36d		106		+25°C		
DC36e		800		+85°C		
DC36f		1000		+105ºC		

Note 1: The test conditions for IIDLE current measurements are as follows:

- Oscillator mode is EC (for 8 MHz and below) and EC+PLL (for above 8 MHz) with OSC1 driven by external square wave from rail-to-rail, (OSC1 input clock input over/undershoot < 100 mV required)
- OSC2/CLKO is configured as an I/O input pin
- USB PLL oscillator is disabled if the USB module is implemented, PBCLK divisor = 1:8
- CPU is in Idle mode, program Flash memory Wait states = 111, Program Cache and Prefetch are disabled and SRAM data memory Wait states = 1
- No peripheral modules are operating, (ON bit = 0)
- WDT, Clock Switching, Fail-Safe Clock Monitor, and Secondary Oscillator are disabled
- All I/O pins are configured as inputs and pulled to VSS
- $\overline{MCLR}$ = VDD
- RTCC and JTAG are disabled

2: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: All parameters are characterized, but only those parameters listed for 4 MHz and 80 MHz are tested at 3.3V in manufacturing.

5. Module: DC Characteristics: Operating Current (I_{PD})

Certain references to Note 6 in Table 31-7 were omitted in the data sheet. These references are shown in **bold** type in the following table.

TABLE 31-7: DC CHARACTERISTICS: POWER-DOWN CURRENT (I_{PD})

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp			
Param. No.	Typical(2)	Max.	Units	Conditions		
Power-Down Current (I_{PD})(1) for PIC32MX575/675/695/775/795 Family Devices						
DC40	10	40	μA	-40°C	2.3V	Base Power-Down Current (Note 6)
DC40a	36	100		+25°C		
DC40b	400	720		+85°C		
DC40h	900	1800		+105°C		
DC40c	41	120		+25°C	3.3V	Base Power-Down Current
DC40d	22	80		-40°C	3.6V	Base Power-Down Current **(Note 6)**
DC40e	42	120		+25°C		
DC40g	315	400(5)		+70°C		
DC40f	410	800		+85°C		
DC40i	1000	2000		+105°C		
Module Differential Current for PIC32MX575/675/695/775/795 Family Devices						
DC41	—	10	μA	—	2.3V	Watchdog Timer Current: ΔIWDT (Notes 3,6)
DC41a	5	—			3.3V	Watchdog Timer Current: ΔIWDT (Note 3)
DC41b	—	20			3.6V	Watchdog Timer Current: ΔIWDT (Note 3,**6**)
DC42	—	40	μA	—	2.3V	RTCC + Timer1 w/32 kHz Crystal: ΔIRTCC (Notes 3,6)
DC42a	23	—			3.3V	RTCC + Timer1 w/32 kHz Crystal: ΔIRTCC (Note 3)
DC42b	—	50			3.6V	RTCC + Timer1 w/32 kHz Crystal: ΔIRTCC (Note 3,**6**)
DC43	—	1300	μA	—	2.5V	ADC: ΔIADC (Notes 3,4,6)
DC43a	1100	—			3.3V	ADC: ΔIADC (Notes 3,4)
DC43b	—	1300			3.6V	ADC: ΔIADC (Notes 3,4,**6**)

Note 1: The test conditions for I_{PD} current measurements are as follows:

- Oscillator mode is EC (for 8 MHz and below) and EC+PLL (for above 8 MHz) with OSC1 driven by external square wave from rail-to-rail, (OSC1 input clock input over/undershoot < 100 mV required)
- OSC2/CLKO is configured as an I/O input pin
- USB PLL oscillator is disabled if the USB module is implemented, PBCLK divisor = 1:8
- CPU is in Sleep mode, program Flash memory Wait states = 111, Program Cache and Prefetch are disabled and SRAM data memory Wait states = 1
- No peripheral modules are operating, (ON bit = 0)
- WDT, Clock Switching, Fail-Safe Clock Monitor, and Secondary Oscillator are disabled
- All I/O pins are configured as inputs and pulled to V_{SS}
- $\overline{MCLR}$ = V_{DD}
- RTCC and JTAG are disabled

2: Data in the "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: The Δ current is the additional current consumed when the module is enabled. This current should be added to the base I_{PD} current.

4: Test conditions for ADC module differential current are as follows: Internal ADC RC oscillator enabled.

5: Data is characterized at +70°C and not tested. Parameter is for design guidance only.

6: This parameter is characterized, but not tested in manufacturing.

TABLE 31-7: DC CHARACTERISTICS: POWER-DOWN CURRENT (I_{PD}) (CONTINUED)

DC CHARACTERISTICS			Standard Operating Conditions: 2.3V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +105°C for V-Temp			
Param. No.	Typical(2)	Max.	Units	Conditions		
Power-Down Current (I_{PD})(1) for PIC32MX534/564/664/764 Family Devices						
DC40g	12	40	μA	-40°C	2.3V	Base Power-Down Current (Note 6)
DC40h	20	120		+25°C		
DC40i	210	600		+85°C		
DC40o	400	1000		+105°C		
DC40j	20	120		+25°C	3.3V	Base Power-Down Current
DC40k	15	80		-40°C	3.6V	Base Power-Down Current **(Note 6)**
DC40l	20	120		+25°C		
DC40m	113	350(5)		+70°C		
DC40n	220	650		+85°C		
DC40p	500	1000		+105°C		
Module Differential Current for PIC32MX534/564/664/764 Family Devices						
DC41c	—	10	μA	—	2.5V	Watchdog Timer Current: ΔI_{WDT} (Notes 3,6)
DC41d	5	—			3.3V	Watchdog Timer Current: ΔI_{WDT} (Note 3)
DC41e	—	20			3.6V	Watchdog Timer Current: ΔI_{WDT} (Note 3,**6**)
DC42c	—	40	μA	—	2.5V	RTCC + Timer1 w/32 kHz Crystal: ΔI_{RTCC} (Notes 3,6)
DC42d	23	—			3.3V	RTCC + Timer1 w/32 kHz Crystal: ΔI_{RTCC} (Note 3)
DC42e	—	50			3.6V	RTCC + Timer1 w/32 kHz Crystal: ΔI_{RTCC} (Note 3,**6**)
DC43c	—	1300	μA	—	2.5V	ADC: ΔI_{ADC} (Notes 3,4,6)
DC43d	1100	—			3.3V	ADC: ΔI_{ADC} (Notes 3,4)
DC43e	—	1300			3.6V	ADC: ΔI_{ADC} (Notes 3,4,**6**)

Note 1: The test conditions for I_{PD} current measurements are as follows:

- Oscillator mode is EC (for 8 MHz and below) and EC+PLL (for above 8 MHz) with OSC1 driven by external square wave from rail-to-rail, (OSC1 input clock input over/undershoot < 100 mV required)
- OSC2/CLKO is configured as an I/O input pin
- USB PLL oscillator is disabled if the USB module is implemented, PBCLK divisor = 1:8
- CPU is in Sleep mode, program Flash memory Wait states = 111, Program Cache and Prefetch are disabled and SRAM data memory Wait states = 1
- No peripheral modules are operating, (ON bit = 0)
- WDT, Clock Switching, Fail-Safe Clock Monitor, and Secondary Oscillator are disabled
- All I/O pins are configured as inputs and pulled to V_{SS}
- $\overline{MCLR}$ = V_{DD}
- RTCC and JTAG are disabled

2: Data in the “Typical” column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: The Δ current is the additional current consumed when the module is enabled. This current should be added to the base I_{PD} current.

4: Test conditions for ADC module differential current are as follows: Internal ADC RC oscillator enabled.

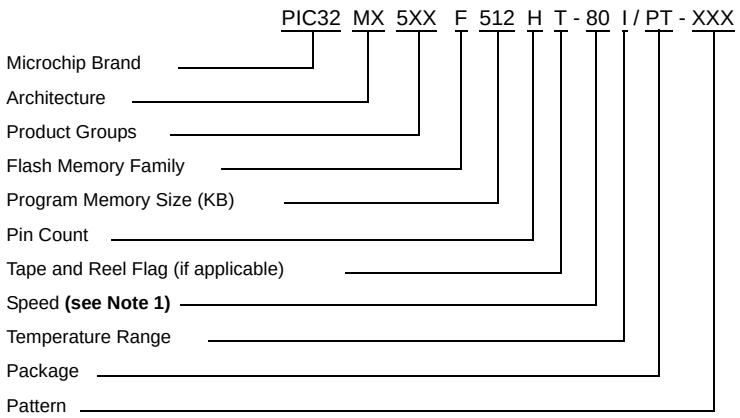
5: Data is characterized at +70°C and not tested. Parameter is for design guidance only.

6: This parameter is characterized, but not tested in manufacturing.

6. Module: Product Identification System

The Product Identification System information was incorrectly specified in the current version of the data sheet. The corrected information is shown in **bold** type.

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.



Example:

PIC32MX575F256H-80I/PT:
General purpose PIC32,
32-bit RISC MCU,
256 KB program memory,
64-pin, Industrial temperature,
TQFP package.

Flash Memory Family

Architecture	MX	= 32-bit RISC MCU core
Product Groups	5XX	= General purpose microcontroller family
	6XX	= General purpose microcontroller family
	7XX	= General purpose microcontroller family
Flash Memory Family	F	= Flash program memory
Program Memory Size	**64**	**= 64K**
	128	**= 128K**
	256	= 256K
	512	= 512K
Pin Count	H	= 64-pin
	L	= 100-pin, **121-pin, 124-pin**
Speed **(see Note 1)**	80	= 80 MHz
Temperature Range	I	= -40°C to +85°C (Industrial)
	V	= -40°C to +105°C (V-Temp)
Package	PT	= 64-Lead (10x10x1 mm) TQFP (Thin Quad Flatpack)
	PT	= 100-Lead (12x12x1 mm) TQFP (Thin Quad Flatpack)
	PF	= 100-Lead (14x14x1 mm) TQFP (Thin Quad Flatpack)
	MR	= 64-Lead (9x9x0.9 mm) QFN (Plastic Quad Flat)
	BG	= 121-Lead (10x10x1.1 mm) TFBGA (Plastic Thin Profile Ball Grid Array)
	TL	= 124-Lead (9x9x0.9 mm) VTLA (Very Thin Leadless Array)
Pattern		Three-digit QTP, SQTP, Code or Special Requirements (blank otherwise)
	ES	= Engineering Sample

Note 1: This option is not available for PIC32MX534/564/664/774 devices.

APPENDIX A: REVISION HISTORY

Rev A Document (7/2010)

Initial release of this document; issued for revision A0 silicon.

Includes silicon issues 1 (JTAG), 2 (CAN), 3-6 (SPI) and 7-9 (UART).

Rev B Document (12/2010)

Added silicon issues 10 (UART), 11 (ADC), 12 (JTAG), 13 (Oscillator), 14 (DMA), 15 (Voltage Regulator) and 16 (USB).

Rev C Document (3/2011)

Updated the data sheet revision from “E” to “F” and updated the current silicon revision to A1 throughout the document.

Added data sheet clarification 1 (Pin Diagrams).

Rev D Document (5/2011)

Updated the data sheet revision from “F” to “G” throughout the document.

Removed data sheet clarification 1.

Rev E Document (10/2011)

Added silicon issues 17 (Oscillator), 18 (I^2C™), and 19 (USB).

Added data sheet clarification 1 (Revision History).

Rev F Document (2/2012)

Updated the current silicon revision to A2 throughout the document.

Added silicon issues 20 (CPU), 21 (CPU), and 22 (Oscillator).

Rev G Document (4/2012)

Updated silicon issues 20 (CPU) and 21 (CPU).

Added silicon issue 23 (Input Capture).

Added silicon issue 24 (USB).

Rev H Document (5/2013)

Added silicon issues 25 (Non-5V Tolerant Pins) and 26 (5V Tolerant Pins).

Removed data sheet clarification 1.

Added data sheet clarifications 1 (DC Characteristics: I/O Pin Input Specifications), 2 (DC Characteristics: Program Memory), 3 (DC Characteristics: Operating Current (IDD)), 4 (DC Characteristics: Operating Current (IIDLE)), 5 (DC Characteristics: Operating Current (IPD)) and 6 (Product Identification System).

NOTES:

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