

# R2A20112ASP

R03DS0047EJ0200

Rev.2.00

## Critical Conduction Mode Interleaved PFC Control IC

Sep 25, 2015

### Description

The R2A20112A controls a boost converter to provide an active power factor correction.

The R2A20112A adopts critical conduction mode for power factor correction and realizes high efficiency and a low switching noise by zero current switching.

Interleaving function improves ripple current on input or output capacitor by 180 degrees phase shift.

Soft-star, the feedback loop short detection, two mode over-voltage-protection, over-current-protection, Over current ON/OFF timer protection for boost Diode short and slave ZCD open detection are built in the R2A20112A, and can constitute a power supply system of high reliability with few external parts.

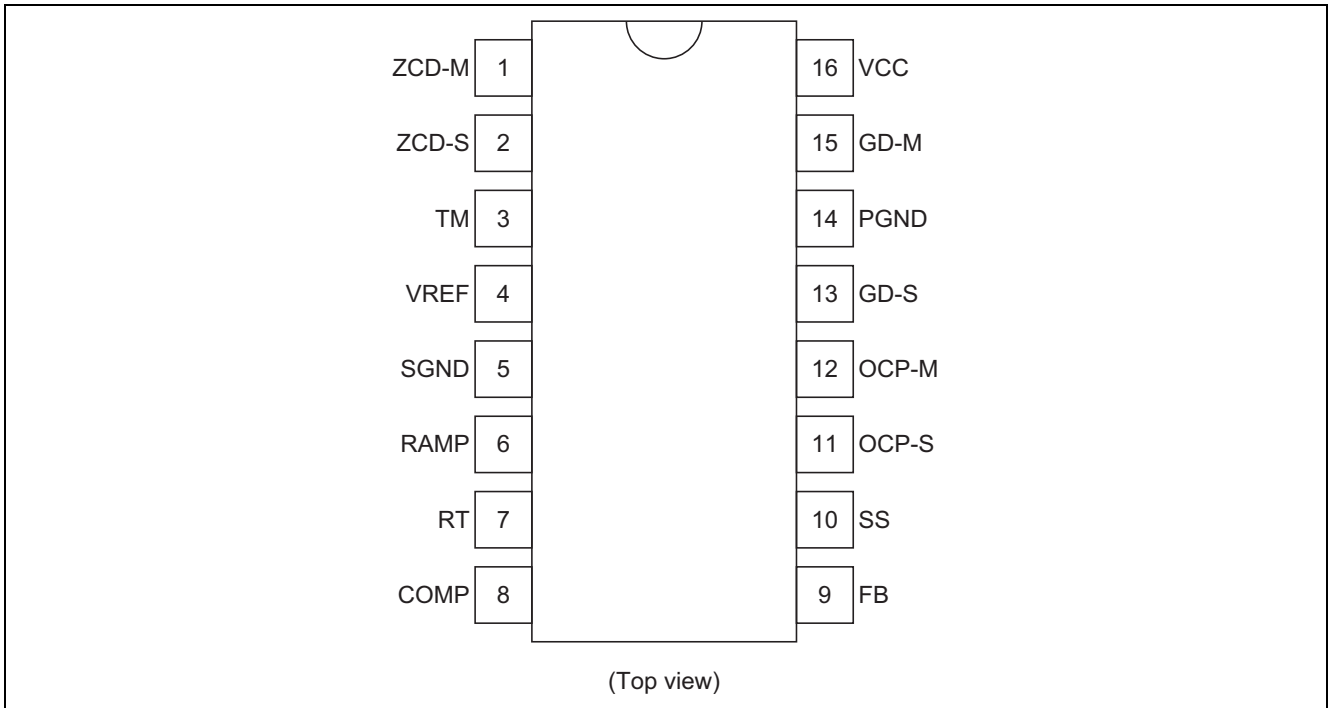
### Features

- Absolute Maximum Ratings
  - Supply voltage  $V_{cc}$ : 24 V
  - Junction temperature  $T_j$ : -40 to +150°C
- Electrical Characteristics
  - VREF output voltage  $V_{ref}$ : 5.0 V  $\pm$  1.5%
  - UVLO operation start voltage  $V_{uvlh}$ : 10.5 V  $\pm$  0.7 V
  - UVLO operation shutdown voltage  $V_{uvll}$ : 9.3 V  $\pm$  0.5 V
  - UVLO hysteresis voltage  $Hys_{uvl}$ : 1.2 V  $\pm$  0.5 V
- Functions
  - Boost converter control with critical conduction mode
  - Interleaving control
  - Soft start function for the reference voltage of Error Amp
  - Two mode PFC output Over-voltage-protection
    - Mode1: Dynamic OVP corresponding to a voltage rise by dynamic load change.
    - Mode2: Static OVP corresponding to over-voltage in stable.
  - PFC output Dynamic-under-voltage-protection (DUVP)
  - Feedback loop open/short detection
  - Master and Slave independence over-current-protection
  - 280  $\mu$ s restart timer
  - Slave ZCD signal open detection
  - Over current ON/OFF timer protection for boost Diode short
- Package
  - Pb-free SOP-16

### Ordering Information

Part No.	Package Name	Package Code	Package Abbreviation	Taping Abbreviation (Quantity)
R2A20112ASPW0	FP-16DAV	PRSP0016DH-B	SP	W (2,000 pcs/reel)

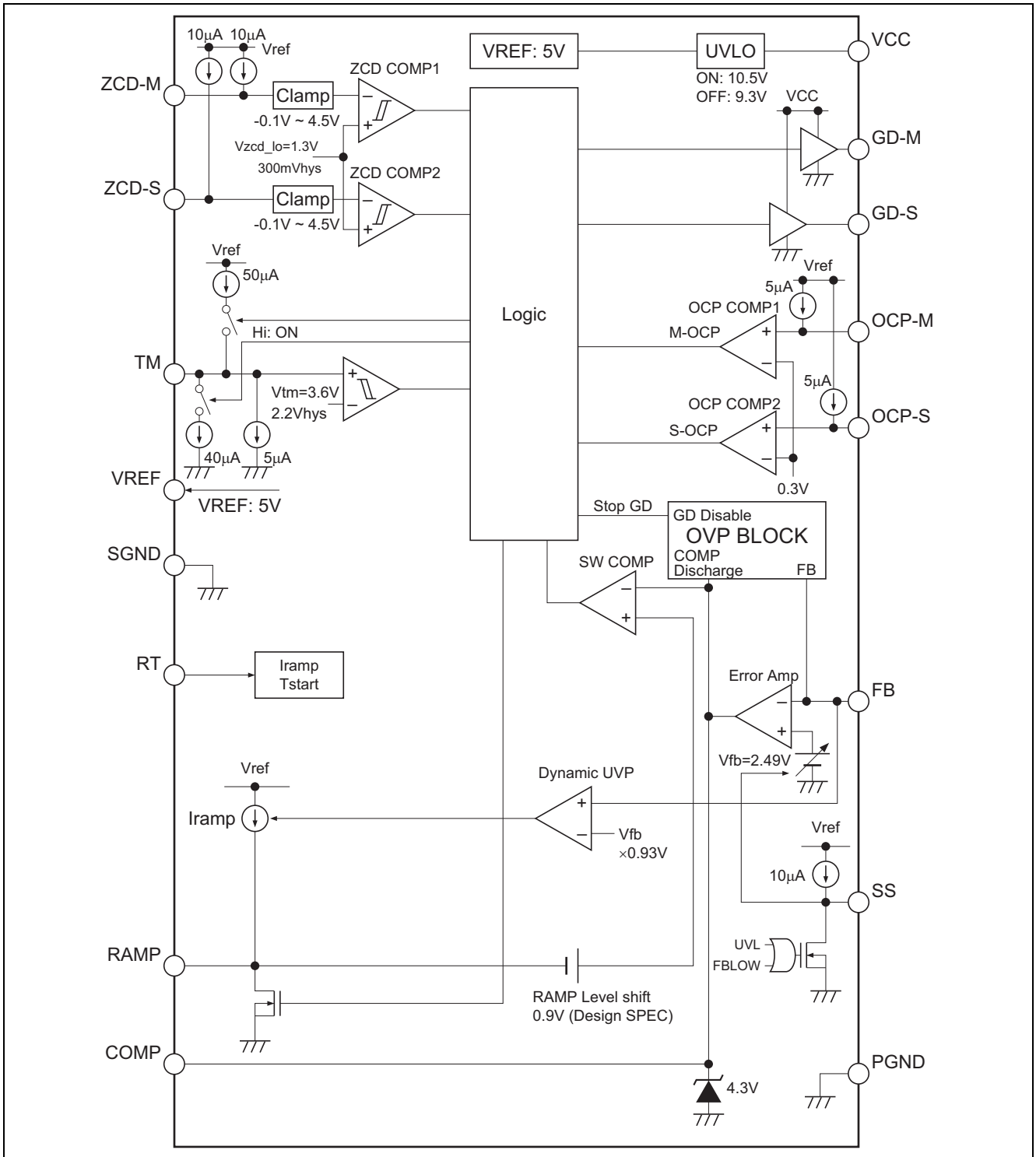
## Pin Arrangement



## Pin Functions

Pin No.	Pin Name	Function
1	ZCD-M	Master converter zero current detection input terminal
2	ZCD-S	Slave converter zero current detection input terminal
3	TM	Over current ON/OFF timer protection terminal
4	VREF	Reference voltage output terminal
5	SGND	Signal Ground
6	RAMP	Ramp waveform setting terminal
7	RT	Oscillator frequency setting terminal
8	COMP	Error amplifier output terminal
9	FB	Error amplifier input terminal
10	SS	Soft start time setting terminal
11	OCP-S	Slave converter overcurrent detection terminal
12	OCP-M	Master converter overcurrent detection terminal
13	GD-S	Slave converter Power MOSFET drive terminal
14	PGND	Power Ground
15	GD-M	Master converter Power MOSFET drive terminal
16	VCC	Supply voltage terminal

**Block Diagram**



## Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit	Notes
Supply voltage	VCC	-0.3 to +24	V	
GD terminal peak current	Ipk-gd	-300 +1200	mA	3
GD terminal DC current	I <sub>dc-gd</sub>	-15 +60	mA	
ZCD terminal current	I <sub>zcd</sub>	+3 -3	mA	
RT terminal current	I <sub>rt</sub>	-200	μA	4
Vref terminal current	I <sub>ref</sub>	-5	mA	
Vref terminal load capacitor	C <sub>ref min</sub>	1000	pF	
	C <sub>ref max</sub>	1	μF	
COMP terminal current	I <sub>comp</sub>	±1	mA	
Terminal voltage	V <sub>t-group1</sub>	-0.3 to V <sub>cc</sub>	V	5
	V <sub>t-group2</sub>	-0.3 to V <sub>ref</sub>	V	6
Vref terminal voltage	V <sub>t-ref</sub>	-0.3 to V <sub>ref</sub> + 0.3	V	
OCP terminal voltage	V <sub>t-ocp</sub>	*-1 to V <sub>ref</sub>	V	7
Power dissipation	P <sub>t</sub>	1	W	8
Operating ambient temperature	T <sub>a-opr</sub>	-40 to +125	°C	
Junction temperature	T <sub>j</sub>	-40 to +150	°C	9
Storage temperature	T <sub>stg</sub>	-55 to +150	°C	

Notes: 1. Rated voltages are with reference to the PGND terminal.

2. For rated currents, inflow to the IC is indicated by (+), and outflow by (-).

3. Shows the transient current when driving a capacitive load.

4. RT terminal's resistor is fixed 33 kΩ to GND.

5. This is the rated voltage for the following pins:

Nothing

6. This is the rated voltage for the following pins:

FB, SS, RAMP, TM

7. Minus value is peak voltage. Do not impress the DC voltage of the minus.

8.  $\theta_{ja} = 120^{\circ}\text{C/W}$

This value is a thing mounting on 40 × 40 (thickness: 1.6 mm) [mm<sup>2</sup>],  
a glass epoxy board of wiring density 10%.

9. Stresses exceeding the absolute maximum ratings may damage the device.

These are stress ratings only. Functional operation above the recommended operating ambient temperature range is not implied.

Extended exposure to stresses above the recommended operating ambient temperature range may affect device reliability.

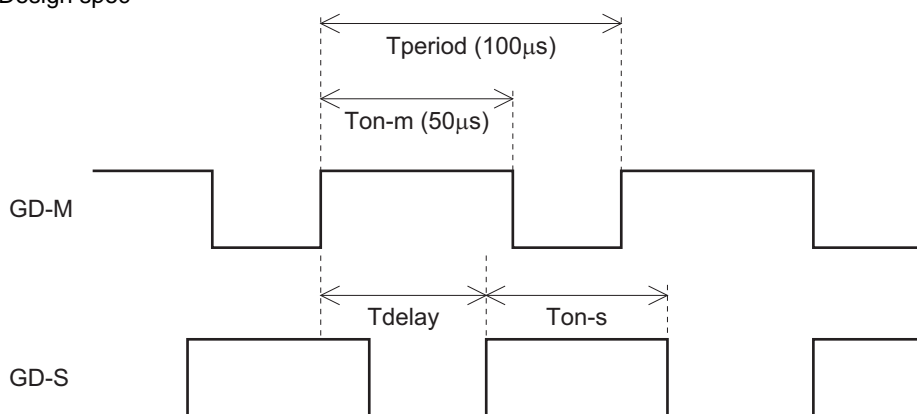
## Electrical Characteristics

(Ta = 25°C, VCC = 12 V, RT = 33 kΩ, RAMP = 820 pF, TM = 2.2 μF, SS = 1.0 μF, OCP = GND)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Supply	UVLO turn-on threshold	Vuvlh	9.8	10.5	11.2	V	
	UVLO turn-off threshold	Vuvll	8.8	9.3	9.8	V	
	UVLO hysteresis	Hysuvl	0.7	1.2	1.7	V	
	Standby current	Istby	—	85	170	μA	VCC = 8.9 V
	Operating current	Icc	—	4.2	6.3	mA	
VREF	Output voltage	Vref	4.925	5.00	5.075	V	Isource = -1 mA
	Line regulation	Vref-line	—	5	20	mV	Isource = -1 mA Vcc = 10 V to 24 V
	Load regulation	Vref-load	—	5	20	mV	Isource = -1 mA to -5 mA
	Temperature stability	dVref	—	±80	—	ppm/°C	Ta = -40 to +125°C *1
Error amplifier	Feedback voltage	Vfb	2.452	2.490	2.528	V	FB-COMP short
	Input bias current	Ifb	-0.5	-0.3	-0.1	μA	Measured pin: FB FB = 3 V *1
	Open loop gain	Av	—	60	—	dB	*1
	Upper clamp voltage	Vclamp-comp	4.2	4.3	4.4	V	FB = 2.0 V
	Low voltage	VI-comp	—	0.1	0.3	V	FB = 3.0 V
	Source current	Isrc-comp	—	-120	—	μA	FB = 1.5 V COMP = 2.5 V *1
	Sink current	Isnk-comp	—	330	—	μA	FB = 3.5 V COMP = 2.5 V
Ramp	RAMP charge current at DUVP disable condition	Ic-ramp1	-60	-50	-40	μA	FB = 2.4 V
	RAMP charge current at DUVP enable condition	Ic-ramp2	-32	-25	-18	μA	FB = 2 V
	RAMP discharge current	Id-ramp	7	15	29	mA	RAMP = 1 V
	Low voltage	VI-ramp	—	17	200	mV	I <sub>sink</sub> = 100 μA
Slave control	Phase delay	Phase	160	180	200	deg	FB = 2.5 V, COMP = 2 V
	On time ratio	Ton-ratio	0	—	5	%	*1, 2

Notes: \*1 Design spec

\*2



$$\text{Phase} = \frac{T_{\text{delay}}}{T_{\text{period}}} \times 360 \text{ [deg]}$$

$$\text{Ton-ratio} = \left(1 - \frac{T_{\text{on-s}}}{T_{\text{on-m}}}\right) \times 100 \text{ [%]}$$

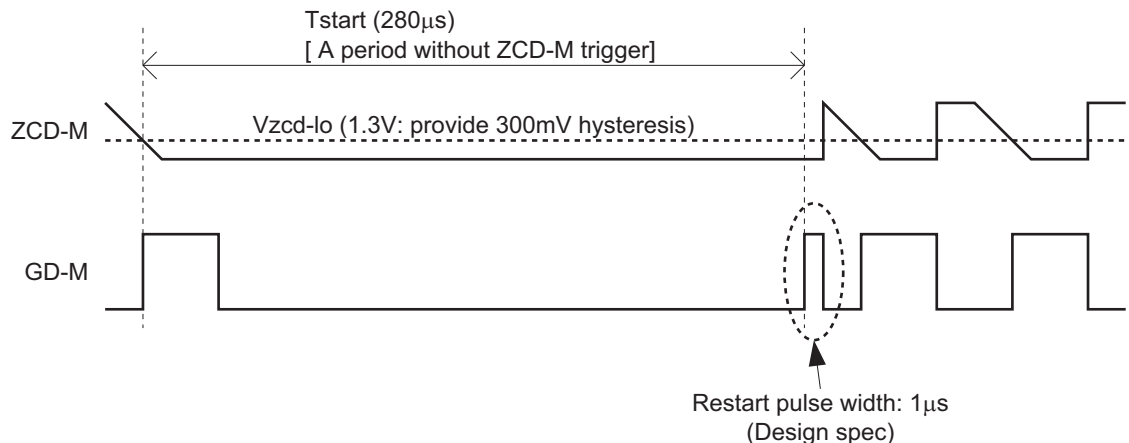
**Electrical Characteristics (cont.)**

(Ta = 25°C, VCC = 12 V, RT = 33 kΩ, RAMP = 820 pF, TM = 2.2 μF, SS = 1.0 μF, OCP = GND)

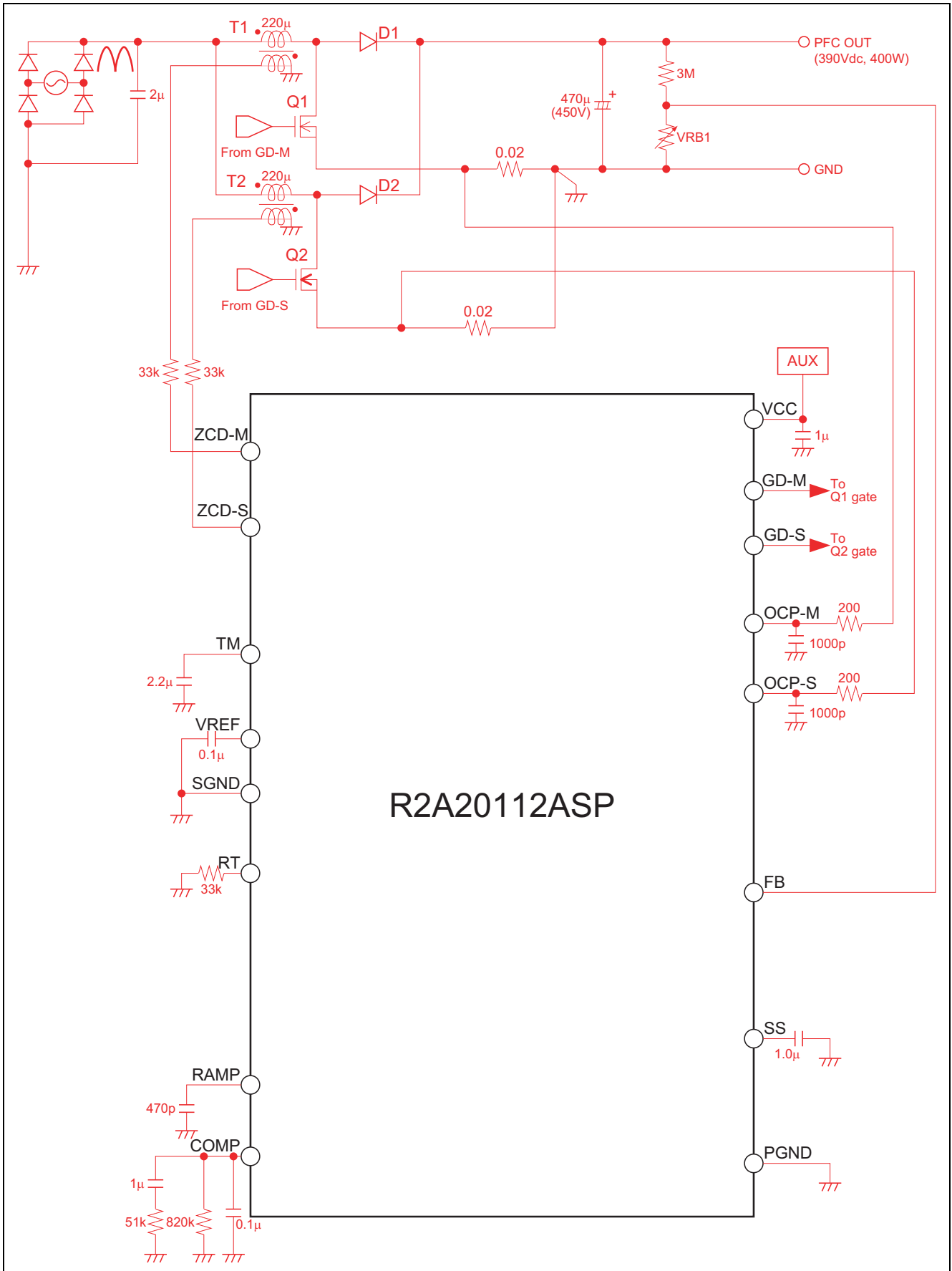
Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Gate drive (GD-M & GD-S)	Gate drive rise time	tr-gd	—	20	100	ns	FB-COMP short CL = 100 pF
	Gate drive fall time	tf-gd	—	5	30	ns	FB-COMP short CL = 100 pF
	Gate drive low voltage	Vol1-gd	—	0.02	0.1	V	Isink = 2 mA
		Vol2-gd	—	0.01	0.2	V	Isink = 1 mA, VCC = 5 V
Gate drive high voltage	Voh-gd	11.5	11.9	—	V	Isource = -2 mA *1	
Over current protection (OCP-M & OCP-S)	OCP threshold voltage	Vocp	0.27	0.30	0.33	V	
	OCP source current	Iocp	-10	-5	-2.5	μA	OCP = 0 V
ON/OFF timer protection for Boost diode short	ON/OFF timer threshold voltage	Vtm	3.52	3.6	3.68	V	
	ON/OFF timer hysteresis	Hys-tm	2.1	2.2	2.3	V	
	Charge current	Isrc-tm	-54	-45	-36	μA	TM = 2 V, OCP-M = 1 V
	Discharge current at TM disable condition	I <sub>snk-tm1</sub>	36	45	54	μA	TM = 2 V
	Discharge current at TM enable condition	I <sub>snk-tm2</sub>	4.2	5	5.8	μA	TM = 5 V to 2 V
PFC output abnormality protection	Dynamic OVP threshold voltage	Vdovp	Vfb× 1.035	Vfb× 1.050	Vfb× 1.065	V	COMP = 2.5 V
	Static OVP threshold voltage	Vsovp	Vfb× 1.075	Vfb× 1.090	Vfb× 1.105	V	COMP = 2.5 V
	Static OVP hysteresis	Hys-sovp	50	100	150	mV	COMP = 2.5 V
	Dynamic UVP threshold voltage	Vduvp	—	Vfb× 0.930	Vfb× 0.950	V	COMP = 2.5 V *1
	FB low detect threshold voltage	Vfblow	0.45	0.50	0.55	V	COMP = 2.5 V
	FB low detect hysteresis	Hysfblow	0.16	0.20	0.24	V	COMP = 2.5 V
Zero current detector (ZCD-M & ZCD-S)	Upper clamp voltage	Vzcdh	4.0	4.5	5.0	V	Isource = -3 mA
	Lower clamp voltage	Vzcdl	-0.5	-0.1	0.4	V	Isink = 3 mA
	ZCD low threshold voltage	Vzcd-lo	0.9	1.3	1.6	V	*1
	ZCD hysteresis	Hyszcd	130	300	410	mV	*1
	Input bias current	Izcd	-14	-10	-6	μA	1.2 V < Vzcd < 2.5 V
ZCD-S open detector	Slave ZCD open detect delay time	tzcds	—	100	—	ms	ZCD-S: OPEN Gate drive 10 kHz *1
Soft start	Charge current	Ic-ss	-14	-10	-6	μA	SS = 3 V, FB = 1 V
Restart	Restart time delay	Tstart	210	280	350	μs	ZCD-M = 10 kΩ to GND ZCD-S = 10 kΩ to GND *2

Notes: \*1 Design spec

\*2

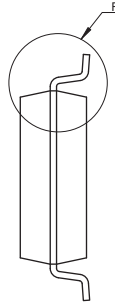
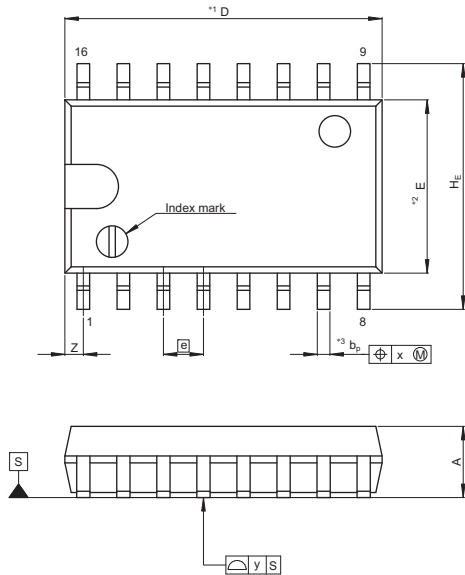


System Diagram

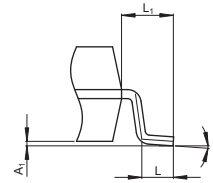
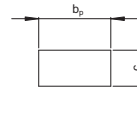


### Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SOP16-5.5x10.06-1.27	PRSP0016DH-B	FP-16DAV	0.24g



Terminal cross section  
( Ni/Pd/Au plating )



Detail F

NOTE)  
1. DIMENSIONS\*\*1 (Nom)\*AND\*\*2\*  
DO NOT INCLUDE MOLD FLASH.  
2. DIMENSION\*\*3\*DOES NOT  
INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	10.06	10.5
E	—	5.50	—
A <sub>2</sub>	—	—	—
A <sub>1</sub>	0.00	0.10	0.20
A	—	—	2.20
b <sub>p</sub>	0.34	0.40	0.46
b <sub>1</sub>	—	—	—
c	0.15	0.20	0.25
c <sub>1</sub>	—	—	—
θ	0°	—	8°
H <sub>E</sub>	7.50	7.80	8.00
[e]	—	1.27	—
x	—	—	0.12
y	—	—	0.15
Z	—	—	0.80
L	0.50	0.70	0.90
L <sub>1</sub>	—	1.15	—

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Tel: +1-408-588-6000, Fax: +1-408-588-6130

**Renesas Electronics Canada Limited**  
9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3  
Tel: +1-905-237-2004

**Renesas Electronics Europe Limited**  
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K  
Tel: +44-1628-585-100, Fax: +44-1628-585-900

**Renesas Electronics Europe GmbH**  
Arcadiastrasse 10, 40472 Düsseldorf, Germany  
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

**Renesas Electronics (China) Co., Ltd.**  
Room 1709, Quantum Plaza, No.27 ZhichunLu Haidian District, Beijing 100191, P.R.China  
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

**Renesas Electronics (Shanghai) Co., Ltd.**  
Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, P. R. China 200333  
Tel: +86-21-2226-0888, Fax: +86-21-2226-0899

**Renesas Electronics Hong Kong Limited**  
Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong  
Tel: +852-2265-8688, Fax: +852-2886-9022

**Renesas Electronics Taiwan Co., Ltd.**  
13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan  
Tel: +886-2-8175-9600, Fax: +886-2-8175-9670

**Renesas Electronics Singapore Pte. Ltd.**  
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949  
Tel: +65-6213-0200, Fax: +65-6213-0300

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Unit 1207, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jin Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia  
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

**Renesas Electronics India Pvt. Ltd.**  
No.777C, 100 Feet Road, HAL II Stage, Indiranagar, Bangalore, India  
Tel: +91-80-67208700, Fax: +91-80-67208777

**Renesas Electronics Korea Co., Ltd.**  
12F., 234 Teheran-ro, Gangnam-Gu, Seoul, 135-080, Korea  
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