

P-Channel 20 V (D-S) MOSFET with Schottky Diode

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A) ^a	Q_g (Typ.)
- 20	0.084 at $V_{GS} = - 10$ V	- 4 ^f	4 nC
	0.108 at $V_{GS} = - 4.5$ V	- 4 ^f	
	0.175 at $V_{GS} = - 2.5$ V	- 3.5	

SCHOTTKY PRODUCT SUMMARY

V_{KA} (V)	V_f (V) Diode Forward Voltage	I_F (A) ^a
20	0.5 at 1 A	2

FEATURES

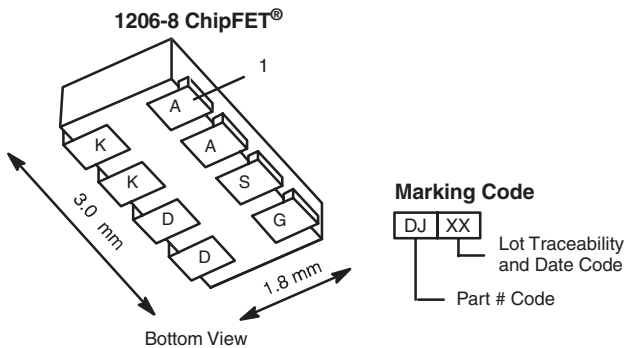
- Halogen-free According to IEC 61249-2-21 Definition
- LITTLE FOOT® Plus Schottky Power MOSFET
- Compliant to RoHS Directive 2002/95/EC



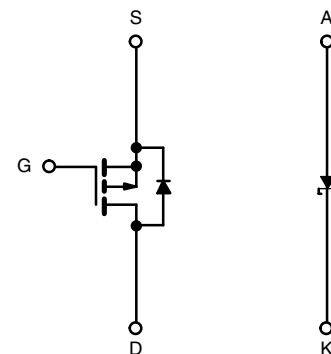
RoHS
COMPLIANT
HALOGEN
FREE
Available

APPLICATIONS

- HDD
- DC/DC Converter
- Asynchronous Rectification



Ordering Information: Si5913DC-T1-E3 (Lead (Pb)-free)
Si5913DC-T1-GE3 (Lead (Pb)-free and Halogen-free)



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS $T_A = 25^\circ\text{C}$, unless otherwise noted

Parameter		Symbol	Limit	Unit	
Drain-Source Voltage (MOSFET)		V _{DS}	- 20	V	
Reverse Voltage (Schottky)		V _{KA}	20		
Gate-Source Voltage (MOSFET)		V _{GS}	± 12		
Continuous Drain Current (T _J = 150 °C) (MOSFET)	T _C = 25 °C	I _D	- 4 ^f	A	
	T _C = 70 °C		- 4 ^f		
	T _A = 25 °C		- 3.7 ^{b, c}		
	T _A = 70 °C		- 2.9 ^{b, c}		
Pulsed Drain Current (MOSFET)		I _{DM}	- 15		
Continuous Source-Drain Diode Current (MOSFET Diode Conduction)	T _C = 25 °C	I _S	- 2.6		
	T _A = 25 °C		- 1.4 ^{b, c}		
Average Forward Current (Schottky)		I _F	2 ^b		
Pulsed Forward Current (Schottky)		I _{FM}	5		
Maximum Power Dissipation (MOSFET)	T _C = 25 °C	P _D	3.1	W	
	T _C = 70 °C		2.0		
	T _A = 25 °C		1.7 ^{b, c}		
	T _A = 70 °C		1.1 ^{b, c}		
Maximum Power Dissipation (Schottky)	T _C = 25 °C		3.1		
	T _C = 70 °C		2.0		
	T _A = 25 °C		1.3 ^{b, c}		
	T _A = 70 °C		0.8 ^{b, c}		
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150	°C	
Soldering Recommendation (Peak Temperature) ^{g, h}			260		

THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient (MOSFET) ^{b, d}	$t \leq 5$ s	R_{thJA}	62	74	°C/W
Maximum Junction-to-Foot (Drain) (MOSFET)	Steady State	R_{thJF}	32	40	
Maximum Junction-to-Ambient (Schottky) ^{b, e}	$t \leq 5$ s	R_{thJA}	77	95	
Maximum Junction-to-Foot (Drain) (Schottky)	Steady State	R_{thJF}	33	40	

Notes:

a. Based on $T_C = 25$ °C.

b. Surface mounted on 1" x 1" FR4 board.

c. $t = 5$ s

d. Maximum under steady state conditions is 115 °C/W.

e. Maximum under steady state conditions is 130 °C/W.

f. Package limited.

g. See Solder Profile (www.vishay.com/doc?73257). The ChipFET is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side soldering interconnection.

h. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.

SPECIFICATIONS $T_J = 25$ °C, unless otherwise noted

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0$ V, $I_D = -250$ μ A	- 20			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = -250$ μ A		- 20		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			3		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = -250$ μ A	- 0.6		- 1.5	V
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0$ V, $V_{GS} = \pm 12$ V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -20$ V, $V_{GS} = 0$ V			- 1	μ A
		$V_{DS} = -20$ V, $V_{GS} = 0$ V, $T_J = 55$ °C			- 10	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \leq 5$ V, $V_{GS} = -10$ V	- 15			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = -10$ V, $I_D = -3.7$ A		0.070	0.084	Ω
		$V_{GS} = -4.5$ V, $I_D = -3.2$ A		0.090	0.108	
		$V_{GS} = -2.5$ V, $I_D = -2.5$ A		0.140	0.175	
Forward Transconductance ^a	g_{fs}	$V_{DS} = -10$ V, $I_D = -3.7$ A		6		S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{DS} = -10$ V, $V_{GS} = 0$ V, $f = 1$ MHz		330		pF
Output Capacitance	C_{oss}			80		
Reverse Transfer Capacitance	C_{rss}			57		
Total Gate Charge	Q_g	$V_{DS} = -10$ V, $V_{GS} = -10$ V, $I_D = -3.7$ A		8	12	nC
Gate-Source Charge	Q_{gs}	$V_{DS} = -10$ V, $V_{GS} = -4.5$ V, $I_D = -3.7$ A		4	6	
Gate-Drain Charge	Q_{gd}			0.8		
Gate Resistance	R_g	$f = 1$ MHz	1.2	6	12	Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -10$ V, $R_L = 3.4$ Ω $I_D \cong -2.9$ A, $V_{GEN} = -10$ V, $R_g = 1$ Ω		3	6	ns
Rise Time	t_r			10	20	
Turn-Off Delay Time	$t_{d(off)}$			16	24	
Fall Time	t_f			8	15	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -10$ V, $R_L = 3.4$ Ω $I_D \cong -2.9$ A, $V_{GEN} = -4.5$ V, $R_g = 1$ Ω		18	27	
Rise Time	t_r			40	60	
Turn-Off Delay Time	$t_{d(off)}$			18	27	
Fall Time	t_f			10	15	



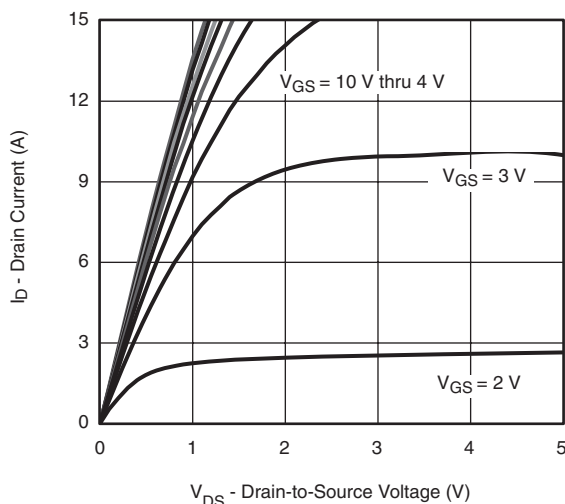
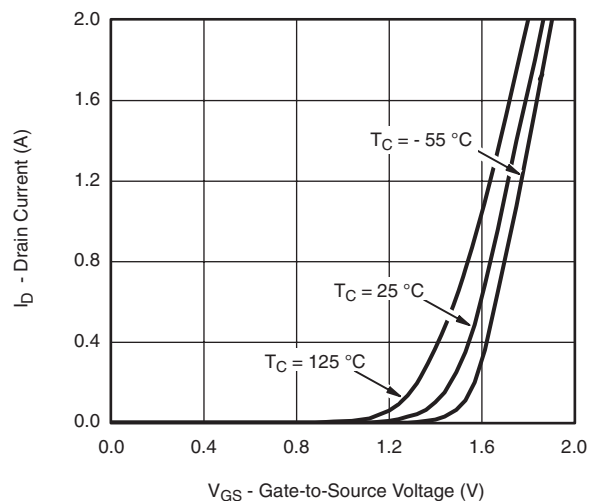
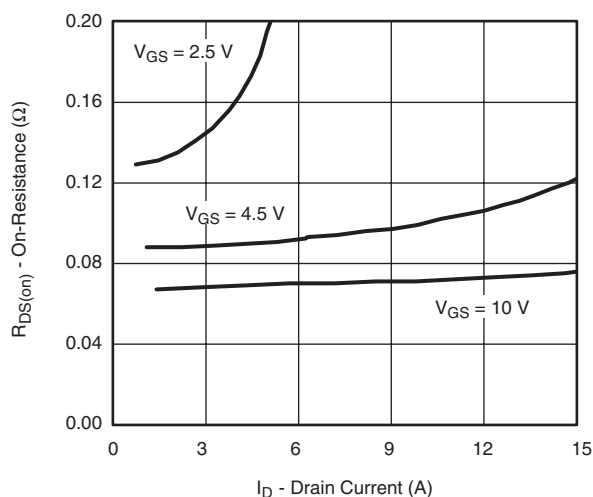
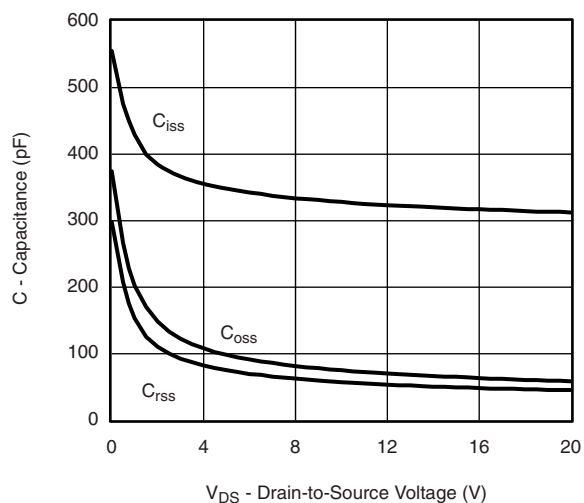
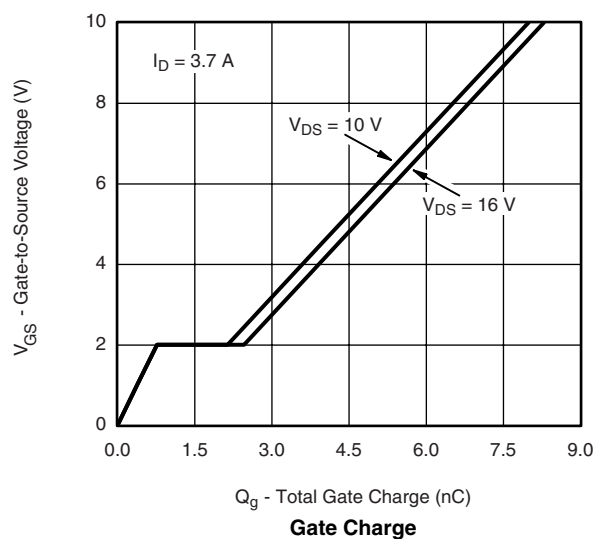
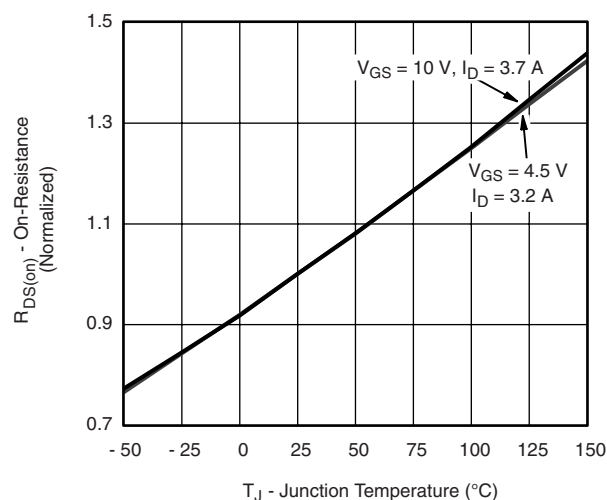
SPECIFICATIONS $T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^{\circ}\text{C}$			- 1.2	A
Pulse Diode Forward Current	I_{SM}				- 15	
Body Diode Voltage	V_{SD}	$I_S = - 2.9\text{ A}$, $V_{GS} = 0\text{ V}$		- 0.75	- 1.2	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = - 2.9\text{ A}$, $dI/dt = 100\text{ A}/\mu\text{s}$, $T_J = 25\text{ }^{\circ}\text{C}$		23	35	ns
Body Diode Reverse Recovery Charge	Q_{rr}			14	21	nC
Reverse Recovery Fall Time	t_a			11		ns
Reverse Recovery Rise Time	t_b			12		

Notes:

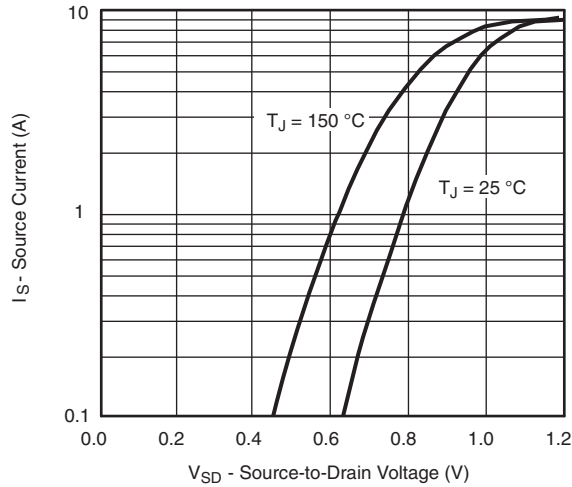
- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.

SCHOTTKY SPECIFICATIONS $T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Forward Voltage Drop	V_F	$I_F = 1\text{ A}$		0.42	0.50	V
		$I_F = 1\text{ A}$, $T_J = 125\text{ }^{\circ}\text{C}$		0.36	0.43	
Maximum Reverse Leakage Current	I_{rm}	$V_r = 5\text{ V}$		0.015	0.08	mA
		$V_r = 5\text{ V}$, $T_J = 85\text{ }^{\circ}\text{C}$		0.50	5.00	
		$V_r = 20\text{ V}$		0.02	0.10	
		$V_r = 20\text{ V}$, $T_J = 85\text{ }^{\circ}\text{C}$		0.7	7.00	
		$V_r = 20\text{ V}$, $T_J = 125\text{ }^{\circ}\text{C}$		5	50	
Junction Capacitance	C_T	$V_r = 10\text{ V}$		60		pF

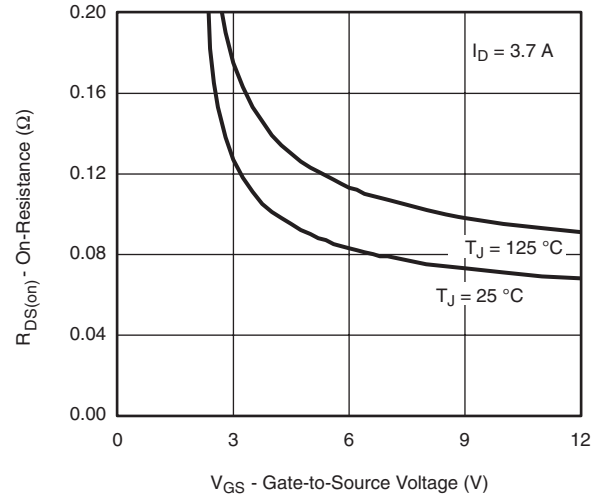
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

MOSFET TYPICAL CHARACTERISTICS $T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted

Output Characteristics

Transfer Characteristics

On-Resistance vs. Drain Current and Gate Voltage

Capacitance

Gate Charge

On-Resistance vs. Junction Temperature

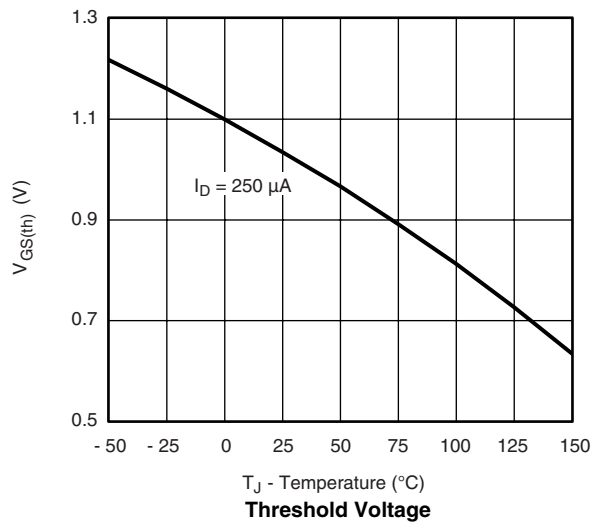
MOSFET TYPICAL CHARACTERISTICS $T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted



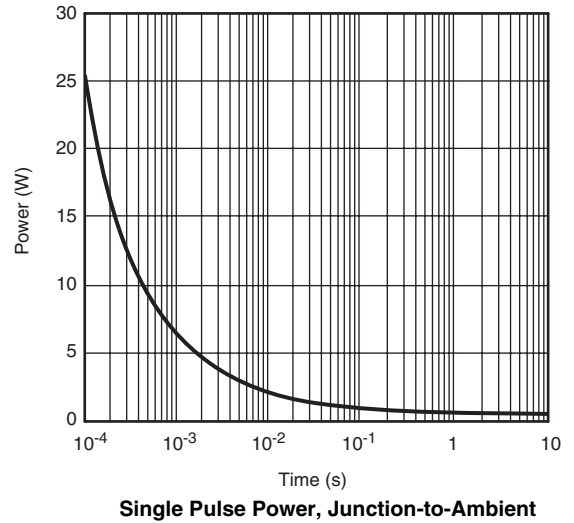
Source-Drain Diode Forward Voltage



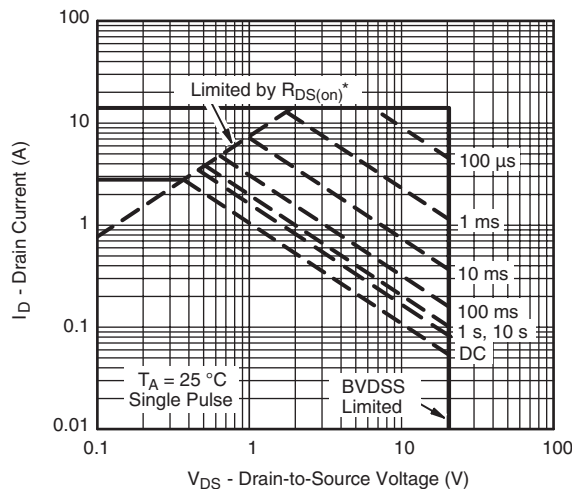
On-Resistance vs. Gate-to-Source Voltage



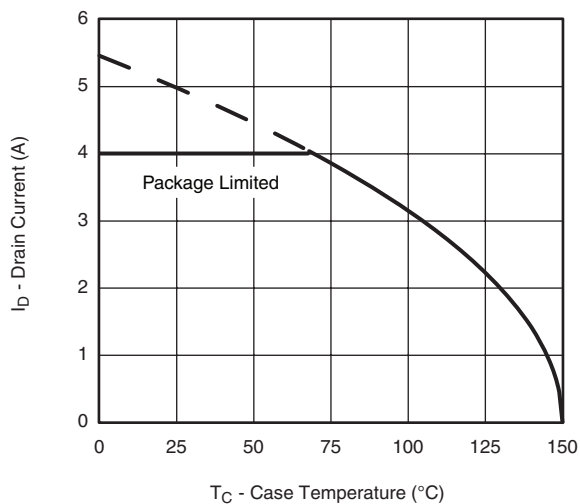
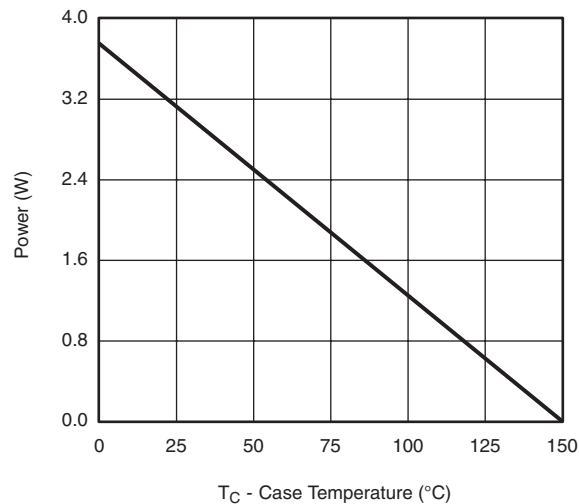
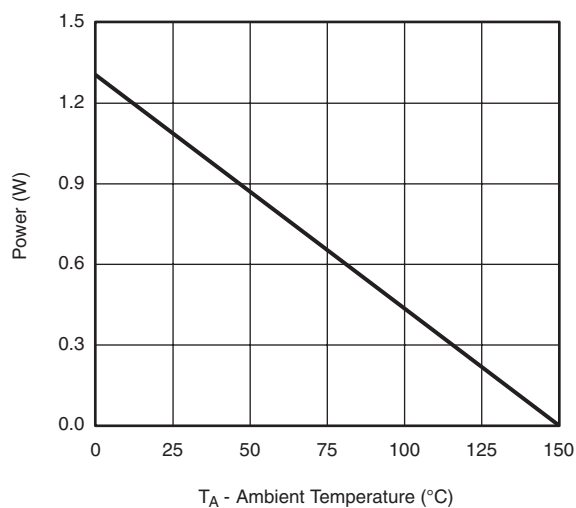
Threshold Voltage



Single Pulse Power, Junction-to-Ambient

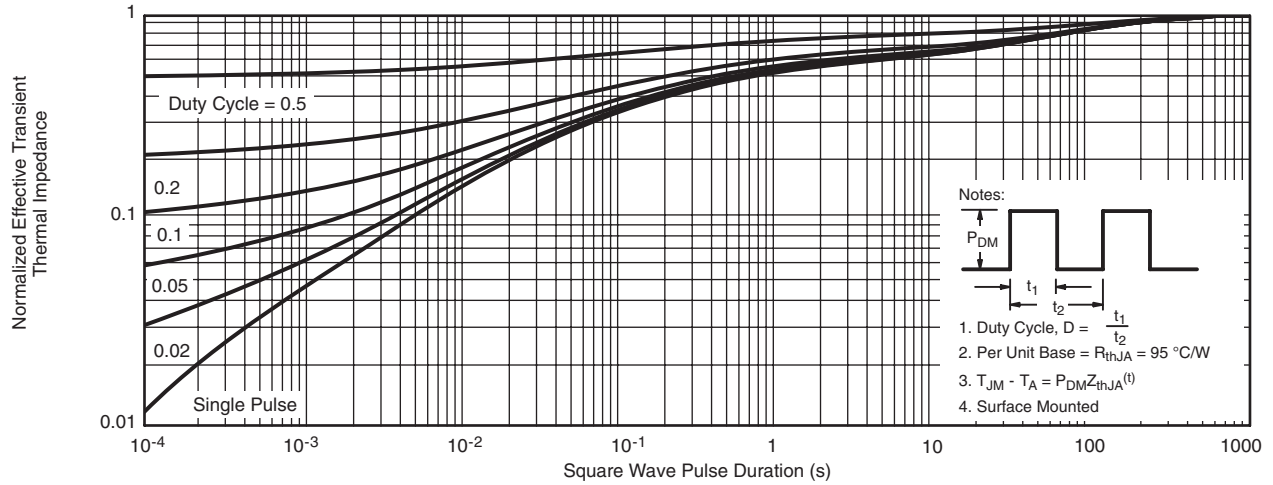


* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified
Safe Operating Area, Junction-to-Case

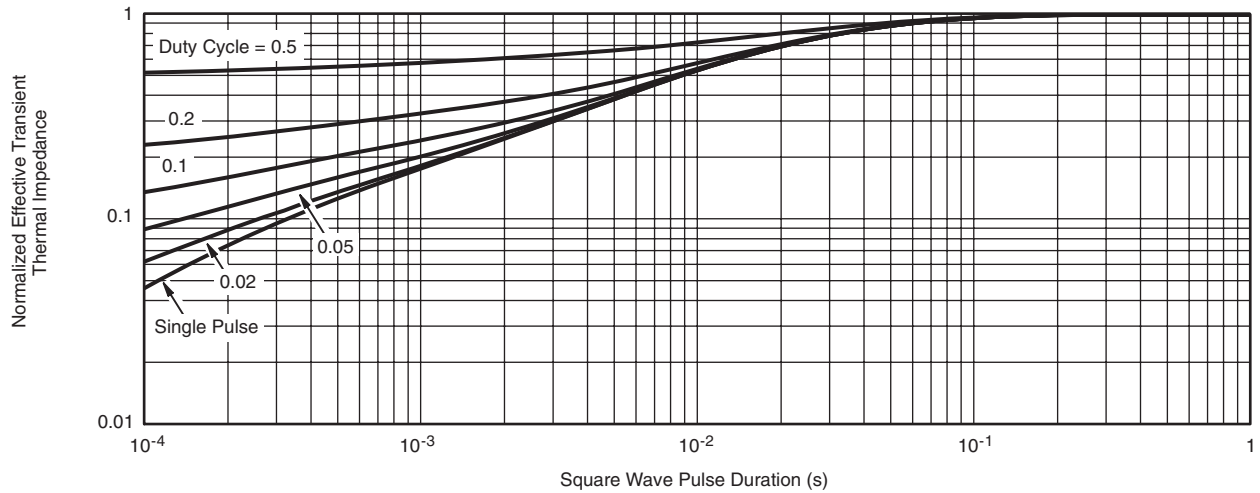
MOSFET TYPICAL CHARACTERISTICS $T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted

Current Derating*

Power Derating, Junction-to-Foot

Power Derating, Junction-to-Ambient

* The power dissipation P_D is based on $T_{J(\max)} = 150\text{ }^{\circ}\text{C}$, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

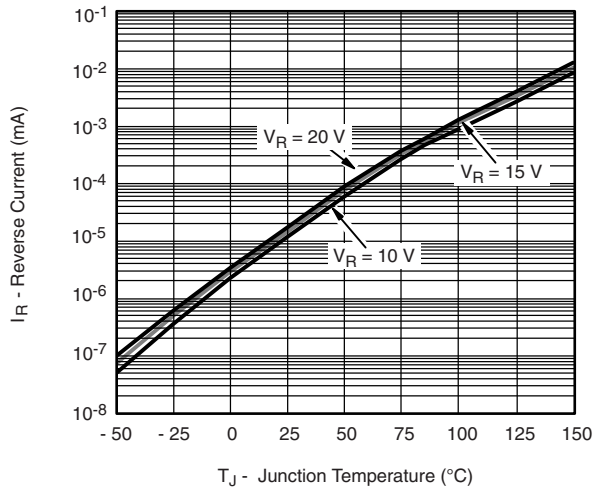
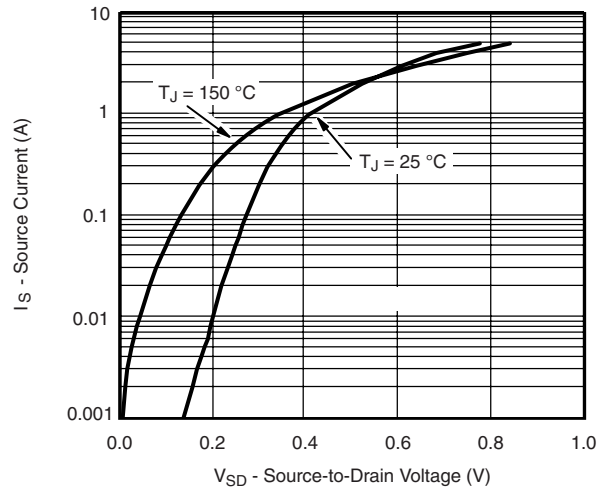
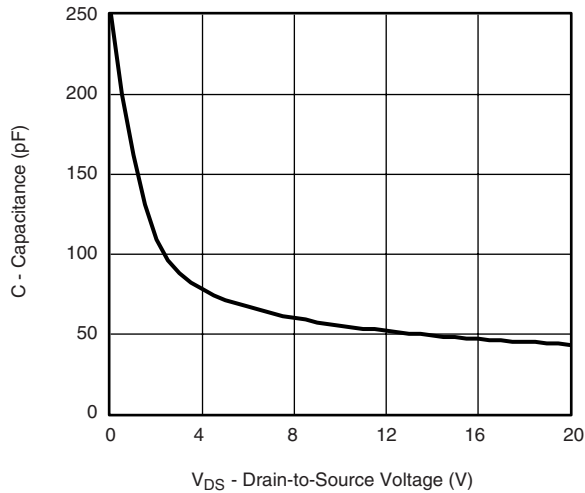
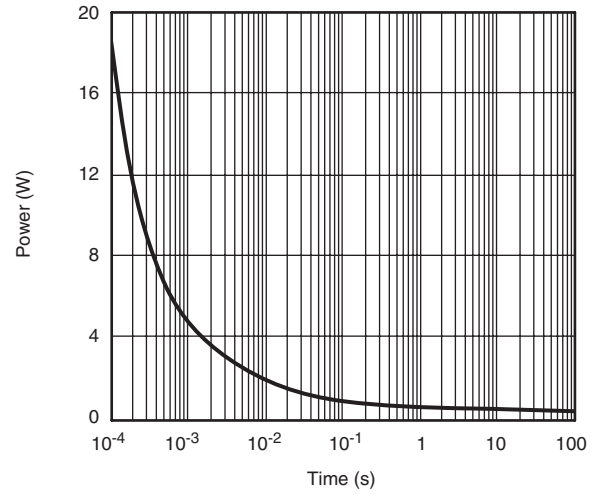
MOSFET TYPICAL CHARACTERISTICS $T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted



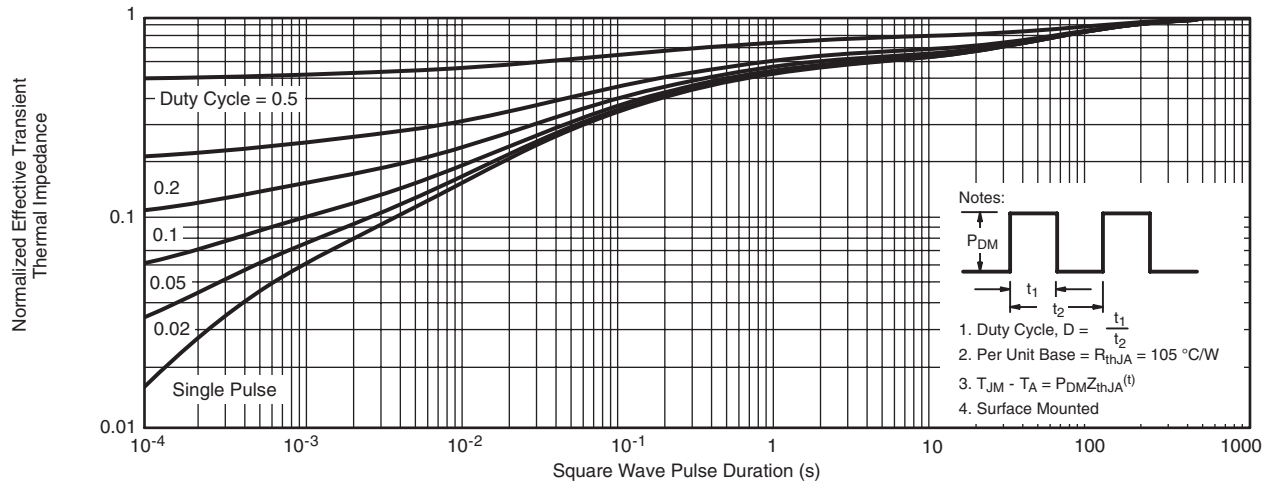
Normalized Thermal Transient Impedance, Junction-to-Ambient



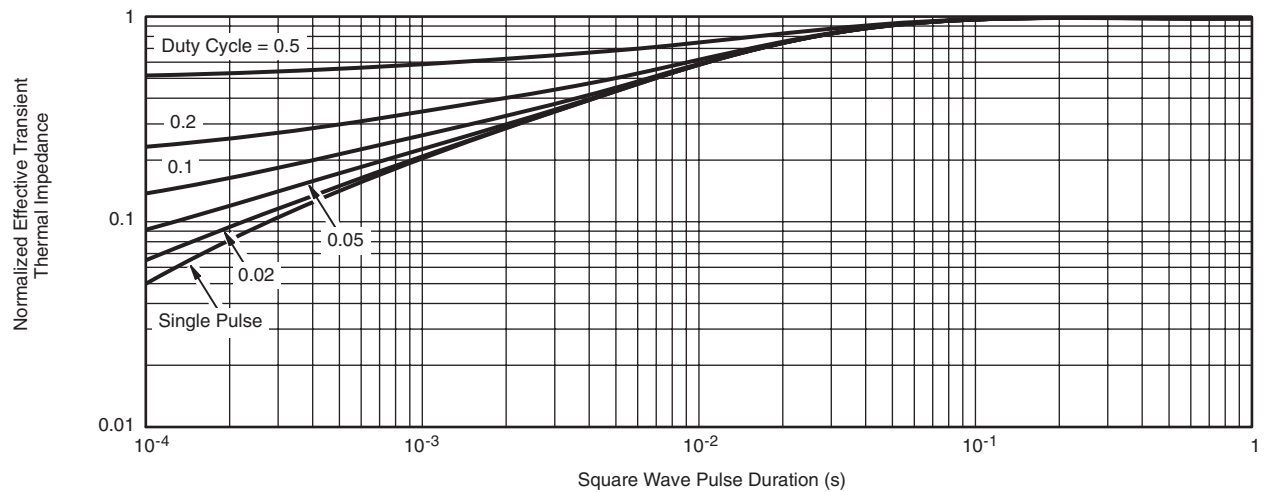
Normalized Thermal Transient Impedance, Junction-to-Foot

SCHOTTKY TYPICAL CHARACTERISTICS $T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted

Reverse Current vs. Junction Temperature

Forward Diode Voltage

Capacitance

Single Pulse Power, Junction-to-Ambient

SCHOTTKY TYPICAL CHARACTERISTICS $T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Ambient

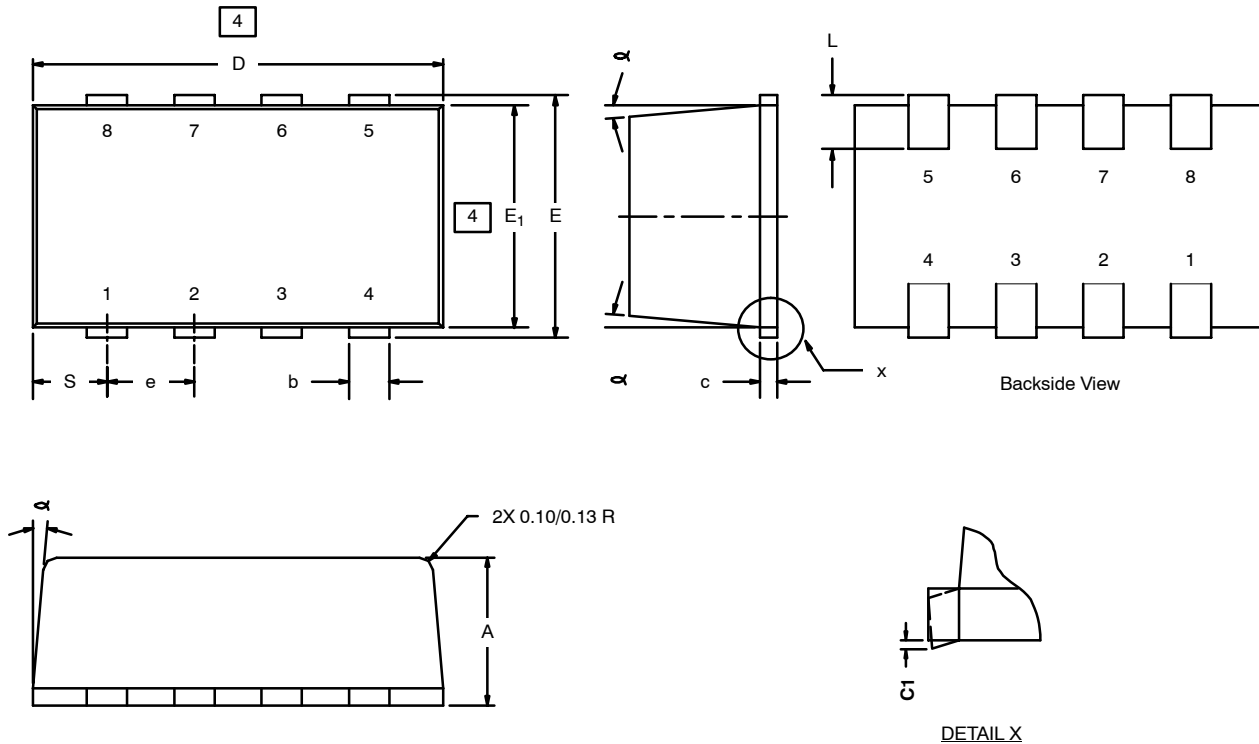


Normalized Thermal Transient Impedance, Junction-to-Foot

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?68920.



1206-8 ChipFET®

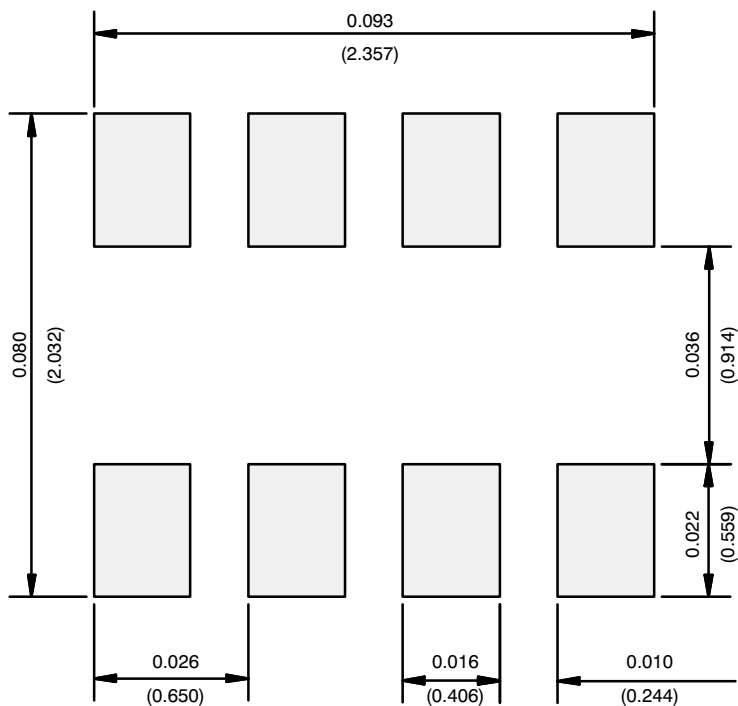


NOTES:

1. All dimensions are in millimeters.
2. Mold gate burrs shall not exceed 0.13 mm per side.
3. Leadframe to molded body offset is horizontal and vertical shall not exceed 0.08 mm.
4. Dimensions exclusive of mold gate burrs.
5. No mold flash allowed on the top and bottom lead surface.

Dim	MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max
A	1.00	–	1.10	0.039	–	0.043
b	0.25	0.30	0.35	0.010	0.012	0.014
c	0.1	0.15	0.20	0.004	0.006	0.008
c1	0	–	0.038	0	–	0.0015
D	2.95	3.05	3.10	0.116	0.120	0.122
E	1.825	1.90	1.975	0.072	0.075	0.078
E ₁	1.55	1.65	1.70	0.061	0.065	0.067
e	0.65 BSC			0.0256 BSC		
L	0.28	–	0.42	0.011	–	0.017
S	0.55 BSC			0.022 BSC		
α	5°Nom			5°Nom		
ECN: C-03528—Rev. F, 19-Jan-04						
DWG: 5547						

RECOMMENDED MINIMUM PADS FOR 1206-8 ChipFET®



Recommended Minimum Pads
Dimensions in Inches/(mm)

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