



P-Channel 8 V (D-S) MOSFET

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)	Q_g (Typ.)
- 8	0.034 at $V_{GS} = - 4.5$ V	- 9 ^a	10.5 nC
	0.063 at $V_{GS} = - 1.8$ V	- 5	
	0.084 at $V_{GS} = - 1.5$ V	- 3	
	0.180 at $V_{GS} = - 1.2$ V	- 1	

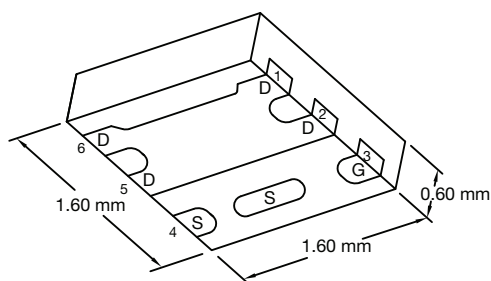
FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET® Power MOSFET
- New Thermally Enhanced PowerPAK® SC-75 Package with ultra-thin 0.6 mm height
 - Small Footprint Area
 - Low On-Resistance
- 100 % R_g Tested
- Typical ESD Performance 2000 V
- Built in ESD Protection with Zener Diode
- Compliant to RoHS Directive 2002/95/EC



RoHS
COMPLIANT
HALOGEN
FREE

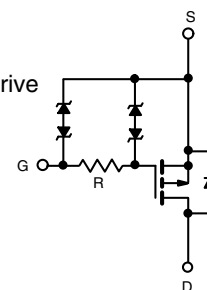
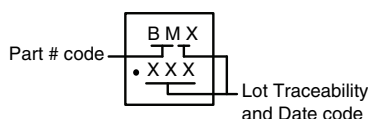
Thin PowerPAK SC-75-6L-Single



APPLICATIONS

- Load Switch for Portable Devices
- Load Switch for Low Voltage Gate Drive

Marking Code



Ordering Information: SiB437EDKT-T1-GE3 (Lead (Pb)-free and Halogen-free)

P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	- 8	V
Gate-Source Voltage	V_{GS}	± 5	
Continuous Drain Current ($T_J = 150$ °C)	$T_C = 25$ °C	- 9 ^a	A
	$T_C = 70$ °C	- 9 ^a	
	$T_A = 25$ °C	- 7.5 ^{b, c}	
	$T_A = 70$ °C	- 6 ^{b, c}	
Pulsed Drain Current	I_{DM}	- 25	
Continuous Source-Drain Diode Current	$T_C = 25$ °C	- 9 ^a	
	$T_A = 25$ °C	- 2 ^{b, c}	
Maximum Power Dissipation	$T_C = 25$ °C	13	W
	$T_C = 70$ °C	8.4	
	$T_A = 25$ °C	2.4 ^{b, c}	
	$T_A = 70$ °C	1.6 ^{b, c}	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150	°C
Soldering Recommendations (Peak Temperature) ^{d, e}		260	

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{b, f}	R_{thJA}	41	51	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	7.5	9.5	

Notes:

a. Package limited.

b. Surface mounted on 1" x 1" FR4 board.

c. $t = 5$ s.

d. See solder profile (www.vishay.com/ppg?73257). The Thin PowerPAK SC-75 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.

f. Maximum under steady state conditions is 105 °C/W.

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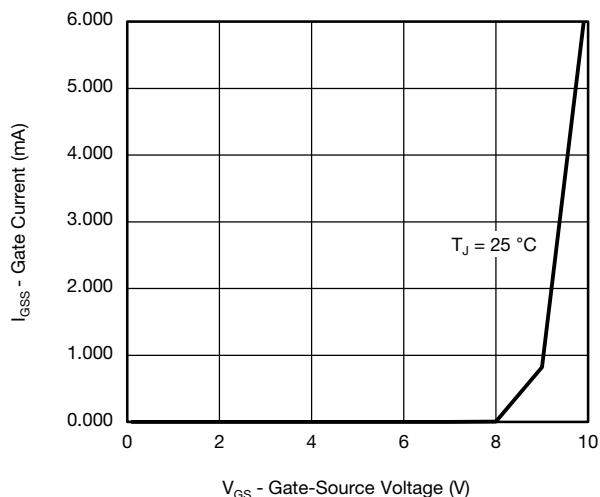
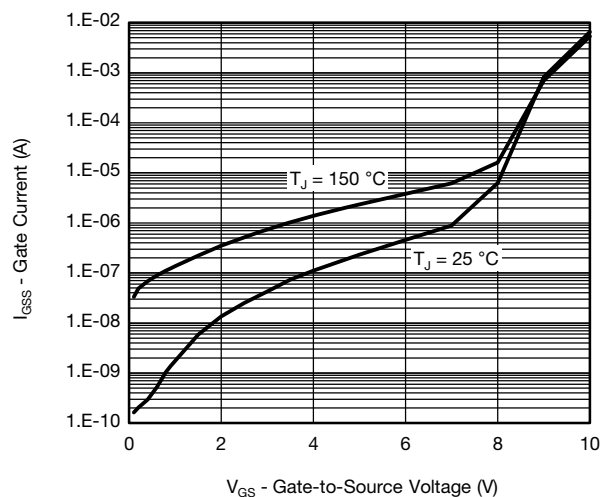
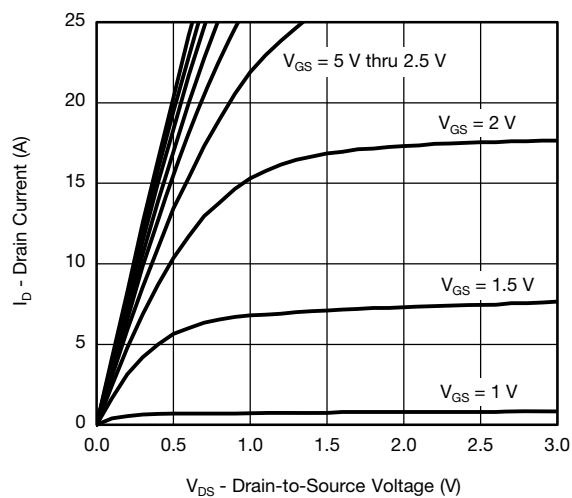
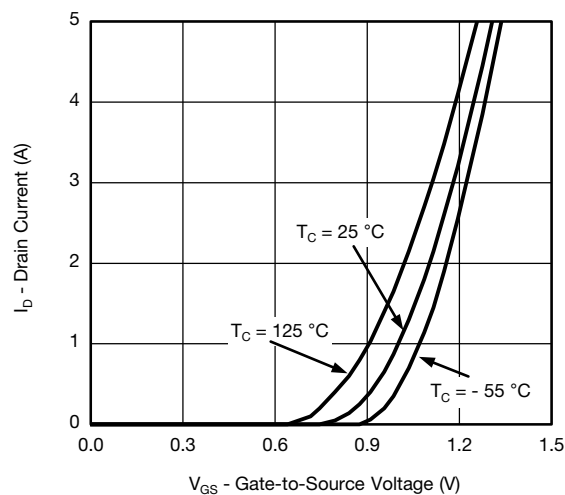
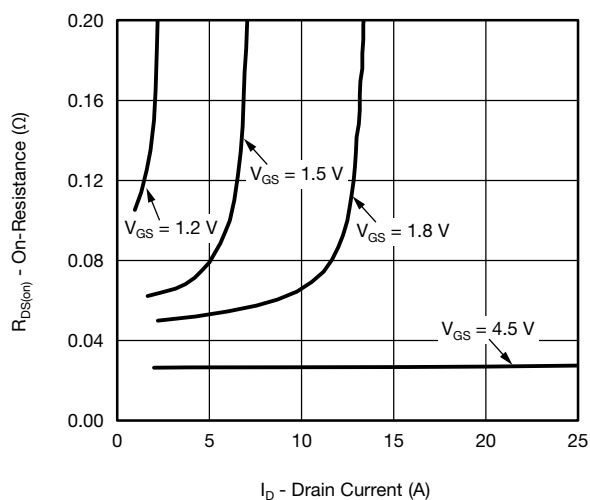
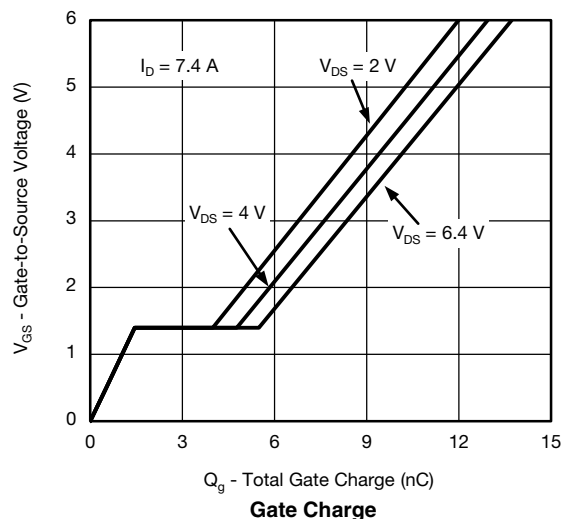
SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = - 250 μA	- 8			V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	I _D = - 250 μA		- 2		mV/°C
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)} /T _J			2.2		
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = - 250 μA	- 0.35		- 0.7	V
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 5 V			± 5	μA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = - 8 V, V _{GS} = 0 V			- 1	
		V _{DS} = - 8 V, V _{GS} = 0 V, T _J = 55 °C			- 10	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≤ - 5 V, V _{GS} = - 4.5 V	- 15			A
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = - 4.5 V, I _D = - 3 A		0.028	0.034	Ω
		V _{GS} = - 1.8 V, I _D = - 1 A		0.050	0.063	
		V _{GS} = - 1.5 V, I _D = - 0.5 A		0.060	0.084	
		V _{GS} = - 1.2 V, I _D = - 0.5 A		0.100	0.180	
Forward Transconductance ^a	g _{fs}	V _{DS} = - 4 V, I _D = - 3 A		14		S
Dynamic ^b						
Total Gate Charge	Q _g	V _{DS} = - 4 V, V _{GS} = - 4.5 V, I _D = - 7.4 A		10.5	16	nC
Gate-Source Charge	Q _{gs}			1.5		
Gate-Drain Charge	Q _{gd}			3.3		
Gate Resistance	R _g	f = 1 MHz	80	400	800	Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = - 4 V, R _L = 0.7 Ω I _D ≅ - 6 A, V _{GEN} = - 4.5 V, R _g = 1 Ω		90	180	ns
Rise Time	t _r			170	340	
Turn-Off Delay Time	t _{d(off)}			690	1380	
Fall Time	t _f			630	1260	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C			- 9	A
Pulse Diode Forward Current	I _{SM}				- 25	
Body Diode Voltage	V _{SD}	I _S = - 6 A, V _{GS} = 0 V		- 0.8	- 1.2	V
Body Diode Reverse Recovery Time	t _{rr}	I _F = - 6 A, dI/dt = 100 A/μs, T _J = 25 °C		30	60	ns
Body Diode Reverse Recovery Charge	Q _{rr}			12	25	nC
Reverse Recovery Fall Time	t _a			12		ns
Reverse Recovery Rise Time	t _b			18		

Notes:

a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

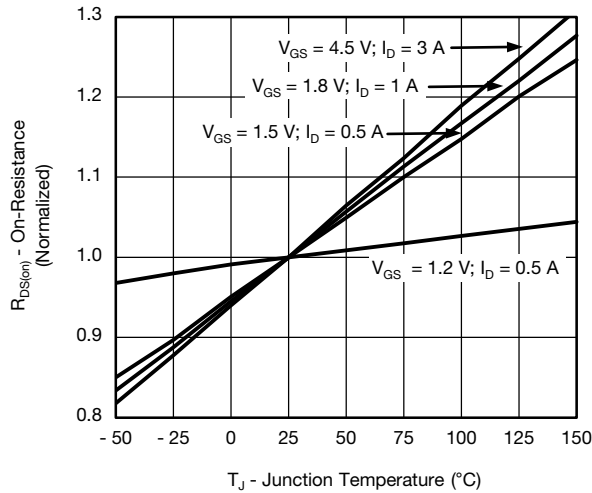
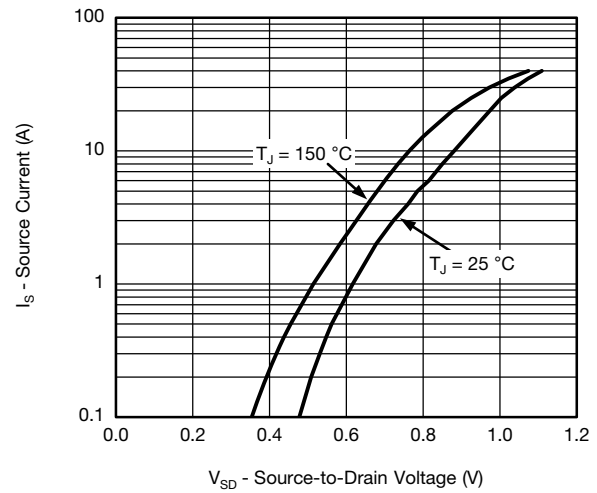
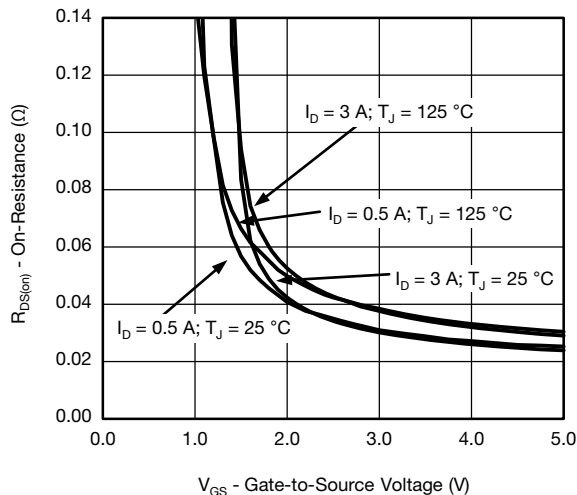
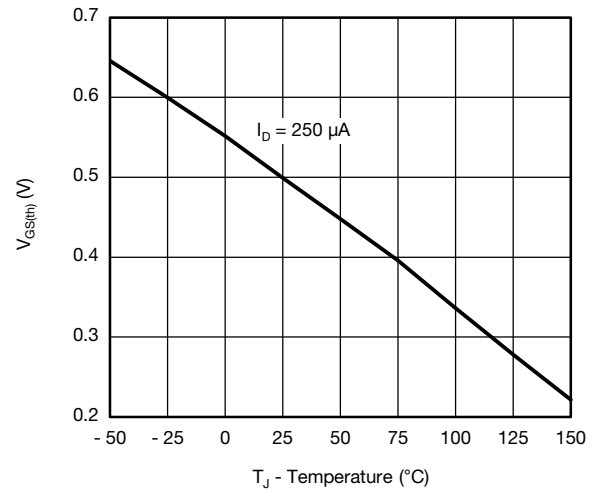
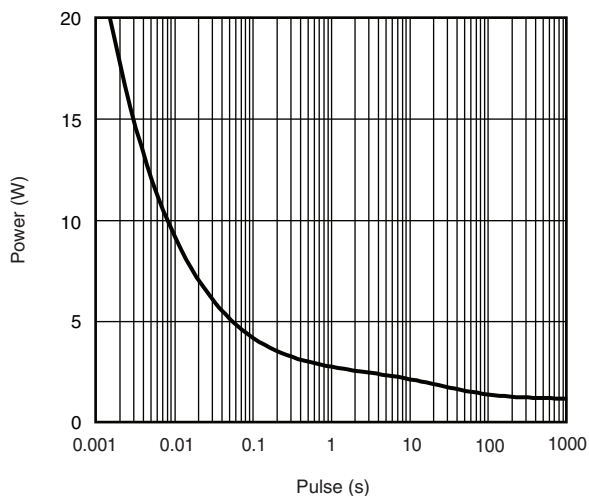
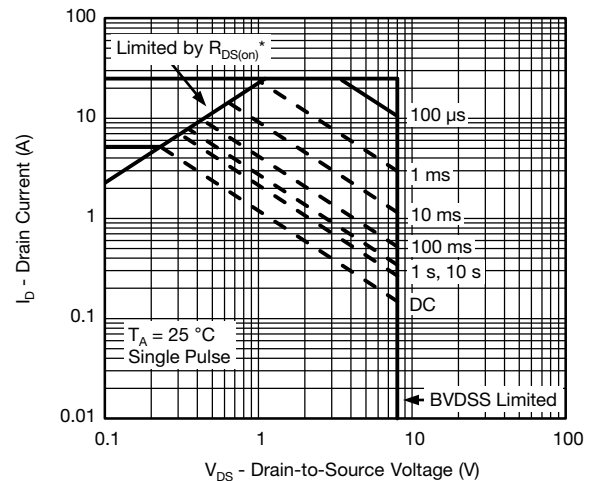
b. Guaranteed by design, not subject to production testing.

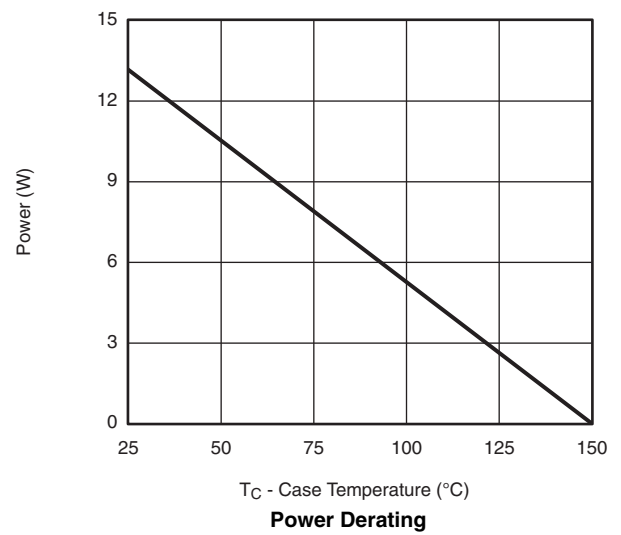
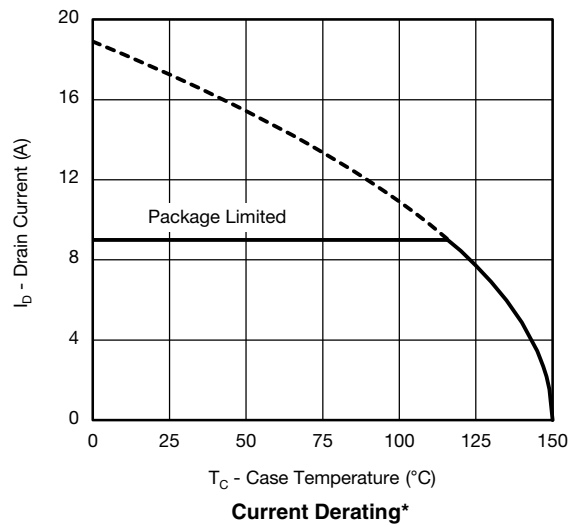
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)**Gate Current vs. Gate-Source Voltage****Gate Current vs. Gate-Source Voltage****Output Characteristics****Transfer Characteristics****On-Resistance vs. Drain Current****Gate Charge**

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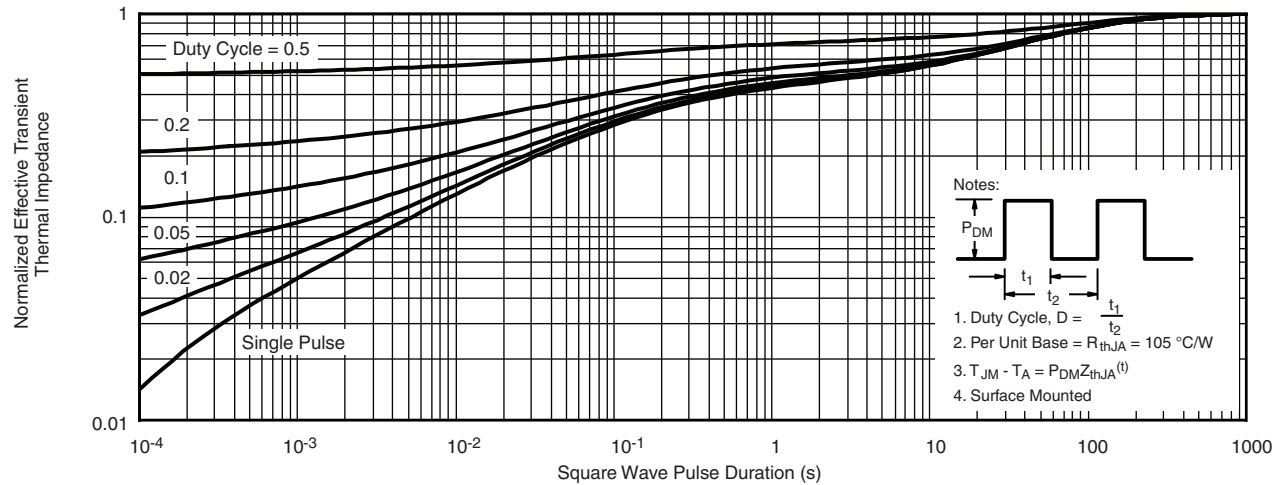
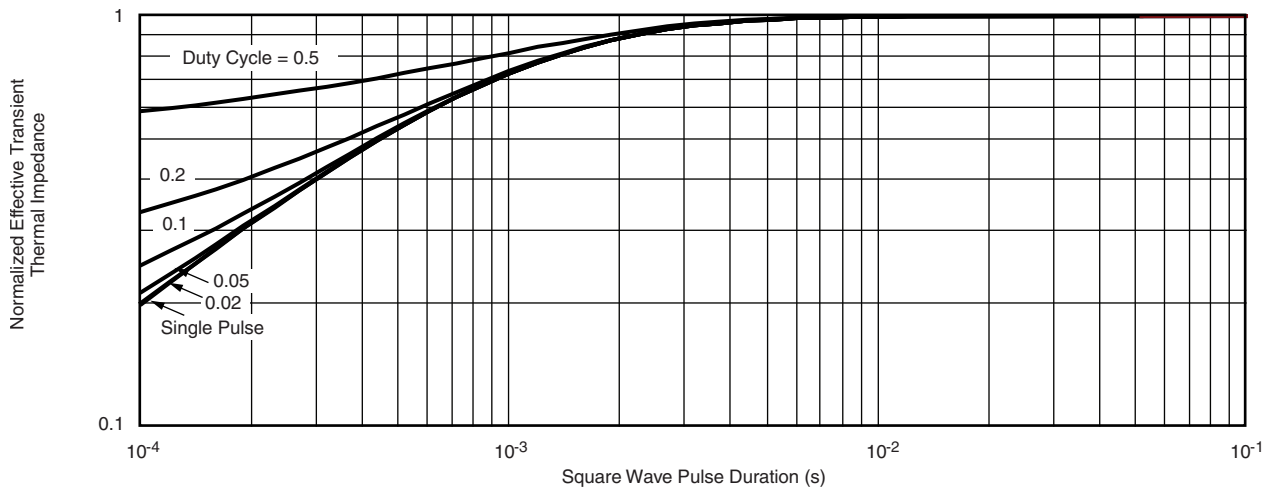
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)**On-Resistance vs. Junction Temperature****Source-Drain Diode Forward Voltage****On-Resistance vs. Gate-to-Source Voltage****Threshold Voltage****Single Pulse Power, Junction-to-Ambient****Safe Operating Area, Junction-to-Ambient**


TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)


* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

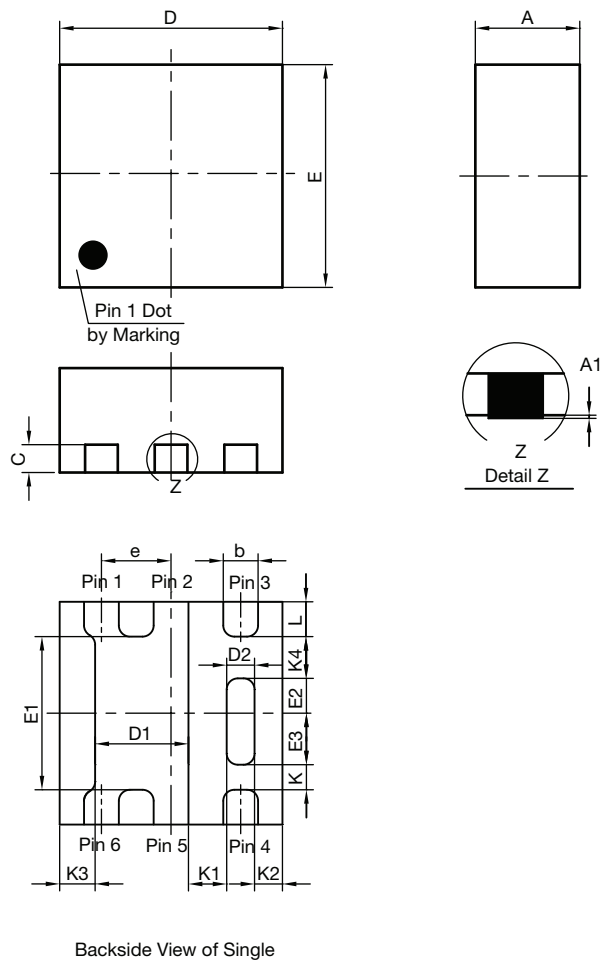
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**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)**Normalized Thermal Transient Impedance, Junction-to-Ambient****Normalized Thermal Transient Impedance, Junction-to-Case**

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?67402.

CASE OUTLINE FOR THIN PPAK SC75 SINGLE



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.525	0.60	0.65	0.0206	0.024	0.026
A1	0	-	0.05	0	-	0.002
b	0.18	0.25	0.33	0.007	0.010	0.013
C	0.15	0.20	0.25	0.006	0.008	0.0010
D	1.53	1.60	1.70	0.060	0.063	0.067
D1	0.57	0.67	0.77	0.022	0.026	0.030
D2	0.10	0.20	0.30	0.004	0.008	0.012
E	1.53	1.60	1.70	0.060	0.063	0.067
E1	1.00	1.10	1.20	0.039	0.043	0.047
E2	0.20	0.25	0.30	0.008	0.010	0.012
E3	0.32	0.37	0.42	0.013	0.015	0.017
e	0.65 BSC			0.020 BSC		
K	0.180 typ.			0.007 typ.		
K1	0.275 typ.			0.011 typ.		
K2	0.200 typ.			0.008 typ.		
K3	0.255 typ.			0.010 typ.		
K4	0.300 typ.			0.012 typ.		
L	0.15	0.25	0.35	0.006	0.010	0.014
ECN: C11-0404-Rev. A, 11-Apr-11						
DWG: 5999						

Note

- All dimensions are in millimeter
- Package outline exclusive of mold flash and metal burr
- Package outline inclusive of plating



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