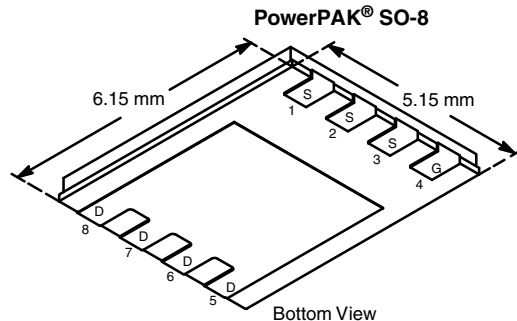


N-Channel 40 V (D-S) MOSFET

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A) ^a	Q_g (Typ.)
40	0.0017 at $V_{GS} = 10$ V	60	34.6 nC
	0.0022 at $V_{GS} = 4.5$ V	60	



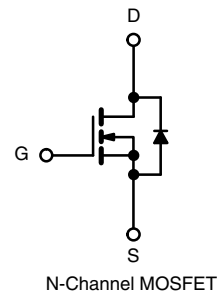
Ordering Information:
SiR640DP-T1-GE3 (Lead (Pb)-free and Halogen-free)

FEATURES

- TrenchFET® Power MOSFET
- Low Q_g for High Efficiency
- 100 % R_g and UIS Tested
- Material categorization:
For definitions of compliance please see
www.vishay.com/doc?99912

APPLICATIONS

- Synchronous Rectification
- DC/DC Converter



ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	40	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ($T_J = 150$ °C)	I_D	$T_C = 25$ °C	A
		$T_C = 70$ °C	
		$T_A = 25$ °C	
		$T_A = 70$ °C	
Pulsed Drain Current ($t = 100$ μ s)	I_{DM}	350	A
Continuous Source-Drain Diode Current	I_S	$T_C = 25$ °C	
		$T_A = 25$ °C	5.6 ^{b, c}
Single Pulse Avalanche Current	I_{AS}	40	mJ
Single Pulse Avalanche Energy	E_{AS}	80	
Maximum Power Dissipation	P_D	$T_C = 25$ °C	W
		$T_C = 70$ °C	
		$T_A = 25$ °C	
		$T_A = 70$ °C	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150	°C
Soldering Recommendations (Peak Temperature) ^{d, e}		260	

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{b, f}	R_{thJA}	15	20	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	0.9	1.2	

Notes:

- Package limited.
- Surface mounted on 1" x 1" FR4 board.
- $t = 10$ s.
- See solder profile (www.vishay.com/doc?73257). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under steady state conditions is 54 °C/W.

SPECIFICATIONS ($T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	40			V
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)} /T _J	I _D = 250 μA		- 5.3		mV/°C
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1		2.3	V
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 40 V, V _{GS} = 0 V			1	μA
		V _{DS} = 40 V, V _{GS} = 0 V, T _J = 55 °C			10	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	30			A
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 20 A		0.0014	0.0017	Ω
		V _{GS} = 4.5 V, I _D = 20 A		0.0018	0.0022	
Forward Transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 20 A		110		S
Dynamic ^b						
Input Capacitance	C _{iss}	V _{DS} = 20 V, V _{GS} = 0 V, f = 1 MHz		4930		pF
Output Capacitance	C _{oss}			3810		
Reverse Transfer Capacitance	C _{rss}			314		
Total Gate Charge	Q _g	V _{DS} = 20 V, V _{GS} = 10 V, I _D = 20 A		75	113	nC
Gate-Source Charge	Q _{gs}	V _{DS} = 20 V, V _{GS} = 4.5 V, I _D = 20 A		34.6	52	
Gate-Drain Charge	Q _{gd}			11		
				8.2		
Gate Resistance	R _g	f = 1 MHz	0.4	1.3	2.6	Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = 20 V, R _L = 2 Ω I _D ≅ 10 A, V _{GEN} = 10 V, R _g = 1 Ω		19	35	ns
Rise Time	t _r			11	20	
Turn-Off Delay Time	t _{d(off)}			50	90	
Fall Time	t _f			10	20	
Turn-On Delay Time	t _{d(on)}	V _{DD} = 20 V, R _L = 2 Ω I _D ≅ 10 A, V _{GEN} = 4.5 V, R _g = 1 Ω		46	90	
Rise Time	t _r			88	170	
Turn-Off Delay Time	t _{d(off)}			56	110	
Fall Time	t _f			25	50	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C			60	A
Pulse Diode Forward Current (t = 100 μs)	I _{SM}				350	
Body Diode Voltage	V _{SD}	I _S = 5 A		0.69	1.1	V
Body Diode Reverse Recovery Time	t _{rr}	I _F = 10 A, dl/dt = 100 A/μs, T _J = 25 °C		83	160	ns
Body Diode Reverse Recovery Charge	Q _{rr}			77	150	nC
Reverse Recovery Fall Time	t _a			26		ns
Reverse Recovery Rise Time	t _b			57		

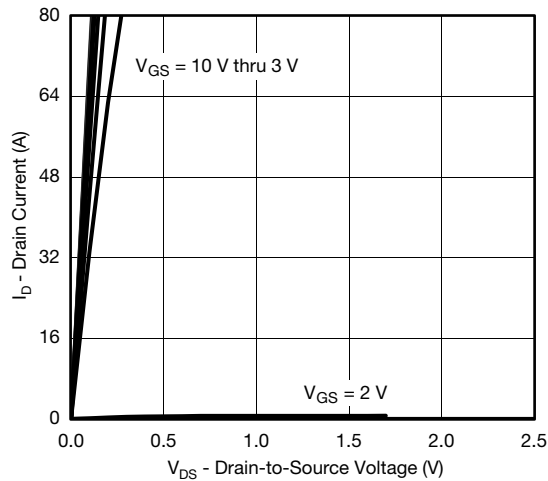
Notes:

a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

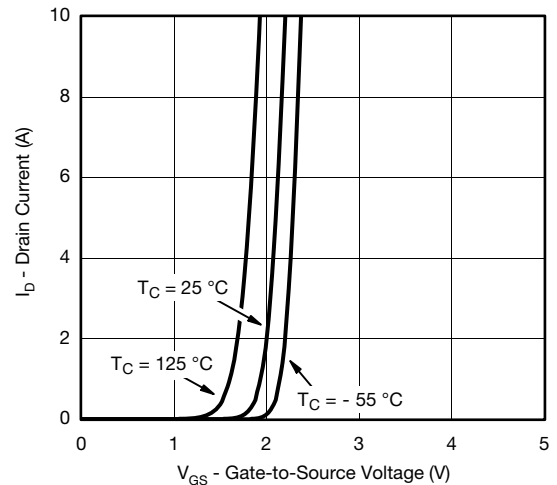
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

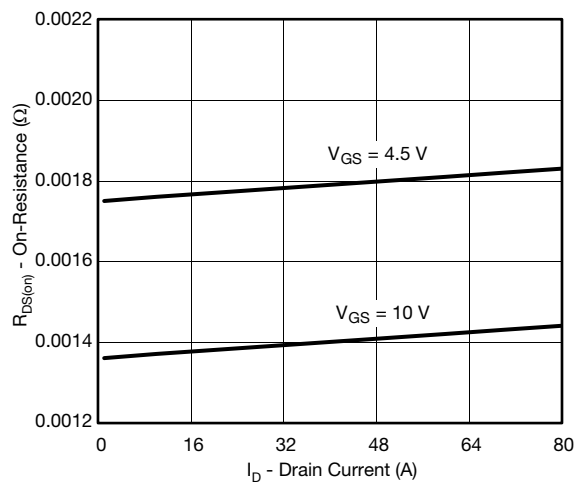
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



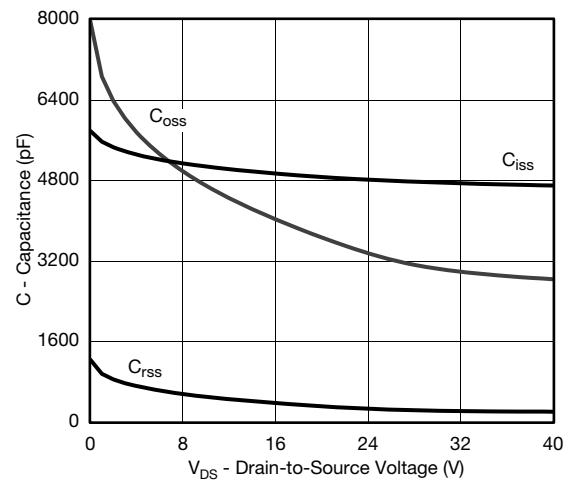
Output Characteristics



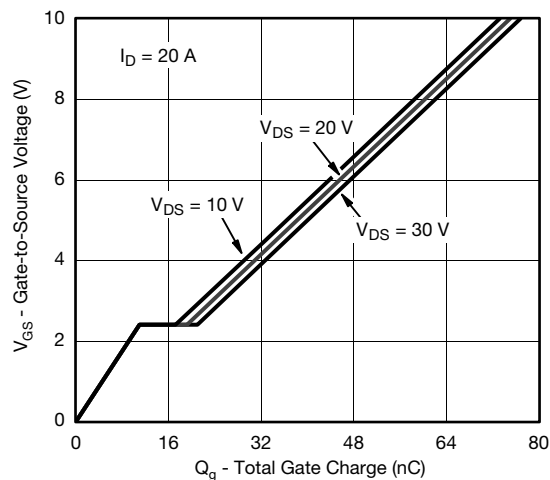
Transfer Characteristics



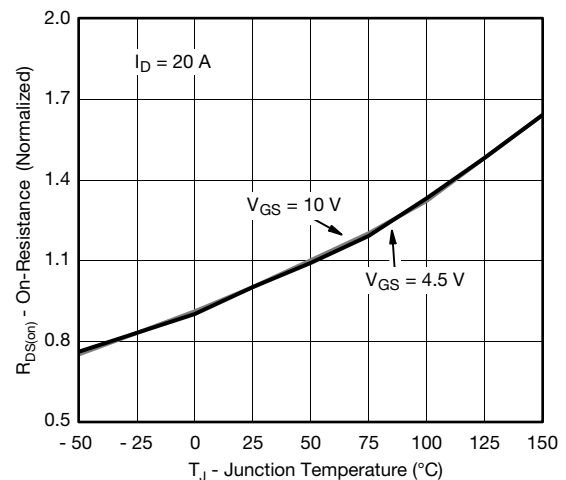
On-Resistance vs. Drain Current and Gate Voltage



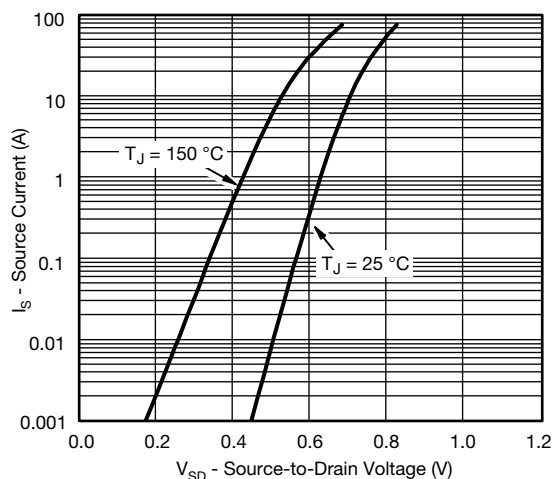
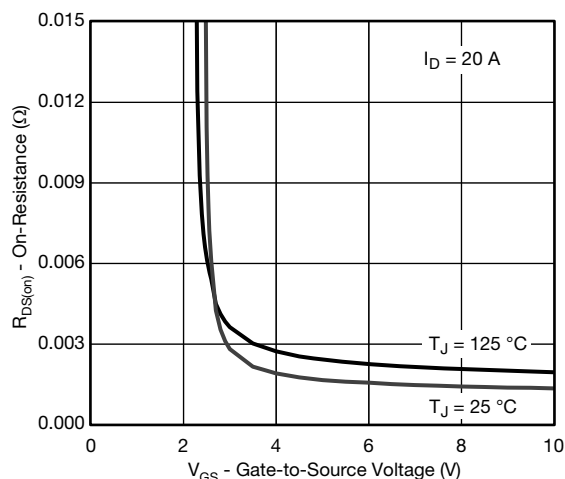
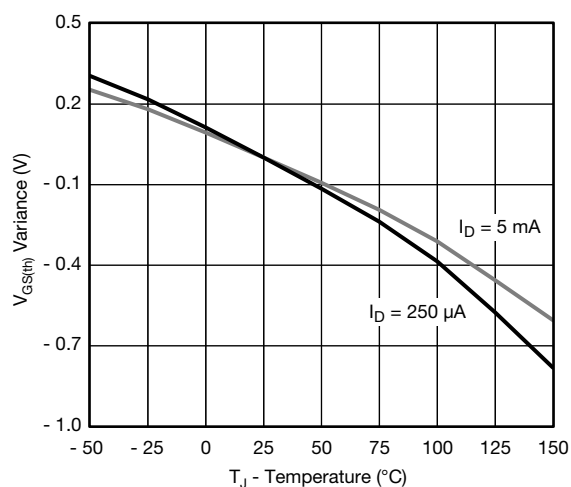
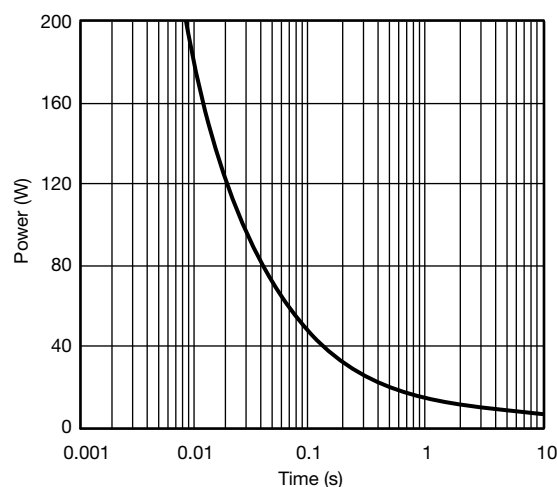
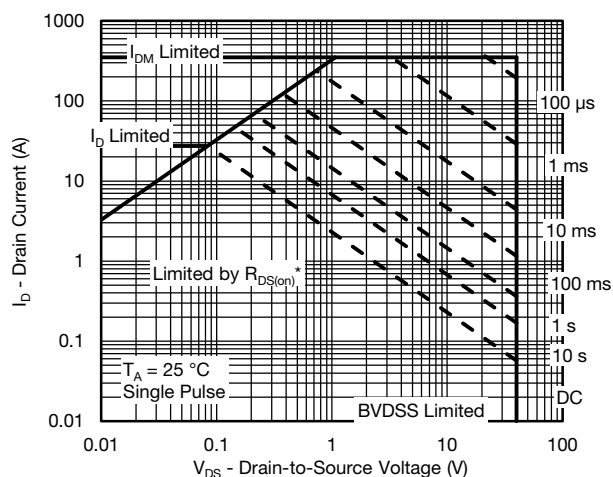
Capacitance



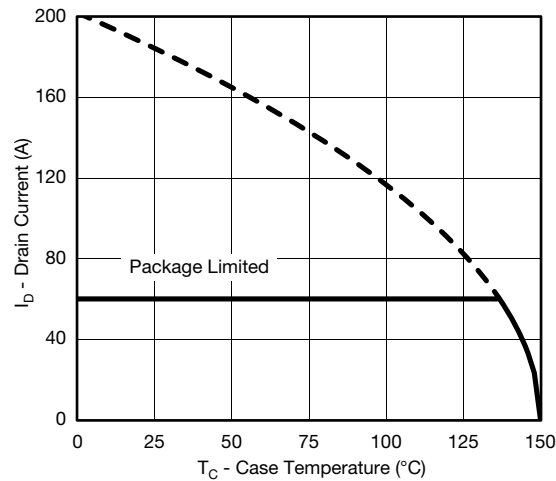
Gate Charge



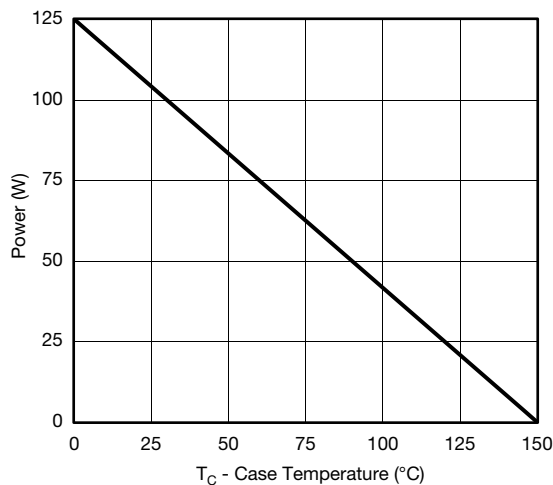
On-Resistance vs. Junction Temperature

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)**Source-Drain Diode Forward Voltage****On-Resistance vs. Gate-to-Source Voltage****Threshold Voltage****Single Pulse Power, Junction-to-Ambient****Safe Operating Area, Junction-to-Ambient**

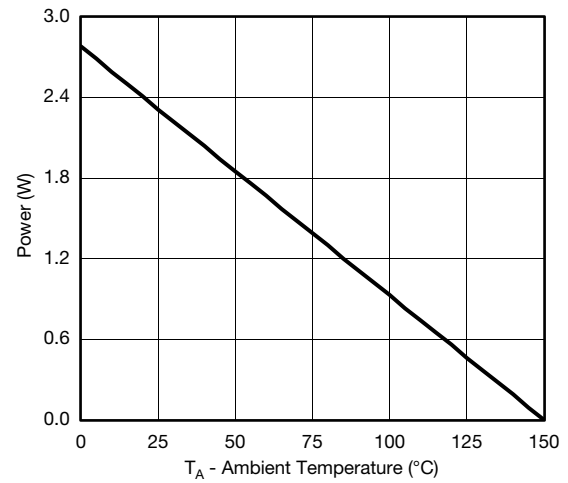
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating*

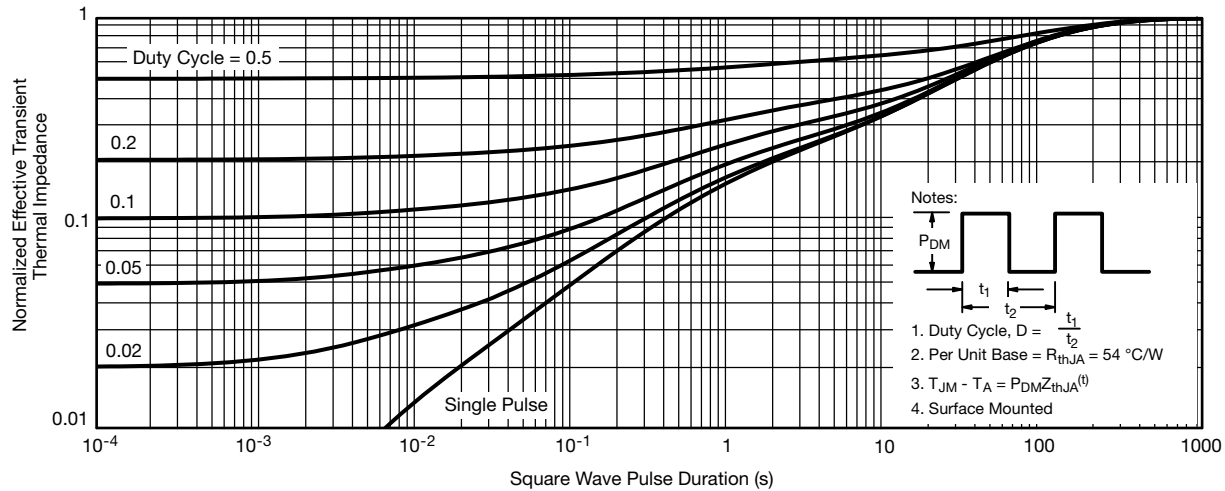
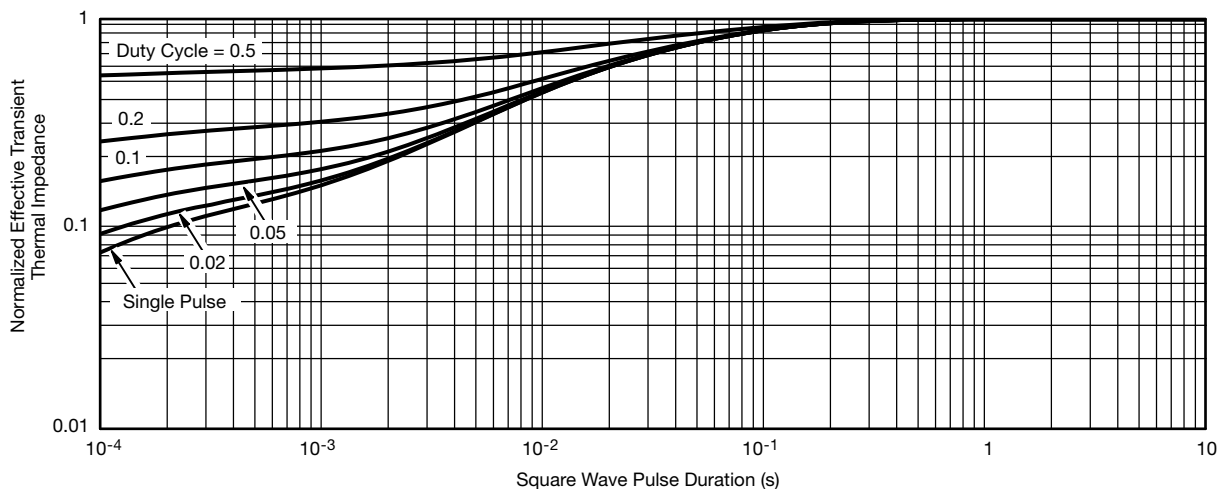


Power, Junction-to-Case



Power, Junction-to-Ambient

* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)**Normalized Thermal Transient Impedance, Junction-to-Ambient****Normalized Thermal Transient Impedance, Junction-to-Case**

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