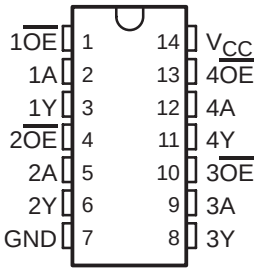
- **State-of-the-Art BiCMOS Design Significantly Reduces I_{CCZ}**
- **High-Impedance State During Power-Up and Power-Down**
- **3-State Outputs Drive Bus Lines or Buffer-Memory Address Registers**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C Method 3015**
- **Package Options Include Plastic Small-Outline (D) Packages and Standard Plastic 300-mil DIPs (N)**

D OR N PACKAGE
(TOP VIEW)



description

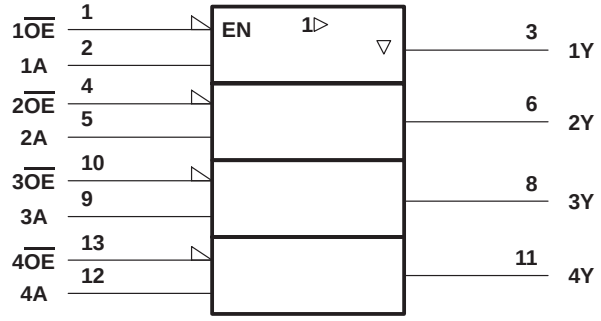
The SN64BCT125A bus buffer features independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable ($\overline{OE}$) input is high.

The SN64BCT125A is characterized for operation from −40°C to 85°C and 0°C to 70°C.

FUNCTION TABLE
(each buffer)

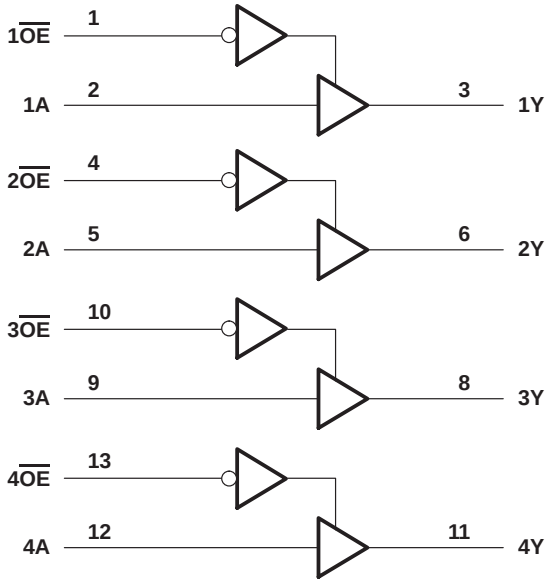
INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . − 0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . − 0.5 V to 7 V
Voltage range applied to any output in the disabled or power-off state, V_O . . . . . − 0.5 V to 5.5 V
Voltage range applied to any output in the high state, V_O . . . . . − 0.5 V to V_{CC}
Current into any output in the low state . . . . . 128 mA
Operating free-air temperature range . . . . . − 40°C to 85°C
Storage temperature range . . . . . − 65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
I_{OH}	High-level output current			−15	mA
I_{OL}	Low-level output current			64	mA
T_A	Operating free-air temperature	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP‡	MAX	UNIT
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA				−1.2	V
V_{OH}	V_{CC} = 4.5 V	I_{OH} = −3 mA		2.4	3.3		V
		I_{OH} = −15 mA		2	3.1		
V_{OL}	V_{CC} = 4.5 V,	I_{OH} = 64 mA			0.42	0.55	V
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V				50	µA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.5 V				−50	µA
I_{OZ}	V_{CC} = 0 to 1.3 V (power up)	V_O = 2.7 V or 0.5 V,	$\overline{OE}$ at 0.8 V			± 50	µA
	V_{CC} = 1.3 V to 0 (power down)					± 50	
I_I	V_{CC} = 0,	V_I = 7 V				0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V				25	µA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.5 V				−20	µA
I_{OS}§	V_{CC} = 5.5 V,	V_O = 0		−100		−225	mA
I_{CCL}	V_{CC} = 5.5 V				46	49	mA
I_{CCH}	V_{CC} = 5.5 V				19	31	mA
I_{CCZ}	V_{CC} = 5.5 V				6	14	mA
C_i	V_{CC} = 5 V,	V_I = 2.5 V or 0.5 V			4		pF
C_o	V_{CC} = 5 V,	V_O = 2.5 V or 0.5 V			9		pF

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω				UNIT
						T_A = −40°C to 85°C		T_A = 0°C to 70°C		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1.6	3.5	5.2	1.6	6	1.6	5.7	ns
t_{PHL}			2.7	5	6.9	2.7	8	2.7	7.7	
t_{PZH}	$\overline{OE}$	Y	3.4	6.7	9	3.4	11.1	3.4	10.3	ns
t_{PZL}			5	8.2	10.4	5	12.8	5	11.7	
t_{PHZ}	$\overline{OE}$	Y	3	5.8	7.4	3	9.4	3	8.9	ns
t_{PLZ}			2.8	5.5	7.3	2.8	9.9	2.8	8.6	

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN64BCT125AD	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	6BCT125A	Samples
SN64BCT125AN	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SN64BCT125AN	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

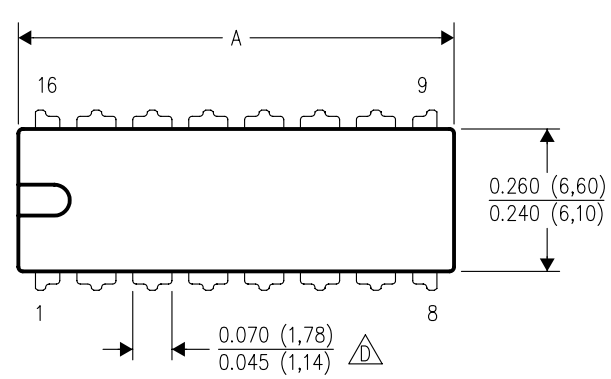
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

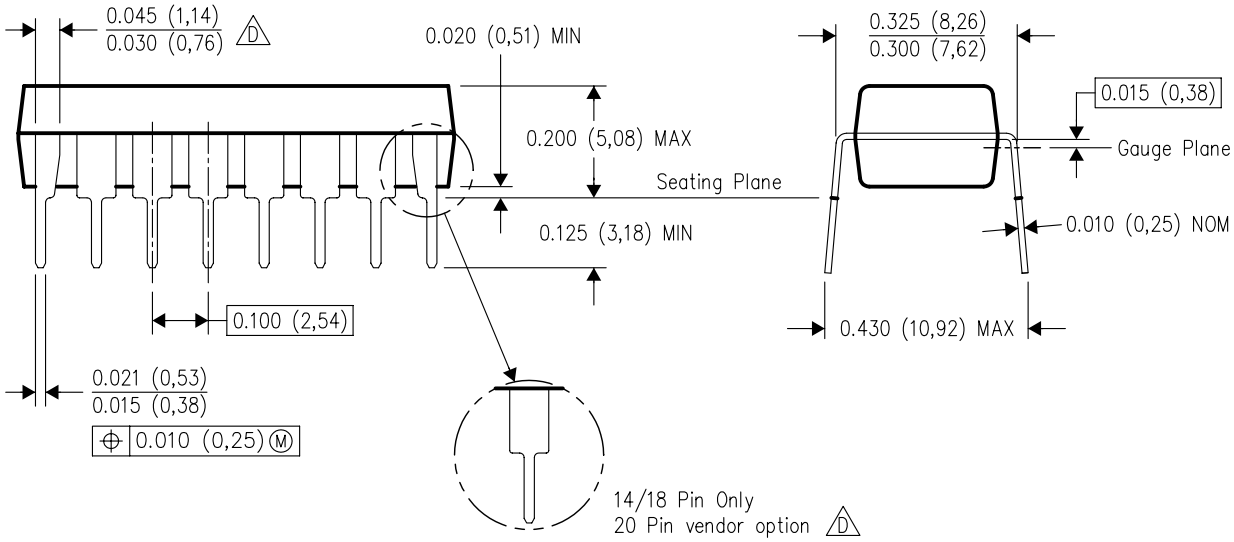
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



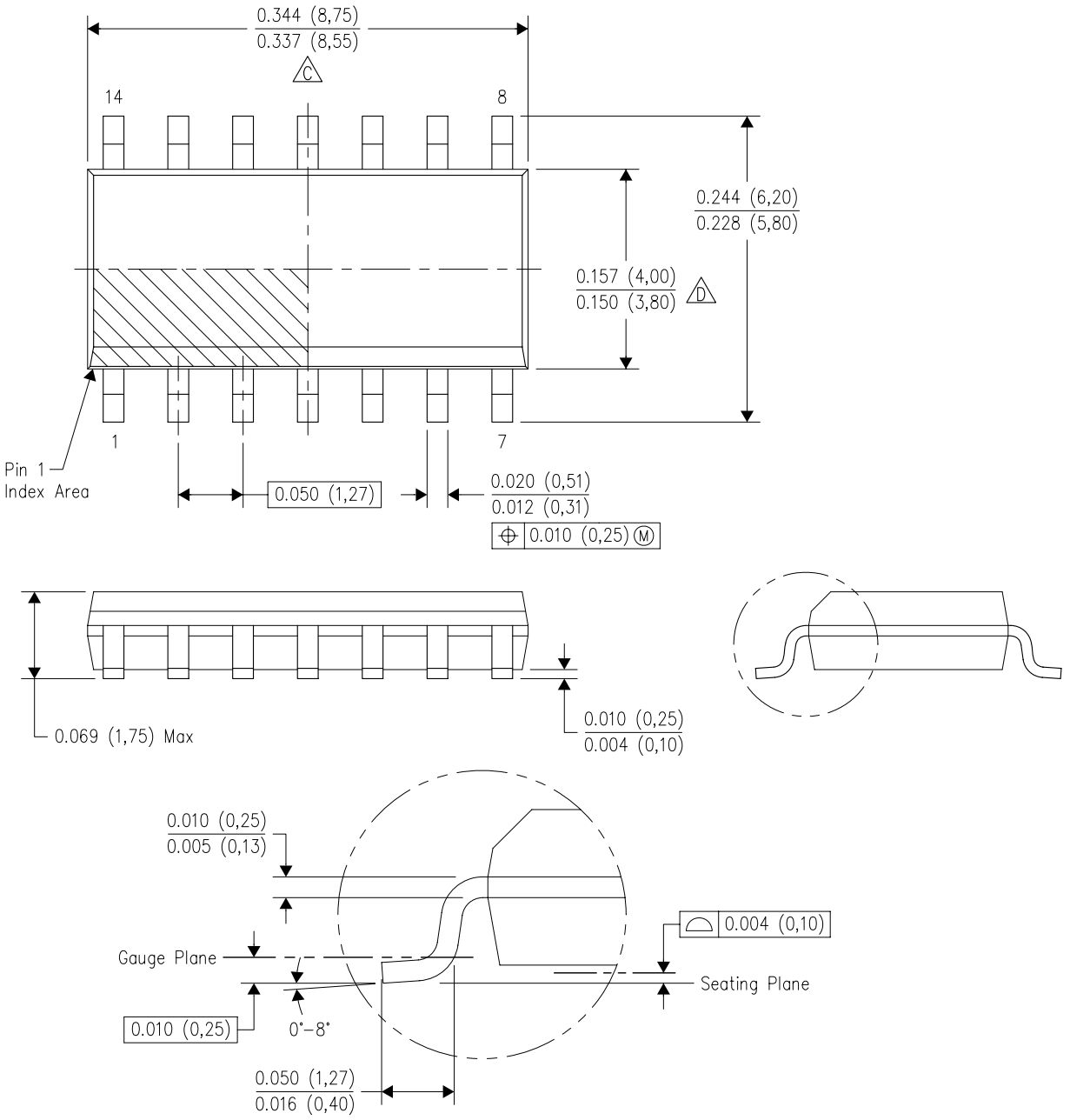
DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

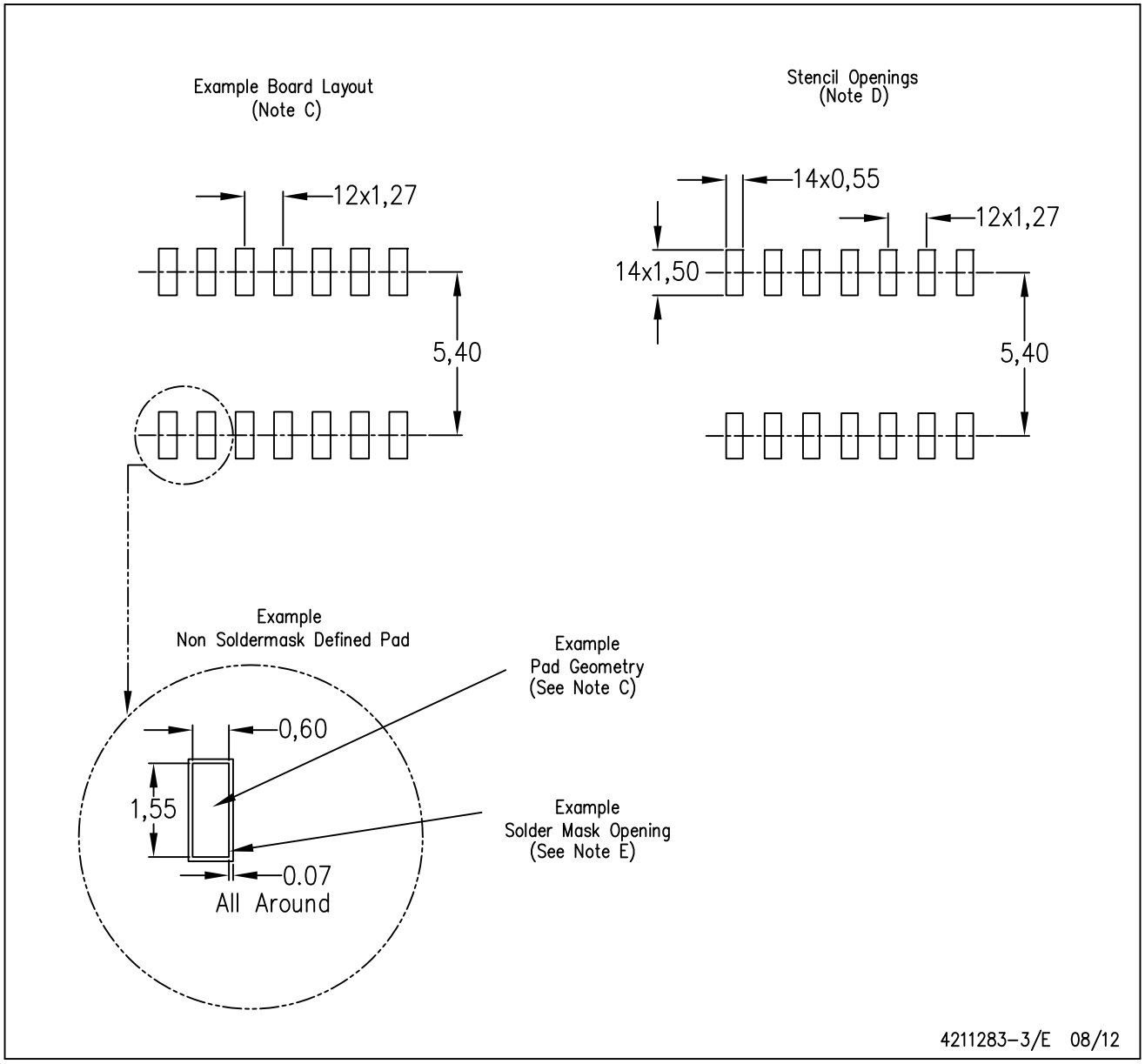
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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