

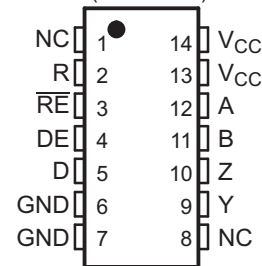
## LOW-POWER DIFFERENTIAL LINE DRIVER AND RECEIVER PAIRS

### FEATURES

- **High-Speed Low-Power LinBICMOS™ Circuitry Designed for Signaling Rates<sup>(1)</sup> of up to 30 Mbps**
- **Bus-Pin ESD Protection 15 kV HBM**
- **Low Disabled Supply-Current Requirements: 700  $\mu$ A Maximum**
- **Designed for High-Speed Multipoint Data Transmission Over Long Cables**
- **Common-Mode Voltage Range of –7 V to 12 V**
- **Low Supply Current: 15 mA Max**
- **Compatible With ANSI Standard TIA/EIA-485-A and ISO 8482:1987(E)**
- **Positive and Negative Output Current Limiting**
- **Driver Thermal Shutdown Protection**

(1) Signaling rate by TIA/EIA-485-A definition restrict transition times to 30% of the bit duration, and much higher signaling rates may be achieved without this requirement as displayed in the *TYPICAL CHARACTERISTICS* of this device.

SN65LBC180AD (Marked as BL180A)  
SN65LBC180AN (Marked as 65LBC180A)  
SN75LBC180AD (Marked as LB180A)  
SN75LBC180AN (Marked as 75LBC180A)  
(TOP VIEW)



NC—No internal connection  
Pins 6 and 7 are connected together internally  
Pins 13 and 14 are connected together internally

### DESCRIPTION

The SN65LBC180A and SN75LBC180A differential driver and receiver pairs are monolithic integrated circuits designed for bidirectional data communication over long cables that take on the characteristics of transmission lines. They are balanced, or differential, voltage mode devices that are compatible with ANSI standard TIA/EIA-485-A and ISO 8482:1987(E). The A version offers improved switching performance over its predecessors without sacrificing significantly more power.

These devices combine a differential line driver and differential input line receiver and operate from a single 5-V power supply. The driver differential outputs and the receiver differential inputs are connected to separate terminals for full-duplex operation and are designed to present minimum loading to the bus when powered off ( $V_{CC} = 0$ ). These parts feature wide positive and negative common-mode voltage ranges, making them suitable for point-to-point or multipoint data bus applications. The devices also provide positive and negative current limiting for protection from line fault conditions. The SN65LBC180A is characterized for operation from –40°C to 85°C, and the SN75LBC180A is characterized for operation from 0°C to 70°C.

**FUNCTION TABLE<sup>(1)</sup>**

| DRIVER     |              |         |   | RECEIVER                                  |              |             |
|------------|--------------|---------|---|-------------------------------------------|--------------|-------------|
| INPUT<br>D | ENABLE<br>DE | OUTPUTS |   | DIFFERENTIAL INPUTS<br>A – B              | ENABLE<br>RE | OUTPUT<br>R |
|            |              | Y       | Z |                                           |              |             |
| H          | H            | H       | L | $V_{ID} \geq 0.2 \text{ V}$               | L            | H           |
| L          | H            | L       | H | $-0.2 \text{ V} < V_{ID} < 0.2 \text{ V}$ | L            | ?           |
| X          | L            | Z       | Z | $V_{ID} \leq -0.2 \text{ V}$              | L            | L           |
| OPEN       | H            | H       | L | X                                         | H            | Z           |
|            |              |         |   | Open circuit                              | L            | H           |

(1) H = high level, L = low level, ? = indeterminate, X = irrelevant, Z = high impedance (off)



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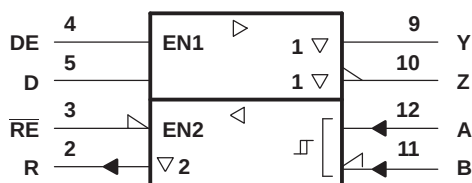
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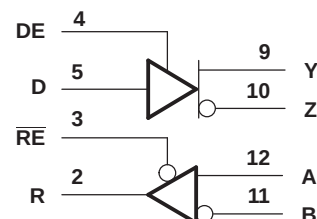
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### LOGIC SYMBOL <sup>(1)</sup>



- (1) This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

### LOGIC DIAGRAM (POSITIVE LOGIC)

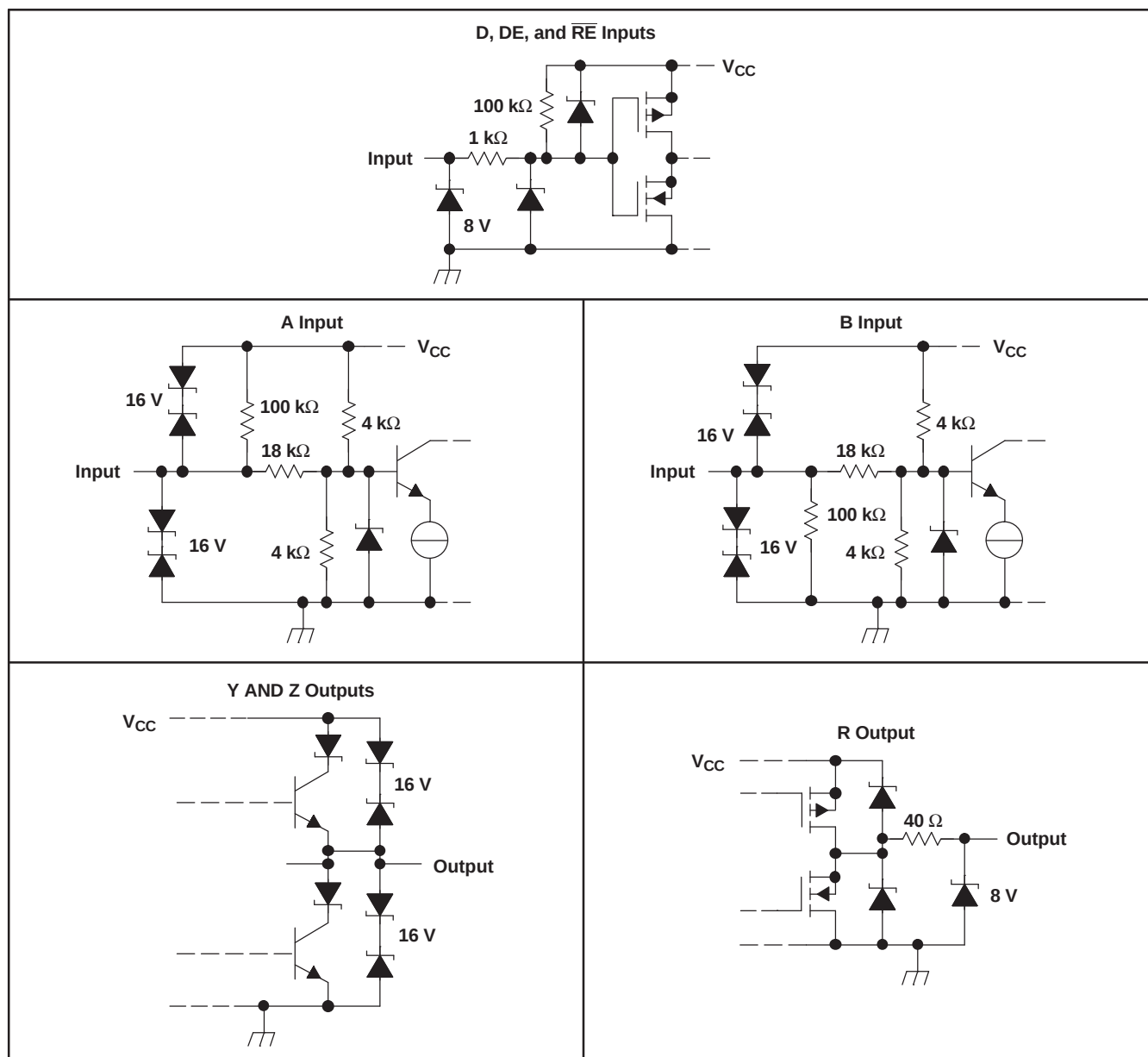


### AVAILABLE OPTIONS <sup>(1)</sup>

| T <sub>A</sub> | PACKAGE                             |                                |
|----------------|-------------------------------------|--------------------------------|
|                | SMALL OUTLINE <sup>(2)</sup><br>(D) | PLASTIC<br>DUAL-IN-LINE<br>(N) |
| 0°C to 70°C    | SN75LBC180AD                        | SN75LBC180AN                   |
| –40°C to 85°C  | SN65LBC180AD                        | SN65LBC180AN                   |

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).  
 (2) The D package is available taped and reeled. Add an R suffix to the part number (i.e., SN65LBC180ADR).

## SCHEMATICS OF INPUTS AND OUTPUTS



## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

|                 |                                                   |                                                       | UNIT                              |
|-----------------|---------------------------------------------------|-------------------------------------------------------|-----------------------------------|
| V <sub>CC</sub> | Supply voltage range <sup>(2)</sup>               |                                                       | –0.3 V to 6 V                     |
| V <sub>I</sub>  | Input voltage range                               | A, B                                                  | –10 V to 15 V                     |
|                 | Voltage range                                     | D, R, DE, $\overline{RE}$                             | –0.3 V to V <sub>CC</sub> + 0.5 V |
| I <sub>O</sub>  | Receiver output current                           |                                                       | ±10 mA                            |
|                 | Continuous total power dissipation <sup>(3)</sup> |                                                       | Internally limited                |
|                 | Total power dissipation                           |                                                       | See Dissipation Rating Table      |
| ESD             | Bus terminals and GND                             | HBM (Human Body Model) EIA/JESD22-A114 <sup>(4)</sup> | ±15 kV                            |
|                 | All pins                                          | HBM (Human Body Model) EIA/JESD22-A114 <sup>(4)</sup> | ±3 kV                             |
|                 |                                                   | MM (Machine Model) EIA/JESD22-A115                    | ±400 V                            |
|                 |                                                   | CDM (Charge Device Model) EIA/JESD22-C101             | ±1.5 kV                           |

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to GND except for differential input or output voltages.
- (3) The maximum operating junction temperature is internally limited. Use the dissipation rating table to operate below this temperature.
- (4) Tested in accordance with MIL-STD-883C, Method 3015.7.

## DISSIPATION RATINGS

| PACKAGE | T <sub>A</sub> ≤ 25°C<br>POWER RATING | DERATING FACTOR <sup>(1)</sup><br>ABOVE T <sub>A</sub> = 25°C | T <sub>A</sub> = 70°C<br>POWER RATING | T <sub>A</sub> = 85°C<br>POWER RATING |
|---------|---------------------------------------|---------------------------------------------------------------|---------------------------------------|---------------------------------------|
| D       | 950 mW                                | 7.6 mW/°C                                                     | 608 mW                                | 494 mW                                |
| N       | 1150 mW                               | 9.2 mW/°C                                                     | 736 mW                                | 598 mW                                |

- (1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

## RECOMMENDED OPERATING CONDITIONS

|                 |                                                         |                            | MIN                | NOM | MAX             | UNIT |
|-----------------|---------------------------------------------------------|----------------------------|--------------------|-----|-----------------|------|
| V <sub>CC</sub> | Supply voltage                                          |                            | 4.75               | 5   | 5.25            | V    |
| V <sub>IH</sub> | High-level input voltage                                | D, DE, and $\overline{RE}$ | 2                  |     | V <sub>CC</sub> | V    |
| V <sub>IL</sub> | Low-level input voltage                                 | D, DE, and $\overline{RE}$ | 0                  |     | 0.8             | V    |
| V <sub>ID</sub> | Differential input voltage <sup>(1)</sup>               |                            | –12 <sup>(2)</sup> |     | 12              | V    |
| V <sub>O</sub>  | Voltage at any bus terminal (separately or common mode) | A, B, Y, or Z              | –7                 |     | 12              | V    |
| V <sub>I</sub>  |                                                         |                            |                    |     |                 |      |
| V <sub>IC</sub> |                                                         |                            |                    |     |                 |      |
| I <sub>OH</sub> | High-level output current                               | Y or Z                     | –60                |     |                 | mA   |
|                 |                                                         | R                          | –8                 |     |                 |      |
| I <sub>OL</sub> | Low-level output current                                | Y or Z                     |                    |     | 60              | mA   |
|                 |                                                         | R                          |                    |     | 8               |      |
| T <sub>A</sub>  | Operating free-air temperature                          |                            | –40                |     | 85              | °C   |
|                 |                                                         |                            | 0                  |     | 70              |      |

- (1) Differential input/output bus voltage is measured at the noninverting terminal with respect to the inverting terminal.
- (2) The algebraic convention, where the least positive (more negative) limit is designated minimum, is used in this data sheet.

## DRIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

| PARAMETER                                                                           | TEST CONDITIONS                                   | MIN                                   | TYP <sup>(1)</sup> | MAX       | UNIT          |
|-------------------------------------------------------------------------------------|---------------------------------------------------|---------------------------------------|--------------------|-----------|---------------|
| $V_{IK}$ Input clamp voltage                                                        | $I_I = -18\text{ mA}$                             | -1.5                                  | -0.8               |           | V             |
| $ V_{OD} $ Differential output voltage magnitude                                    | $R_L = 54\ \Omega$ ,<br>See Figure 1              | SN65LBC180A                           |                    | 1 1.5 3   | V             |
|                                                                                     |                                                   | SN75LBC180A                           |                    | 1.1 1.5 3 |               |
|                                                                                     | $R_L = 60\ \Omega$ ,<br>See Figure 2              | SN65LBC180A                           |                    | 1 1.5 3   | V             |
|                                                                                     |                                                   | SN75LBC180A                           |                    | 1.1 1.5 3 |               |
| $\Delta  V_{OD} $ Change in magnitude of differential output voltage <sup>(2)</sup> | See Figure 1 and Figure 2                         | -0.2                                  |                    | 0.2       | V             |
| $V_{OC(ss)}$ Steady-state common-mode output voltage                                | See Figure 1                                      | 1.8                                   | 2.4                | 2.8       | V             |
| $\Delta V_{OC}$ Change in steady-state common-mode output voltage <sup>(2)</sup>    |                                                   | -0.1                                  |                    | 0.1       | V             |
| $I_O$ Output current with power off                                                 | $V_{CC} = 0$ , $V_O = -7\text{ V to }12\text{ V}$ | -10                                   |                    | 10        | $\mu\text{A}$ |
| $I_{IH}$ High-level input current                                                   | $V_I = 2\text{ V}$                                | -100                                  |                    |           | $\mu\text{A}$ |
| $I_{IL}$ Low-level input current                                                    | $V_I = 0.8\text{ V}$                              | -100                                  |                    |           | $\mu\text{A}$ |
| $I_{OS}$ Short-circuit output current                                               | $-7\text{ V} \leq V_O \leq 12\text{ V}$           | -250                                  | $\pm 70$           | 250       | mA            |
| $I_{CC}$ Supply current                                                             | $V_I = 0\text{ or }V_{CC}$ ,<br>No load           | Receiver disabled and driver enabled  |                    | 5.5 9     | mA            |
|                                                                                     |                                                   | Receiver disabled and driver disabled |                    | 0.5 1     |               |
|                                                                                     |                                                   | Receiver enabled and driver enabled   |                    | 8.5 15    |               |

(1) All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

(2)  $\Delta |V_{OD}|$  and  $\Delta |V_{OC}|$  are the changes in the steady-state magnitude of  $V_{OD}$  and  $V_{OC}$ , respectively, that occur when the input is changed from a high level to a low level.

## DRIVER SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

| PARAMETER                                                             | TEST CONDITIONS                                             | MIN | TYP | MAX | UNIT |
|-----------------------------------------------------------------------|-------------------------------------------------------------|-----|-----|-----|------|
| $t_{PLH}$ Propagation delay time, low-to-high-level output            | $R_L = 54\ \Omega$ , $C_L = 50\text{ pF}$ ,<br>See Figure 3 | 2   | 6   | 12  | ns   |
| $t_{PHL}$ Propagation delay time, high-to-low-level output            |                                                             | 2   | 6   | 12  | ns   |
| $t_{sk(p)}$ Pulse skew ( $ t_{PLH} - t_{PHL} $ )                      |                                                             |     | 0.3 | 1   | ns   |
| $t_r$ Differential output signal rise time                            |                                                             | 4   | 7.5 | 11  | ns   |
| $t_f$ Differential output signal fall time                            |                                                             | 4   | 7.5 | 11  | ns   |
| $t_{PZH}$ Propagation delay time, high-impedance-to-high-level output | $R_L = 110\ \Omega$ , See Figure 4                          |     | 12  | 22  | ns   |
| $t_{PZL}$ Propagation delay time, high-impedance-to-low-level output  | $R_L = 110\ \Omega$ , See Figure 5                          |     | 12  | 22  | ns   |
| $t_{PHZ}$ Propagation delay time, high-level-to-high-impedance output | $R_L = 110\ \Omega$ , See Figure 4                          |     | 12  | 22  | ns   |
| $t_{PLZ}$ Propagation delay time, low-level-to-high-impedance output  | $R_L = 110\ \Omega$ , See Figure 5                          |     | 12  | 22  | ns   |

## RECEIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

| PARAMETER                                            | TEST CONDITIONS                     | MIN                                   | TYP <sup>(1)</sup> | MAX  | UNIT    |
|------------------------------------------------------|-------------------------------------|---------------------------------------|--------------------|------|---------|
| $V_{IT+}$ Positive-going input threshold voltage     | $I_O = -8$ mA                       |                                       |                    | 0.2  | V       |
| $V_{IT-}$ Negative-going input threshold voltage     | $I_O = 8$ mA                        | -0.2                                  |                    |      | V       |
| $V_{hys}$ Hysteresis voltage ( $V_{IT+} - V_{IT-}$ ) |                                     |                                       | 50                 |      | mV      |
| $V_{IK}$ Enable-input clamp voltage                  | $I_I = -18$ mA                      | -1.5                                  | -0.8               |      | V       |
| $V_{OH}$ High-level output voltage                   | $V_{ID} = 200$ mV, $I_{OH} = -8$ mA | 4                                     | 4.9                |      | V       |
| $V_{OL}$ Low-level output voltage                    | $V_{ID} = -200$ mV, $I_{OL} = 8$ mA |                                       | 0.1                | 0.8  | V       |
| $I_{OZ}$ High-impedance-state output current         | $V_O = 0$ V to $V_{CC}$             | -1                                    |                    | 1    | $\mu$ A |
| $I_{IH}$ High-level enable-input current             | $V_{IH} = 2.4$ V                    | -100                                  |                    |      | $\mu$ A |
| $I_{IL}$ Low-level enable-input current              | $V_{IL} = 0.4$ V                    | -100                                  |                    |      | $\mu$ A |
| $I_I$ Bus input current                              | $V_I = 12$ V,<br>$V_{CC} = 5$ V     | Other input at 0 V                    | 0.4                | 1    | mA      |
|                                                      | $V_I = 12$ V,<br>$V_{CC} = 0$       |                                       | 0.5                | 1    |         |
|                                                      | $V_I = -7$ V,<br>$V_{CC} = 5$ V     |                                       | -0.8               | -0.4 |         |
|                                                      | $V_I = -7$ V,<br>$V_{CC} = 0$       |                                       | -0.8               | -0.3 |         |
| $I_{CC}$ Supply current                              | $V_I = 0$ or $V_{CC}$ ,<br>No load  | Receiver enabled and driver disabled  | 4.5                | 7.5  | mA      |
|                                                      |                                     | Receiver disabled and driver disabled | 0.5                | 1    |         |
|                                                      |                                     | Receiver enabled and driver enabled   | 8.5                | 15   |         |

(1) All typical values are at  $V_{CC} = 5$  V and  $T_A = 25^\circ\text{C}$ .

## RECEIVER SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

| PARAMETER                                                  | TEST CONDITIONS                                            | MIN | TYP | MAX | UNIT |
|------------------------------------------------------------|------------------------------------------------------------|-----|-----|-----|------|
| $t_{PLH}$ Propagation delay time, low-to-high-level output | $V_{ID} = -1.5$ V to $1.5$ V, See <a href="#">Figure 7</a> | 7   | 13  | 20  | ns   |
| $t_{PHL}$ Propagation delay time, high-to-low-level output |                                                            | 7   | 13  | 20  | ns   |
| $t_{sk(p)}$ Pulse skew ( $ t_{PHL} - t_{PLH} $ )           |                                                            |     | 0.5 | 1.5 | ns   |
| $t_r$ Output signal rise time                              |                                                            |     | 2.1 | 3.3 | ns   |
| $t_f$ Output signal fall time                              | See <a href="#">Figure 7</a>                               |     | 2.1 | 3.3 | ns   |
| $t_{PZH}$ Output enable time to high level                 | $C_L = 10$ pF, See <a href="#">Figure 8</a>                |     | 30  | 45  | ns   |
| $t_{PZL}$ Output enable time to low level                  |                                                            |     | 30  | 45  | ns   |
| $t_{PHZ}$ Output disable time from high level              |                                                            |     | 20  | 40  | ns   |
| $t_{PLZ}$ Output disable time from low level               |                                                            |     | 20  | 40  | ns   |

## PARAMETER MEASUREMENT INFORMATION

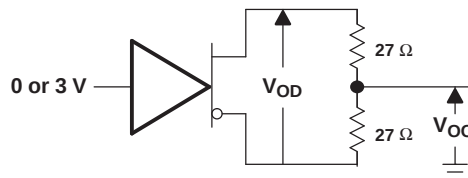
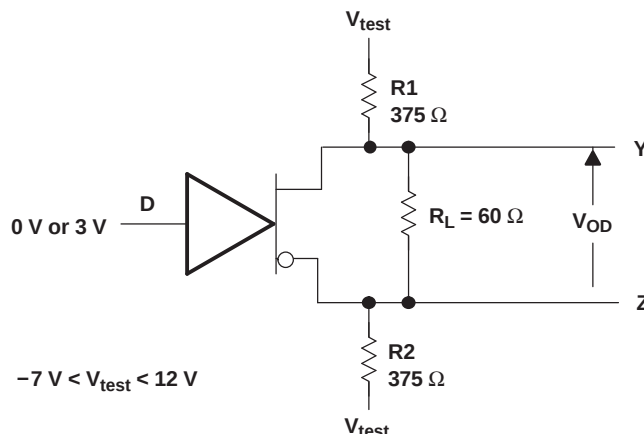
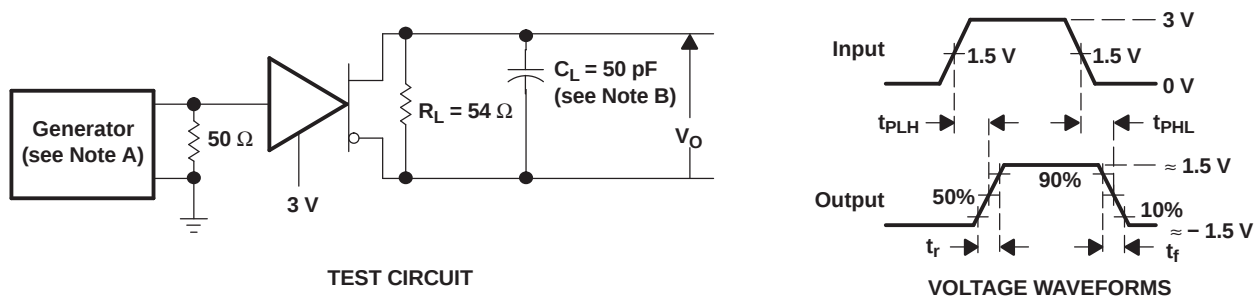


Figure 1. Driver  $V_{OD}$  and  $V_{OC}$

## PARAMETER MEASUREMENT INFORMATION (continued)

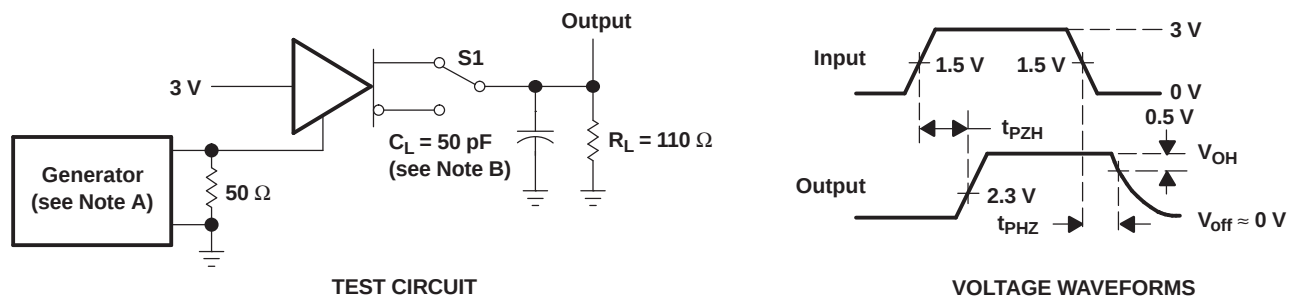


**Figure 2. Driver  $V_{OD}$**



- A. The input pulse is supplied by a generator having the following characteristics:  $PRR \leq 1$  MHz, 50% duty cycle,  $t_r \leq 6$  ns,  $t_f \leq 6$  ns,  $Z_O = 50 \Omega$ .
- B.  $C_L$  includes probe and jig capacitance.

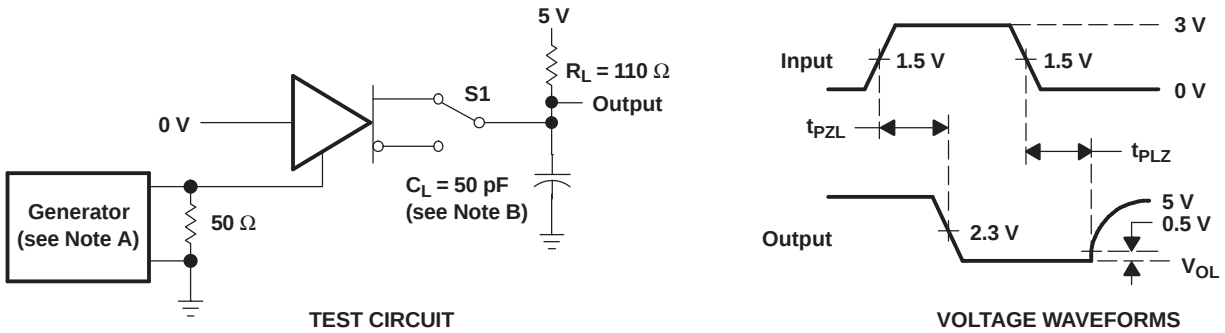
**Figure 3. Driver Test Circuit and Voltage Waveforms**



- A. The input pulse is supplied by a generator having the following characteristics:  $PRR \leq 1$  MHz, 50% duty cycle,  $t_r \leq 6$  ns,  $t_f \leq 6$  ns,  $Z_O = 50 \Omega$ .
- B.  $C_L$  includes probe and jig capacitance.

**Figure 4. Driver Test Circuit and Voltage Waveforms**

## PARAMETER MEASUREMENT INFORMATION (continued)



- A. The input pulse is supplied by a generator having the following characteristics:  $\text{PRR} \leq 1\ \text{MHz}$ , 50% duty cycle,  $t_r \leq 6\ \text{ns}$ ,  $t_f \leq 6\ \text{ns}$ ,  $Z_O = 50\ \Omega$ .
- B.  $C_L$  includes probe and jig capacitance.

Figure 5. Driver Test Circuit and Voltage Waveforms

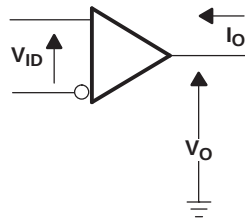
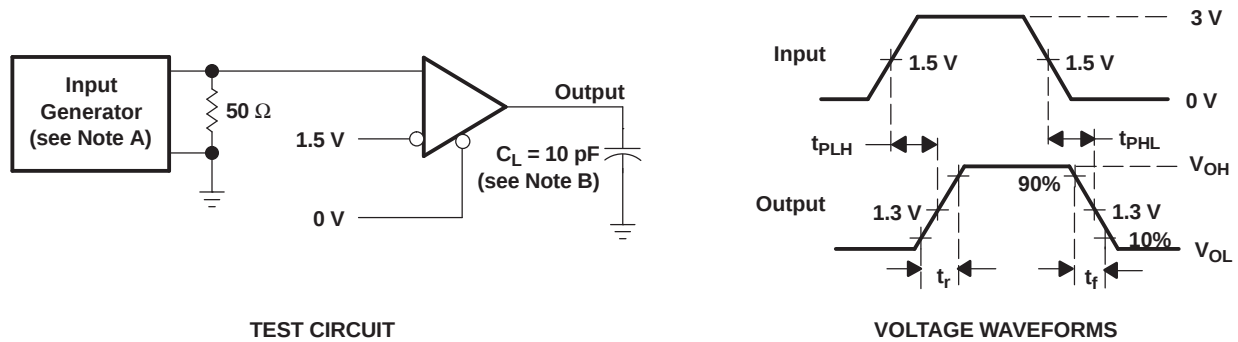


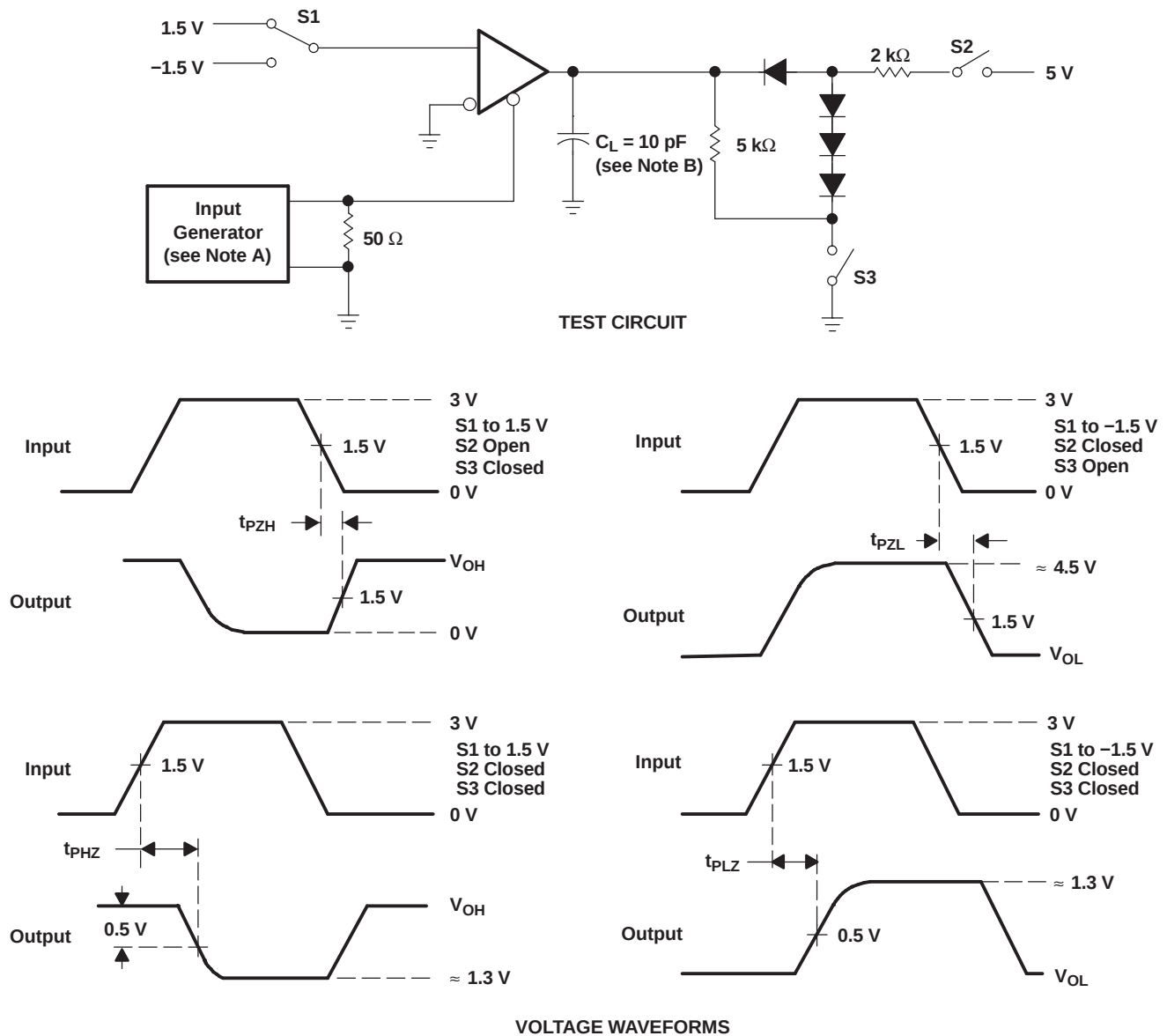
Figure 6. Receiver  $V_{OH}$  and  $V_{OL}$



- A. The input pulse is supplied by a generator having the following characteristics:  $\text{PRR} \leq 1\ \text{MHz}$ , 50% duty cycle,  $t_r \leq 6\ \text{ns}$ ,  $t_f \leq 6\ \text{ns}$ ,  $Z_O = 50\ \Omega$ .
- B.  $C_L$  includes probe and jig capacitance.

Figure 7. Receiver Test Circuit and Voltage Waveforms

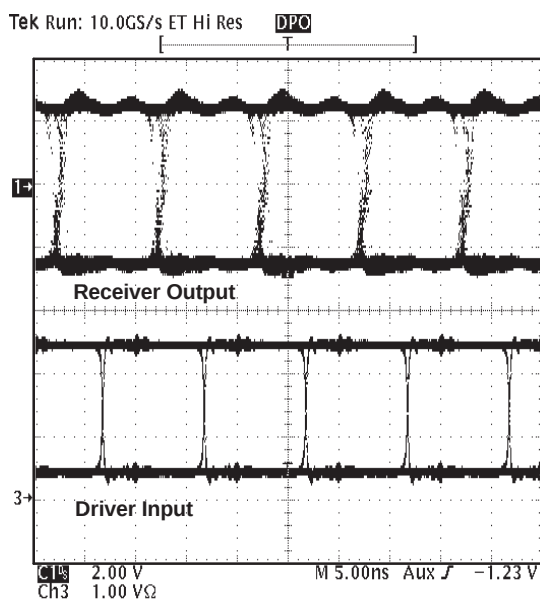
## PARAMETER MEASUREMENT INFORMATION (continued)



- A. The input pulse is supplied by a generator having the following characteristics:  $PRR \leq 1$  MHz, 50% duty cycle,  $t_r \leq 6$  ns,  $t_f \leq 6$  ns,  $Z_O = 50 \Omega$ .
- B.  $C_L$  includes probe and jig capacitance.

**Figure 8. Receiver Output Enable and Disable Times**

## TYPICAL CHARACTERISTICS



**Figure 9. Typical Waveform of Nonreturn-to-Zero (NRZ), Pseudorandom Binary Sequence (PRBS) Data at 100 Mbps Through 15m, of CAT 5 Unshielded Twisted Pair (UTP) Cable**

TIA/EIA-485-A defines a maximum signaling rate as that in which the transition time of the voltage transition of a logic-state change remains less than or equal to 30% of the bit length. Transition times of greater length perform quite well even though they do not meet the standard by definition.

## TYPICAL CHARACTERISTICS (continued)

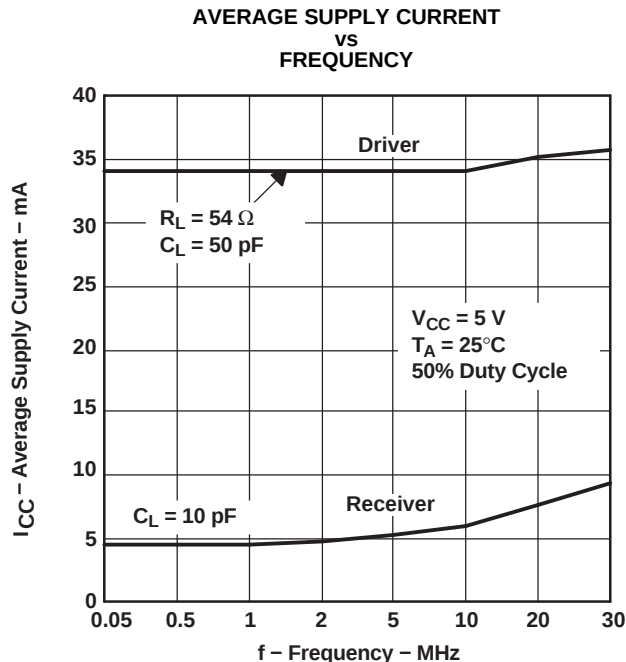


Figure 10.

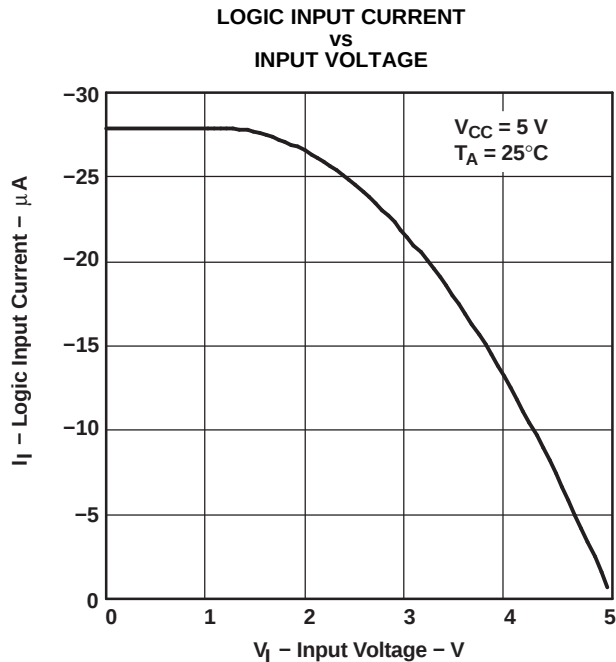


Figure 11.

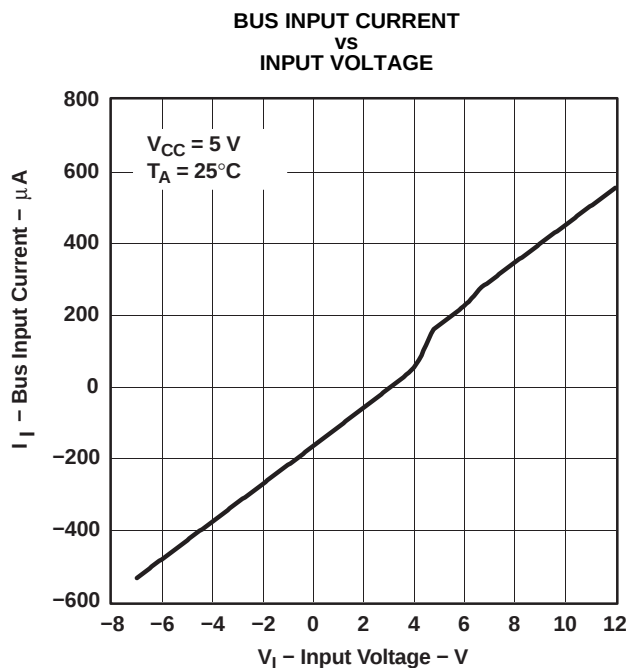


Figure 12.

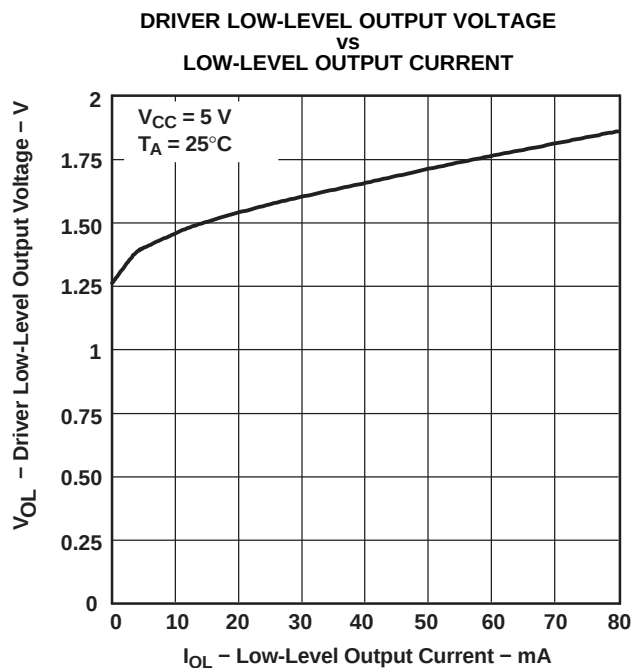


Figure 13.

## TYPICAL CHARACTERISTICS (continued)

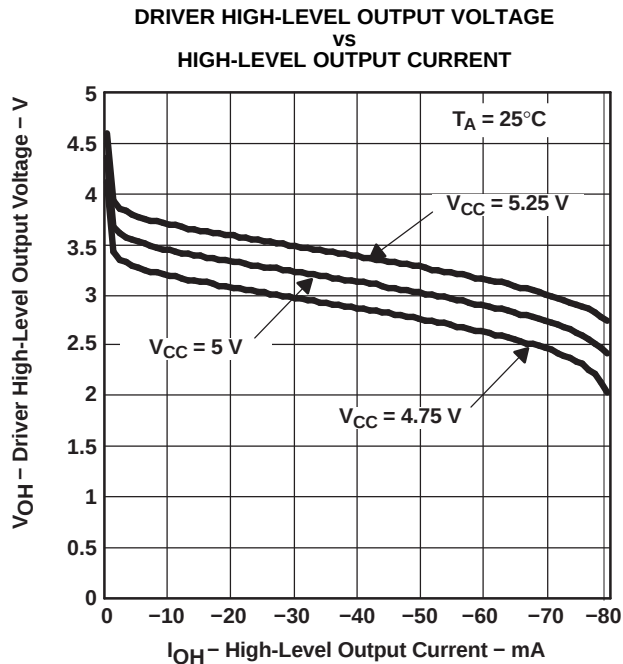


Figure 14.

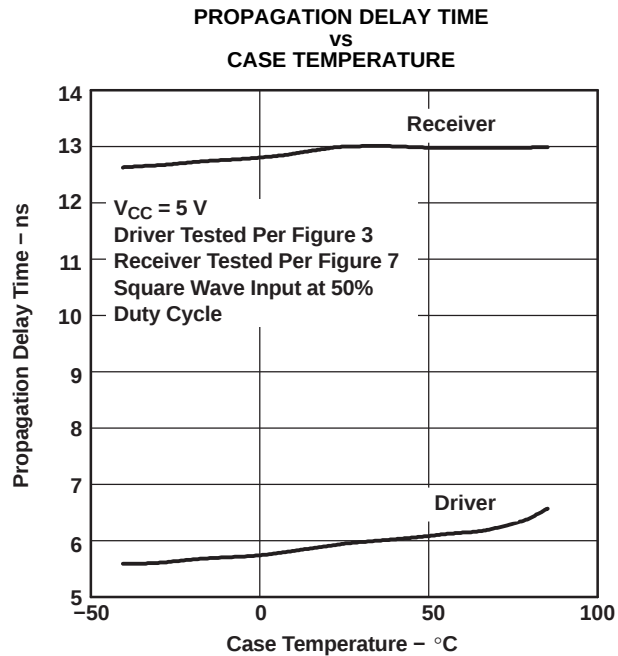
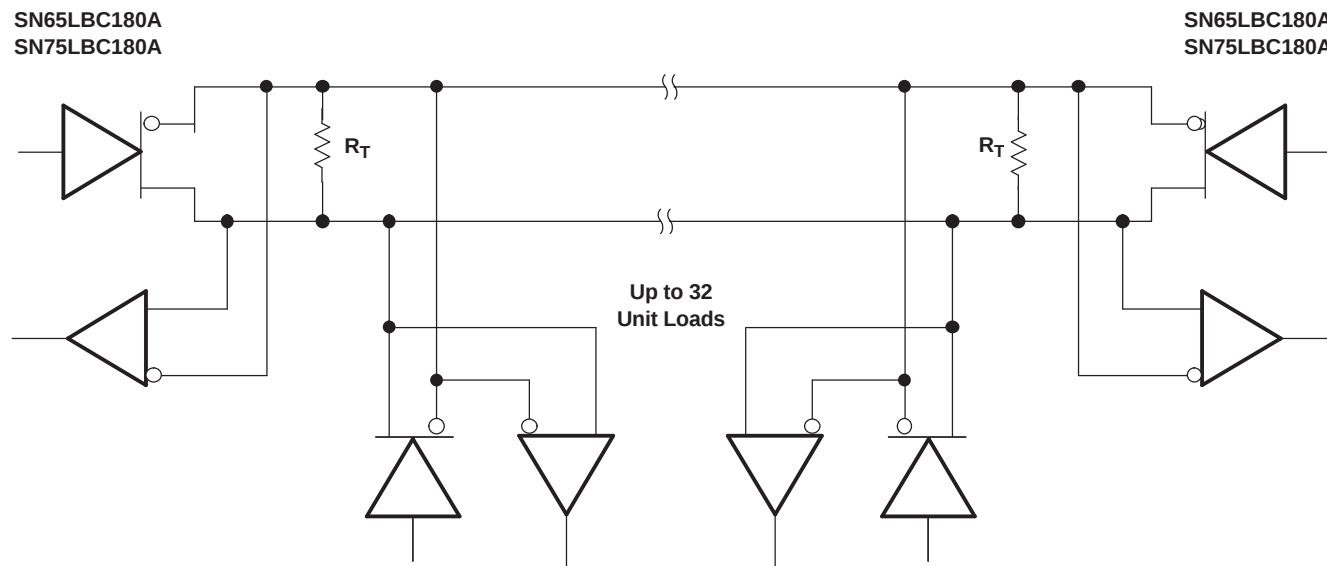


Figure 15.

## APPLICATION INFORMATION



- A. The line should be terminated at both ends in its characteristic impedance ( $R_T = Z_0$ ). Stub lengths off the main line should be kept as short as possible. One SN65LBC180A typically represents less than one unit load.

**Figure 16. Typical Application Circuit**

## Revision History

## PACKAGING INFORMATION

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2)            | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| SN65LBC180AD     | ACTIVE        | SOIC         | D                  | 14   | 50             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | BL180A                  | <a href="#">Samples</a> |
| SN65LBC180ADG4   | ACTIVE        | SOIC         | D                  | 14   | 50             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | BL180A                  | <a href="#">Samples</a> |
| SN65LBC180ADR    | ACTIVE        | SOIC         | D                  | 14   | 2500           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | BL180A                  | <a href="#">Samples</a> |
| SN65LBC180ADRG4  | ACTIVE        | SOIC         | D                  | 14   |                | TBD                        | Call TI                 | Call TI              | -40 to 85    |                         | <a href="#">Samples</a> |
| SN65LBC180AN     | ACTIVE        | PDIP         | N                  | 14   | 25             | Pb-Free<br>(RoHS)          | CU NIPDAU               | N / A for Pkg Type   | -40 to 85    | 65LBC180A               | <a href="#">Samples</a> |
| SN75LBC180AD     | ACTIVE        | SOIC         | D                  | 14   | 50             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | LB180A                  | <a href="#">Samples</a> |
| SN75LBC180ADG4   | ACTIVE        | SOIC         | D                  | 14   | 50             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | LB180A                  | <a href="#">Samples</a> |
| SN75LBC180ADR    | ACTIVE        | SOIC         | D                  | 14   | 2500           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | LB180A                  | <a href="#">Samples</a> |
| SN75LBC180ADRG4  | ACTIVE        | SOIC         | D                  | 14   | 2500           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | LB180A                  | <a href="#">Samples</a> |
| SN75LBC180AN     | ACTIVE        | PDIP         | N                  | 14   | 25             | Pb-Free<br>(RoHS)          | CU NIPDAU               | N / A for Pkg Type   | 0 to 70      | 75LBC180A               | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

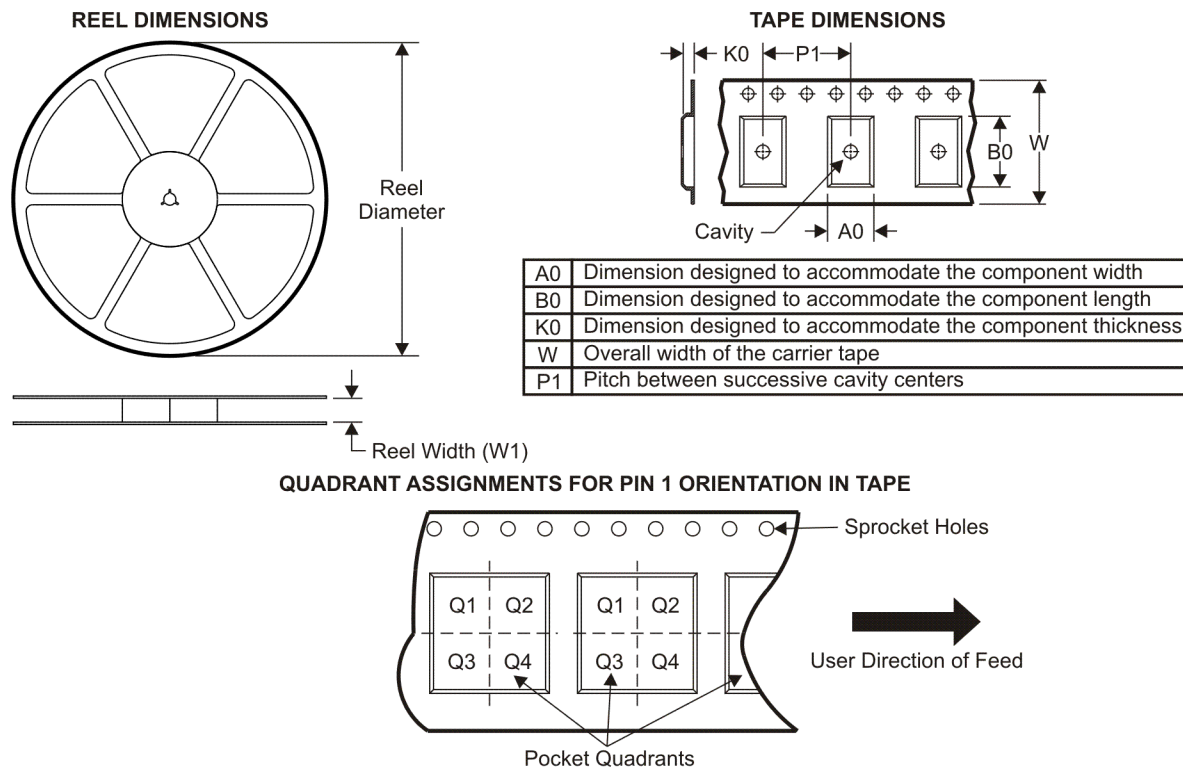
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

- <sup>(3)</sup> MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- <sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- <sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- <sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN65LBC180ADR | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |
| SN75LBC180ADR | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device        | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN65LBC180ADR | SOIC         | D               | 14   | 2500 | 333.2       | 345.9      | 28.6        |
| SN75LBC180ADR | SOIC         | D               | 14   | 2500 | 333.2       | 345.9      | 28.6        |

## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



| PINS **             | 14               | 16               | 18               | 20               |
|---------------------|------------------|------------------|------------------|------------------|
| DIM                 |                  |                  |                  |                  |
| A MAX               | 0.775<br>(19,69) | 0.775<br>(19,69) | 0.920<br>(23,37) | 1.060<br>(26,92) |
| A MIN               | 0.745<br>(18,92) | 0.745<br>(18,92) | 0.850<br>(21,59) | 0.940<br>(23,88) |
| MS-001<br>VARIATION | AA               | BB               | AC               | AD               |



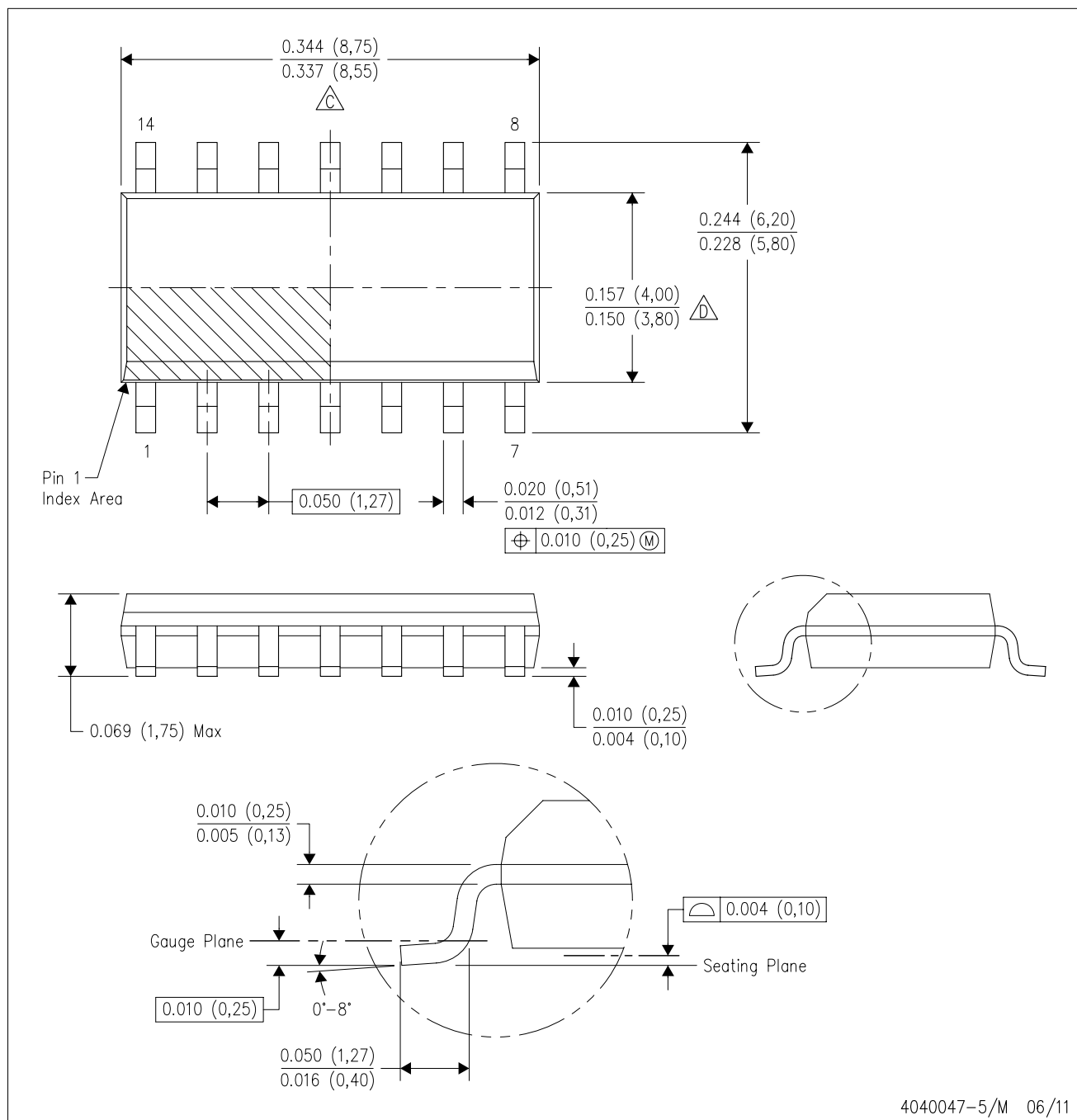
14/18 Pin Only  
20 Pin vendor option

4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040047-5/M 06/11

NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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|                               |                                                                                          |
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