

SN54AHC240, SN74AHC240 OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCLS251H – OCTOBER 1995 – REVISED JULY 2003

- Operating Range 2-V to 5.5-V V_{CC}
- Latch-Up Performance Exceeds 250 mA Per JESD 17

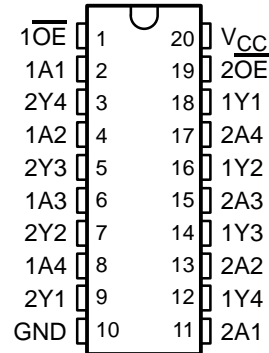
description/ordering information

These octal buffers/drivers are designed specifically to improve the performance and density of 3-state memory-address drivers, clock drivers, and bus-oriented receivers and transmitters.

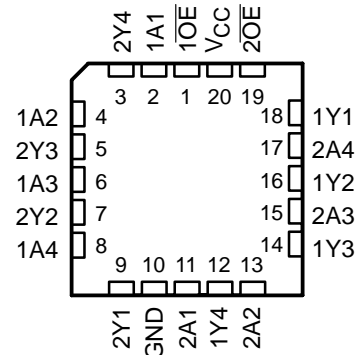
The 'AHC240 devices are organized as two 4-bit buffers/line drivers with separate output-enable (\overline{OE}) inputs. When \overline{OE} is low, the device passes data from the A inputs to the Y outputs. When \overline{OE} is high, the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

SN54AHC240 . . . J OR W PACKAGE
SN74AHC240 . . . DB, DGV, DW, N, NS, OR PW PACKAGE
(TOP VIEW)



SN54AHC240 . . . FK PACKAGE
(TOP VIEW)



ORDERING INFORMATION

| T_A | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|---------------|---------------|-----------------------|------------------|
| -40°C to 85°C | PDIP – N | Tube | SN74AHC240N | SN74AHC240N |
| | SOIC – DW | Tube | SN74AHC240DW | AHC240 |
| | | Tape and reel | SN74AHC240DWR | |
| | SOP – NS | Tape and reel | SN74AHC240NSR | AHC240 |
| | SSOP – DB | Tape and reel | SN74AHC240DBR | HA240 |
| | TSSOP – PW | Tube | SN74AHC240PW | HA240 |
| | | Tape and reel | SN74AHC240PWR | |
| TVSOP – DGV | Tape and reel | SN74AHC240DGV | HA240 | |
| -55°C to 125°C | CDIP – J | Tube | SNJ54AHC240J | SNJ54AHC240J |
| | CFP – W | Tube | SNJ54AHC240W | SNJ54AHC240W |
| | LCCC – FK | Tube | SNJ54AHC240FK | SNJ54AHC240FK |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

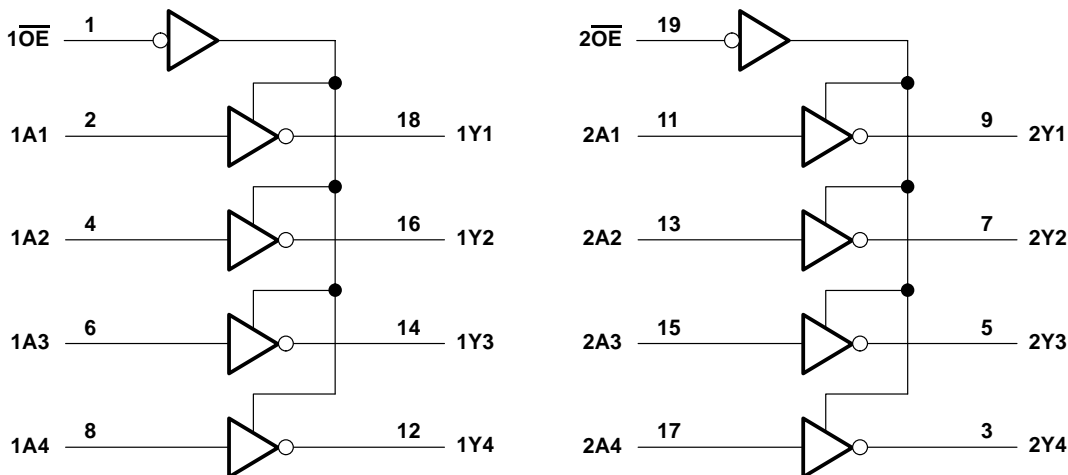
SN54AHC240, SN74AHC240 OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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FUNCTION TABLE
(each 4-bit buffer/driver)

| INPUTS | | OUTPUT |
|-----------------|---|--------|
| \overline{OE} | A | Y |
| L | H | L |
| L | L | H |
| H | X | Z |

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|--|----------------------------|
| Supply voltage range, V_{CC} | -0.5 V to 7 V |
| Input voltage range, V_I (see Note 1) | -0.5 V to 7 V |
| Output voltage range, V_O (see Note 1) | -0.5 V to $V_{CC} + 0.5$ V |
| Input clamp current, I_{IK} ($V_I < 0$) | -20 mA |
| Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) | ± 20 mA |
| Continuous output current, I_O ($V_O = 0$ to V_{CC}) | ± 25 mA |
| Continuous current through V_{CC} or GND | ± 75 mA |
| Package thermal impedance, θ_{JA} (see Note 2): | |
| DB package | 70°C/W |
| DGV package | 92°C/W |
| DW package | 58°C/W |
| N package | 69°C/W |
| NS package | 60°C/W |
| PW package | 83°C/W |
| Storage temperature range, T_{stg} | -65°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

SN54AHC240, SN74AHC240 OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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recommended operating conditions (see Note 3)

| | | SN54AHC240 | | SN74AHC240 | | UNIT |
|-----------------|------------------------------------|---------------------------------|-----------------|------------|-----------------|------|
| | | MIN | MAX | MIN | MAX | |
| V _{CC} | Supply voltage | 2 | 5.5 | 2 | 5.5 | V |
| V _{IH} | High-level input voltage | V _{CC} = 2 V | | 1.5 | | V |
| | | V _{CC} = 3 V | | 2.1 | | |
| | | V _{CC} = 5.5 V | | 3.85 | | |
| V _{IL} | Low-level input voltage | V _{CC} = 2 V | | 0.5 | | V |
| | | V _{CC} = 3 V | | 0.9 | | |
| | | V _{CC} = 5.5 V | | 1.65 | | |
| V _I | Input voltage | 0 | 5.5 | 0 | 5.5 | V |
| V _O | Output voltage | 0 | V _{CC} | 0 | V _{CC} | V |
| I _{OH} | High-level output current | V _{CC} = 2 V | | -50 | | μA |
| | | V _{CC} = 3.3 V ± 0.3 V | | -4 | | |
| | | V _{CC} = 5 V ± 0.5 V | | -8 | | |
| I _{OL} | Low-level output current | V _{CC} = 2 V | | 50 | | μA |
| | | V _{CC} = 3.3 V ± 0.3 V | | 4 | | |
| | | V _{CC} = 5 V ± 0.5 V | | 8 | | |
| Δt/Δv | Input transition rise or fall rate | V _{CC} = 3.3 V ± 0.3 V | | 100 | | ns/V |
| | | V _{CC} = 5 V ± 0.5 V | | 20 | | |
| T _A | Operating free-air temperature | -55 | 125 | -40 | 85 | °C |

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | T _A = 25°C | | | SN54AHC240 | | SN74AHC240 | | UNIT |
|-------------------|--|-----------------|-----------------------|-----|-------|------------|------|------------|-----|------|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| V _{OH} | I _{OH} = -50 μA | 2 V | 1.9 | 2 | | 1.9 | | 1.9 | V | |
| | | 3 V | 2.9 | 3 | | 2.9 | | 2.9 | | |
| | | 4.5 V | 4.4 | 4.5 | | 4.4 | | 4.4 | | |
| | I _{OH} = -4 mA | 3 V | 2.58 | | | 2.48 | | 2.48 | | |
| | I _{OH} = -8 mA | 4.5 V | 3.94 | | | 3.8 | | 3.8 | | |
| V _{OL} | I _{OL} = 50 μA | 2 V | | | 0.1 | | 0.1 | 0.1 | V | |
| | | 3 V | | | 0.1 | | 0.1 | 0.1 | | |
| | | 4.5 V | | | 0.1 | | 0.1 | 0.1 | | |
| | I _{OL} = 4 mA | 3 V | | | 0.36 | | 0.5 | 0.44 | | |
| | I _{OL} = 8 mA | 4.5 V | | | 0.36 | | 0.5 | 0.44 | | |
| I _I | V _I = 5.5 V or GND | 0 V to 5.5 V | | | ±0.1 | | ±1* | ±1 | μA | |
| I _{OZ} † | V _O = V _{CC} or GND, V _I (OE) = V _{IL} or V _{IH} | 5.5 V | | | ±0.25 | | ±2.5 | ±2.5 | μA | |
| I _{CC} | V _I = V _{CC} or GND, I _O = 0 | 5.5 V | | | 4 | | 40 | 40 | μA | |
| C _i | V _I = V _{CC} or GND | 5 V | | 2.5 | 10 | | | 10 | pF | |
| C _o | V _O = V _{CC} or GND | 5 V | | 3.5 | | | | | pF | |

* On products compliant to MIL-PRF-38535, this parameter is not production tested at V_{CC} = 0 V.

† The parameter I_{OZ} includes the input leakage current.



**SN54AHC240, SN74AHC240
OCTAL BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS**

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**switching characteristics over recommended operating free-air temperature range,
V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | T _A = 25°C | | | SN54AHC240 | | SN74AHC240 | | UNIT |
|--------------------|-----------------|-------------|------------------------|-----------------------|-------|-----|------------|-----|------------|-----|------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| t _{PLH} | A | Y | C _L = 15 pF | 5.3* | 7.5* | 1* | 9* | 1 | 9 | ns | |
| t _{PHL} | | | | 5.3* | 7.5* | 1* | 9* | 1 | 9 | | |
| t _{PZH} | \overline{OE} | Y | C _L = 15 pF | 6.6* | 10.6* | 1* | 12.5* | 1 | 12.5 | ns | |
| t _{PZL} | | | | 6.6* | 10.6* | 1* | 12.5* | 1 | 12.5 | | |
| t _{PHZ} | \overline{OE} | Y | C _L = 15 pF | 7.8* | 11.5* | 1* | 12.5* | 1 | 12.5 | ns | |
| t _{PLZ} | | | | 7.8* | 11.5* | 1* | 12.5* | 1 | 12.5 | | |
| t _{PLH} | A | Y | C _L = 50 pF | 7.8 | 11 | 1 | 12.5 | 1 | 12.5 | ns | |
| t _{PHL} | | | | 7.8 | 11 | 1 | 12.5 | 1 | 12.5 | | |
| t _{PZH} | \overline{OE} | Y | C _L = 50 pF | 9.1 | 14.1 | 1 | 16 | 1 | 16 | ns | |
| t _{PZL} | | | | 9.1 | 14.1 | 1 | 16 | 1 | 16 | | |
| t _{PHZ} | \overline{OE} | Y | C _L = 50 pF | 10.3 | 14 | 1 | 16 | 1 | 16 | ns | |
| t _{PLZ} | | | | 10.3 | 14 | 1 | 16 | 1 | 16 | | |
| t _{sk(o)} | | | C _L = 50 pF | | 1.5** | | | | 1.5 | ns | |

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

** On products compliant to MIL-PRF-38535, this parameter does not apply.

**switching characteristics over recommended operating free-air temperature range,
V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | T _A = 25°C | | | SN54AHC240 | | SN74AHC240 | | UNIT |
|--------------------|-----------------|-------------|------------------------|-----------------------|------|-----|------------|-----|------------|-----|------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| t _{PLH} | A | Y | C _L = 15 pF | 3.6* | 5.5* | 1* | 6.5* | 1 | 6.5 | ns | |
| t _{PHL} | | | | 3.6* | 5.5* | 1* | 6.5* | 1 | 6.5 | | |
| t _{PZH} | \overline{OE} | Y | C _L = 15 pF | 4.7* | 7.3* | 1* | 8.5* | 1 | 8.5 | ns | |
| t _{PZL} | | | | 4.7* | 7.3* | 1* | 8.5* | 1 | 8.5 | | |
| t _{PHZ} | \overline{OE} | Y | C _L = 15 pF | 5.2* | 7.2* | 1* | 8.5* | 1 | 8.5 | ns | |
| t _{PLZ} | | | | 5.2* | 7.2* | 1* | 8.5* | 1 | 8.5 | | |
| t _{PLH} | A | Y | C _L = 50 pF | 5.1 | 7.5 | 1 | 8.5 | 1 | 8.5 | ns | |
| t _{PHL} | | | | 5.1 | 7.5 | 1 | 8.5 | 1 | 8.5 | | |
| t _{PZH} | \overline{OE} | Y | C _L = 50 pF | 6.2 | 9.3 | 1 | 10.5 | 1 | 10.5 | ns | |
| t _{PZL} | | | | 6.2 | 9.3 | 1 | 10.5 | 1 | 10.5 | | |
| t _{PHZ} | \overline{OE} | Y | C _L = 50 pF | 6.7 | 9.2 | 1 | 10.5 | 1 | 10.5 | ns | |
| t _{PLZ} | | | | 6.7 | 9.2 | 1 | 10.5 | 1 | 10.5 | | |
| t _{sk(o)} | | | C _L = 50 pF | | 1** | | | | 1 | ns | |

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

** On products compliant to MIL-PRF-38535, this parameter does not apply.



**SN54AHC240, SN74AHC240
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noise characteristics, $V_{CC} = 5\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ (see Note 4)

| PARAMETER | SN74AHC240 | | | UNIT |
|--|------------|------|-----|------|
| | MIN | TYP | MAX | |
| $V_{OL(P)}$ Quiet output, maximum dynamic V_{OL} | | 0.6 | | V |
| $V_{OL(V)}$ Quiet output, minimum dynamic V_{OL} | | -0.6 | | V |
| $V_{OH(V)}$ Quiet output, minimum dynamic V_{OH} | | 4.6 | | V |
| $V_{IH(D)}$ High-level dynamic input voltage | 3.5 | | | V |
| $V_{IL(D)}$ Low-level dynamic input voltage | | | 1.5 | V |

NOTE 4: Characteristics are for surface-mount packages only.

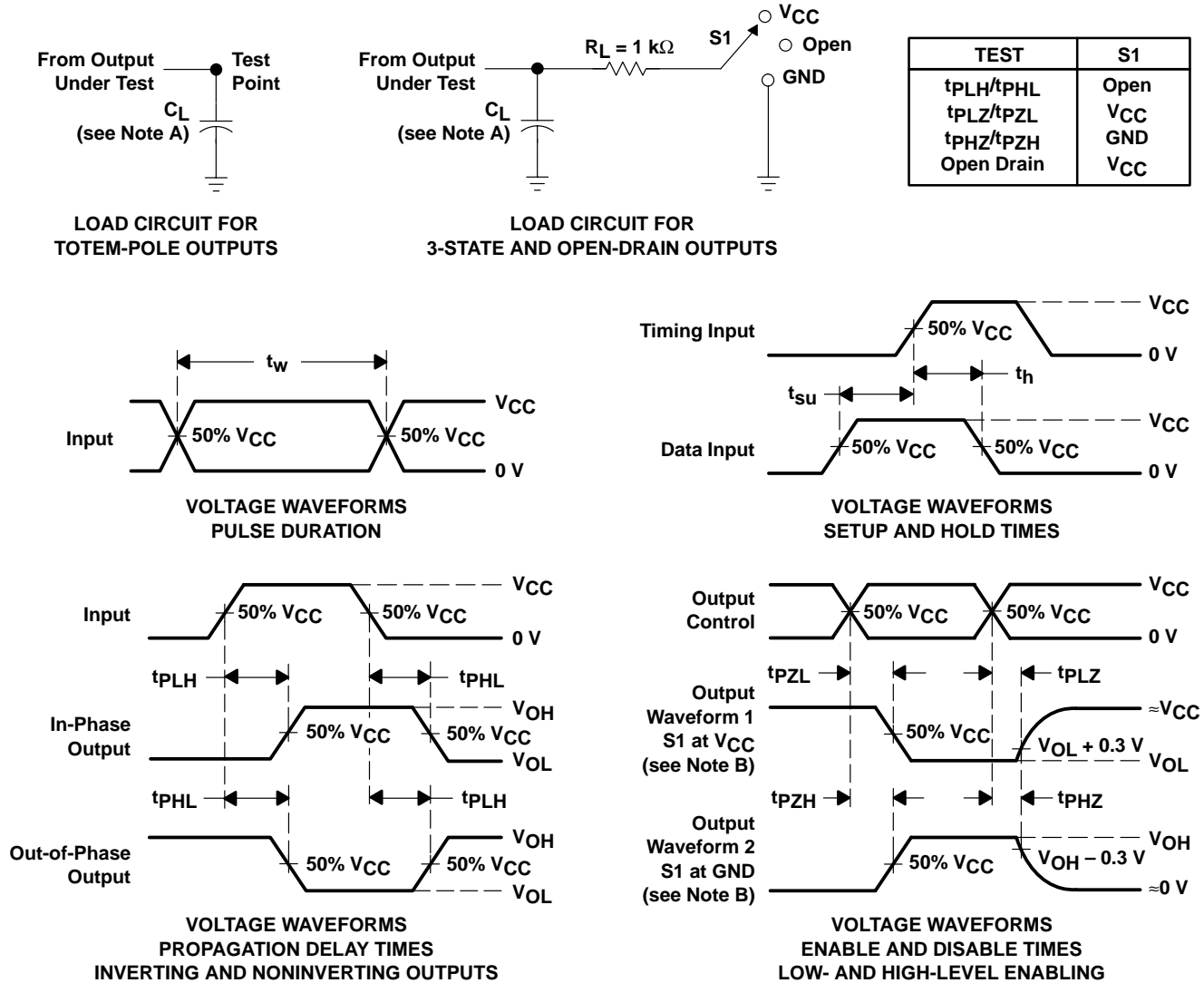
operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

| PARAMETER | TEST CONDITIONS | TYP | UNIT |
|--|-----------------------------|-----|------|
| C_{pd} Power dissipation capacitance | No load, $f = 1\text{ MHz}$ | 10 | pF |

SN54AHC240, SN74AHC240 OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
 - D. The outputs are measured one at a time with one input transition per measurement.
 - E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|--|-------------------------|
| 5962-9680701Q2A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | 5962- 9680701Q2A SNJ54AHC 240FK | Samples |
| 5962-9680701QRA | ACTIVE | CDIP | J | 20 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 5962-9680701QR A SNJ54AHC240J | Samples |
| 5962-9680701QSA | ACTIVE | CFP | W | 20 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 5962-9680701QS A SNJ54AHC240W | Samples |
| SN74AHC240DBLE | OBSOLETE | SSOP | DB | 20 | | TBD | Call TI | Call TI | -40 to 85 | | |
| SN74AHC240DW | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | AHC240 | Samples |
| SN74AHC240DWR | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | AHC240 | Samples |
| SN74AHC240N | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -40 to 85 | SN74AHC240N | Samples |
| SN74AHC240NSR | ACTIVE | SO | NS | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | AHC240 | Samples |
| SN74AHC240PW | ACTIVE | TSSOP | PW | 20 | 70 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HA240 | Samples |
| SN74AHC240PWLE | OBSOLETE | TSSOP | PW | 20 | | TBD | Call TI | Call TI | -40 to 85 | | |
| SN74AHC240PWR | ACTIVE | TSSOP | PW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HA240 | Samples |
| SN74AHC240PWRE4 | ACTIVE | TSSOP | PW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HA240 | Samples |
| SN74AHC240PWRG4 | ACTIVE | TSSOP | PW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HA240 | Samples |
| SNJ54AHC240FK | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | 5962- 9680701Q2A SNJ54AHC 240FK | Samples |
| SNJ54AHC240J | ACTIVE | CDIP | J | 20 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 5962-9680701QR A SNJ54AHC240J | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|-------------------------|----------------------|--------------|-------------------------------------|----------------|
| SNJ54AHC240W | ACTIVE | CFP | W | 20 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 5962-9680701QS A SNJ54AHC240W | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN54AHC240, SN74AHC240 :

- Catalog: [SN74AHC240](#)
- Military: [SN54AHC240](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74AHC240DWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |
| SN74AHC240NSR | SO | NS | 20 | 2000 | 330.0 | 24.4 | 9.0 | 13.0 | 2.4 | 4.0 | 24.0 | Q1 |
| SN74AHC240PWR | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.1 | 1.6 | 8.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74AHC240DWR | SOIC | DW | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74AHC240NSR | SO | NS | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74AHC240PWR | TSSOP | PW | 20 | 2000 | 367.0 | 367.0 | 38.0 |

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within Mil-Std 1835 GDFP2-F20

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



| NO. OF TERMINALS ** | A | | B | |
|---------------------|------------------|------------------|------------------|------------------|
| | MIN | MAX | MIN | MAX |
| 20 | 0.342 (8,69) | 0.358 (9,09) | 0.307 (7,80) | 0.358 (9,09) |
| 28 | 0.442 (11,23) | 0.458 (11,63) | 0.406 (10,31) | 0.458 (11,63) |
| 44 | 0.640 (16,26) | 0.660 (16,76) | 0.495 (12,58) | 0.560 (14,22) |
| 52 | 0.740 (18,78) | 0.761 (19,32) | 0.495 (12,58) | 0.560 (14,22) |
| 68 | 0.938 (23,83) | 0.962 (24,43) | 0.850 (21,6) | 0.858 (21,8) |
| 84 | 1.141 (28,99) | 1.165 (29,59) | 1.047 (26,6) | 1.063 (27,0) |



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW (R-PDSO-G20)

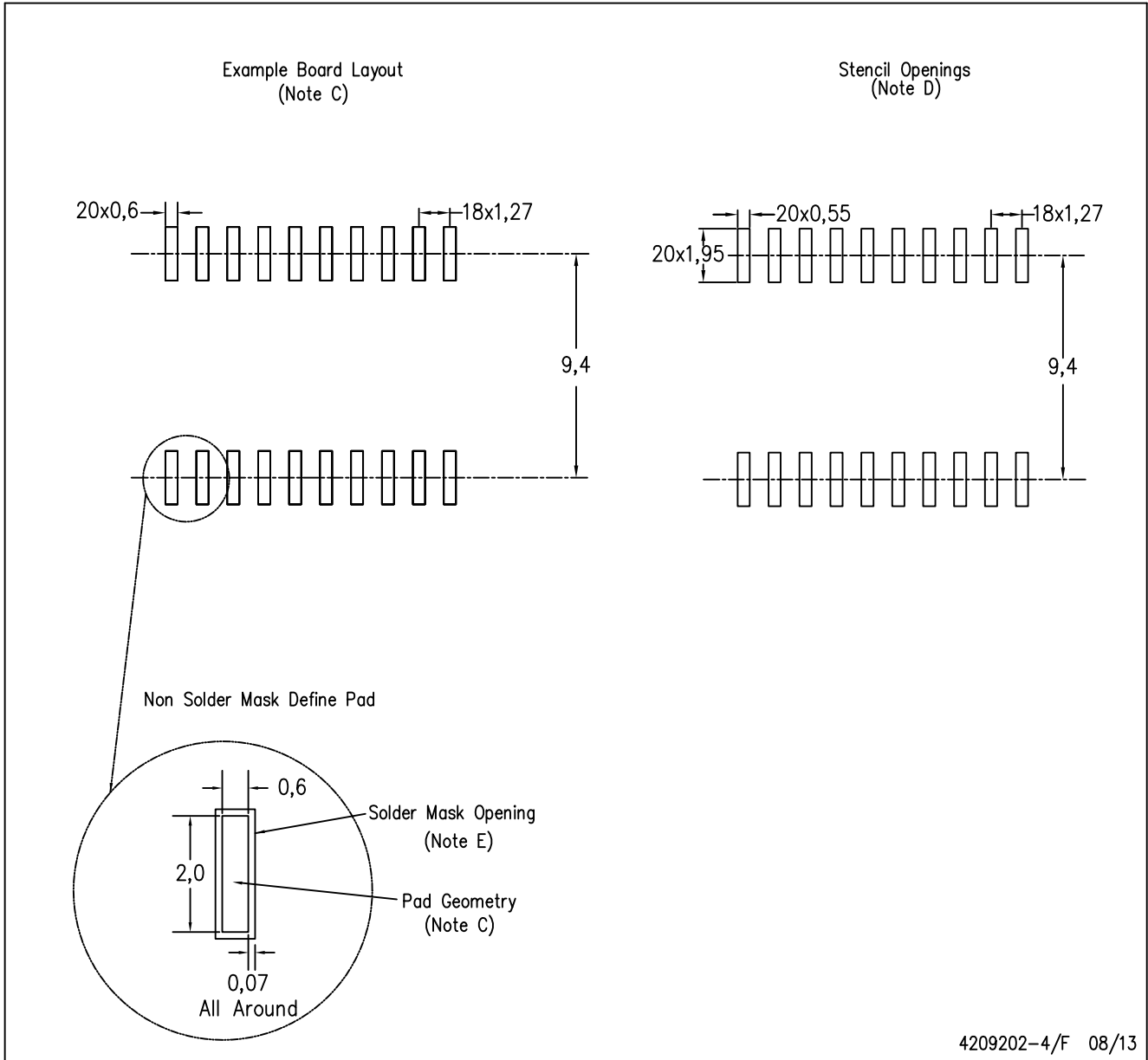
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-013 variation AC.

DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE

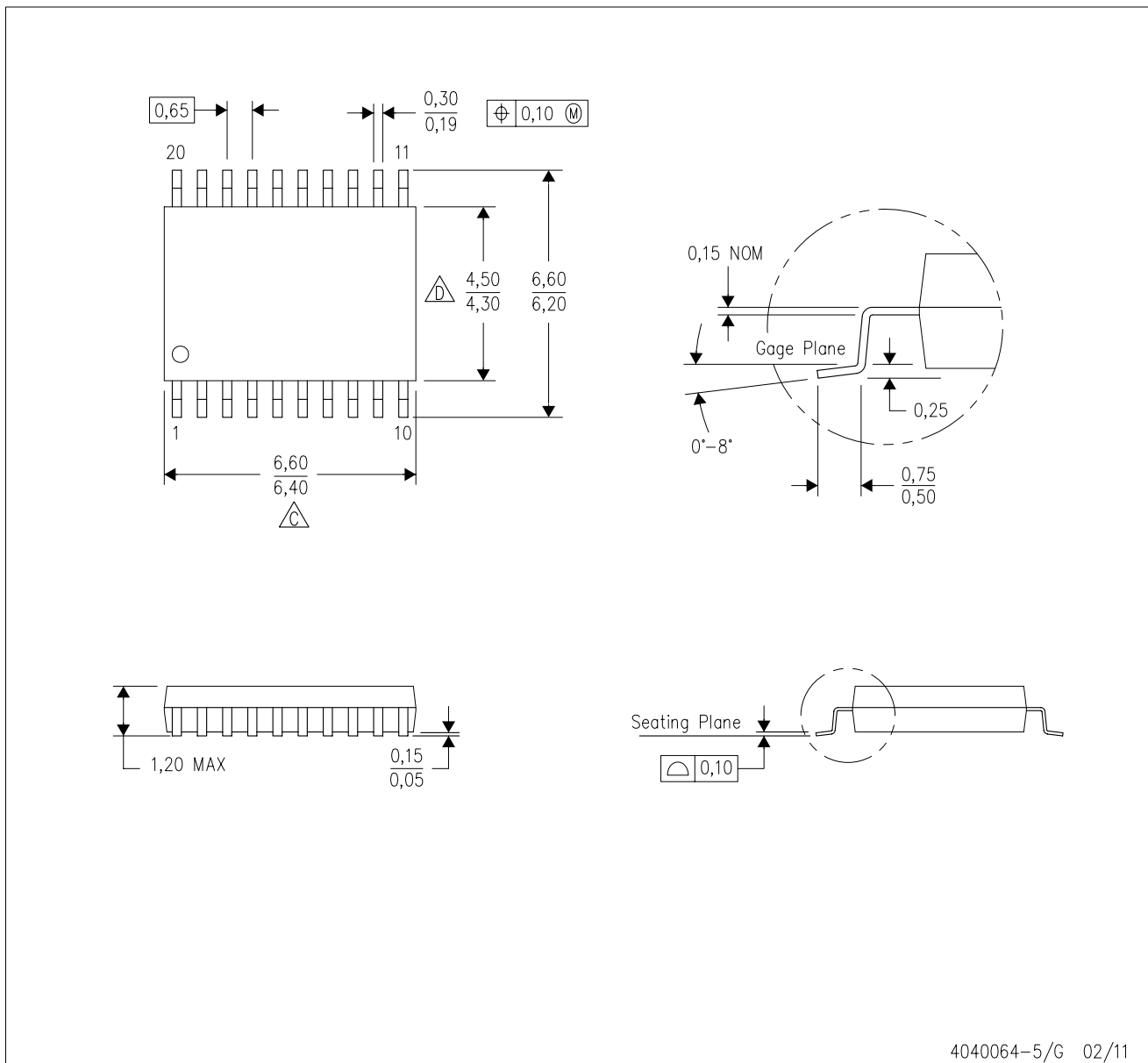


4209202-4/F 08/13

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Refer to IPC7351 for alternate board design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE

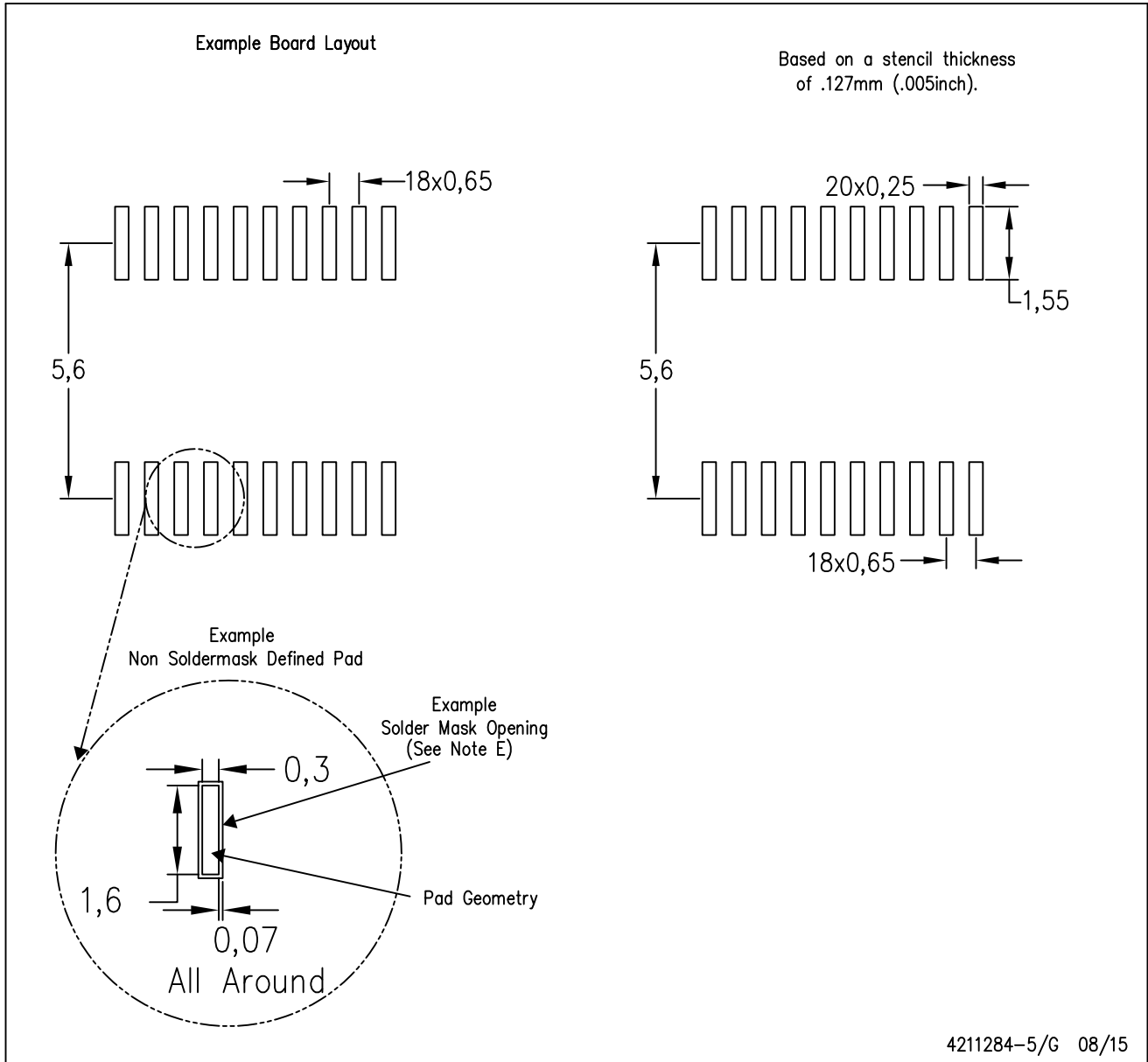


4040064-5/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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