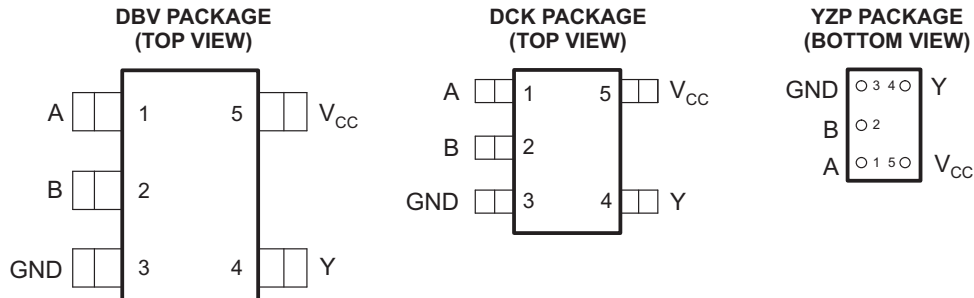


FEATURES

- Available in the Texas Instruments NanoFree™ Package
- Optimized for 1.8-V Operation and Is 3.6-V I/O Tolerant to Support Mixed-Mode Signal Operation
- I_{off} Supports Partial Power-Down-Mode Operation
- Sub-1-V Operable
- Max t_{pd} of 2.5 ns at 1.8 V
- Low Power Consumption, 10- μ A Max I_{CC}
- ± 8 -mA Output Drive at 1.8 V
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)



See mechanical drawings for dimensions.

DESCRIPTION/ORDERING INFORMATION

This single 2-input exclusive-OR gate is operational at 0.8-V to 2.7-V V_{CC} , but is designed specifically for 1.65-V to 1.95-V V_{CC} operation.

The SN74AUC1G86 performs the Boolean function $Y = A \oplus B$ or $Y = \bar{A}B + A\bar{B}$ in positive logic.

A common application is as a true/complement element. If the input is low, the other input is reproduced in true form at the output. If the input is high, the signal on the other input is reproduced inverted at the output.

NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

ORDERING INFORMATION

| T_A | PACKAGE ⁽¹⁾⁽²⁾ | | ORDERABLE PART NUMBER | TOP-SIDE MARKING ⁽³⁾ |
|---------------|--|--------------|-----------------------|---------------------------------|
| –40°C to 85°C | NanoFree™ WCSP (DSBGA) – YZP (Pb-free) | Reel of 3000 | SN74AUC1G86YZPR | – – _UH_ |
| | SOT (SOT-23) – DBV | Reel of 3000 | SN74AUC1G86DBVR | U86_ |
| | SOT (SC-70) – DCK | Reel of 3000 | SN74AUC1G86DCKR | UH_ |

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

(3) DBV/DCK: The actual top-side marking has one additional character that designates the assembly/test site.

YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

NanoFree is a trademark of Texas Instruments.

SN74AUC1G86 SINGLE 2-INPUT EXCLUSIVE-OR GATE

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FUNCTION TABLE

| INPUTS | | OUTPUT Y |
|--------|---|-------------|
| A | B | |
| L | L | L |
| L | H | H |
| H | L | H |
| H | H | L |

EXCLUSIVE-OR LOGIC

An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.



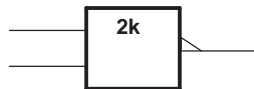
These are five equivalent exclusive-OR symbols valid for an SN74AUC1G86 gate in positive logic; negation may be shown at any two ports.

LOGIC-IDENTITY ELEMENT



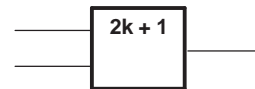
The output is active (low) if all inputs stand at the same logic level (i.e., $A = B$).

EVEN-PARITY ELEMENT



The output is active (low) if an even number of inputs (i.e., 0 or 2) are active.

ODD-PARITY ELEMENT



The output is active (high) if an odd number of inputs (i.e., only 1 of the 2) are active.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---------------|---|-------------|----------------|--------------------|
| V_{CC} | Supply voltage range | -0.5 | 3.6 | V |
| V_I | Input voltage range ⁽²⁾ | -0.5 | 3.6 | V |
| V_O | Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾ | -0.5 | 3.6 | V |
| V_O | Output voltage range ⁽²⁾ | -0.5 | $V_{CC} + 0.5$ | V |
| I_{IK} | Input clamp current | $V_I < 0$ | | -50 mA |
| I_{OK} | Output clamp current | $V_O < 0$ | | -50 mA |
| I_O | Continuous output current | | | ± 20 mA |
| | Continuous current through V_{CC} or GND | | | ± 100 mA |
| θ_{JA} | Package thermal impedance ⁽³⁾ | DBV package | | 206 |
| | | DCK package | | 252 |
| | | YZP package | | 154 |
| T_{stg} | Storage temperature range | -65 | 150 | $^{\circ}\text{C}$ |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS⁽¹⁾

| | | MIN | MAX | UNIT |
|---------------------|------------------------------------|--|----------------------|------|
| V_{CC} | Supply voltage | 0.8 | 2.7 | V |
| V_{IH} | High-level input voltage | $V_{CC} = 0.8\text{ V}$ | V_{CC} | V |
| | | $V_{CC} = 1.1\text{ V to }1.95\text{ V}$ | $0.65 \times V_{CC}$ | |
| | | $V_{CC} = 2.3\text{ V to }2.7\text{ V}$ | 1.7 | |
| V_{IL} | Low-level input voltage | $V_{CC} = 0.8\text{ V}$ | 0 | V |
| | | $V_{CC} = 1.1\text{ V to }1.95\text{ V}$ | $0.35 \times V_{CC}$ | |
| | | $V_{CC} = 2.3\text{ V to }2.7\text{ V}$ | 0.7 | |
| V_I | Input voltage | 0 | 3.6 | V |
| V_O | Output voltage | 0 | V_{CC} | V |
| I_{OH} | High-level output current | $V_{CC} = 0.8\text{ V}$ | -0.7 | mA |
| | | $V_{CC} = 1.1\text{ V}$ | -3 | |
| | | $V_{CC} = 1.4\text{ V}$ | -5 | |
| | | $V_{CC} = 1.65\text{ V}$ | -8 | |
| | | $V_{CC} = 2.3\text{ V}$ | -9 | |
| I_{OL} | Low-level output current | $V_{CC} = 0.8\text{ V}$ | 0.7 | mA |
| | | $V_{CC} = 1.1\text{ V}$ | 3 | |
| | | $V_{CC} = 1.4\text{ V}$ | 5 | |
| | | $V_{CC} = 1.65\text{ V}$ | 8 | |
| | | $V_{CC} = 2.3\text{ V}$ | 9 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | 20 | ns/V |
| T_A | Operating free-air temperature | -40 | 85 | °C |

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V_{CC} | MIN | TYP ⁽¹⁾ | MAX | UNIT |
|-----------|---------------------------------------|----------------|----------------|--------------------|----------|---------------|
| V_{OH} | $I_{OH} = -100\ \mu\text{A}$ | 0.8 V to 2.7 V | $V_{CC} - 0.1$ | | | V |
| | $I_{OH} = -0.7\text{ mA}$ | 0.8 V | | 0.55 | | |
| | $I_{OH} = -3\text{ mA}$ | 1.1 V | | 0.8 | | |
| | $I_{OH} = -5\text{ mA}$ | 1.4 V | | 1 | | |
| | $I_{OH} = -8\text{ mA}$ | 1.65 V | | 1.2 | | |
| | $I_{OH} = -9\text{ mA}$ | 2.3 V | | 1.8 | | |
| V_{OL} | $I_{OL} = 100\ \mu\text{A}$ | 0.8 V to 2.7 V | | | 0.2 | V |
| | $I_{OL} = 0.7\text{ mA}$ | 0.8 V | | 0.25 | | |
| | $I_{OL} = 3\text{ mA}$ | 1.1 V | | | 0.3 | |
| | $I_{OL} = 5\text{ mA}$ | 1.4 V | | | 0.4 | |
| | $I_{OL} = 8\text{ mA}$ | 1.65 V | | | 0.45 | |
| | $I_{OL} = 9\text{ mA}$ | 2.3 V | | | 0.6 | |
| I_i | A or B input $V_I = V_{CC}$ or GND | 0 to 2.7 V | | | ± 5 | μA |
| I_{off} | V_I or $V_O = 2.7\text{ V}$ | 0 | | | ± 10 | μA |
| I_{CC} | $V_I = V_{CC}$ or GND, $I_O = 0$ | 0.8 V to 2.7 V | | | 10 | μA |
| C_i | $V_I = V_{CC}$ or GND | 2.5 V | | 2.5 | | pF |

(1) All typical values are at $T_A = 25^\circ\text{C}$.

SN74AUC1G86

SINGLE 2-INPUT EXCLUSIVE-OR GATE

SCES389J–MARCH 2002–REVISED NOVEMBER 2007

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, $C_L = 15$ pF (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC} = 0.8$ V | $V_{CC} = 1.2$ V ± 0.1 V | | $V_{CC} = 1.5$ V ± 0.1 V | | $V_{CC} = 1.8$ V ± 0.15 V | | | $V_{CC} = 2.5$ V ± 0.2 V | | UNIT |
|-----------|--------------|-------------|------------------|---------------------------------|-----|---------------------------------|-----|----------------------------------|-----|-----|---------------------------------|-----|------|
| | | | TYP | MIN | MAX | MIN | MAX | MIN | TYP | MAX | MIN | MAX | |
| t_{pd} | A | Y | 5.5 | 0.8 | 3.8 | 0.5 | 2.6 | 0.4 | 1 | 1.7 | 0.3 | 1.3 | ns |
| | B | | 5 | 0.8 | 3.8 | 0.5 | 2.6 | 0.4 | 1 | 1.7 | 0.3 | 1.2 | |

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, $C_L = 30$ pF (unless otherwise noted) (see Figure 1)

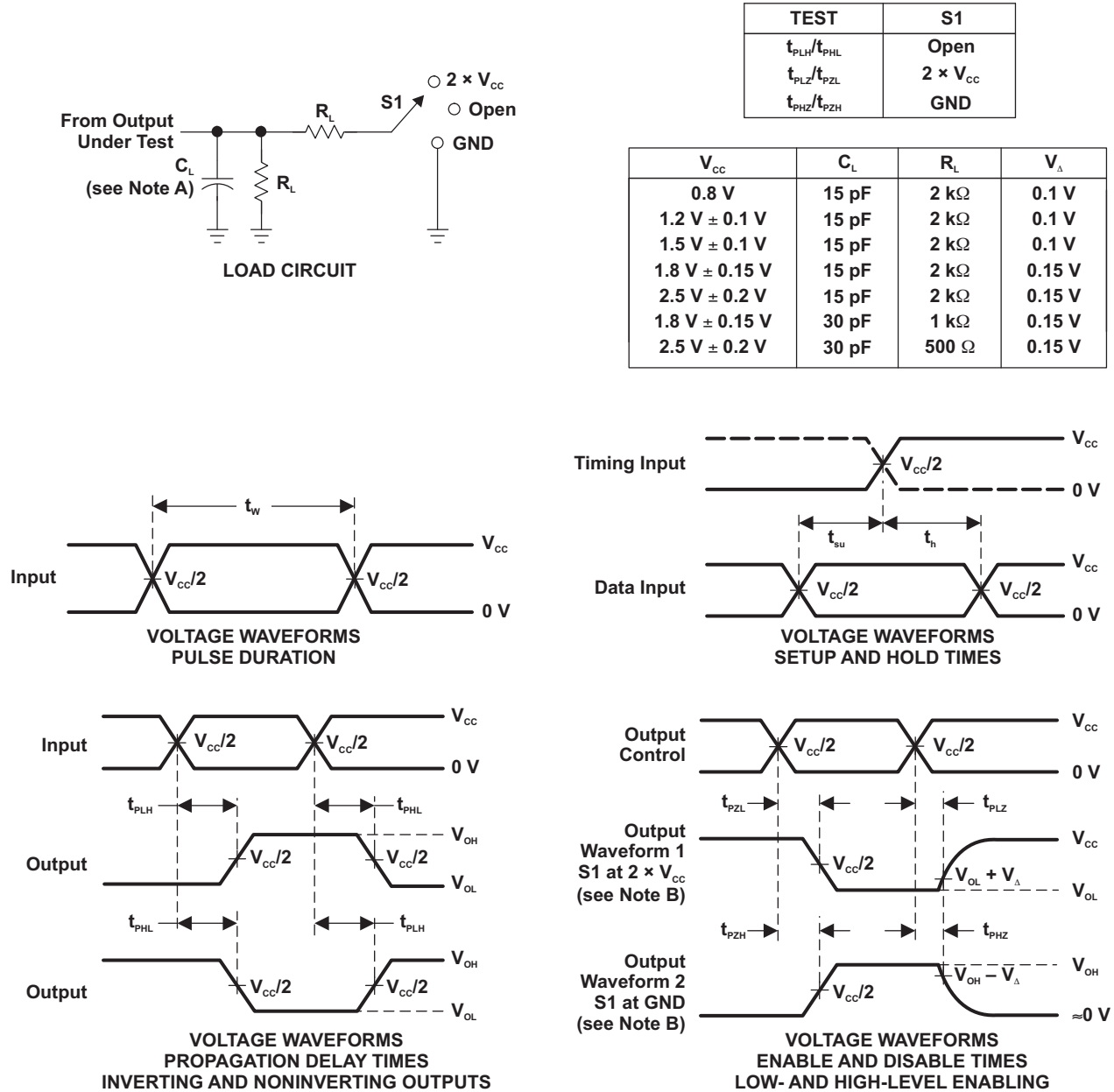
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC} = 1.8$ V ± 0.15 V | | | $V_{CC} = 2.5$ V ± 0.2 V | | UNIT |
|-----------|--------------|-------------|----------------------------------|-----|-----|---------------------------------|-----|------|
| | | | MIN | TYP | MAX | MIN | MAX | |
| t_{pd} | A | Y | 0.8 | 1.5 | 2.6 | 0.7 | 2 | ns |
| | B | | 0.8 | 1.5 | 2.6 | 0.7 | 2 | |

OPERATING CHARACTERISTICS

$T_A = 25^\circ\text{C}$

| PARAMETER | TEST CONDITIONS | $V_{CC} = 0.8$ V | $V_{CC} = 1.2$ V | $V_{CC} = 1.5$ V | $V_{CC} = 1.8$ V | $V_{CC} = 2.5$ V | UNIT |
|--|-----------------|------------------|------------------|------------------|------------------|------------------|------|
| | | TYP | TYP | TYP | TYP | TYP | |
| C_{pd} Power dissipation capacitance | $f = 10$ MHz | 16 | 16 | 16.5 | 17 | 18.5 | pF |

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_o = 50 \Omega$, slew rate ≥ 1 V/ns.
 D. The outputs are measured one at a time, with one transition per measurement.
 E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 F. t_{PZL} and t_{PZH} are the same as t_{en} .
 G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|-------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| SN74AUC1G86DBVR | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | U86R | Samples |
| SN74AUC1G86DBVRE4 | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | U86R | Samples |
| SN74AUC1G86DCKR | ACTIVE | SC70 | DCK | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | UHR | Samples |
| SN74AUC1G86YZPR | ACTIVE | DSBGA | YZP | 5 | 3000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | (UH7 ~ UHN) | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74AUC1G86DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| SN74AUC1G86DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 8.4 | 2.47 | 2.3 | 1.25 | 4.0 | 8.0 | Q3 |
| SN74AUC1G86YZPR | DSBGA | YZP | 5 | 3000 | 178.0 | 9.2 | 1.02 | 1.52 | 0.63 | 4.0 | 8.0 | Q1 |

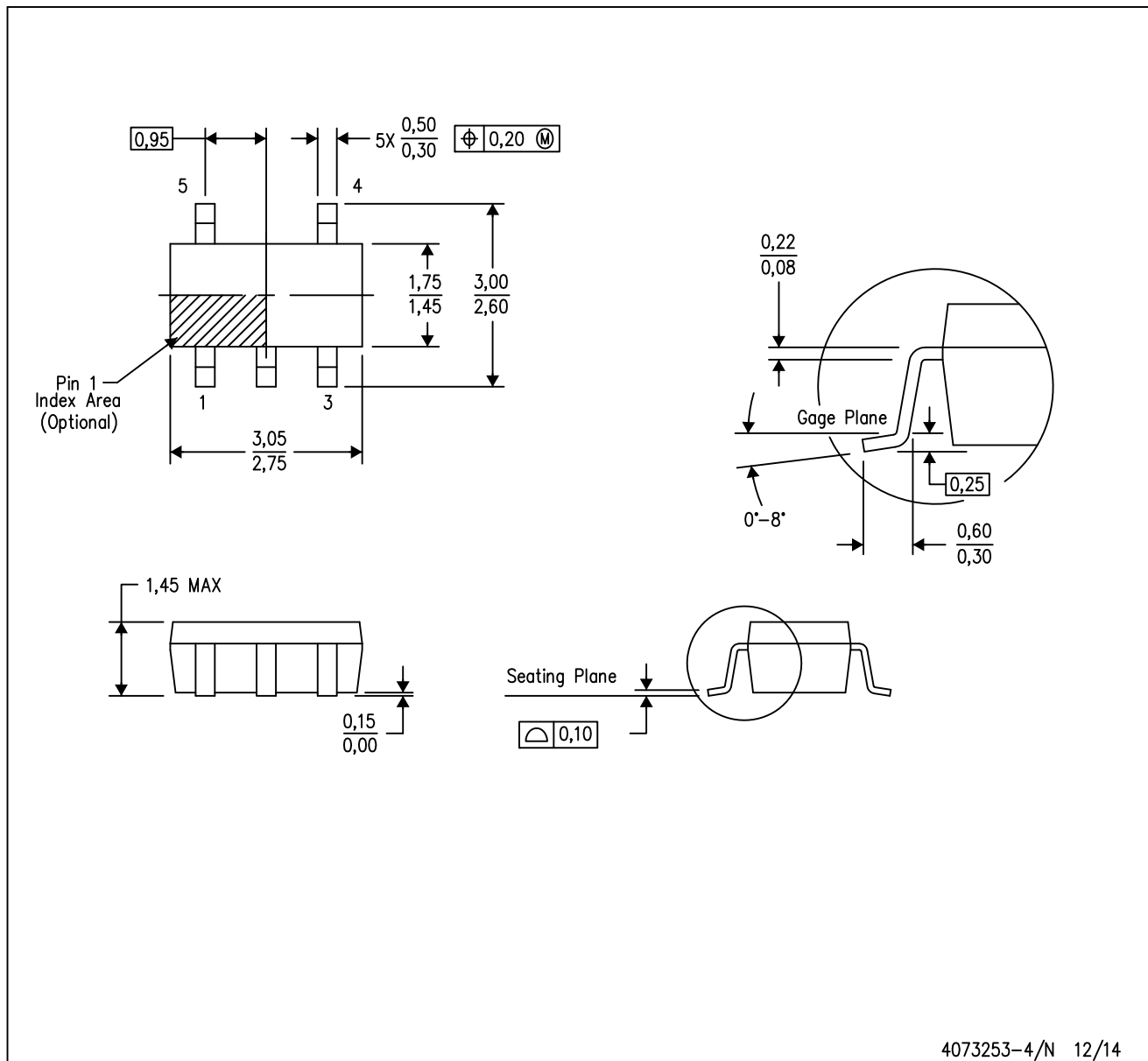
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74AUC1G86DBVR | SOT-23 | DBV | 5 | 3000 | 202.0 | 201.0 | 28.0 |
| SN74AUC1G86DCKR | SC70 | DCK | 5 | 3000 | 202.0 | 201.0 | 28.0 |
| SN74AUC1G86YZPR | DSBGA | YZP | 5 | 3000 | 220.0 | 220.0 | 35.0 |

DBV (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - Falls within JEDEC MO-178 Variation AA.

DBV (R-PDSO-G5)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

DCK (R-PDSO-G5)

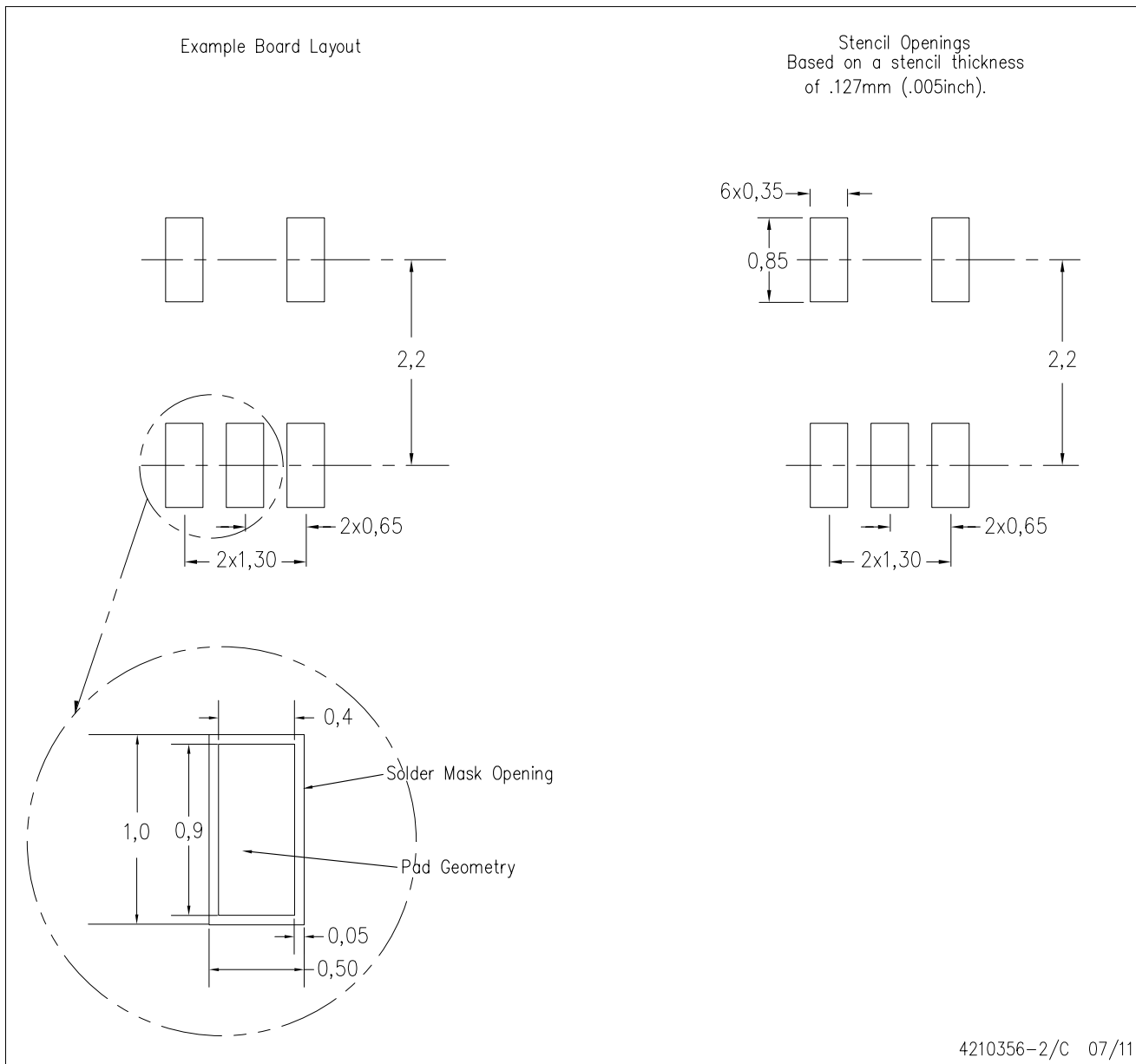
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Falls within JEDEC MO-203 variation AA.

DCK (R-PDSO-G5)

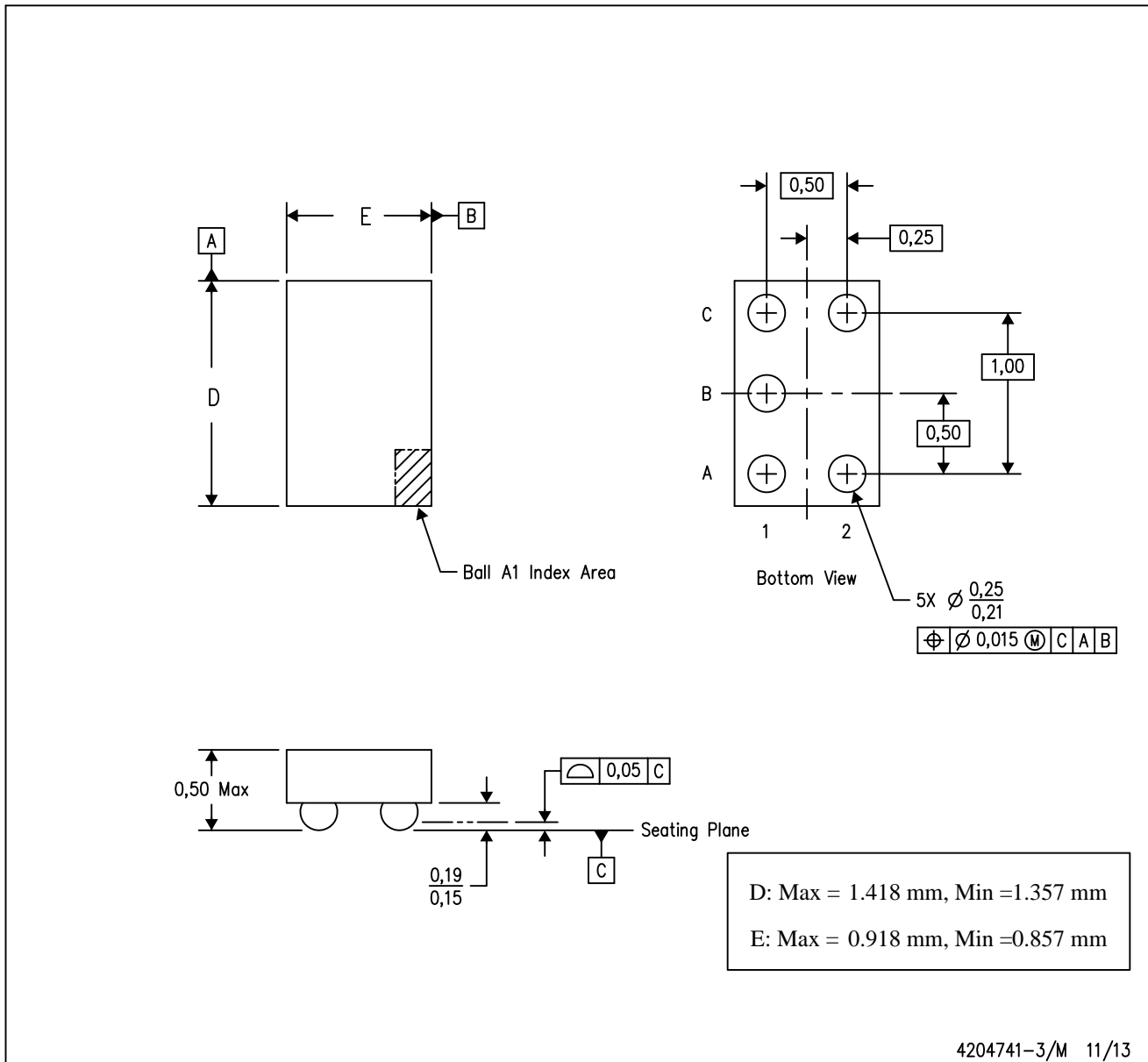
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

YZP (R-XBGA-N5)

DIE-SIZE BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. NanoFree™ package configuration.

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