

SN74AUCH32374

32-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

SCES476 – AUGUST 2003

- Member of the Texas Instruments Widebus+™ Family
- Optimized for 1.8-V Operation and is 3.6-V I/O Tolerant to Support Mixed-Mode Signal Operation
- I_{off} Supports Partial-Power-Down Mode Operation
- Sub 1-V Operable
- Max t_{pd} of 2.8 ns at 1.8 V
- Low Power Consumption, 40- μ A Max I_{CC}
- ± 8 -mA Output Drive at 1.8 V
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

description/ordering information

This 32-bit edge-triggered D-type flip-flop is operational at 0.8-V to 2.7-V V_{CC} , but is designed specifically for 1.65-V to 1.95-V V_{CC} operation.

The SN74AUCH32374 is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers. It can be used as four 8-bit flip-flops, two 16-bit flip-flops, or one 32-bit flip-flop. On the positive transition of the clock (CLK) input, the Q outputs of the flip-flop take on the logic levels set up at the data (D) inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

$\overline{OE}$ does not affect internal operations of the latch. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	LFBGA – GKE	Tape and reel	SN74AUCH32374GKER	MK374

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus+ is a trademark of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



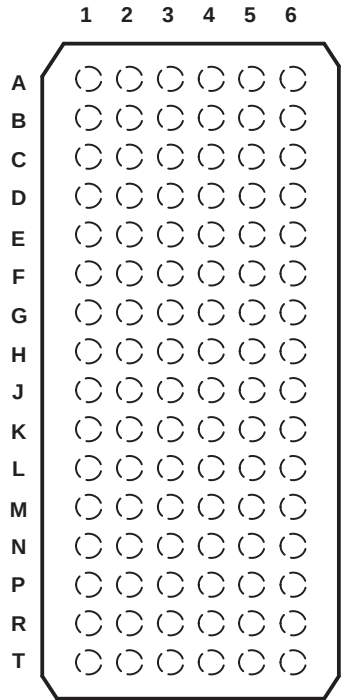
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2003, Texas Instruments Incorporated

SN74AUCH32374
32-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP
WITH 3-STATE OUTPUTS

SCES476 – AUGUST 2003

GKE PACKAGE
(TOP VIEW)



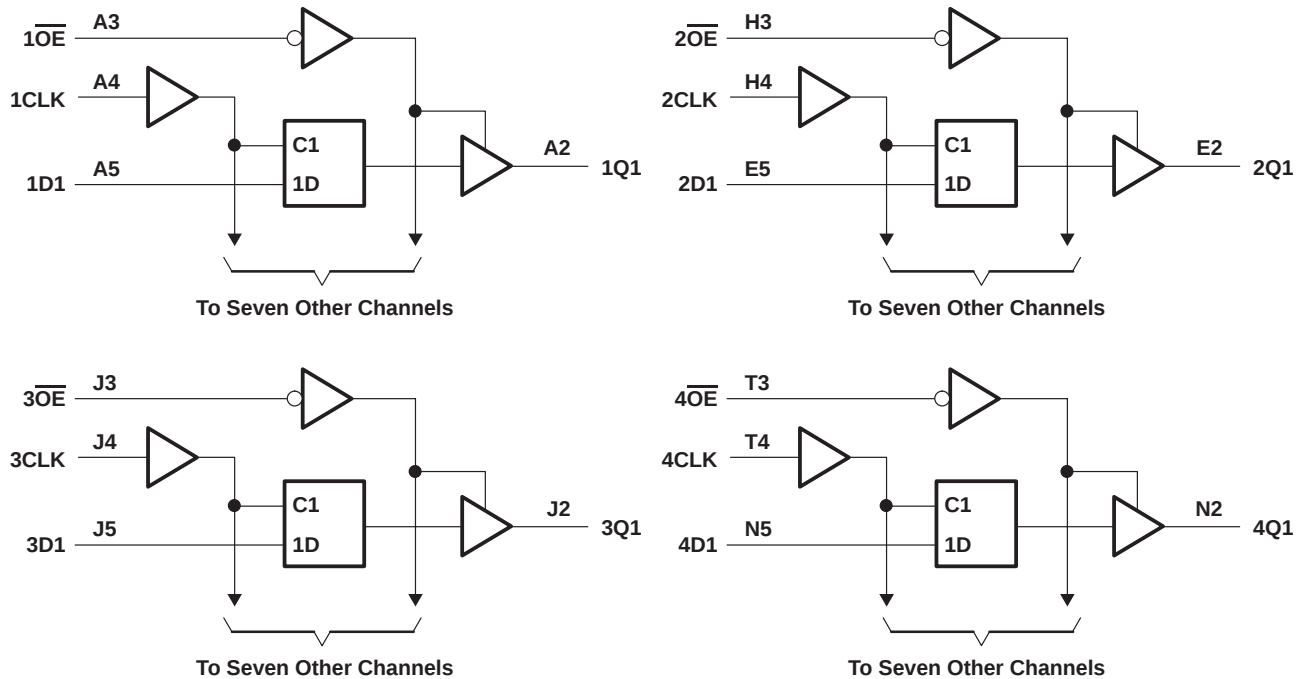
terminal assignments

	1	2	3	4	5	6
A	1Q2	1Q1	1 $\overline{\text{OE}}$	1CLK	1D1	1D2
B	1Q4	1Q3	GND	GND	1D3	1D4
C	1Q6	1Q5	V _{CC}	V _{CC}	1D5	1D6
D	1Q8	1Q7	GND	GND	1D7	1D8
E	2Q2	2Q1	GND	GND	2D1	2D2
F	2Q4	2Q3	V _{CC}	V _{CC}	2D3	2D4
G	2Q6	2Q5	GND	GND	2D5	2D6
H	2Q7	2Q8	2 $\overline{\text{OE}}$	2CLK	2D8	2D7
J	3Q2	3Q1	3 $\overline{\text{OE}}$	3CLK	3D1	3D2
K	3Q4	3Q3	GND	GND	3D3	3D4
L	3Q6	3Q5	V _{CC}	V _{CC}	3D5	3D6
M	3Q8	3Q7	GND	GND	3D7	3D8
N	4Q2	4Q1	GND	GND	4D1	4D2
P	4Q4	4Q3	V _{CC}	V _{CC}	4D3	4D4
R	4Q6	4Q5	GND	GND	4D5	4D6
T	4Q7	4Q8	4 $\overline{\text{OE}}$	4CLK	4D8	4D7

FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT Q
$\overline{\text{OE}}$	CLK	D	
L	↑	H	H
L	↑	L	L
L	H or L	X	Q ₀
H	X	X	Z

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 3.6 V
Input voltage range, V_I (see Note 1)	–0.5 V to 3.6 V
Voltage range applied to any output in the high-impedance or power-off state, V_O	
(see Note 1)	–0.5 V to 3.6 V
Output voltage range, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O	±20 mA
Continuous current through V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 2)	40°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

SN74AUCH32374

32-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

SCES476 – AUGUST 2003

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	0.8	2.7	V
V_{IH}	High-level input voltage	$V_{CC} = 0.8\text{ V}$	V_{CC}	V
		$V_{CC} = 1.1\text{ V to }1.95\text{ V}$	$0.65 \times V_{CC}$	
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	1.7	
V_{IL}	Low-level input voltage	$V_{CC} = 0.8\text{ V}$	0	V
		$V_{CC} = 1.1\text{ V to }1.95\text{ V}$	$0.35 \times V_{CC}$	
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	0.7	
V_I	Input voltage	0	3.6	V
V_O	Output voltage	Active state	0	V_{CC}
		3-state	0	3.6
I_{OH}	High-level output current	$V_{CC} = 0.8\text{ V}$	-0.7	mA
		$V_{CC} = 1.1\text{ V}$	-3	
		$V_{CC} = 1.4\text{ V}$	-5	
		$V_{CC} = 1.65\text{ V}$	-8	
		$V_{CC} = 2.3\text{ V}$	-9	
I_{OL}	Low-level output current	$V_{CC} = 0.8\text{ V}$	0.7	mA
		$V_{CC} = 1.1\text{ V}$	3	
		$V_{CC} = 1.4\text{ V}$	5	
		$V_{CC} = 1.65\text{ V}$	8	
		$V_{CC} = 2.3\text{ V}$	9	
$\Delta t/\Delta v$	Input transition rise or fall rate		20	ns/V
T_A	Operating free-air temperature	-40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN74AUCH32374
32-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP
WITH 3-STATE OUTPUTS
 SCES476 – AUGUST 2003

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP [†]	MAX	UNIT
V _{OH}		I _{OH} = -100 μA	0.8 V to 2.7 V	V _{CC} -0.1			V
		I _{OH} = -0.7 mA	0.8 V	0.55			
		I _{OH} = -3 mA	1.1 V	0.8			
		I _{OH} = -5 mA	1.4 V	1			
		I _{OH} = -8 mA	1.65 V	1.2			
		I _{OH} = -9 mA	2.3 V	1.8			
V _{OL}		I _{OL} = 100 μA	0.8 V to 2.7 V	0.2			V
		I _{OL} = 0.7 mA	0.8 V	0.25			
		I _{OL} = 3 mA	1.1 V	0.3			
		I _{OL} = 5 mA	1.4 V	0.4			
		I _{OL} = 8 mA	1.65 V	0.45			
		I _{OL} = 9 mA	2.3 V	0.6			
I _I	All inputs	V _I = V _{CC} or GND	0 to 2.7 V	±5			μA
I _{BHL} [‡]		V _I = 0.35 V	1.1 V	10			μA
		V _I = 0.47 V	1.4 V	15			
		V _I = 0.57 V	1.65 V	20			
		V _I = 0.7 V	2.3 V	40			
I _{BHH} [§]		V _I = 0.8 V	1.1 V	-5			μA
		V _I = 0.9 V	1.4 V	-15			
		V _I = 1.07 V	1.65 V	-20			
		V _I = 1.7 V	2.3 V	-40			
I _{BHLO} [¶]		V _I = 0 to V _{CC}	1.3 V	75			μA
			1.6 V	125			
			1.95 V	175			
			2.7 V	275			
I _{BHHO} [#]		V _I = 0 to V _{CC}	1.3 V	-75			μA
			1.6 V	-125			
			1.95 V	-175			
			2.7 V	-275			
I _{off}		V _I or V _O = 2.7 V	0	±10			μA
I _{OZ}		V _O = V _{CC} or GND	2.7 V	±10			μA
I _{CC}		V _I = V _{CC} or GND, I _O = 0	0.8 V to 2.7 V	40			μA
C _i		V _I = V _{CC} or GND	2.5 V	3			pF
C _O		V _O = V _{CC} or GND	2.5 V	5			pF

[†] All typical values are at T_A = 25°C.

[‡] The bus-hold circuit can sink at least the minimum low sustaining current at V_{IL} max. I_{BHL} should be measured after lowering V_{IN} to GND and then raising it to V_{IL} max.

[§] The bus-hold circuit can source at least the minimum high sustaining current at V_{IH} min. I_{BHH} should be measured after raising V_{IN} to V_{CC} and then lowering it to V_{IH} min.

[¶] An external driver must source at least I_{BHLO} to switch this node from low to high.

[#] An external driver must sink at least I_{BHHO} to switch this node from high to low.



SN74AUCH32374

32-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

SCES476 – AUGUST 2003

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		V _{CC} = 0.8 V	V _{CC} = 1.2 V ± 0.1 V		V _{CC} = 1.5 V ± 0.1 V		V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		UNIT
		TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency	85	250		250		250		250		MHz
t _w	Pulse duration, CLK high or low	5.9	1.9		1.9		1.9		1.9		ns
t _{su}	Setup time, data before CLK↑	1.4	1.2		0.7		0.6		0.6		ns
t _h	Hold time, data after CLK↑	0.1	0.4		0.4		0.4		0.4		ns

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 0.8 V	V _{CC} = 1.2 V ± 0.1 V		V _{CC} = 1.5 V ± 0.1 V		V _{CC} = 1.8 V ± 0.15 V			V _{CC} = 2.5 V ± 0.2 V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX	
f _{max}			85	250		250		250			250		MHz
t _{pd}	CLK	Q	7.3	1	4.5	0.8	2.9	0.7	1.5	2.8	0.7	2.2	ns
t _{en}	$\overline{\text{OE}}$	Q	7	1.2	5.3	0.8	3.6	0.8	1.5	2.9	0.7	2.2	ns
t _{dis}	$\overline{\text{OE}}$	Q	8.2	2	7.1	1	4.8	1.4	2.7	4.5	0.5	2.2	ns

operating characteristics, T_A = 25°C[†]

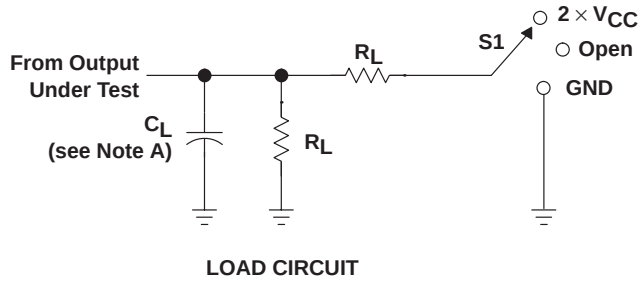
PARAMETER			TEST CONDITIONS	V _{CC} = 0.8 V	V _{CC} = 1.2 V	V _{CC} = 1.5 V	V _{CC} = 1.8 V	V _{CC} = 2.5 V	UNIT
				TYP	TYP	TYP	TYP	TYP	
C _{pd} [‡] (each output)	Power dissipation capacitance	Outputs enabled, 1 output switching	1 f _{data} = 5 MHz 1 f _{clk} = 10 MHz 1 f _{out} = 5 MHz $\overline{\text{OE}}$ = GND C _L = 0 pF	24	24	24.1	26.2	31.2	pF
C _{pd} (Z)	Power dissipation capacitance	Outputs disabled, 1 clock and 1 data switching	1 f _{data} = 5 MHz 1 f _{clk} = 10 MHz f _{out} = not switching $\overline{\text{OE}}$ = V _{CC} C _L = 0 pF	7.5	7.5	8	9.4	13.2	pF
C _{pd} [§] (each clock)	Power dissipation capacitance	Outputs disabled, clock only switching	1 f _{data} = 0 MHz 1 f _{clk} = 10 MHz f _{out} = not switching $\overline{\text{OE}}$ = V _{CC} C _L = 0 pF	13.8	13.8	14	14.7	17.5	pF

[†] Total device C_{pd} for multiple (n) outputs switching and (y) clocks inputs switching = {n * C_{pd} (each output)} + {y * C_{pd} (each clock)}.

[‡] C_{pd} (each output) is the C_{pd} for each data bit (input and output circuitry) as it operates at 5 MHz (Note: the clock is operating at 10 MHz in this test, but its I_{CC} component has been subtracted out).

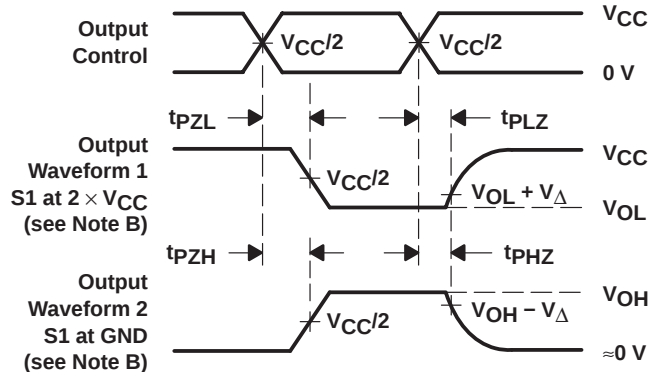
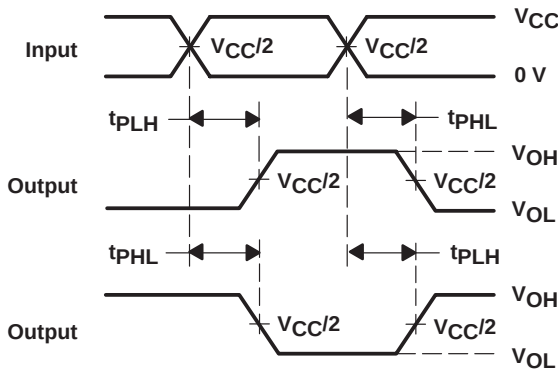
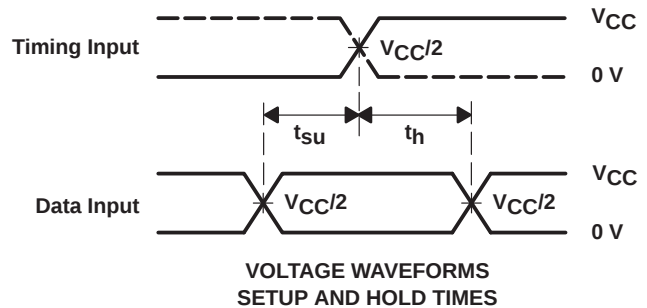
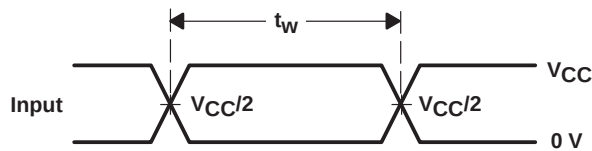
[§] C_{pd} (each clock) is the C_{pd} for the clock circuitry only as it operates at 10 MHz.

PARAMETER MEASUREMENT INFORMATION



TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND

V_{CC}	C_L	R_L	V_{Δ}
0.8 V	15 pF	2 k Ω	0.1 V
$1.2 \text{ V} \pm 0.1 \text{ V}$	15 pF	2 k Ω	0.1 V
$1.5 \text{ V} \pm 0.1 \text{ V}$	15 pF	2 k Ω	0.1 V
$1.8 \text{ V} \pm 0.15 \text{ V}$	30 pF	1 k Ω	0.15 V
$2.5 \text{ V} \pm 0.2 \text{ V}$	30 pF	500 Ω	0.15 V



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O = 50 \Omega$, slew rate ≥ 1 V/ns.
 D. The outputs are measured one at a time with one transition per measurement.
 E. t_{PLZ} and t_{PHZ} are the same as t_{dLs} .
 F. t_{PZL} and t_{PZH} are the same as t_{en} .
 G. t_{PLH} and t_{PHL} are the same as t_{pd} .
 H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AUCH32374GKER	OBSOLETE	LFBGA	GKE	96		TBD	Call TI	Call TI	-40 to 85		
SN74AUCH32374ZKER	ACTIVE	LFBGA	ZKE	96	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	-40 to 85	MK374	Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

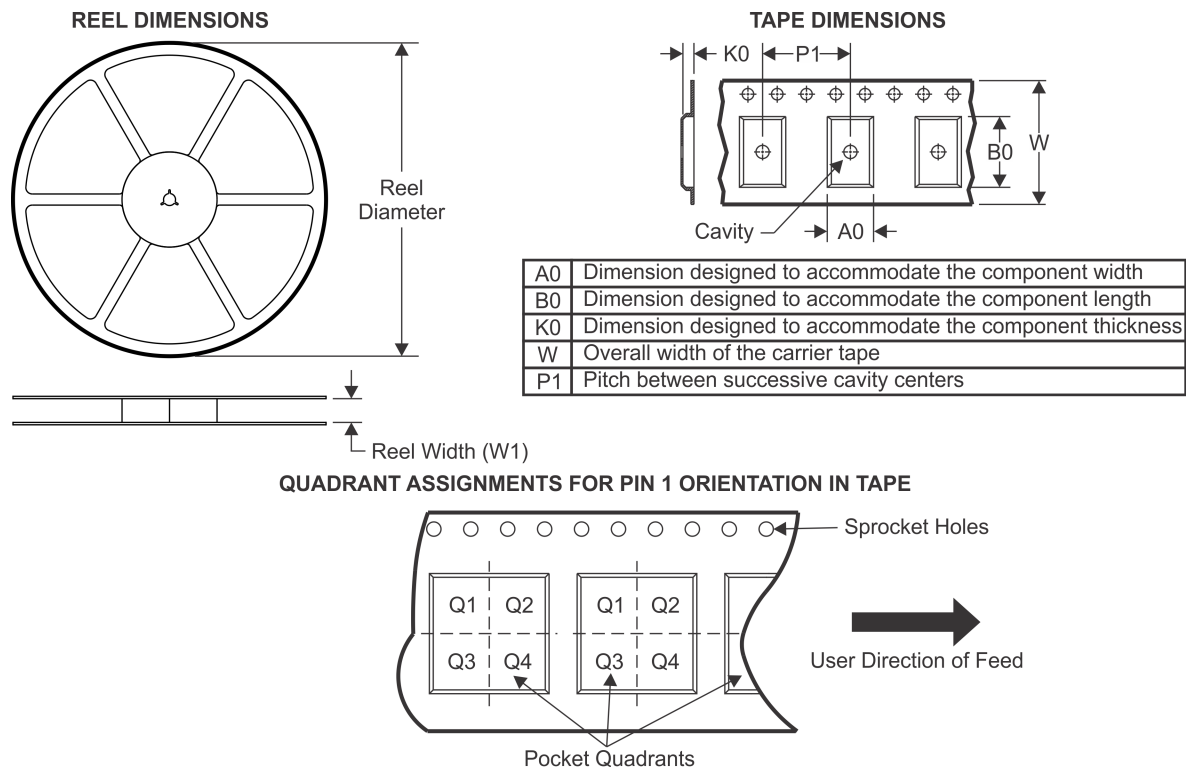


www.ti.com

PACKAGE OPTION ADDENDUM

17-May-2014

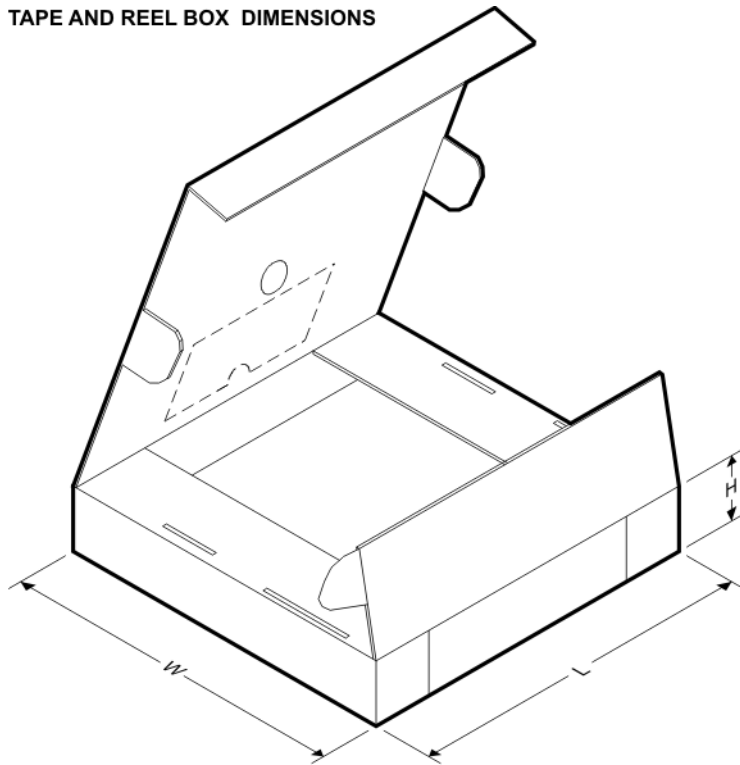
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUCH32374ZKER	LFBGA	ZKE	96	1000	330.0	24.4	5.7	13.7	2.0	8.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS

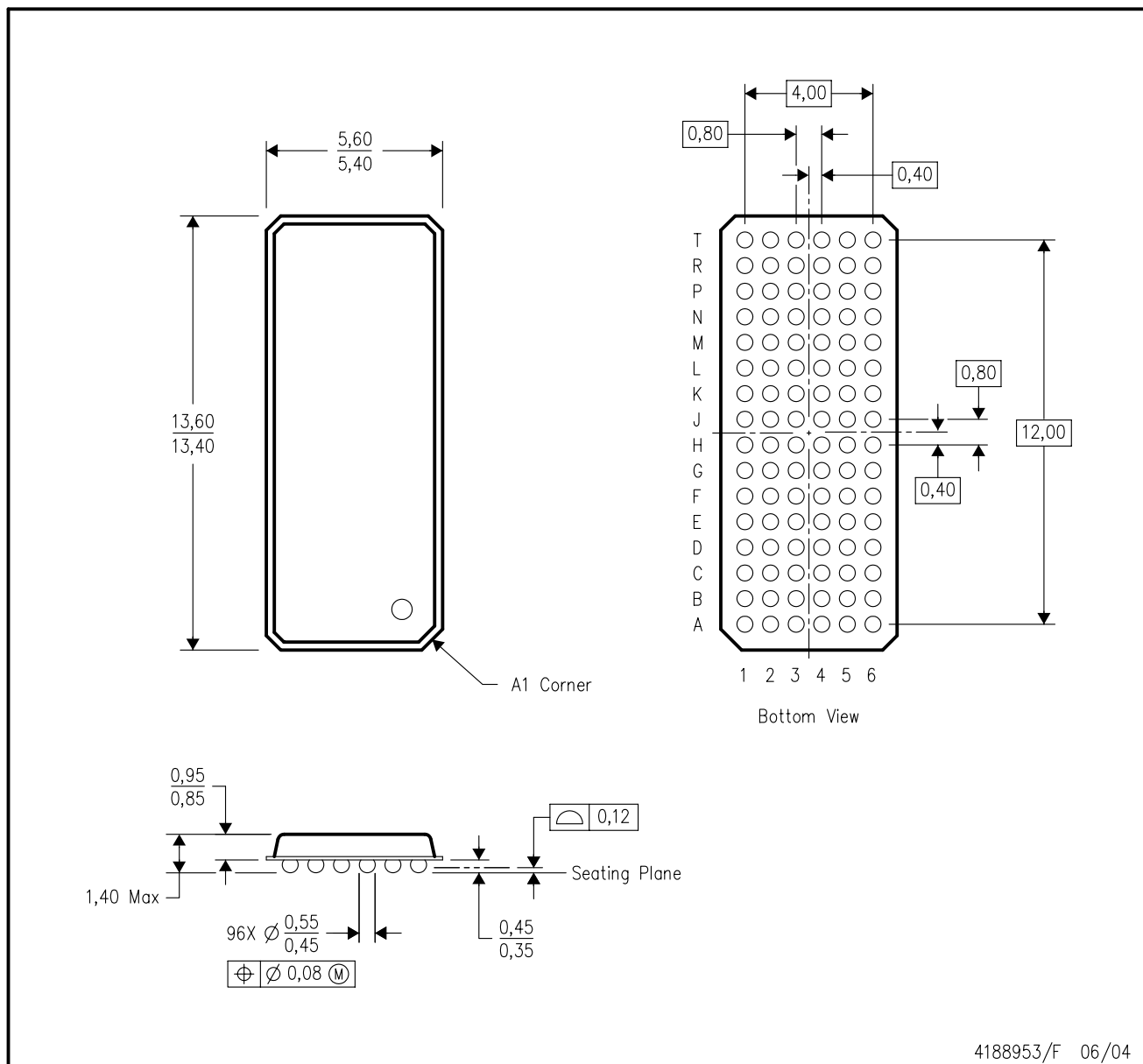


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUCH32374ZKER	LFBGA	ZKE	96	1000	336.6	336.6	41.3

GKE (R-PBGA-N96)

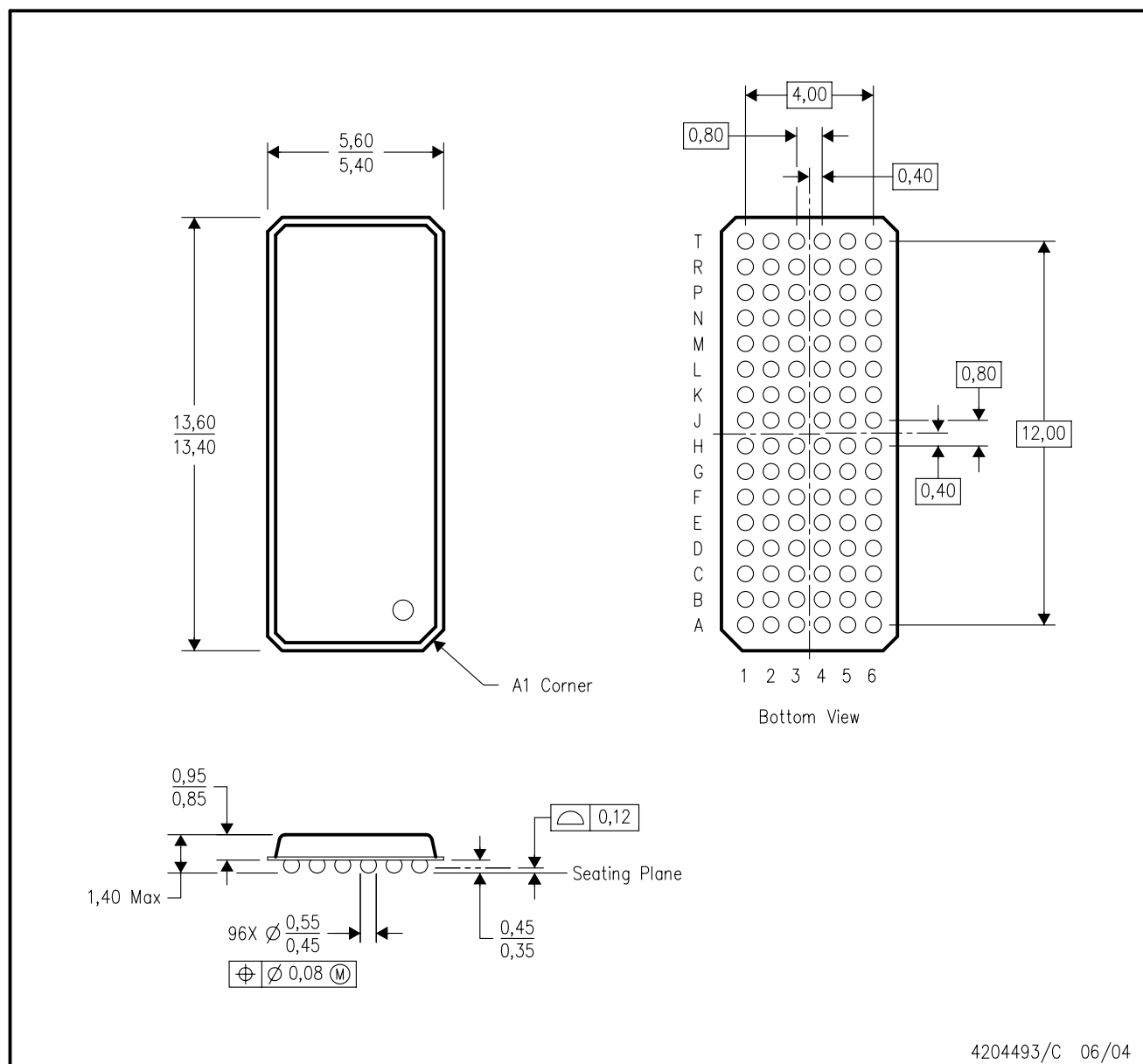
PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MO-205 variation CC.
 - D. This package is tin-lead (SnPb). Refer to the 96 ZKE package (drawing 4204493) for lead-free.

ZKE (R-PBGA-N96)

PLASTIC BALL GRID ARRAY



- NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO-205 variation CC.
D. This package is lead-free. Refer to the 96 GKE package (drawing 4188953) for tin-lead (SnPb).

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Applications Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications

Automotive and Transportation	www.ti.com/automotive
Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Video and Imaging	www.ti.com/video

TI E2E Community

e2e.ti.com