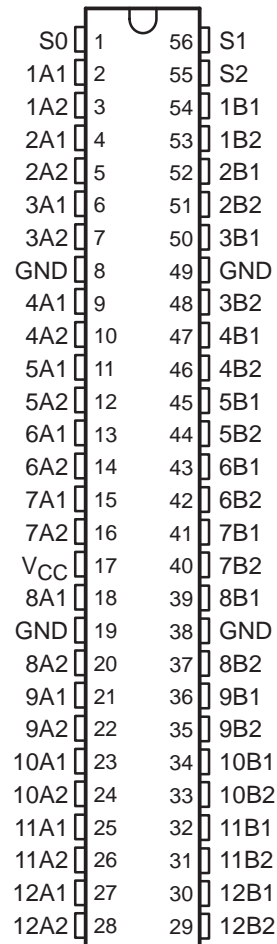


# SN54CBT16212A, SN74CBT16212A 24-BIT FET BUS-EXCHANGE SWITCHES

SCDS007U – NOVEMBER 1992 – REVISED JUNE 2005

- Members of the Texas Instruments Widebus™ Family
- 5-Ω Switch Connection Between Two Ports
- TTL-Compatible Input Levels
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22 – 200-V Machine Model (A115-A)

SN54CBT16212A . . . WD PACKAGE  
SN74CBT16212A . . . DGG, DGV, OR DL PACKAGE  
(TOP VIEW)



## description/ordering information

The 'CBT16212A devices provide 24 bits of high-speed TTL-compatible bus switching or exchanging. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

Each device operates as a 24-bit bus switch or a 12-bit bus exchanger that provides data exchanging between the four signal ports via the data-select (S0, S1, S2) terminals.

## ORDERING INFORMATION

| T <sub>A</sub>        | PACKAGE†          |               | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|-----------------------|-------------------|---------------|-----------------------|------------------|
| -40°C to 85°C         | SSOP – DL         | Tube          | SN74CBT16212ADL       | CBT16212A        |
|                       |                   | Tape and reel | SN74CBT16212ADLR      |                  |
|                       | TSSOP – DGG       | Tape and reel | SN74CBT16212ADGGR     | CBT16212A        |
|                       | TVSOP – DGV       | Tape and reel | SN74CBT16212ADGVR     | CY212A           |
|                       | VFBGA – GQL       | Tape and reel | SN74CBT16212AGQLR     | CY212A           |
| VFBGA – ZQL (Pb-free) | SN74CBT16212AZQLR |               |                       |                  |
| -55°C to 125°C        | CFP – WD          | Tube          | SNJ54CBT16212AWD      | SNJ54CBT16212AWD |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus is a trademark of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



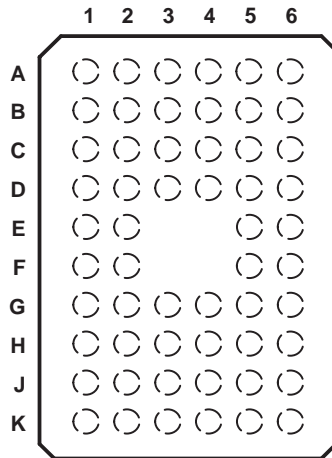
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2005, Texas Instruments Incorporated  
On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

# SN54CBT16212A, SN74CBT16212A 24-BIT FET BUS-EXCHANGE SWITCHES

SCDS007U – NOVEMBER 1992 – REVISED JUNE 2005

GQL OR ZQL PACKAGE  
(TOP VIEW)



terminal assignments

|   | 1    | 2    | 3    | 4    | 5    | 6    |
|---|------|------|------|------|------|------|
| A | 1A2  | 1A1  | S0   | S1   | S2   | 1B1  |
| B | 3A1  | 2A2  | 2A1  | 1B2  | 2B1  | 2B2  |
| C | 4A1  | GND  | 3A2  | 3B1  | GND  | 3B2  |
| D | 5A2  | 4A2  | 5A1  | 4B2  | 4B1  | 5B1  |
| E | 6A2  | 6A1  |      |      | 5B2  | 6B1  |
| F | 7A1  | 7A2  |      |      | 7B1  | 6B2  |
| G | VCC  | GND  | 8A1  | 8B1  | GND  | 7B2  |
| H | 8A2  | 9A1  | 9A2  | 9B2  | 9B1  | 8B2  |
| J | 10A1 | 10A2 | 11A1 | 11B1 | 10B2 | 10B1 |
| K | 11A2 | 12A1 | 12A2 | 12B2 | 12B1 | 11B2 |

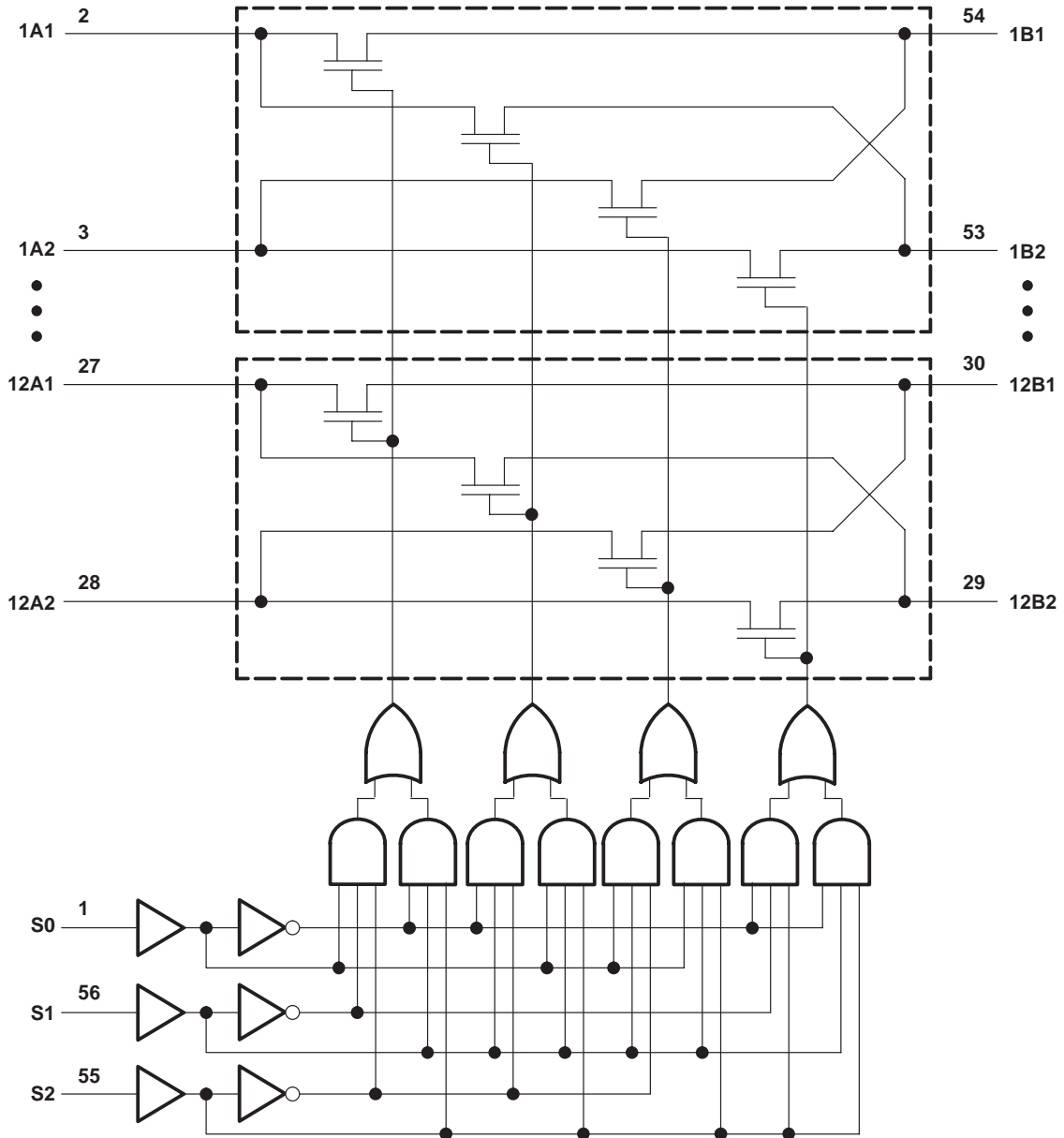
FUNCTION TABLE

| INPUTS |    |    | INPUTS/OUTPUTS |         | FUNCTION                               |
|--------|----|----|----------------|---------|----------------------------------------|
| S2     | S1 | S0 | A1             | A2      |                                        |
| L      | L  | L  | Z              | Z       | Disconnect                             |
| L      | L  | H  | B1 port        | Z       | A1 port = B1 port                      |
| L      | H  | L  | B2 port        | Z       | A1 port = B2 port                      |
| L      | H  | H  | Z              | B1 port | A2 port = B1 port                      |
| H      | L  | L  | Z              | B2 port | A2 port = B2 port                      |
| H      | L  | H  | Z              | Z       | Disconnect                             |
| H      | H  | L  | B1 port        | B2 port | A1 port = B1 port<br>A2 port = B2 port |
| H      | H  | H  | B2 port        | B1 port | A1 port = B2 port<br>A2 port = B1 port |

# SN54CBT16212A, SN74CBT16212A 24-BIT FET BUS-EXCHANGE SWITCHES

SCDS007U – NOVEMBER 1992 – REVISED JUNE 2005

## logic diagram (positive logic)



Pin numbers shown are for the DGG, DGV, DL, and WD packages.

# SN54CBT16212A, SN74CBT16212A 24-BIT FET BUS-EXCHANGE SWITCHES

SCDS007U – NOVEMBER 1992 – REVISED JUNE 2005

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

|                                                                    |                |
|--------------------------------------------------------------------|----------------|
| Supply voltage range, $V_{CC}$                                     | -0.5 V to 7 V  |
| Input voltage range, $V_I$ (see Note 1)                            | -0.5 V to 7 V  |
| Continuous channel current                                         | 128 mA         |
| Input clamp current, $I_{IK}$ ( $V_I < 0$ )                        | -50 mA         |
| Package thermal impedance, $\theta_{JA}$ (see Note 2): DGG package | 64°C/W         |
| DGV package                                                        | 48°C/W         |
| DL package                                                         | 56°C/W         |
| GQL/ZQL package                                                    | 42°C/W         |
| Storage temperature range, $T_{stg}$                               | -65°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.

## recommended operating conditions (see Note 3)

|                                           | SN54CBT16212A |     | SN74CBT16212A |     | UNIT |
|-------------------------------------------|---------------|-----|---------------|-----|------|
|                                           | MIN           | MAX | MIN           | MAX |      |
| $V_{CC}$ Supply voltage                   | 4             | 5.5 | 4             | 5.5 | V    |
| $V_{IH}$ High-level control input voltage | 2             |     | 2             |     | V    |
| $V_{IL}$ Low-level control input voltage  |               | 0.8 |               | 0.8 | V    |
| $T_A$ Operating free-air temperature      | -55           | 125 | -40           | 85  | °C   |

NOTE 3: All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER         | TEST CONDITIONS                                                                            | SN54CBT16212A  |               | SN74CBT16212A |     | UNIT |      |     |
|-------------------|--------------------------------------------------------------------------------------------|----------------|---------------|---------------|-----|------|------|-----|
|                   |                                                                                            | MIN            | TYP‡          | MAX           | MIN |      | TYP‡ | MAX |
| $V_{IK}$          | $V_{CC} = 4.5$ V, $I_I = -18$ mA                                                           |                |               | -1.2          |     | -1.2 | V    |     |
| $I_I$             | $V_{CC} = 0$ , $V_I = 5.5$ V                                                               |                |               | 10            |     | 10   | μA   |     |
|                   | $V_{CC} = 5.5$ V, $V_I = 5.5$ V or GND                                                     |                |               | ±1            |     | ±1   |      |     |
| $I_{CC}$          | $V_{CC} = 5.5$ V, $I_O = 0$ , $V_I = V_{CC}$ or GND                                        |                |               | 3.2           |     | 3    | μA   |     |
| $\Delta I_{CC}$ § | Control inputs<br>$V_{CC} = 5.5$ V, One input at 3.4 V,<br>Other inputs at $V_{CC}$ or GND |                |               | 2.5           |     | 2.5  | mA   |     |
| $C_i$             | Control inputs<br>$V_I = 3$ V or 0                                                         |                |               | 2.5           |     | 2.5  | pF   |     |
| $C_{io(off)}$     | $V_O = 3$ V or 0, $S_0, S_1,$ and $S_2 =$ GND                                              |                |               | 7.5           |     | 7.5  | pF   |     |
| $r_{on}$ ¶        | $V_{CC} = 4$ V,<br>TYP at $V_{CC} = 4$ V                                                   | $V_I = 2.4$ V, | $I_I = 15$ mA | 14            | 20  | 14   | 20   | Ω   |
|                   | $V_{CC} = 4.5$ V                                                                           | $V_I = 0$      | $I_I = 64$ mA | 4             | 10  | 4    | 7    |     |
|                   |                                                                                            |                | $I_I = 30$ mA | 4             | 10  | 4    | 7    |     |
|                   |                                                                                            | $V_I = 2.4$ V, | $I_I = 15$ mA | 6             | 14  | 6    | 12   |     |

‡ All typical values are at  $V_{CC} = 5$  V (unless otherwise noted),  $T_A = 25^\circ\text{C}$ .

§ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than  $V_{CC}$  or GND.

¶ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.



# SN54CBT16212A, SN74CBT16212A 24-BIT FET BUS-EXCHANGE SWITCHES

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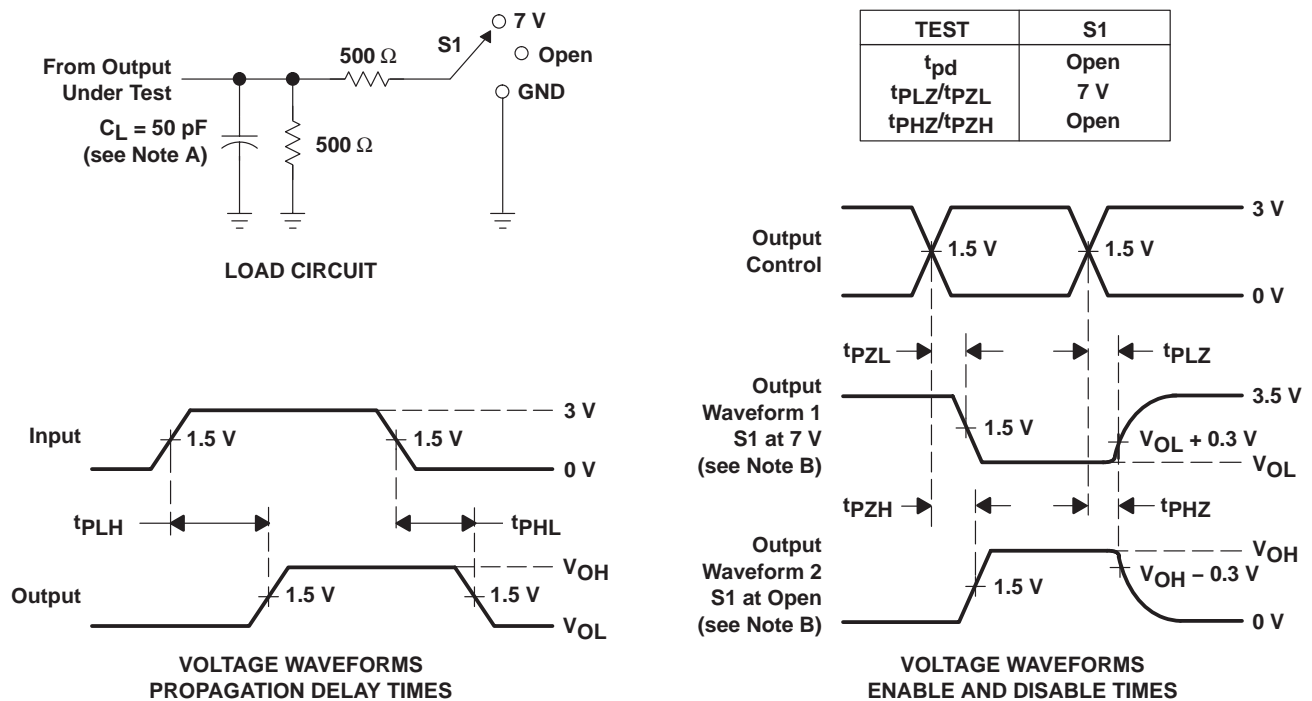
switching characteristics over recommended operating free-air temperature range,  $C_L = 50$  pF (unless otherwise noted) (see Figure 1)

| PARAMETER        | FROM (INPUT) | TO (OUTPUT) | SN54CBT16212A  |      |                            |      | SN74CBT16212A  |      |                            |      | UNIT |
|------------------|--------------|-------------|----------------|------|----------------------------|------|----------------|------|----------------------------|------|------|
|                  |              |             | $V_{CC} = 4$ V |      | $V_{CC} = 5$ V $\pm 0.5$ V |      | $V_{CC} = 4$ V |      | $V_{CC} = 5$ V $\pm 0.5$ V |      |      |
|                  |              |             | MIN            | MAX  | MIN                        | MAX  | MIN            | MAX  | MIN                        | MAX  |      |
| $t_{pd}^\dagger$ | A or B       | B or A      |                |      |                            | 0.8* |                | 0.35 |                            | 0.25 | ns   |
| $t_{pd}$         | S            | A or B      |                | 14   | 1.5                        | 13   |                | 10   | 1.5                        | 9.1  | ns   |
| $t_{en}$         | S            | A or B      |                | 15   | 1.5                        | 13.7 |                | 10.4 | 1.5                        | 9.7  | ns   |
| $t_{dis}$        | S            | A or B      |                | 14.2 | 1.5                        | 13.5 |                | 9.2  | 1.5                        | 8.8  | ns   |

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

## PARAMETER MEASUREMENT INFORMATION



- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50$   $\Omega$ ,  $t_r \leq 2.5$  ns,  $t_f \leq 2.5$  ns.
  - The outputs are measured one at a time, with one transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
  - All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

| Orderable Device   | Status<br>(1) | Package Type               | Package Drawing | Pins | Package Qty | Eco Plan<br>(2)            | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5)                     | Samples                 |
|--------------------|---------------|----------------------------|-----------------|------|-------------|----------------------------|-------------------------|----------------------|--------------|---------------------------------------------|-------------------------|
| 5962-9852101QXA    | ACTIVE        | CFP                        | WD              | 56   | 1           | TBD                        | A42                     | N / A for Pkg Type   | -55 to 125   | 5962-9852101QX<br>A<br>SNJ54CBT16212A<br>WD | <a href="#">Samples</a> |
| 74CBT16212ADGGRG4  | ACTIVE        | TSSOP                      | DGG             | 56   | 2000        | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | CBT16212A                                   | <a href="#">Samples</a> |
| SN74CBT16212ADGGR  | ACTIVE        | TSSOP                      | DGG             | 56   | 2000        | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | CBT16212A                                   | <a href="#">Samples</a> |
| SN74CBT16212ADGVR  | ACTIVE        | TVSOP                      | DGV             | 56   | 2000        | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | CY212A                                      | <a href="#">Samples</a> |
| SN74CBT16212ADL    | ACTIVE        | SSOP                       | DL              | 56   | 20          | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | CBT16212A                                   | <a href="#">Samples</a> |
| SN74CBT16212ADLG4  | ACTIVE        | SSOP                       | DL              | 56   | 20          | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | CBT16212A                                   | <a href="#">Samples</a> |
| SN74CBT16212ADLR   | ACTIVE        | SSOP                       | DL              | 56   | 1000        | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | CBT16212A                                   | <a href="#">Samples</a> |
| SN74CBT16212ADLRG4 | ACTIVE        | SSOP                       | DL              | 56   | 1000        | Green (RoHS<br>& no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | CBT16212A                                   | <a href="#">Samples</a> |
| SN74CBT16212AZQLR  | ACTIVE        | BGA<br>MICROSTAR<br>JUNIOR | ZQL             | 56   | 1000        | Green (RoHS<br>& no Sb/Br) | SNAGCU                  | Level-1-260C-UNLIM   | -40 to 85    | CY212A                                      | <a href="#">Samples</a> |
| SNJ54CBT16212AWD   | ACTIVE        | CFP                        | WD              | 56   | 1           | TBD                        | A42                     | N / A for Pkg Type   | -55 to 125   | 5962-9852101QX<br>A<br>SNJ54CBT16212A<br>WD | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

---

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN54CBT16212A, SN74CBT16212A :**

● Catalog: [SN74CBT16212A](#)

● Military: [SN54CBT16212A](#)

NOTE: Qualified Version Definitions:

● Catalog - TI's standard catalog product

● Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

| Device            | Package Type         | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------------|----------------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74CBT16212ADGGR | TSSOP                | DGG             | 56   | 2000 | 330.0              | 24.4               | 8.6     | 15.6    | 1.8     | 12.0    | 24.0   | Q1            |
| SN74CBT16212ADGVR | TVSOP                | DGV             | 56   | 2000 | 330.0              | 24.4               | 6.8     | 11.7    | 1.6     | 12.0    | 24.0   | Q1            |
| SN74CBT16212ADLR  | SSOP                 | DL              | 56   | 1000 | 330.0              | 32.4               | 11.35   | 18.67   | 3.1     | 16.0    | 32.0   | Q1            |
| SN74CBT16212AZQLR | BGA MICROSTAR JUNIOR | ZQL             | 56   | 1000 | 330.0              | 16.4               | 4.8     | 7.3     | 1.5     | 8.0     | 16.0   | Q1            |

**TAPE AND REEL BOX DIMENSIONS**

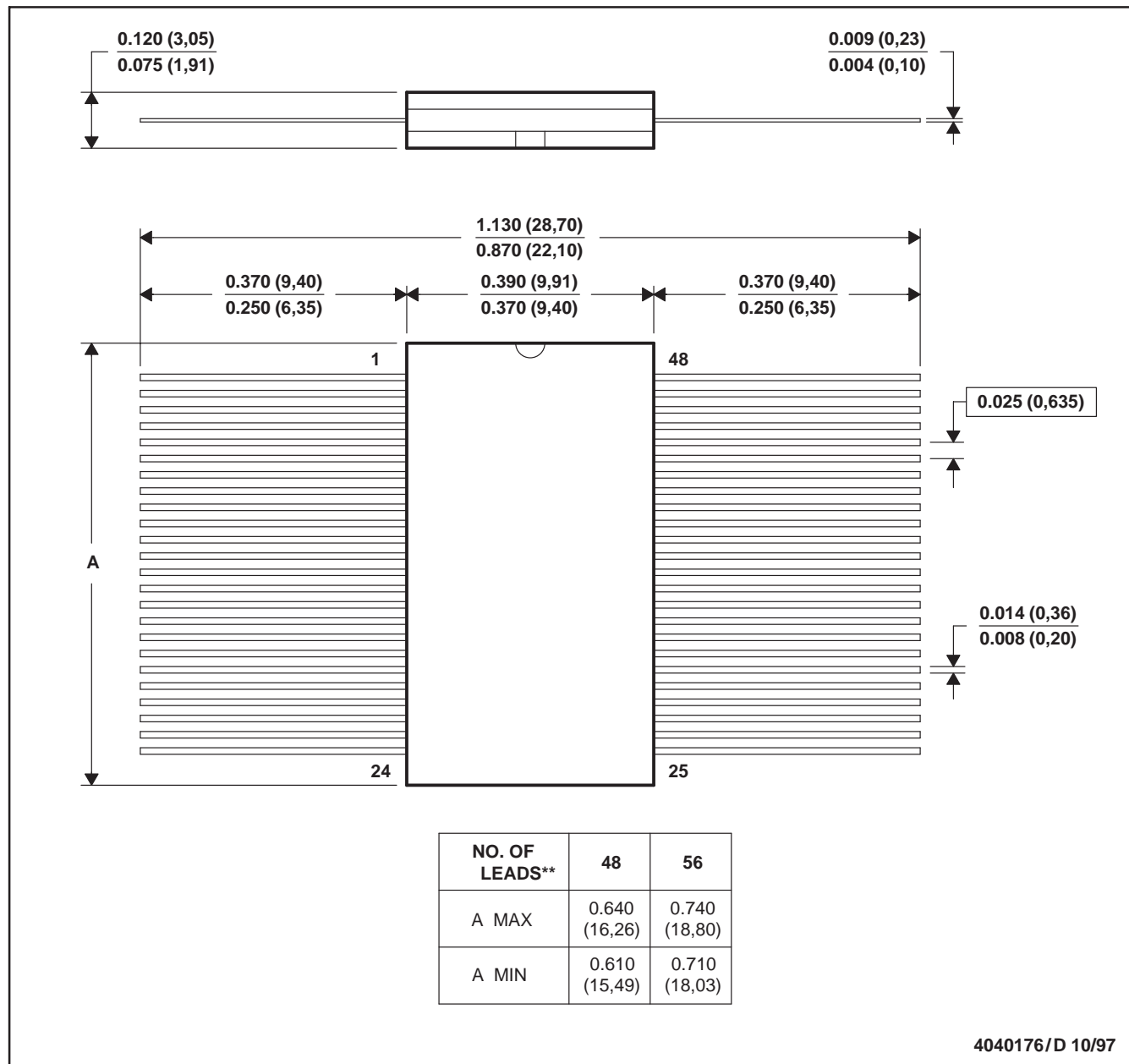

\*All dimensions are nominal

| Device            | Package Type         | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-------------------|----------------------|-----------------|------|------|-------------|------------|-------------|
| SN74CBT16212ADGGR | TSSOP                | DGG             | 56   | 2000 | 367.0       | 367.0      | 45.0        |
| SN74CBT16212ADGVR | TVSOP                | DGV             | 56   | 2000 | 367.0       | 367.0      | 45.0        |
| SN74CBT16212ADLR  | SSOP                 | DL              | 56   | 1000 | 367.0       | 367.0      | 55.0        |
| SN74CBT16212AZQLR | BGA MICROSTAR JUNIOR | ZQL             | 56   | 1000 | 336.6       | 336.6      | 28.6        |

WD (R-GDFP-F\*\*)

CERAMIC DUAL FLATPACK

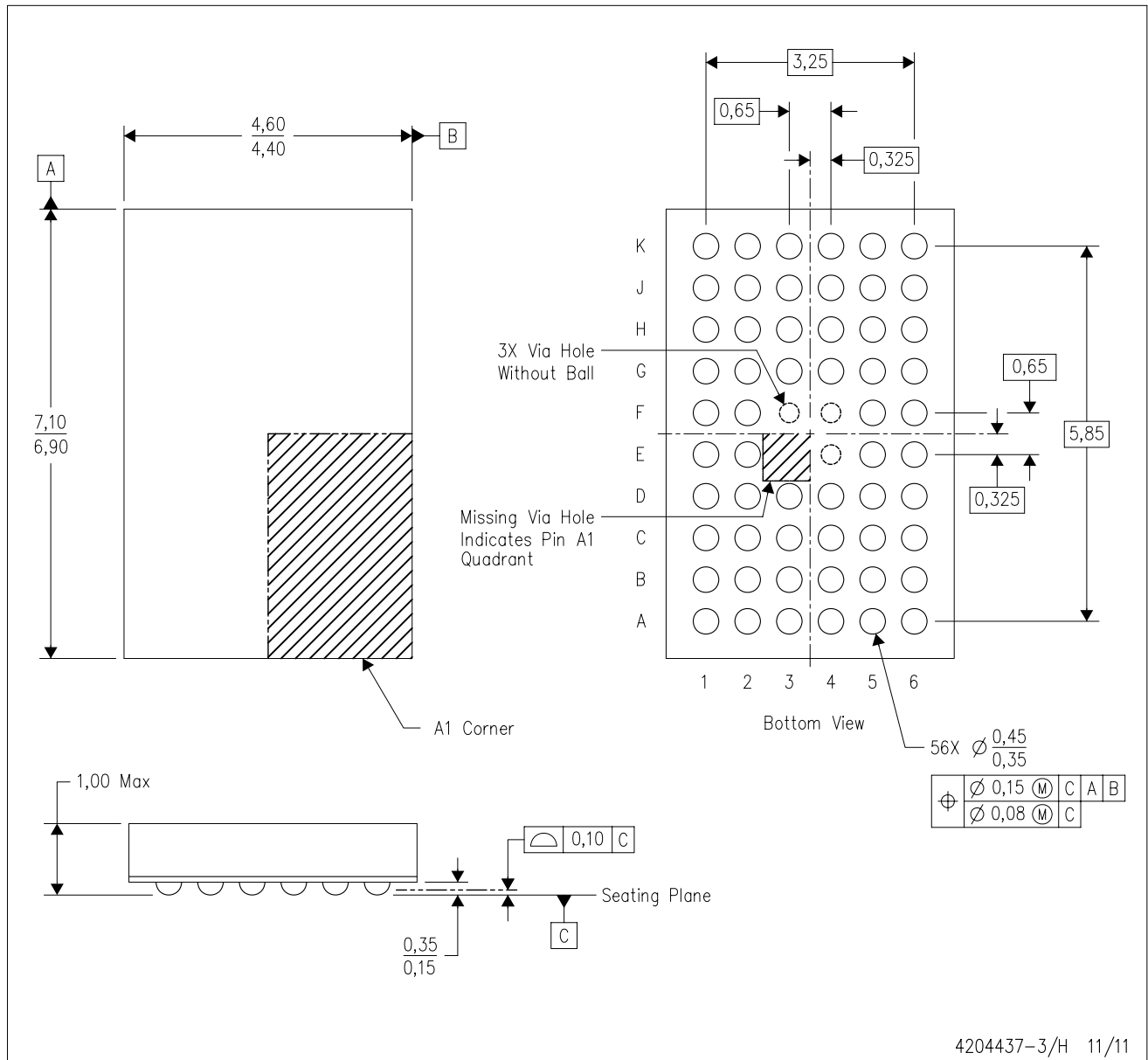
48 LEADS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. This package can be hermetically sealed with a ceramic lid using glass frit.  
 D. Index point is provided on cap for terminal identification only  
 E. Falls within MIL STD 1835: GDFP1-F48 and JEDEC MO-146AA  
 GDFP1-F56 and JEDEC MO-146AB

ZQL (R-PBGA-N56)

PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MO-285 variation BA-2.
  - D. This package is Pb-free. Refer to the 56 GQL package (drawing 4200583) for tin-lead (SnPb).

DGV (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



4073251/E 08/00

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

# MECHANICAL DATA

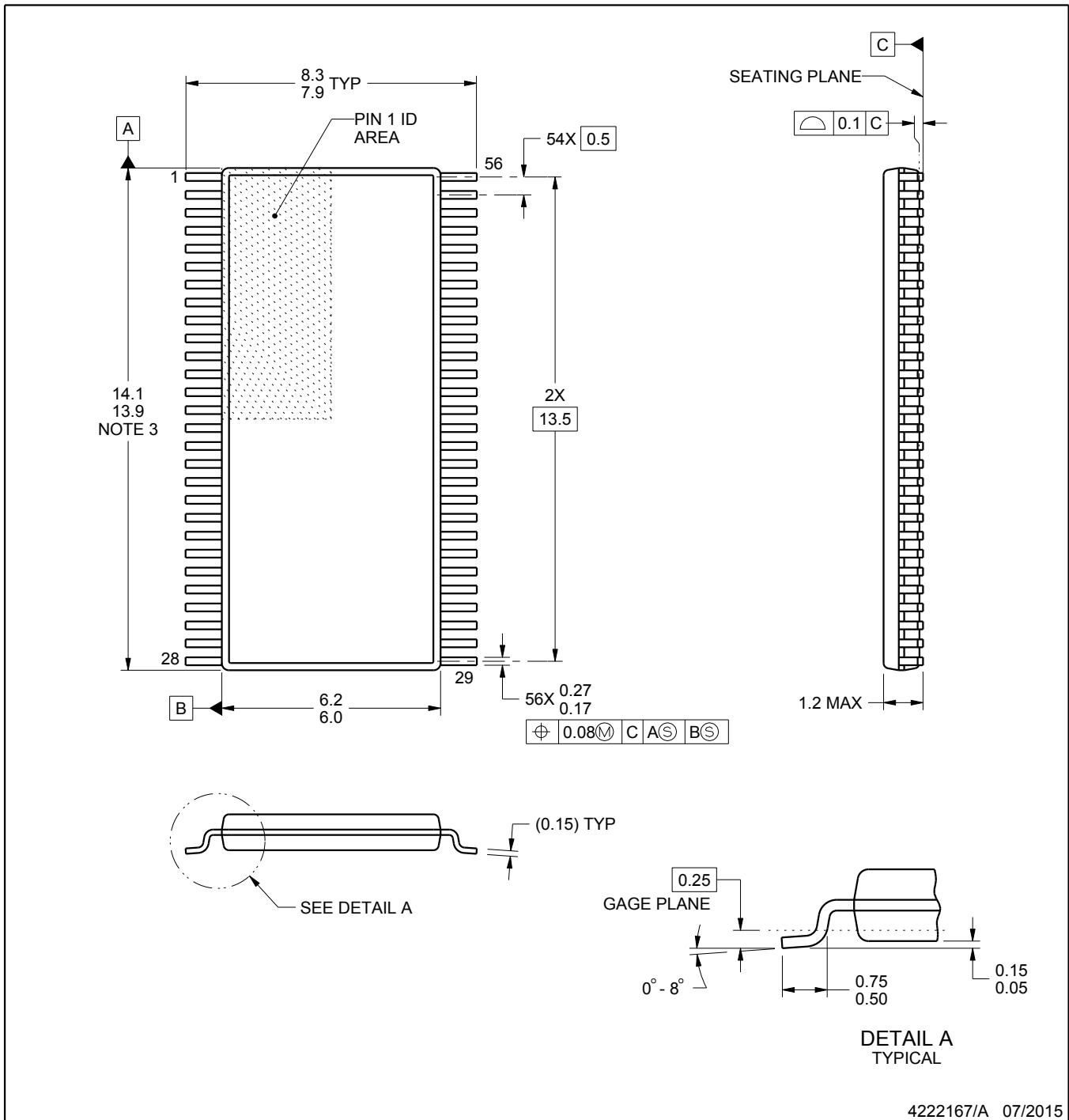
DL (R-PDSO-G56)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MO-118

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NOTES:

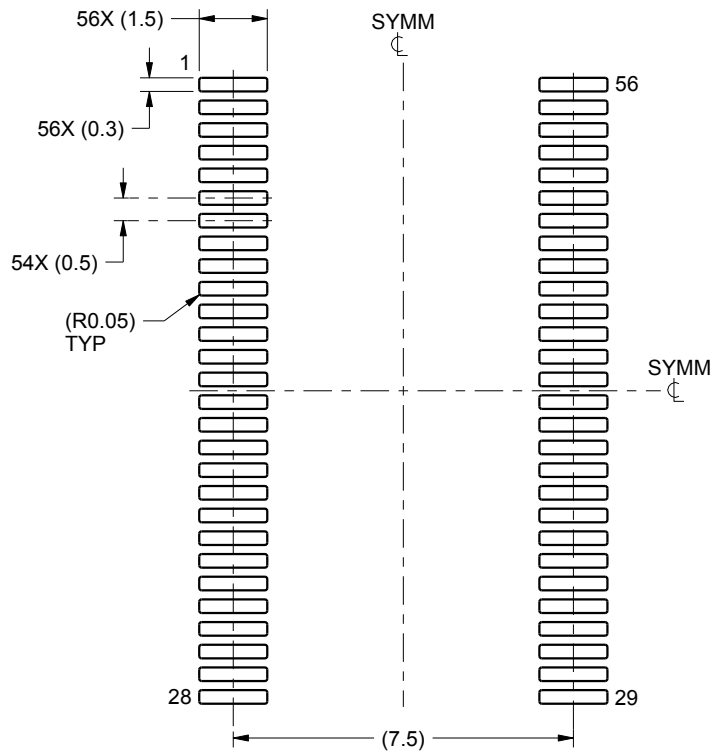
- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

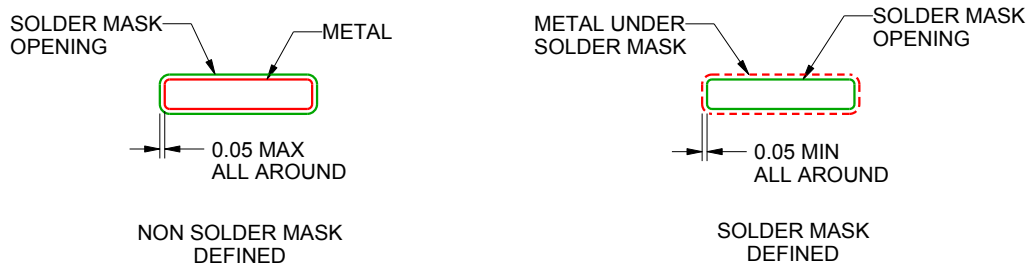
DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

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NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

## IMPORTANT NOTICE

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