

# SN54LS292, SN54LS294, SN74LS292, SN74LS294 PROGRAMMABLE FREQUENCY DIVIDERS/DIGITAL TIMERS

SDLS153 – D2628, JANUARY 1981 – REVISED MARCH 1988

- **Count Divider Chain**
- **Digitally Programmable from  $2^2$  to  $2^n$**   
( $n = 31$  for 'LS292,  $n = 15$  for 'LS294)
- **Useable Frequency Range from DC to 30 MHz**
- **Easily Expandable**
- **Applications**
  - **Frequency Division**
  - **Digital Timing**

## description

These programmable frequency dividers/digital timers contain 31 flip-flops plus 30 gates ('LS292) or 15 flip-flops plus 29 gates ('LS294) on a single chip. The count modulo is under digital control of the inputs provided.

Both types feature an active-low clear input to initialize the state of all flip-flops. To facilitate incoming inspection, test points are provided (TP1, TP2, and TP3 on the 'LS292 and TP on the 'LS294). These test points are not intended to drive system loads. Both types feature two clock inputs; either one may be used for clock gating. (See the function table below.)

A brief look at the digital timing capabilities of the 'LS292 will show that with a 1-MHz input frequency, programming for  $2^{10}$  will give a period of 1.024 ms, and  $2^{20}$  will give a period of 1.05 sec,  $2^{26}$  will give a period of 1.12 min, and  $2^{31}$  will give a period of 35.79 min.

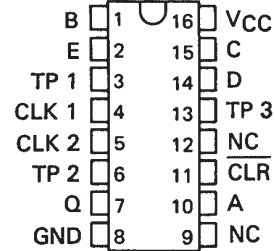
These devices are easily cascadable giving limitless possibilities to timing delays that can be achieved.

FUNCTION TABLE

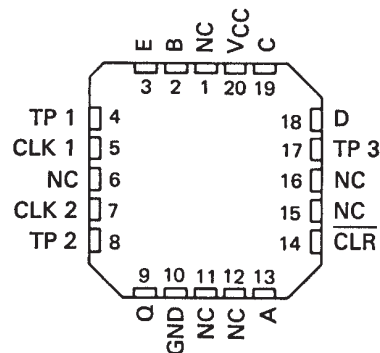
CLEAR	CLK 1	CLK 2	Q OUTPUT MODE
L	X	X	Cleared to L
H	↑	L	Count
H	L	↑	Count
H	H	X	Inhibit
H	X	H	Inhibit

SN54LS292 . . . J OR W PACKAGE  
SN74LS292 . . . N PACKAGE

(TOP VIEW)

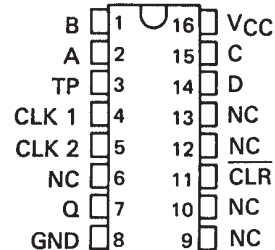


SN54LS292 . . . FK PACKAGE  
(TOP VIEW)

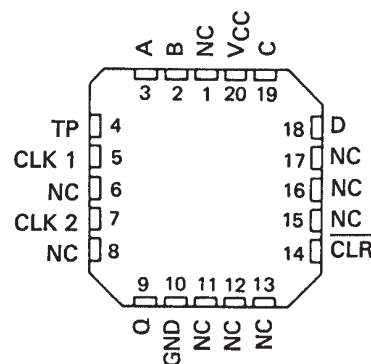


SN54LS294 . . . J OR W PACKAGE  
SN74LS294 . . . N PACKAGE

(TOP VIEW)



SN54LS294 . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



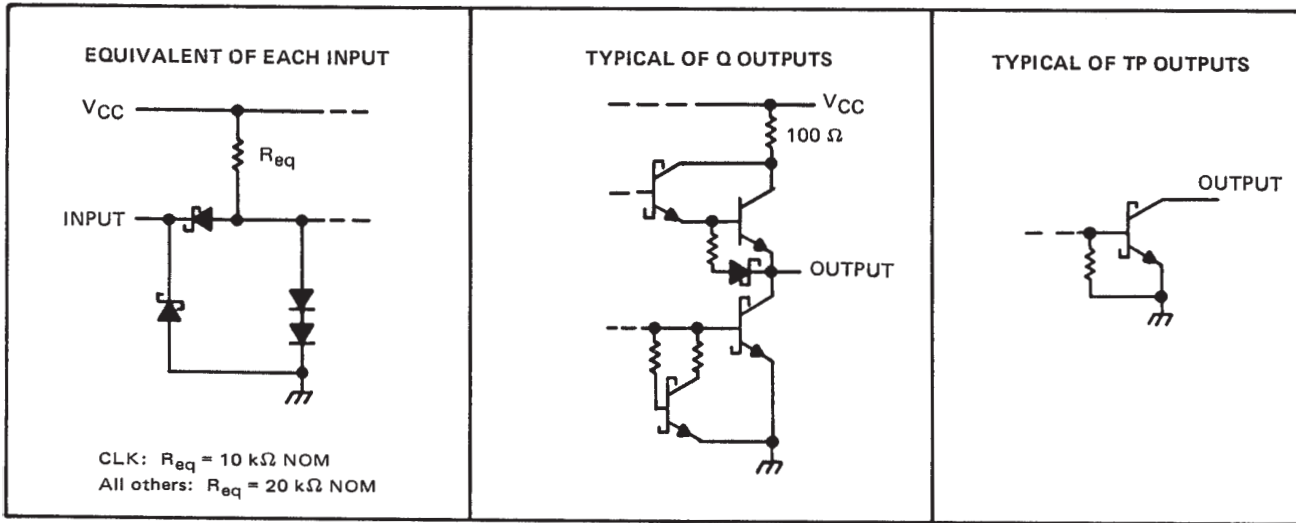
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# SN54LS292, SN54LS294, SN74LS292, SN74LS294 PROGRAMMABLE FREQUENCY DIVIDERS/DIGITAL TIMERS

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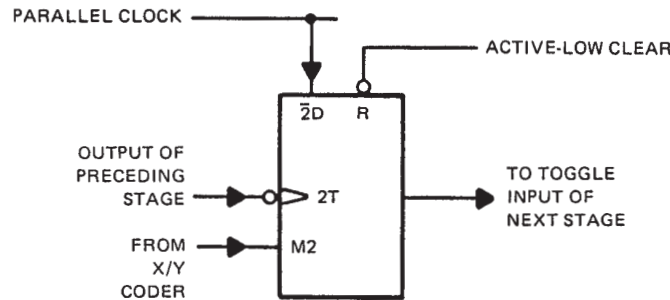
## schematics of inputs and outputs



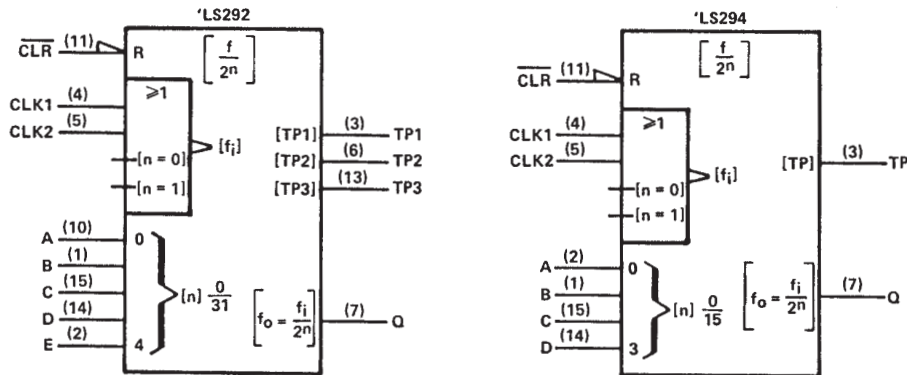
## operation

The functional block diagram shows that the count modulo is controlled by an X/Y decoder connected to the mode control inputs of several flip-flops. These flip-flops with mode controls each have a "D" input connected to the parallel clock line and a "T" input driven by the preceding stage. The parallel clock frequency is always the input frequency divided by four.

The X/Y decoder output selected by the programming inputs goes low. While a mode control is low, the "D" input of that flip-flop is enabled, and the signal from the parallel clock line ( $f_{in} \div 4$ ) is passed to the "T" input of the following stage. All the other mode controls are high enabling the "T" inputs and causing each flip-flop in turn to divide by two.



## logic symbols†



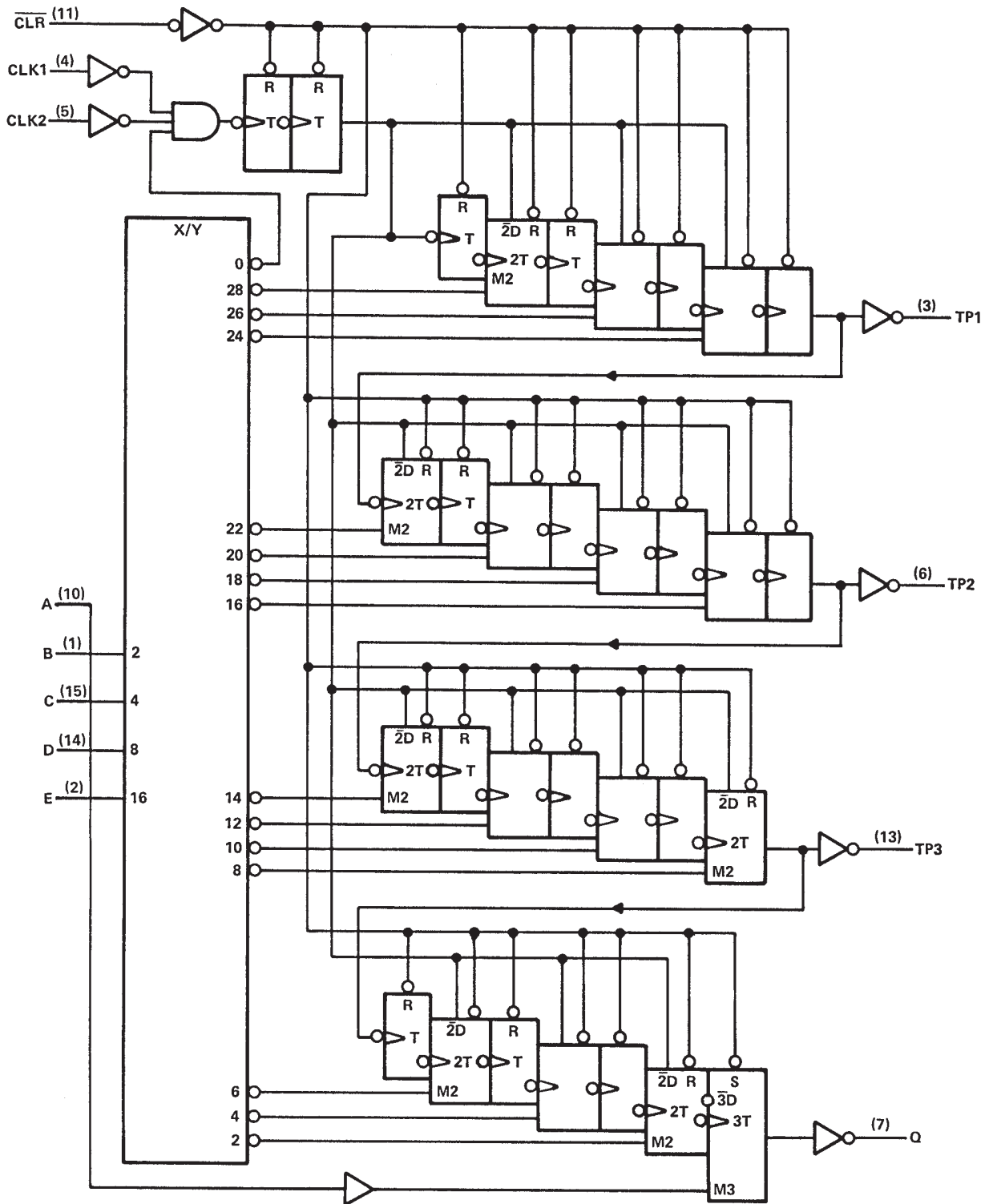
†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for J, N, and W packages.

# SN54LS292, SN54LS294, SN74LS292, SN74LS294 PROGRAMMABLE FREQUENCY DIVIDERS/DIGITAL TIMERS

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logic diagram (positive logic)

'LS292



Pin numbers shown are for J, N, and W packages.

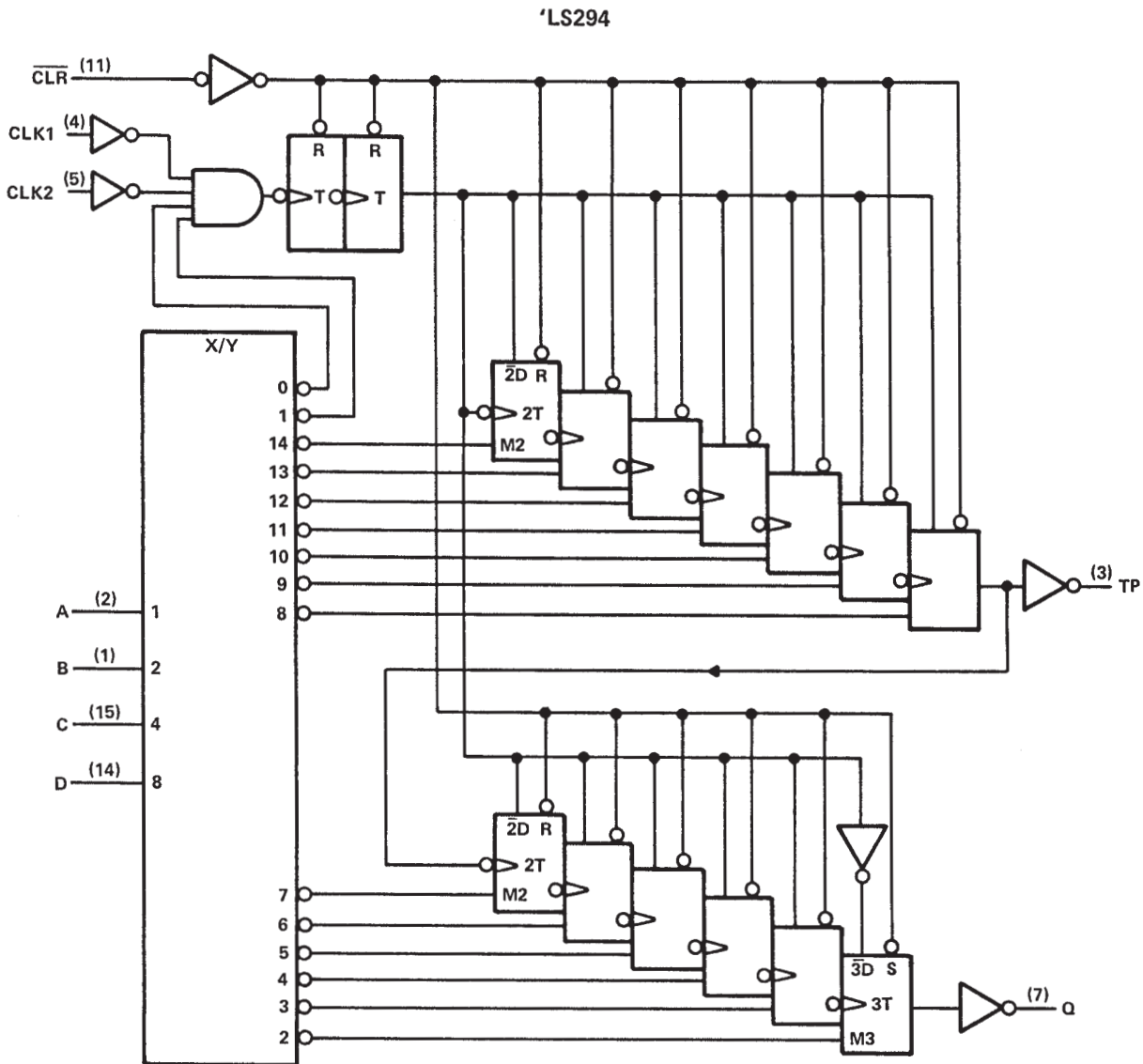


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# SN54LS292, SN54LS294, SN74LS292, SN74LS294 PROGRAMMABLE FREQUENCY DIVIDERS/DIGITAL TIMERS

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logic diagram (positive logic)



Pin numbers shown are for J, N, and W packages.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1)	7 V
Input voltage	7 V
Operating free-air temperature range: SN54LS292, SN54LS294	-55°C to 125°C
SN74LS292, SN74LS294	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.



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# SN54LS292, SN54LS294, SN74LS292, SN74LS294 PROGRAMMABLE FREQUENCY DIVIDERS/DIGITAL TIMERS

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## recommended operating conditions

		SN54LS'			SN74LS'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V <sub>IH</sub>	High-level input voltage	2			2			V
V <sub>IL</sub>	Low-level input voltage				0.8			V
I <sub>OH</sub>	High-level output current (Q only)				-1.2			mA
I <sub>OL</sub>	Low-level output current (Q only)				24			mA
f <sub>clock</sub>	Clock frequency	0	30		0	30		MHz
t <sub>w</sub>	Duration of clock input pulse	16			16			ns
t <sub>w</sub>	Duration of clear pulse	'LS292		55		55		ns
		'LS294		35		35		
t <sub>su</sub>	Clear inactive-state setup time	15			15			ns
T <sub>A</sub>	Operating free-air temperature	-55		125		0 70		°C

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS'			SN74LS'			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V <sub>IK</sub>		V <sub>CC</sub> = MIN, I <sub>I</sub> = -18 mA		-1.5			-1.5			V
V <sub>OH</sub>	Q	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = MAX, I <sub>OH</sub> = -1.2 mA		2.4	3.4		2.4	3.4		V
V <sub>OL</sub>	Q	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = MAX	I <sub>OL</sub> = 12 mA	0.25	0.4		0.25	0.4		V
			I <sub>OL</sub> = 24 mA				0.35	0.5		
			I <sub>OL</sub> = 0.5 mA				0.25	0.4		
I <sub>I</sub>		V <sub>CC</sub> = MAX, V <sub>I</sub> = 7 V		0.1			0.1			mA
I <sub>IH</sub>		V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7 V		20			20			μA
I <sub>IL</sub>	CLK1, CLK2	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4 V		-0.8			-0.8			mA
	All others			-0.4			-0.4			
I <sub>OS</sub> §	Q	V <sub>CC</sub> = MAX		-30		-130	-30		-130	mA
I <sub>CC</sub>	'LS292	V <sub>CC</sub> = MAX, All inputs grounded, All outputs open		40	75		40	75		mA
	'LS294			30	50		30	50		

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

§ The duration of the short-circuit should not exceed one second.

¶ The TP output or outputs are not intended to drive external loads but are solely provided for test points.

# SN54LS292, SN54LS294, SN74LS292, SN74LS294 PROGRAMMABLE FREQUENCY DIVIDERS/DIGITAL TIMERS

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switching characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ ,  $R_L = 667\ \Omega$ ,  $C_L = 45\text{ pF}$  (see Figure 1)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS292			'LS294			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
$f_{\text{max}}$	CLK1 or 2			30	50		30	50	MHz	
$t_{\text{PLH}}$		Q	Modulo set at 22, A thru E = LLLHL ('LS292) A thru D = LLHL ('LS294)	55	90		55	90	ns	
$t_{\text{PHL}}$		Q		80	120		80	120	ns	
$t_{\text{PHL}}$	CLR	Q		85	130		35	65	ns	

† $f_{\text{MAX}}$  = maximum clock frequency

$t_{\text{PLH}}$  = Propagation delay time, low-to-high-level output

$t_{\text{PHL}}$  = Propagation delay time, high-to-low-level output

NOTE 2: Load circuits and voltage waveforms are shown in Section 1. To be used on TP outputs only.

'LS292 FUNCTION TABLE

PROGRAMMING INPUTS					FREQUENCY DIVISION							
					Q		TP1		TP2		TP3	
E	D	C	B	A	BINARY	DECIMAL	BINARY	DECIMAL	BINARY	DECIMAL	BINARY	DECIMAL
L	L	L	L	L	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit
L	L	L	L	H	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit	Inhibit
L	L	L	H	L	2 <sup>2</sup>	4	2 <sup>9</sup>	512	2 <sup>17</sup>	131,072	2 <sup>24</sup>	16,777,216
L	L	L	H	H	2 <sup>3</sup>	8	2 <sup>9</sup>	512	2 <sup>17</sup>	131,072	2 <sup>24</sup>	16,777,216
L	L	H	L	L	2 <sup>4</sup>	16	2 <sup>9</sup>	512	2 <sup>17</sup>	131,072	2 <sup>24</sup>	16,777,216
L	L	H	L	H	2 <sup>5</sup>	32	2 <sup>9</sup>	512	2 <sup>17</sup>	131,072	2 <sup>24</sup>	16,777,216
L	L	H	H	L	2 <sup>6</sup>	64	2 <sup>9</sup>	512	2 <sup>17</sup>	131,072	2 <sup>24</sup>	16,777,216
L	L	H	H	H	2 <sup>7</sup>	128	2 <sup>9</sup>	512	2 <sup>17</sup>	131,072	2 <sup>24</sup>	16,777,216
L	H	L	L	L	2 <sup>8</sup>	256	2 <sup>9</sup>	512	2 <sup>17</sup>	131,072	2 <sup>2</sup>	4
L	H	L	L	H	2 <sup>9</sup>	512	2 <sup>9</sup>	512	2 <sup>17</sup>	131,072	2 <sup>2</sup>	4
L	H	L	H	L	2 <sup>10</sup>	1,024	2 <sup>9</sup>	512	2 <sup>17</sup>	131,072	2 <sup>4</sup>	16
L	H	L	H	H	2 <sup>11</sup>	2,048	2 <sup>9</sup>	512	2 <sup>17</sup>	131,072	2 <sup>4</sup>	16
L	H	H	L	L	2 <sup>12</sup>	4,096	2 <sup>9</sup>	512	2 <sup>17</sup>	131,072	2 <sup>6</sup>	64
L	H	H	L	H	2 <sup>13</sup>	8,192	2 <sup>9</sup>	512	2 <sup>17</sup>	131,072	2 <sup>6</sup>	64
L	H	H	H	L	2 <sup>14</sup>	16,384	2 <sup>9</sup>	512	Disabled Low		2 <sup>8</sup>	256
L	H	H	H	H	2 <sup>15</sup>	32,768	2 <sup>9</sup>	512	Disabled Low		2 <sup>8</sup>	256
H	L	L	L	L	2 <sup>16</sup>	65,536	2 <sup>9</sup>	512	2 <sup>3</sup>	8	2 <sup>10</sup>	1,024
H	L	L	L	H	2 <sup>17</sup>	131,072	2 <sup>9</sup>	512	2 <sup>3</sup>	8	2 <sup>10</sup>	1,024
H	L	L	H	L	2 <sup>18</sup>	262,144	2 <sup>9</sup>	512	2 <sup>5</sup>	32	2 <sup>12</sup>	4,096
H	L	L	H	H	2 <sup>19</sup>	524,288	2 <sup>9</sup>	512	2 <sup>5</sup>	32	2 <sup>12</sup>	4,096
H	L	H	L	L	2 <sup>20</sup>	1,048,576	2 <sup>9</sup>	512	2 <sup>7</sup>	128	2 <sup>14</sup>	16,384
H	L	H	L	H	2 <sup>21</sup>	2,097,152	2 <sup>9</sup>	512	2 <sup>7</sup>	128	2 <sup>14</sup>	16,384
H	L	H	H	L	2 <sup>22</sup>	4,194,304	Disabled Low		2 <sup>9</sup>	512	2 <sup>16</sup>	65,536
H	L	H	H	H	2 <sup>23</sup>	8,388,608	Disabled Low		2 <sup>9</sup>	512	2 <sup>16</sup>	65,536
H	H	L	L	L	2 <sup>24</sup>	16,777,216	2 <sup>3</sup>	8	2 <sup>11</sup>	2,048	2 <sup>18</sup>	262,144
H	H	L	L	H	2 <sup>25</sup>	33,554,432	2 <sup>3</sup>	8	2 <sup>11</sup>	2,048	2 <sup>18</sup>	262,144
H	H	L	H	L	2 <sup>26</sup>	67,108,864	2 <sup>5</sup>	32	2 <sup>13</sup>	8,192	2 <sup>20</sup>	1,048,576
H	H	L	H	H	2 <sup>27</sup>	134,217,728	2 <sup>5</sup>	32	2 <sup>13</sup>	8,192	2 <sup>20</sup>	1,048,576
H	H	H	L	L	2 <sup>28</sup>	268,435,456	2 <sup>7</sup>	128	2 <sup>15</sup>	32,768	2 <sup>22</sup>	4,194,304
H	H	H	L	H	2 <sup>29</sup>	536,870,912	2 <sup>7</sup>	128	2 <sup>15</sup>	32,768	2 <sup>22</sup>	4,194,304
H	H	H	H	L	2 <sup>30</sup>	1,073,741,824	2 <sup>9</sup>	512	2 <sup>17</sup>	131,072	2 <sup>24</sup>	16,777,216
H	H	H	H	H	2 <sup>31</sup>	2,147,483,648	2 <sup>9</sup>	512	2 <sup>17</sup>	131,072	2 <sup>24</sup>	16,777,216



# SN54LS292, SN54LS294, SN74LS292, SN74LS294 PROGRAMMABLE FREQUENCY DIVIDERS/DIGITAL TIMERS

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'LS294 FUNCTION TABLE

PROGRAMMING INPUTS				FREQUENCY DIVISION			
				Q		TP	
D	C	B	A	BINARY	DECIMAL	BINARY	DECIMAL
L	L	L	L	Inhibit	Inhibit	Inhibit	Inhibit
L	L	L	H	Inhibit	Inhibit	Inhibit	Inhibit
L	L	H	L	2 <sup>2</sup>	4	2 <sup>9</sup>	512
L	L	H	H	2 <sup>3</sup>	8	2 <sup>9</sup>	512
L	H	L	L	2 <sup>4</sup>	16	2 <sup>9</sup>	512
L	H	L	H	2 <sup>5</sup>	32	2 <sup>9</sup>	512
L	H	H	L	2 <sup>6</sup>	64	2 <sup>9</sup>	512
L	H	H	H	2 <sup>7</sup>	128	Disabled Low	
H	L	L	L	2 <sup>8</sup>	256	2 <sup>2</sup>	4
H	L	L	H	2 <sup>9</sup>	512	2 <sup>3</sup>	8
H	L	H	L	2 <sup>10</sup>	1,024	2 <sup>4</sup>	16
H	L	H	H	2 <sup>11</sup>	2,048	2 <sup>5</sup>	32
H	H	L	L	2 <sup>12</sup>	4,096	2 <sup>6</sup>	64
H	H	L	H	2 <sup>13</sup>	8,192	2 <sup>7</sup>	128
H	H	H	L	2 <sup>14</sup>	16,384	2 <sup>8</sup>	256
H	H	H	H	2 <sup>15</sup>	32,768	2 <sup>9</sup>	512

switching loads

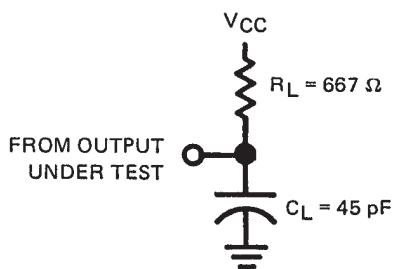
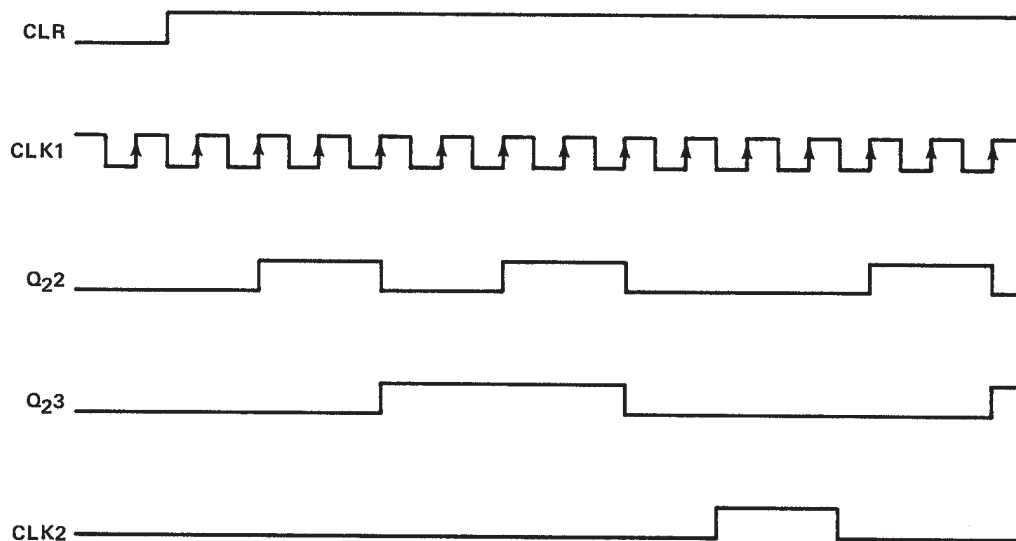





FIGURE 1

'LS292 and 'LS294 timing diagram



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LS292N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS292N	
SN74LS292N3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI	0 to 70		
SN74LS292N3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI	0 to 70		
SN74LS294N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS294N	
SN74LS294N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74LS294N	

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - D The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

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