

SNx4LV245A Octal Bus Transceivers With 3-State Outputs

1 Features

- 2-V to 5.5-V V_{CC} Operation
- Max t_{pd} of 6.5 ns at 5 V
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) >2.3 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Support Mixed-Mode Voltage Operation on All Ports
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

2 Applications

- Servers
- LED Displays
- Network Switches
- Telecom Infrastructure
- Motor Drivers
- I/O Expanders

3 Description

These octal bus transceivers are designed for 2-V to 5.5-V V_{CC} operation.

Device Information

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|-------------|------------|--------------------|
| SNx4LV245A | SSOP (20) | 7.20 mm × 5.30 mm |
| | TVSOP (20) | 5.00 mm × 4.40 mm |
| | TSSOP (20) | 6.50 mm × 4.40 mm |
| | VQFN (20) | 4.50 mm × 3.50 mm |
| | SOIC (20) | 12.80 mm × 7.50 mm |

4 Simplified Schematic

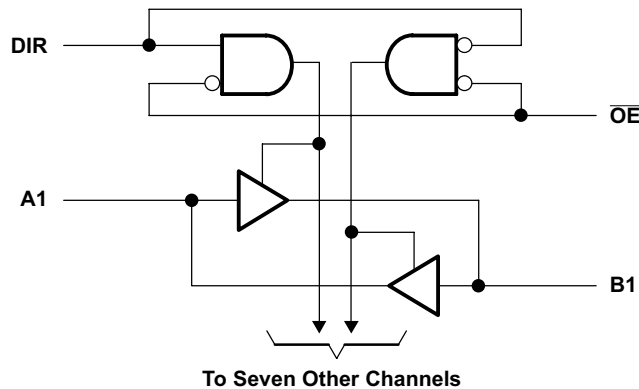


Table of Contents

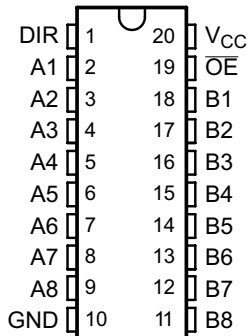
| | | | |
|-------------------------------------------------------------------------------|-----------|------------------------------------------------------------------|-----------|
| 1 Features | 1 | 9 Detailed Description | 11 |
| 2 Applications | 1 | 9.1 Overview | 11 |
| 3 Description | 1 | 9.2 Functional Block Diagram | 11 |
| 4 Simplified Schematic | 1 | 9.3 Feature Description | 11 |
| 5 Revision History | 2 | 9.4 Device Functional Modes | 11 |
| 6 Pin Configuration and Functions | 3 | 10 Application and Implementation | 12 |
| 7 Specifications | 5 | 10.1 Application Information | 12 |
| 7.1 Absolute Maximum Ratings | 5 | 10.2 Typical Application | 12 |
| 7.2 Handling Ratings | 5 | 11 Power Supply Recommendations | 13 |
| 7.3 Recommended Operating Conditions | 6 | 12 Layout | 13 |
| 7.4 Thermal Information | 6 | 12.1 Layout Guidelines | 13 |
| 7.5 Electrical Characteristics | 7 | 12.2 Layout Example | 13 |
| 7.6 Switching Characteristics, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ | 7 | 13 Device and Documentation Support | 14 |
| 7.7 Switching Characteristics, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ | 8 | 13.1 Related Links | 14 |
| 7.8 Switching Characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ | 8 | 13.2 Trademarks | 14 |
| 7.9 Noise Characteristics | 8 | 13.3 Electrostatic Discharge Caution | 14 |
| 7.10 Operating Characteristics | 8 | 13.4 Glossary | 14 |
| 7.11 Typical Characteristics | 9 | 14 Mechanical, Packaging, and Orderable Information | 14 |
| 8 Parameter Measurement Information | 10 | | |

5 Revision History

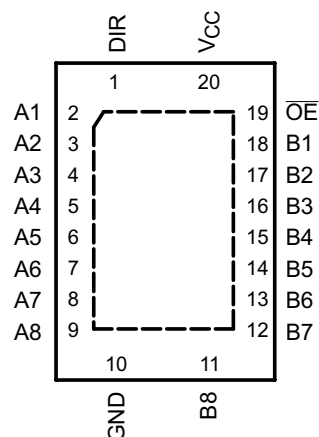
| Changes from Revision N (August 2012) to Revision O | Page |
|----------------------------------------------------------------------------------------------|------|
| • Updated document to new TI data sheet format | 1 |
| • Deleted Ordering Information table. | 1 |
| • Added Applications | 1 |
| • Added Device Information table. | 1 |
| • Added Pin Functions table | 3 |
| • Added Handling Ratings table | 5 |
| • Changed MAX operating temperature to 125°C in Recommended Operating Conditions table. | 6 |
| • Added –40°C to 125°C for SN74LV245A in Electrical Characteristics table | 7 |
| • Added –40°C to 125°C for SN74LV245A in all three Switching Characteristics tables. | 7 |
| • Added Typical Characteristics | 9 |
| • Added Detailed Description section | 11 |
| • Added Application and Implementation section | 12 |
| • Added Power Supply Recommendations and Layout sections | 13 |

6 Pin Configuration and Functions

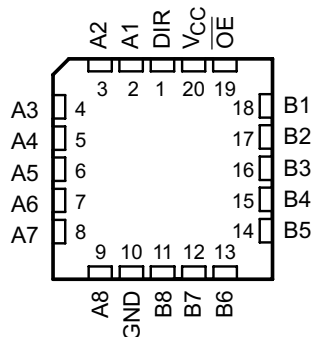
SN54LV245A . . . J OR W PACKAGE
SN74LV245A . . . DB, DGV, DW, NS,
OR PW PACKAGE
(TOP VIEW)



SN74LV245A . . . RGY PACKAGE
(TOP VIEW)

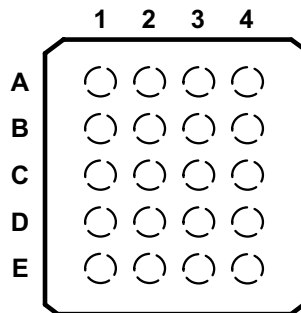


SN54LV245A . . . FK PACKAGE
(TOP VIEW)



Pin Functions

| PIN | | I/O | DESCRIPTION |
|-----|-----------------|-----|---------------|
| NO. | NAME | | |
| 1 | DIR | I | Direction Pin |
| 2 | A1 | I/O | A1 I/O |
| 3 | A2 | I/O | A2 I/O |
| 4 | A3 | I/O | A3 I/O |
| 5 | A4 | I/O | A4 I/O |
| 6 | A5 | I/O | A5 I/O |
| 7 | A6 | I/O | A6 I/O |
| 8 | A7 | I/O | A7 I/O |
| 9 | A8 | I/O | A8 I/O |
| 10 | GND | — | Ground Pin |
| 11 | B8 | I/O | B8 I/O |
| 12 | B7 | I/O | B7 I/O |
| 13 | B6 | I/O | B6 I/O |
| 14 | B5 | I/O | B5 I/O |
| 15 | B4 | I/O | B4 I/O |
| 16 | B3 | I/O | B3 I/O |
| 17 | B2 | I/O | B2 I/O |
| 18 | B1 | I/O | B1 I/O |
| 19 | \overline{OE} | I | Output Enable |
| 20 | V _{CC} | — | Power Pin |

**GQN PACKAGE
(TOP VIEW)**

Pin Assignments

| | 1 | 2 | 3 | 4 |
|---|-----|-----|-----------------|-----------------|
| A | A1 | DIR | V _{CC} | \overline{OE} |
| B | A3 | B2 | A2 | B1 |
| C | A5 | A4 | B4 | B3 |
| D | A7 | B6 | A6 | B5 |
| E | GND | A8 | B8 | B7 |

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | MIN | MAX | UNIT | |
|----------|---------------------------------------------------------------------------------------------|---------------------------------|----------------|------|---|
| V_{CC} | Supply voltage range | -0.5 | 7 | V | |
| V_I | Input voltage range | Except I/O ports ⁽²⁾ | -0.5 | 7 | V |
| | | I/O ports ⁽²⁾⁽³⁾ | -0.5 | 7 | |
| V_O | Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾ | -0.5 | 7 | V | |
| V_O | Output voltage range applied in the high or low state ⁽²⁾⁽³⁾ | -0.5 | $V_{CC} + 0.5$ | V | |
| I_{IK} | Input clamp current | $V_I < 0$ | -20 | mA | |
| I_{OK} | Output clamp current | $V_O < 0$ | -50 | mA | |
| I_O | Continuous output current | $V_O = 0$ to V_{CC} | ±35 | mA | |
| | Continuous current through V_{CC} or GND | | ±70 | mA | |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) This value is limited to 5.5-V maximum.

7.2 Handling Ratings

| | | MIN | MAX | UNIT | |
|-------------|---------------------------|------------------------------------------------------------------------------------------|-----|------|---|
| T_{stg} | Storage temperature range | -65 | 150 | °C | |
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾ | 0 | 2000 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾ | 0 | 1000 | |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

 over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | SN54LV245A ⁽²⁾ | | SN74LV245A | | UNIT | |
|-----------------|------------------------------------|----------------------------------|-----------------------|-----------------------|-----------------------|-----------------|---|
| | | MIN | MAX | MIN | MAX | | |
| V _{CC} | Supply voltage | 2 | 5.5 | 2 | 5.5 | V | |
| V _{IH} | High-level input voltage | V _{CC} = 2 V | 1.5 | 1.5 | | V | |
| | | V _{CC} = 2.3 V to 2.7 V | V _{CC} × 0.7 | V _{CC} × 0.7 | | | |
| | | V _{CC} = 3 V to 3.6 V | V _{CC} × 0.7 | V _{CC} × 0.7 | | | |
| | | V _{CC} = 4.5 V to 5.5 V | V _{CC} × 0.7 | V _{CC} × 0.7 | | | |
| V _{IL} | Low-level input voltage | V _{CC} = 2 V | | 0.5 | 0.5 | V | |
| | | V _{CC} = 2.3 V to 2.7 V | | V _{CC} × 0.3 | V _{CC} × 0.3 | | |
| | | V _{CC} = 3 V to 3.6 V | | V _{CC} × 0.3 | V _{CC} × 0.3 | | |
| | | V _{CC} = 4.5 V to 5.5 V | | V _{CC} × 0.3 | V _{CC} × 0.3 | | |
| V _I | Input voltage | 0 | 5.5 | 0 | 5.5 | V | |
| V _O | Output voltage | High or low state | 0 | V _{CC} | 0 | V _{CC} | V |
| | | 3-state | 0 | 5.5 | 0 | 5.5 | |
| I _{OH} | High-level output current | V _{CC} = 2 V | | –50 | –50 | μA | |
| | | V _{CC} = 2.3 V to 2.7 V | | –2 | –2 | mA | |
| | | V _{CC} = 3 V to 3.6 V | | –8 | –8 | | |
| | | V _{CC} = 4.5 V to 5.5 V | | –16 | –16 | | |
| I _{OL} | Low-level output current | V _{CC} = 2 V | | 50 | 50 | μA | |
| | | V _{CC} = 2.3 V to 2.7 V | | 2 | 2 | mA | |
| | | V _{CC} = 3 V to 3.6 V | | 8 | 8 | | |
| | | V _{CC} = 4.5 V to 5.5 V | | 16 | 16 | | |
| Δt/Δv | Input transition rise or fall rate | V _{CC} = 2.3 V to 2.7 V | | 200 | 200 | ns/V | |
| | | V _{CC} = 3 V to 3.6 V | | 100 | 100 | | |
| | | V _{CC} = 4.5 V to 5.5 V | | 20 | 20 | | |
| T _A | Operating free-air temperature | –55 | 125 | –40 | 125 | °C | |

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs (SCBA004)*.

(2) Product Preview

7.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | SN74LV245A | | | | | | UNIT |
|-------------------------------|----------------------------------------------|------------|-------|------|------|-------|------|------|
| | | DB | DGV | DW | NS | PW | RGY | |
| | | 20 PINS | | | | | | |
| R _{θJA} | Junction-to-ambient thermal resistance | 94.6 | 114.8 | 77.5 | 76.6 | 101.5 | 34.1 | °C/W |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | 56.3 | 30.1 | 43.7 | 43.0 | 35.6 | 38.4 | |
| R _{θJB} | Junction-to-board thermal resistance | 49.8 | 56.3 | 45.1 | 44.1 | 52.5 | 12.0 | |
| ψ _{JT} | Junction-to-top characterization parameter | 18.3 | 0.9 | 16.9 | 16.7 | 2.2 | 0.8 | |
| ψ _{JB} | Junction-to-board characterization parameter | 49.4 | 55.6 | 44.7 | 43.7 | 52.0 | 12.0 | |
| R _{θJC(bot)} | Junction-to-case (bottom) thermal resistance | — | — | — | — | — | 7.1 | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report ([SPRA953](#)).

7.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | SN54LV245A ⁽¹⁾ | | | –40°C to 85°C SN74LV245A | | | –40°C to 125°C SN74LV245A | | | UNIT | |
|------------------|--------------------------|-------------------------------------------------------------|---------------------------|-----|-----|-----------------------------|-----|-----|------------------------------|-----|-----|------|----|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | | |
| V _{OH} | I _{OH} = –50 μA | 2 V to 5.5 V | V _{CC} – 0.1 | | | V _{CC} – 0.1 | | | V _{CC} – 0.1 | | | V | |
| | I _{OH} = –2 mA | 2.3 V | 2 | | | 2 | | | 2 | | | | |
| | I _{OH} = –8 mA | 3 V | 2.48 | | | 2.48 | | | 2.48 | | | | |
| | I _{OH} = –16 mA | 4.5 V | 3.8 | | | 3.8 | | | 3.8 | | | | |
| V _{OL} | I _{OL} = 50 μA | 2 V to 5.5 V | 0.1 | | | 0.1 | | | 0.1 | | | V | |
| | I _{OL} = 2 mA | 2.3 V | 0.4 | | | 0.4 | | | 0.4 | | | | |
| | I _{OL} = 8 mA | 3 V | 0.44 | | | 0.44 | | | 0.44 | | | | |
| | I _{OL} = 16 mA | 4.5 V | 0.55 | | | 0.55 | | | 0.55 | | | | |
| I _I | Control inputs | V _I = 5.5 V or GND | 0 to 5.5 V | | | ±1 | | | ±1 | | | μA | |
| I _{OZ} | A or B port | V _O = V _{CC} or GND | 5.5 V | | | ±5 | | | ±5 | | | μA | |
| I _{CC} | | V _I = V _{CC} or GND, I _O = 0 | 5.5 V | | | 20 | | | 20 | | | μA | |
| I _{off} | | V _I or V _O = 0 to 5.5 V | 0 | | | 5 | | | 5 | | | μA | |
| C _i | Control inputs | V _I = V _{CC} or GND | 3.3 V | 3 | | | 3 | | | | | | pF |
| | | | 5 V | 3 | | | 3 | | | | | | |
| C _{io} | A or B port | V _O = V _{CC} or GND | 3.3 V | 5.5 | | | 5.5 | | | | | | pF |
| | | | 5 V | 5.5 | | | 5.5 | | | | | | |

(1) Product Preview

7.6 Switching Characteristics, V_{CC} = 2.5 V ± 0.2 V

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | T _A = 25°C | | | SN54LV245A ⁽¹⁾ | | SN74LV245A | | –40°C to 125°C SN74LV245A | | UNIT |
|--------------------|------------------------|-------------|------------------------|-----------------------------------------|-----|-----|---------------------------|-------------------|------------|-----|------------------------------|-----|------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| t _{pd} | A or B | B or A | C _L = 15 pF | 8.3 ⁽²⁾ 13 ⁽²⁾ | | | 1 ⁽²⁾ | 15 ⁽²⁾ | 1 | 15 | 1 | 17 | ns |
| t _{en} | $\overline{\text{OE}}$ | A or B | | 11.8 ⁽²⁾ 19.9 ⁽²⁾ | | | 1 ⁽²⁾ | 22 ⁽²⁾ | 1 | 22 | 1 | 24 | |
| t _{dis} | $\overline{\text{OE}}$ | A or B | | 11.8 ⁽²⁾ 18.1 ⁽²⁾ | | | 1 ⁽²⁾ | 20 ⁽²⁾ | 1 | 20 | 1 | 22 | |
| t _{pd} | A or B | B or A | C _L = 50 pF | 11.2 15.9 | | | 1 | 18 | 1 | 18 | 1 | 21 | ns |
| t _{en} | $\overline{\text{OE}}$ | A or B | | 14.1 22.7 | | | 1 | 26 | 1 | 26 | 1 | 28 | |
| t _{dis} | $\overline{\text{OE}}$ | A or B | | 17.6 23.1 | | | 1 | 25 | 1 | 25 | 1 | 27 | |
| t _{sk(o)} | | | | 2 | | | | | 2 | | | | |

(1) Product Preview

(2) On products compliant to MIL-PRF-38535, this parameter is not production tested.

SN54LV245A, SN74LV245A

SCLS3820 – SEPTEMBER 1997 – REVISED SEPTEMBER 2014

www.ti.com

7.7 Switching Characteristics, $V_{CC} = 3.3 V \pm 0.3 V$

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A = 25^\circ\text{C}$ | | | SN54LV245A ⁽¹⁾ | | SN74LV245A | | -40°C to 125°C SN74LV245A | | UNIT |
|-------------|-----------------|-------------|-----------------------|--------------------------|--------------------|---------------------|---------------------------|---------------------|------------|------|------------------------------|------|------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| t_{pd} | A or B | B or A | $C_L = 15 \text{ pF}$ | | 5.9 ⁽²⁾ | 8.4 ⁽²⁾ | 1 ⁽²⁾ | 10 ⁽²⁾ | 1 | 10 | 1 | 11 | ns |
| t_{en} | \overline{OE} | A or B | | | 8.2 ⁽²⁾ | 13.2 ⁽²⁾ | 1 ⁽²⁾ | 15.5 ⁽²⁾ | 1 | 15.5 | 1 | 16.5 | |
| t_{dis} | \overline{OE} | A or B | | | 9.6 ⁽²⁾ | 16.5 ⁽²⁾ | 1 ⁽²⁾ | 19.5 ⁽²⁾ | 1 | 19.5 | 1 | 20.5 | |
| t_{pd} | A or B | B or A | $C_L = 50 \text{ pF}$ | | 7.9 | 11.9 | 1 | 13.5 | 1 | 13.5 | 1 | 14.5 | ns |
| t_{en} | \overline{OE} | A or B | | | 9.9 | 16.7 | 1 | 19 | 1 | 19 | 1 | 20 | |
| t_{dis} | \overline{OE} | A or B | | | 13.9 | 19.8 | 1 | 22 | 1 | 22 | 1 | 23 | |
| $t_{sk(o)}$ | | | | | | 1.5 | | | | 1.5 | | | |

(1) Product Preview

(2) On products compliant to MIL-PRF-38535, this parameter is not production tested.

7.8 Switching Characteristics, $V_{CC} = 5 V \pm 0.5 V$

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A = 25^\circ\text{C}$ | | | SN54LV245A ⁽¹⁾ | | SN74LV245A | | -40°C to 125°C SN74LV245A | | UNIT |
|-------------|-----------------|-------------|-----------------------|--------------------------|--------------------|---------------------|---------------------------|---------------------|------------|------|------------------------------|------|------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| t_{pd} | A or B | B or A | $C_L = 15 \text{ pF}$ | | 4.3 ⁽²⁾ | 5.5 ⁽²⁾ | 1 ⁽²⁾ | 6.5 ⁽²⁾ | 1 | 6.5 | 1 | 7 | ns |
| t_{en} | \overline{OE} | A or B | | | 5.7 ⁽²⁾ | 8.5 ⁽²⁾ | 1 ⁽²⁾ | 10.6 ⁽²⁾ | 1 | 10 | 1 | 10.5 | |
| t_{dis} | \overline{OE} | A or B | | | 7.8 ⁽²⁾ | 12.8 ⁽²⁾ | 1 ⁽²⁾ | 14.7 ⁽²⁾ | 1 | 14.2 | 1 | 14.7 | |
| t_{pd} | A or B | B or A | $C_L = 50 \text{ pF}$ | | 5.6 | 7.5 | 1 | 8.5 | 1 | 8.5 | 1 | 9 | ns |
| t_{en} | \overline{OE} | A or B | | | 7 | 10.6 | 1 | 12 | 1 | 12 | 1 | 12.5 | |
| t_{dis} | \overline{OE} | A or B | | | 10.9 | 14.7 | 1 | 16 | 1 | 16 | 1 | 16.5 | |
| $t_{sk(o)}$ | | | | | | 1 | | | | 1 | | | |

(1) Product Preview

(2) On products compliant to MIL-PRF-38535, this parameter is not production tested.

7.9 Noise Characteristics⁽¹⁾

$V_{CC} = 3.3 V$, $C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$

| PARAMETER | DESCRIPTION | SN74LV245A | | | UNIT |
|-------------|----------------------------------------|------------|------|------|------|
| | | MIN | TYP | MAX | |
| $V_{OL(P)}$ | Quiet output, maximum dynamic V_{OL} | | 0.5 | 0.8 | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic V_{OL} | | -0.4 | -0.8 | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic V_{OH} | | 2.9 | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 2.31 | | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | 0.99 | | | V |

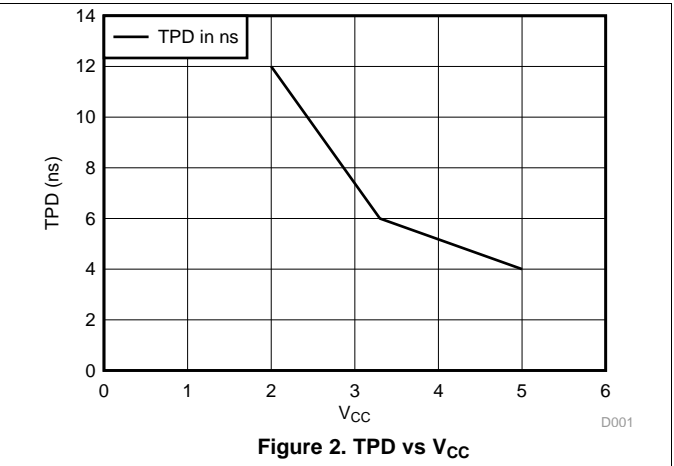
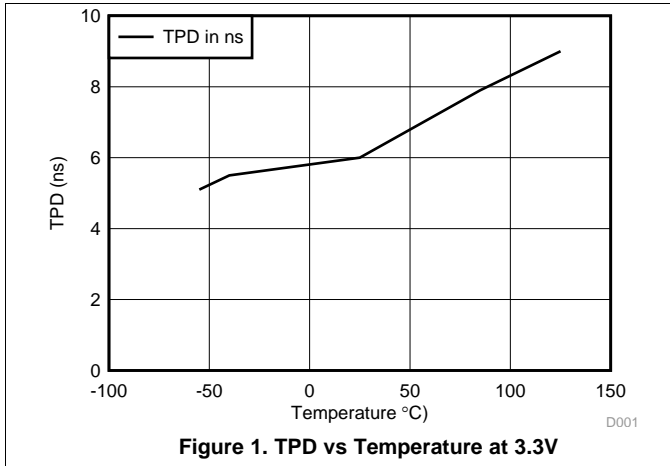
(1) Characteristics are for surface-mount packages only.

7.10 Operating Characteristics

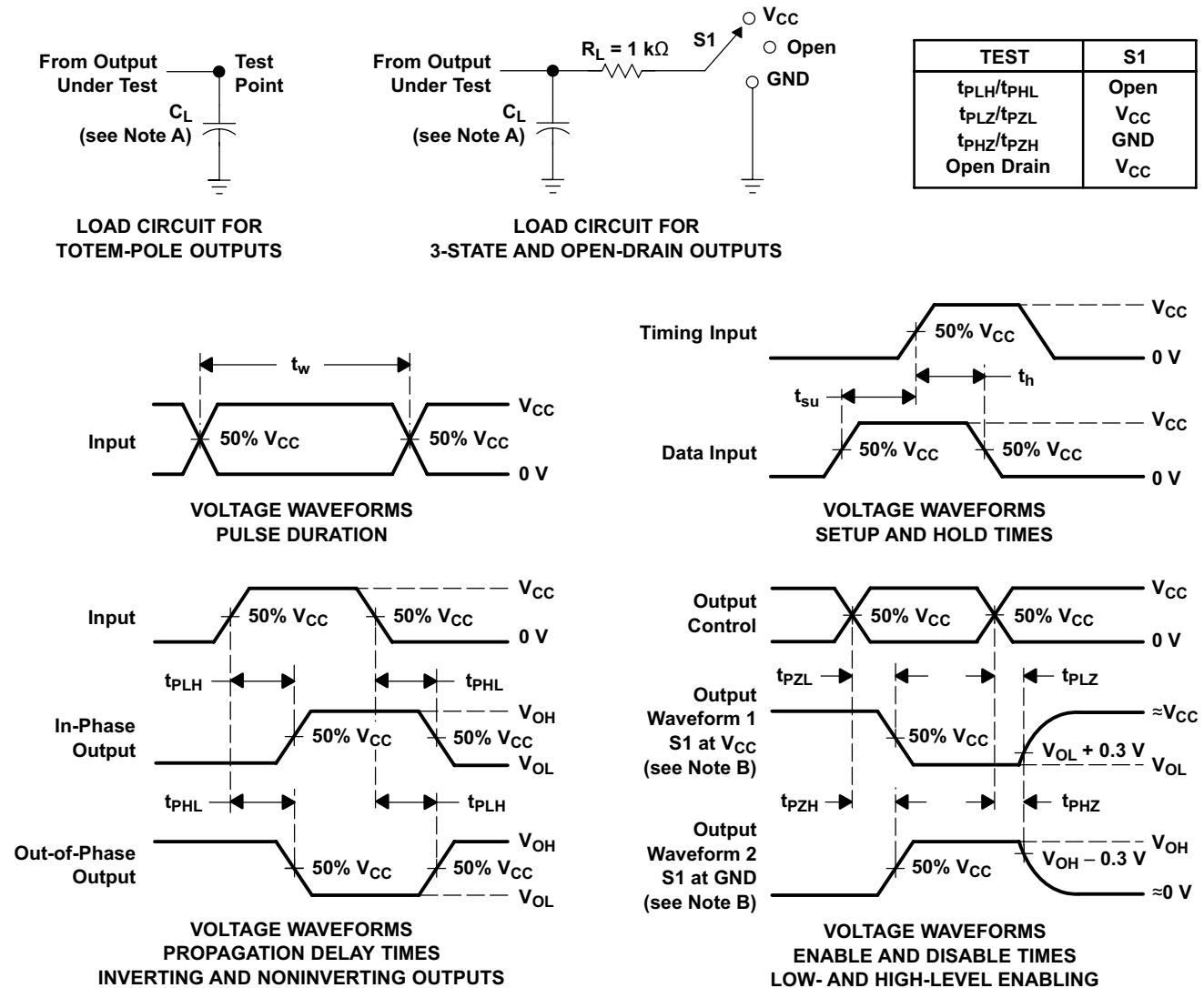
$T_A = 25^\circ\text{C}$

| PARAMETER | TEST CONDITIONS | V_{CC} | TYP | UNIT |
|-----------|-------------------------------|----------------------------------------------|-------------|------|
| C_{pd} | Power dissipation capacitance | | | pF |
| | Outputs enabled | $C_L = 50 \text{ pF}$, $f = 10 \text{ MHz}$ | 3.3 V 20 | |
| | | | 5 V 25 | |

7.11 Typical Characteristics



8 Parameter Measurement Information



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r \leq 3$ ns, $t_f \leq 3$ ns.
 - D. The outputs are measured one at a time, with one input transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PHL} and t_{PLH} are the same as t_{pd} .
 - H. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

9 Detailed Description

9.1 Overview

The SNx4LV245A devices are designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the device so the buses are effectively isolated.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

These devices are fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

9.2 Functional Block Diagram

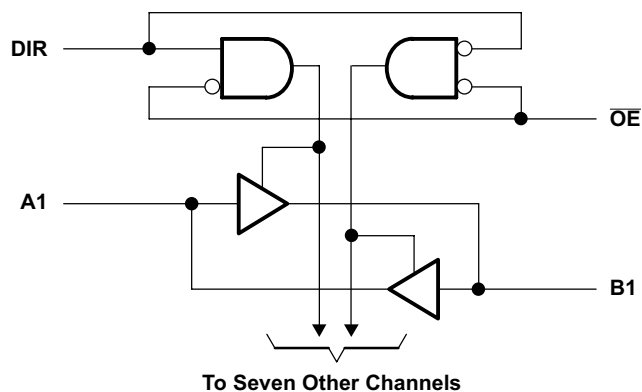


Figure 4. Logic Diagram (Positive Logic)

9.3 Feature Description

- Allows down voltage translation from 5 V to 3.3 V
 - Inputs accept voltage levels up to 5.5 V
- Slow edge rates minimize output ringing

9.4 Device Functional Modes

Table 1. Function Table

| INPUTS | | OPERATION |
|-----------------|-----|-----------------|
| \overline{OE} | DIR | |
| L | L | B data to A bus |
| L | H | A data to B bus |
| H | X | Isolation |

10 Application and Implementation

10.1 Application Information

The SNx4LV245A is a low-drive CMOS device that can be used for a multitude of bus-interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs. The inputs can accept voltages to 5.5 V at any valid V_{CC} making the device ideal for down translation.

10.2 Typical Application

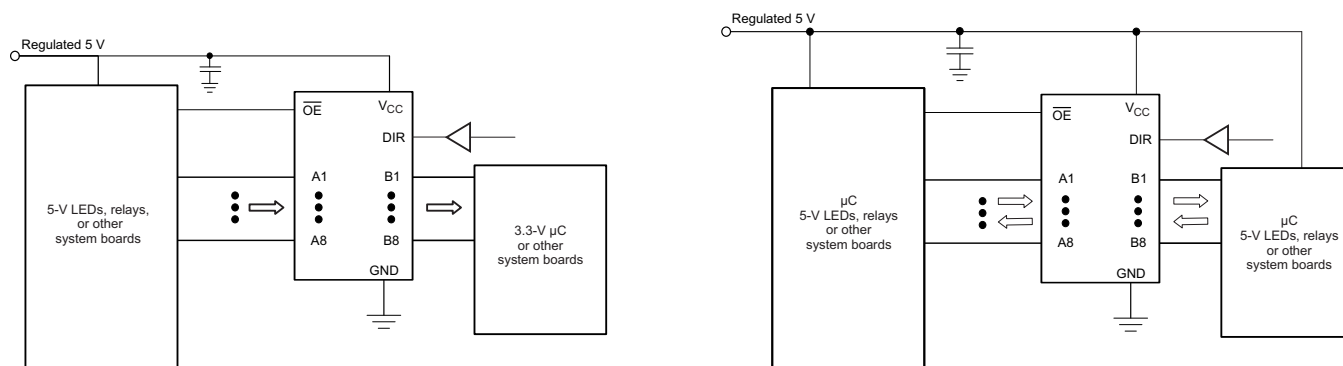


Figure 5. Typical Application Schematic

10.2.1 Design Requirements

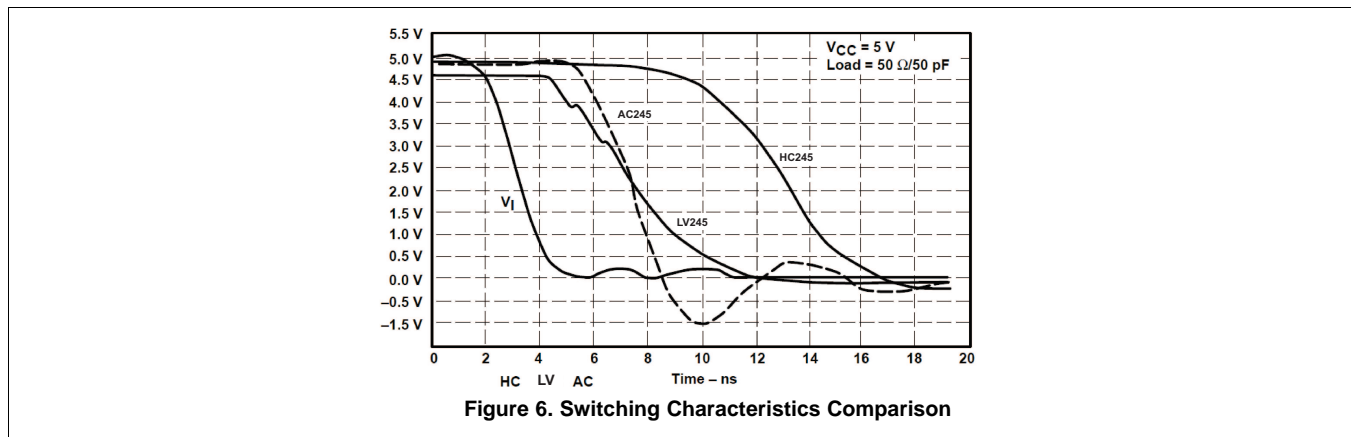
This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention, because it can drive currents that would exceed maximum limits. Outputs can be combined to produce higher drive, but the high drive will also create faster edges into light loads; therefore, routing and load conditions should be considered to prevent ringing.

10.2.2 Detailed Design Procedure

1. Recommended Input Conditions:
 - Rise time and fall time specifications, see $(\Delta t/\Delta V)$ in [Recommended Operating Conditions](#) table.
 - Specified high and low levels, see $(V_{IH}$ and $V_{IL})$ in [Recommended Operating Conditions](#) table.
 - Inputs are overvoltage tolerant, allowing them to go as high as 5.5 V at any valid V_{CC} .
2. Recommend Output Conditions:
 - Load currents should not exceed 35 mA per output and 70 mA total for the part.
 - Outputs should not be pulled above V_{CC} .

Typical Application (continued)

10.2.3 Application Curves



11 Power Supply Recommendations

The power supply can be any voltage between the Min and Max supply voltage rating located in the [Recommended Operating Conditions](#) table.

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 μF is recommended and if there are multiple V_{CC} terminals then 0.01 μF or 0.022 μF is recommended for each power terminal. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 μF and 1 μF are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

12 Layout

12.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified in [Figure 7](#) are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} , whichever makes more sense or is more convenient. It is generally acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the outputs section of the part when asserted. This will not disable the input section of the I/Os so they cannot float when disabled.

12.2 Layout Example

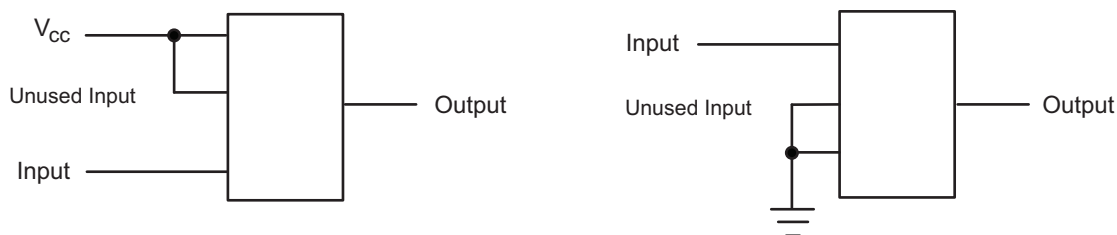


Figure 7. Layout Diagram

13 Device and Documentation Support

13.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|------------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| SN54LV245A | Click here | Click here | Click here | Click here | Click here |
| SN74LV245A | Click here | Click here | Click here | Click here | Click here |

13.2 Trademarks

All trademarks are the property of their respective owners.

13.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.4 Glossary

[SLYZ022](#) — *TI Glossary*.



This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| SN74LV245ADBLE | OBSOLETE | SSOP | DB | 20 | | TBD | Call TI | Call TI | -40 to 125 | | |
| SN74LV245ADBR | ACTIVE | SSOP | DB | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV245A | Samples |
| SN74LV245ADGVR | ACTIVE | TVSOP | DGV | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV245A | Samples |
| SN74LV245ADGVRG4 | ACTIVE | TVSOP | DGV | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV245A | Samples |
| SN74LV245ADW | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV245A | Samples |
| SN74LV245ADWE4 | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV245A | Samples |
| SN74LV245ADWG4 | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV245A | Samples |
| SN74LV245ADWR | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV245A | Samples |
| SN74LV245ADWRG4 | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV245A | Samples |
| SN74LV245ANSR | ACTIVE | SO | NS | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 74LV245A | Samples |
| SN74LV245ANSRG4 | ACTIVE | SO | NS | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 74LV245A | Samples |
| SN74LV245APW | ACTIVE | TSSOP | PW | 20 | 70 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV245A | Samples |
| SN74LV245APWG4 | ACTIVE | TSSOP | PW | 20 | 70 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV245A | Samples |
| SN74LV245APWLE | OBSOLETE | TSSOP | PW | 20 | | TBD | Call TI | Call TI | -40 to 125 | | |
| SN74LV245APWR | ACTIVE | TSSOP | PW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU CU SN | Level-1-260C-UNLIM | -40 to 125 | LV245A | Samples |
| SN74LV245APWRE4 | ACTIVE | TSSOP | PW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV245A | Samples |
| SN74LV245APWRG3 | ACTIVE | TSSOP | PW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -40 to 125 | LV245A | Samples |
| SN74LV245APWRG4 | ACTIVE | TSSOP | PW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LV245A | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|----------------------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------------------------------------------------------------------|
| SN74LV245ARGYR | ACTIVE | VQFN | RGY | 20 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | LV245A |  |
| SN74LV245AZQNR | ACTIVE | BGA MICROSTAR JUNIOR | ZQN | 20 | 1000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | LV245A |  |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|----------------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LV245ADBR | SSOP | DB | 20 | 2000 | 330.0 | 16.4 | 8.2 | 7.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74LV245ADGVR | TVSOP | DGV | 20 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LV245ADWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |
| SN74LV245ANSR | SO | NS | 20 | 2000 | 330.0 | 24.4 | 9.0 | 13.0 | 2.4 | 4.0 | 24.0 | Q1 |
| SN74LV245APWR | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.1 | 1.6 | 8.0 | 16.0 | Q1 |
| SN74LV245APWR | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.1 | 1.6 | 8.0 | 16.0 | Q1 |
| SN74LV245APWRG3 | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.1 | 1.6 | 8.0 | 16.0 | Q1 |
| SN74LV245ARGYR | VQFN | RGY | 20 | 3000 | 330.0 | 12.4 | 3.8 | 4.8 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LV245AZQNR | BGA MICROSTAR JUNIOR | ZQN | 20 | 1000 | 330.0 | 12.4 | 3.3 | 4.3 | 1.6 | 8.0 | 12.0 | Q1 |

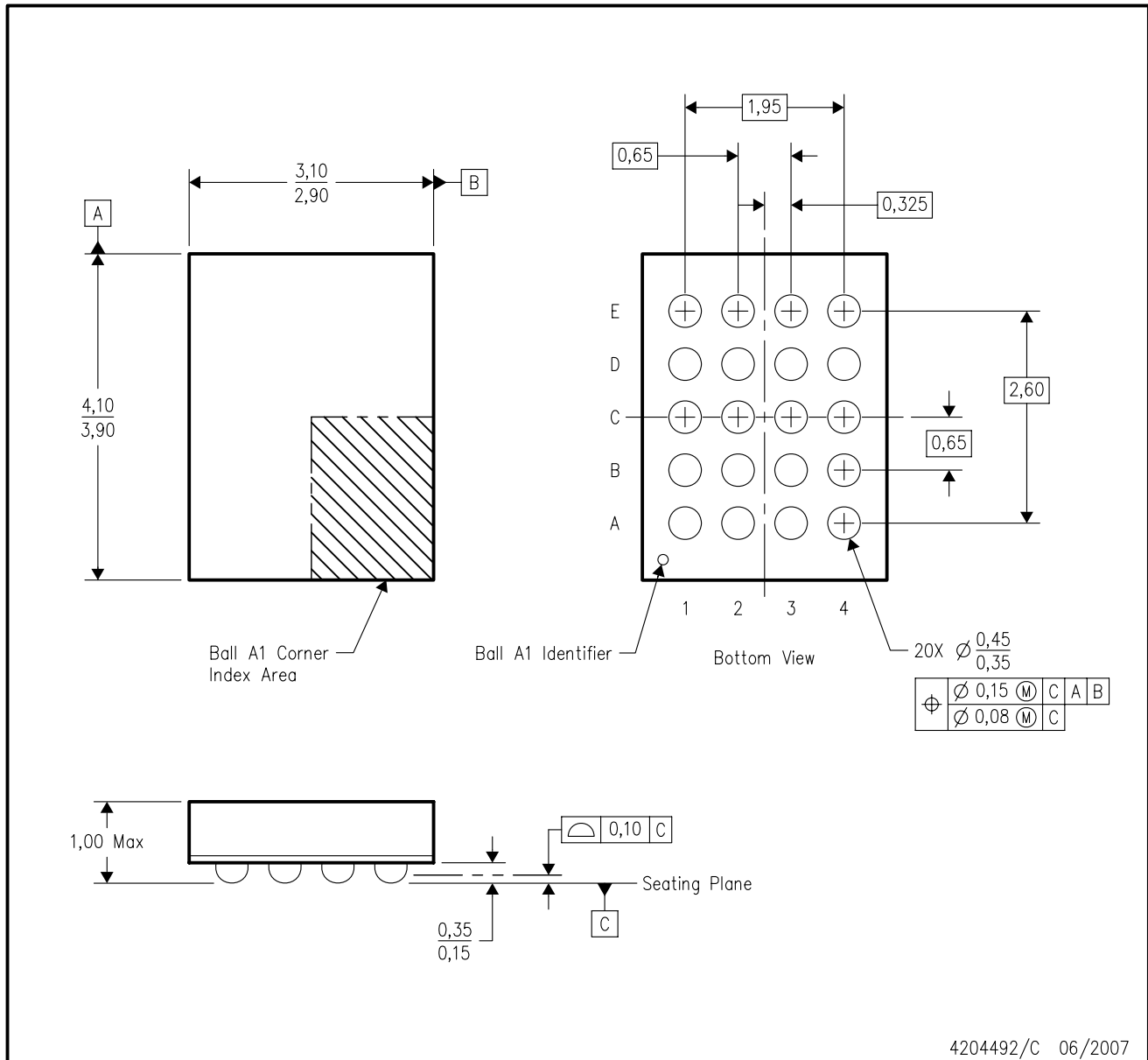
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-----------------|----------------------|-----------------|------|------|-------------|------------|-------------|
| SN74LV245ADBR | SSOP | DB | 20 | 2000 | 367.0 | 367.0 | 38.0 |
| SN74LV245ADGVR | TVSOP | DGV | 20 | 2000 | 367.0 | 367.0 | 35.0 |
| SN74LV245ADWR | SOIC | DW | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74LV245ANSR | SO | NS | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74LV245APWR | TSSOP | PW | 20 | 2000 | 364.0 | 364.0 | 27.0 |
| SN74LV245APWR | TSSOP | PW | 20 | 2000 | 367.0 | 367.0 | 38.0 |
| SN74LV245APWRG3 | TSSOP | PW | 20 | 2000 | 364.0 | 364.0 | 27.0 |
| SN74LV245ARGYR | VQFN | RGY | 20 | 3000 | 367.0 | 367.0 | 35.0 |
| SN74LV245AZQNR | BGA MICROSTAR JUNIOR | ZQN | 20 | 1000 | 338.1 | 338.1 | 20.6 |

ZQN (R-PBGA-N20)

PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MO-285 variation BC-2.
 - D. This package is lead-free. Refer to the 20 GQN package (drawing 4200704) for tin-lead (SnPb).

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

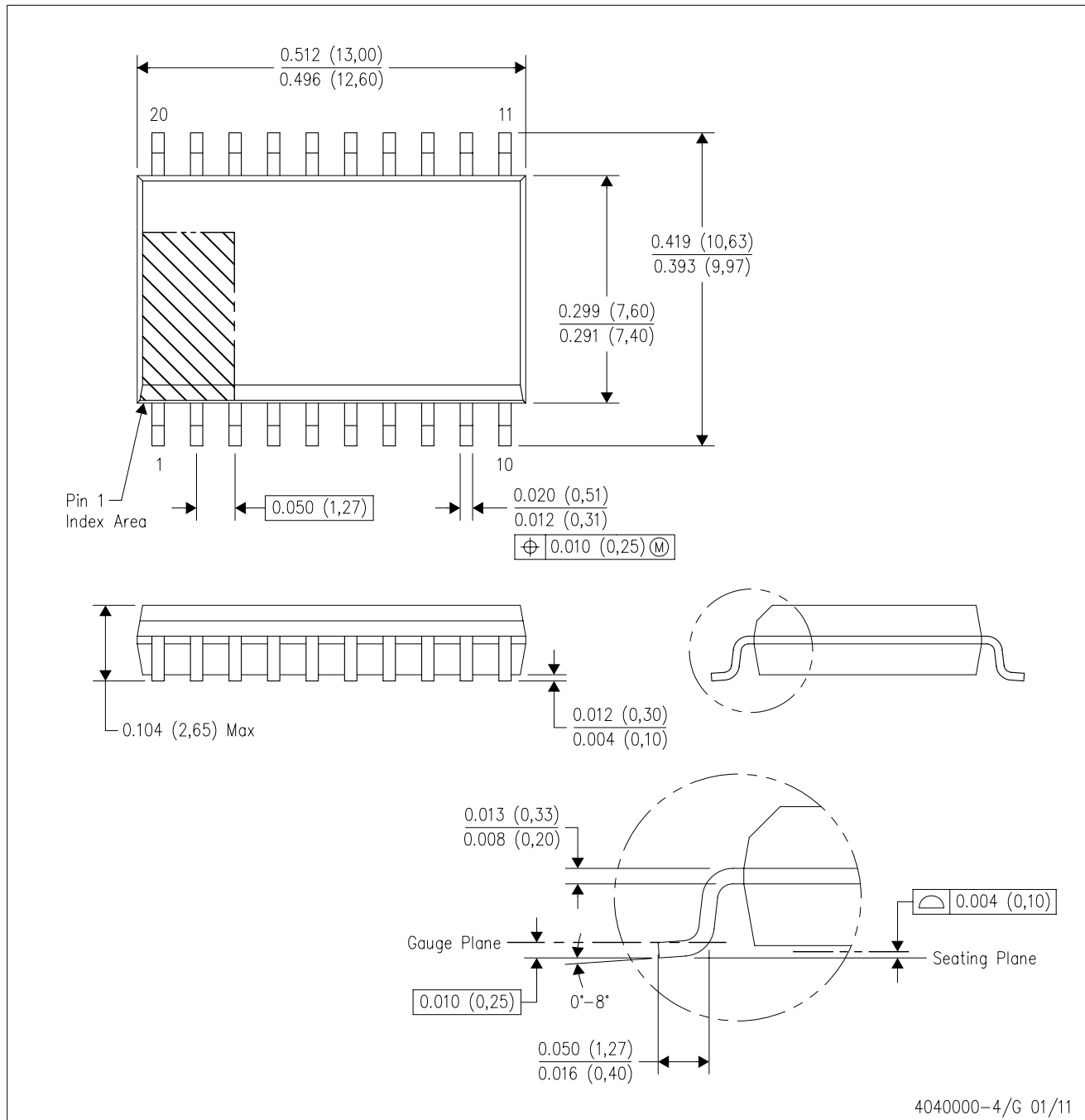
24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

DW (R-PDSO-G20)

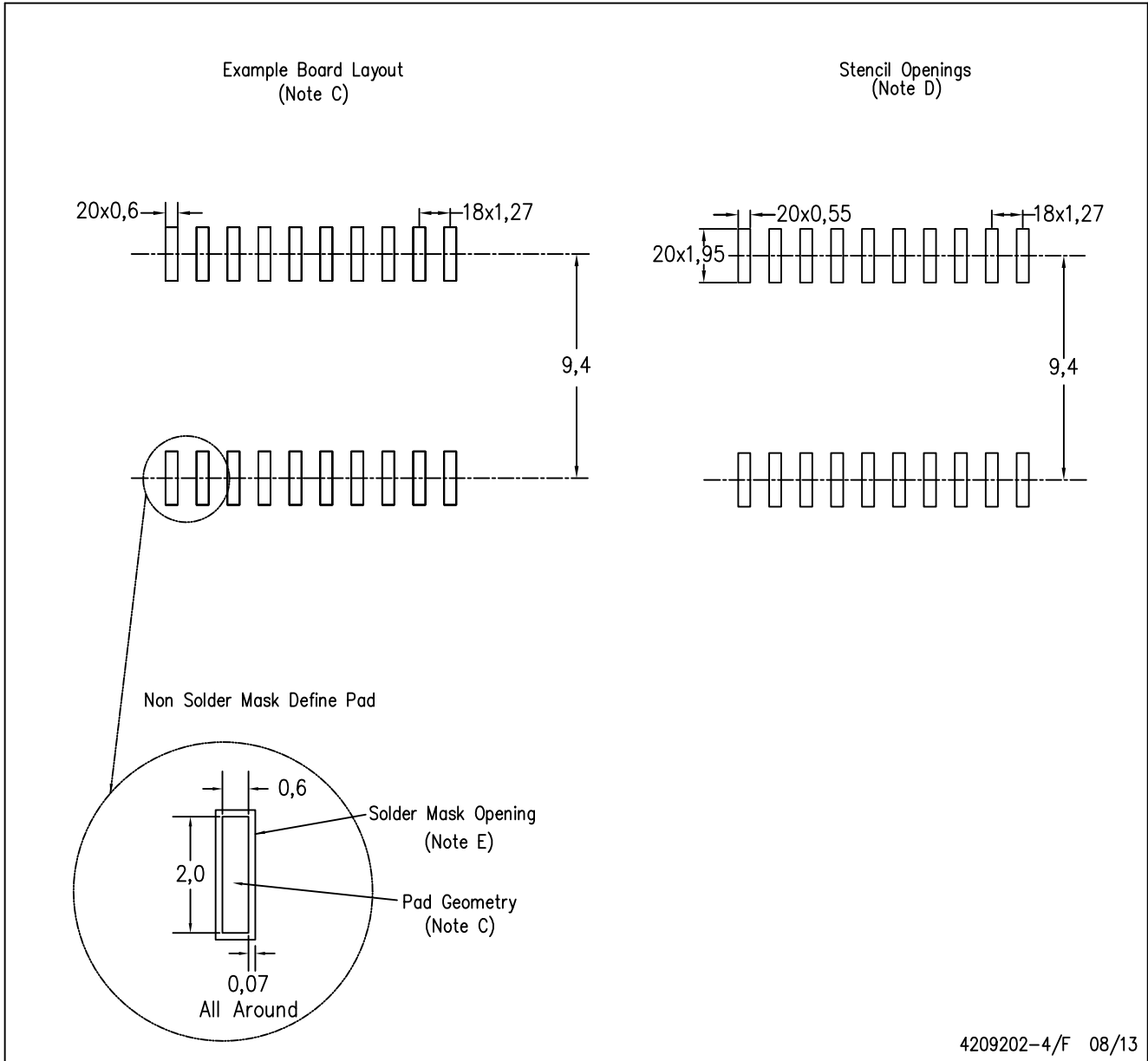
PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - Falls within JEDEC MS-013 variation AC.

DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



4209202-4/F 08/13

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Refer to IPC7351 for alternate board design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

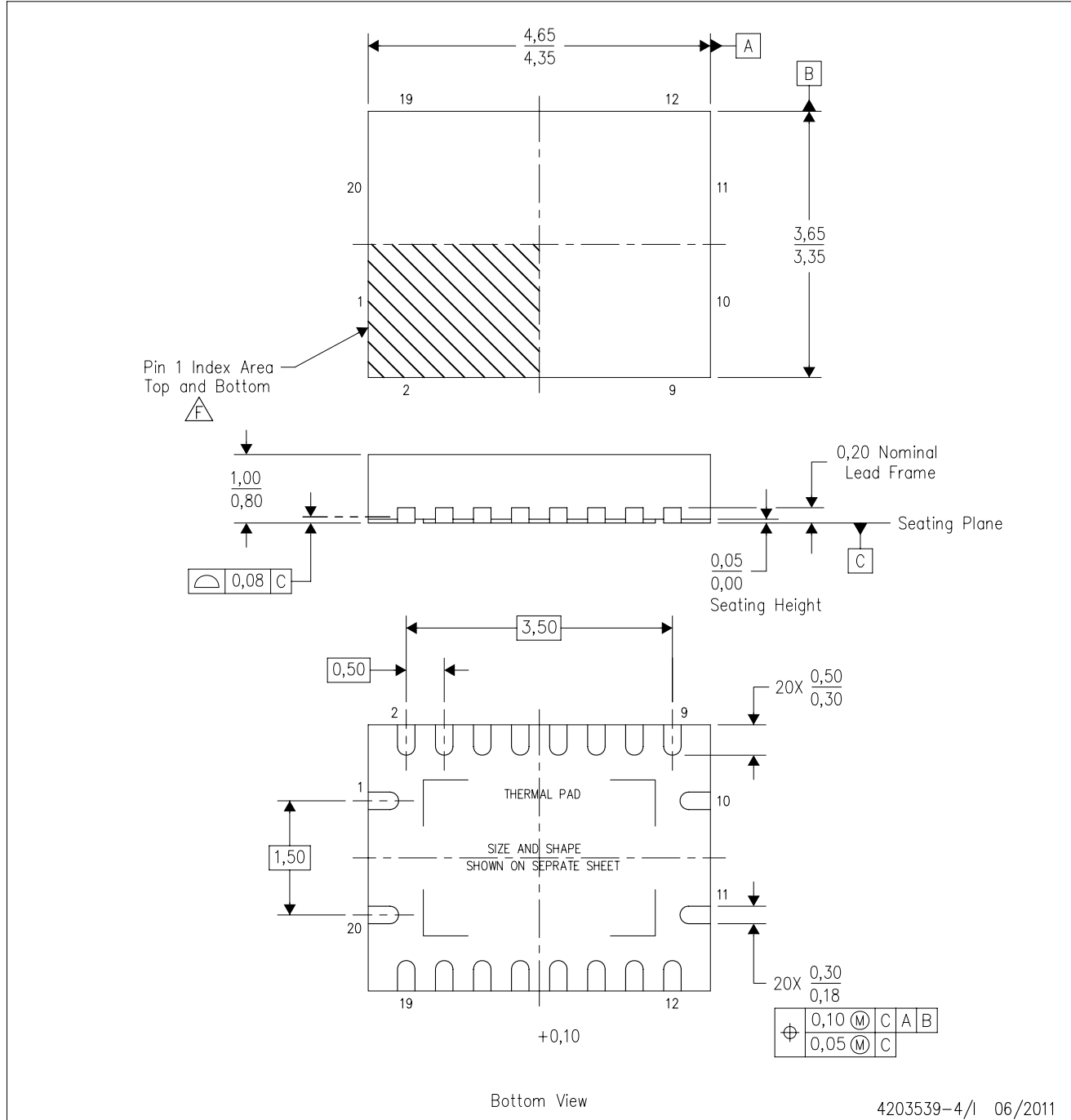
28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

RGY (R-PVQFN-N20)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - QFN (Quad Flatpack No-Lead) package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
 - Package complies to JEDEC MO-241 variation BA.

RGY (R-PVQFN-N20)

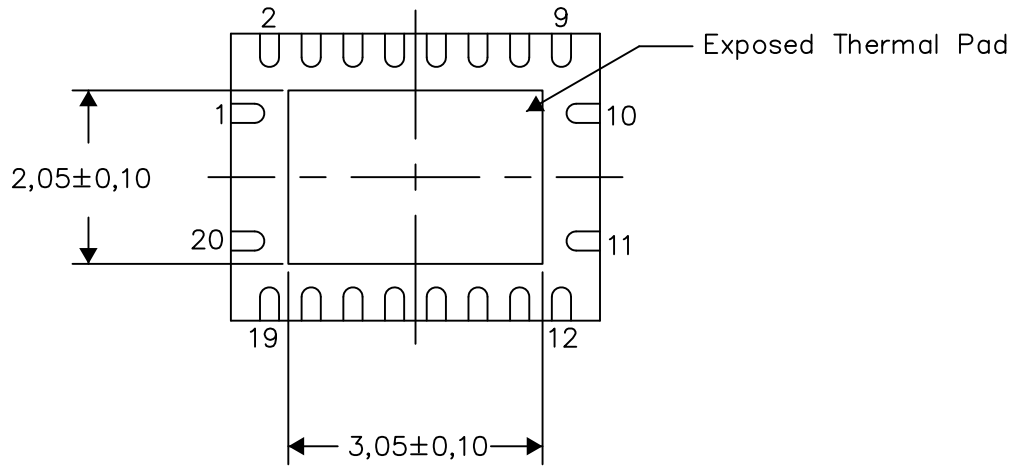
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

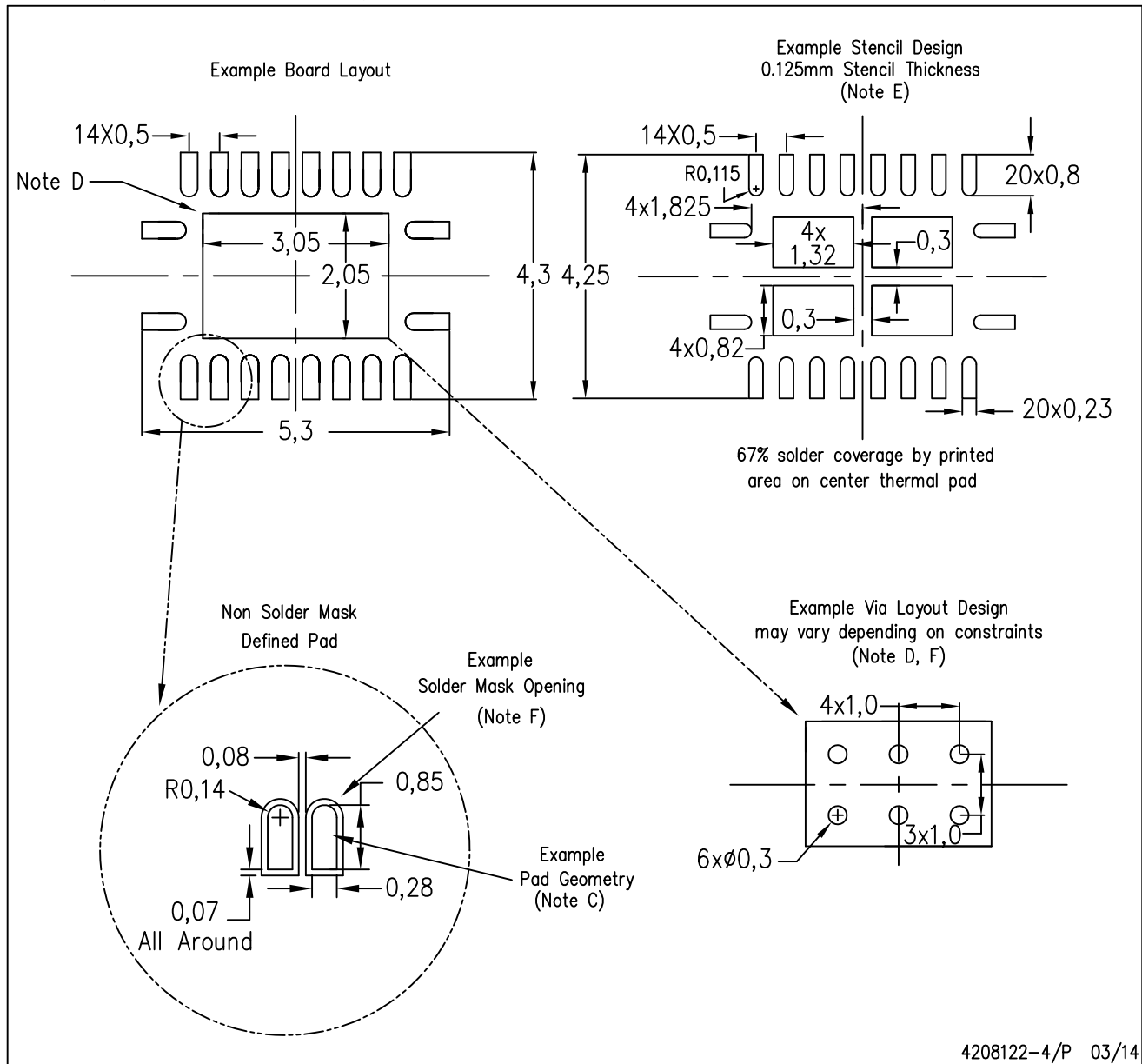
Exposed Thermal Pad Dimensions

4206353-4/P 03/14

NOTE: All linear dimensions are in millimeters

RGY (R-PVQFN-N20)

PLASTIC QUAD FLATPACK NO-LEAD



4208122-4/P 03/14

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products

| | |
|------------------------------|--------------------------------------------------------------------------------------|
| Audio | www.ti.com/audio |
| Amplifiers | amplifier.ti.com |
| Data Converters | dataconverter.ti.com |
| DLP® Products | www.dlp.com |
| DSP | dsp.ti.com |
| Clocks and Timers | www.ti.com/clocks |
| Interface | interface.ti.com |
| Logic | logic.ti.com |
| Power Mgmt | power.ti.com |
| Microcontrollers | microcontroller.ti.com |
| RFID | www.ti-rfid.com |
| OMAP Applications Processors | www.ti.com/omap |
| Wireless Connectivity | www.ti.com/wirelessconnectivity |

Applications

| | |
|-------------------------------|------------------------------------------------------------------------------------------|
| Automotive and Transportation | www.ti.com/automotive |
| Communications and Telecom | www.ti.com/communications |
| Computers and Peripherals | www.ti.com/computers |
| Consumer Electronics | www.ti.com/consumer-apps |
| Energy and Lighting | www.ti.com/energy |
| Industrial | www.ti.com/industrial |
| Medical | www.ti.com/medical |
| Security | www.ti.com/security |
| Space, Avionics and Defense | www.ti.com/space-avionics-defense |
| Video and Imaging | www.ti.com/video |

TI E2E Community

e2e.ti.com