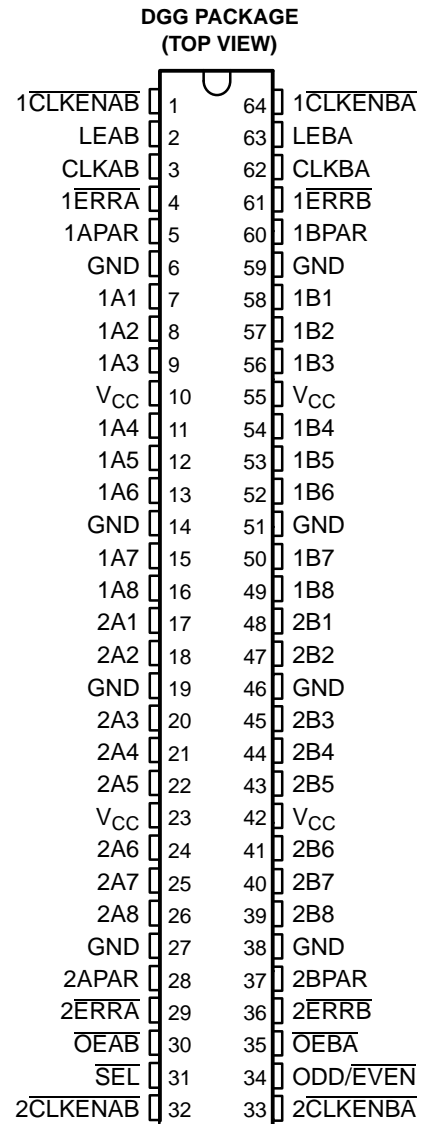


## FEATURES

- Member of the Texas Instruments Widebus+™ Family
- UBT™ Transceiver Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Modes
- Operates From 1.65 V to 3.6 V
- Inputs Accept Voltages to 5.5 V
- Max  $t_{pd}$  of 5.4 ns at 3.3 V
- Typical  $V_{OLP}$  (Output Ground Bounce) < 0.8 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot) > 2 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Simultaneously Generates and Checks Parity
- Option to Select Generate Parity and Check or Feedthrough Data/Parity in A-to-B or B-to-A Direction
- Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V  $V_{CC}$ )
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class I
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)



## DESCRIPTION/ORDERING INFORMATION

This 18-bit (dual-octal) noninverting registered transceiver is designed for 1.65-V to 3.6-V  $V_{CC}$  operation.

The SN74LVCH16901 is a dual 9-bit to dual 9-bit parity transceiver with registers. The device can operate as a feed-through transceiver, or it can generate/check parity from the two 8-bit data buses in either direction.

### ORDERING INFORMATION

$T_A$	PACKAGE <sup>(1)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	TSSOP – DGG	Tape and reel	SN74LVCH16901DGGR	LVCH16901

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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**SN74LVCH16901**  
**18-BIT UNIVERSAL BUS TRANSCEIVER**  
**WITH PARITY GENERATORS/CHECKERS**

Not Recommended For New Designs



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**DESCRIPTION/ORDERING INFORMATION (CONTINUED)**

The SN74LVCH16901 features independent clock (CLKAB or CLKBA), latch-enable (LEAB or LEBA), and dual 9-bit clock-enable ( $\overline{\text{CLKENAB}}$  or  $\overline{\text{CLKENBA}}$ ) inputs. It also provides parity-enable ( $\overline{\text{SEL}}$ ) and parity-select (ODD/EVEN) inputs and separate error-signal ( $\overline{\text{ERRA}}$  or  $\overline{\text{ERRB}}$ ) outputs for checking parity. The direction of data flow is controlled by output-enable ( $\overline{\text{OEAB}}$  and  $\overline{\text{OEBA}}$ ) inputs. When  $\overline{\text{SEL}}$  is low, the parity functions are enabled. When  $\overline{\text{SEL}}$  is high, the parity functions are disabled, and the device acts as an 18-bit registered transceiver.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

To ensure the high-impedance state during power up or power down,  $\overline{\text{OE}}$  should be tied to  $V_{\text{CC}}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

This device is fully specified for partial-power-down applications using  $I_{\text{off}}$ . The  $I_{\text{off}}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

**FUNCTION TABLES**

**FUNCTION<sup>(1)</sup>**

INPUTS					OUTPUT B
$\overline{\text{CLKENAB}}$	$\overline{\text{OEAB}}$	LEAB	CLKAB	A	
X	H	X	X	X	Z
X	L	H	X	L	L
X	L	H	X	H	H
H	L	L	X	X	$B_0^{(2)}$
L	L	L	↑	L	L
L	L	L	↑	H	H
L	L	L	L	X	$B_0^{(2)}$
L	L	L	H	X	$B_0^{(3)}$

- (1) A-to-B data flow is shown: B-to-A flow is similar, but uses  $\overline{\text{OEBA}}$ , LEBA, and  $\overline{\text{CLKENBA}}$ .
- (2) Output level before the indicated steady-state input conditions were established
- (3) Output level before the indicated steady-state input conditions were established, provided that CLKAB was low before LEAB went low

**PARITY ENABLE**

INPUTS			OPERATION OR FUNCTION	
$\overline{\text{SEL}}$	$\overline{\text{OEBA}}$	$\overline{\text{OEAB}}$		
L	H	L	Parity is checked on port A and is generated on port B.	
L	L	H	Parity is checked on port B and is generated on port A.	
L	H	H	Parity is checked on port B and port A.	
L	L	L	Parity is generated on port A and B if device is in FF mode.	
H	L	L	Parity functions are disabled; device acts as a standard 18-bit registered transceiver.	
H	L	H		$Q_A$ data to B, $Q_B$ data to A
H	H	L		$Q_B$ data to A
H	H	H		$Q_A$ data to B
			Isolation	

## FUNCTION TABLES (CONTINUED)

## PARITY

INPUTS								OUTPUTS			
SEL	$\overline{OEBA}$	$\overline{OEAB}$	ODD/EVEN	$\Sigma$ OF INPUTS A1–A8 = H	$\Sigma$ OF INPUTS B1–B8 = H	APAR	BPAR	APAR	$\overline{ERRA}$	BPAR	$\overline{ERRB}$
L	H	L	L	0, 2, 4, 6, 8	N/A	L	N/A	N/A	H	L	Z
L	H	L	L	1, 3, 5, 7	N/A	L	N/A	N/A	L	H	Z
L	H	L	L	0, 2, 4, 6, 8	N/A	H	N/A	N/A	L	L	Z
L	H	L	L	1, 3, 5, 7	N/A	H	N/A	N/A	H	H	Z
L	L	H	L	N/A	0, 2, 4, 6, 8	N/A	L	L	Z	N/A	H
L	L	H	L	N/A	1, 3, 5, 7	N/A	L	H	Z	N/A	L
L	L	H	L	N/A	0, 2, 4, 6, 8	N/A	H	L	Z	N/A	L
L	L	H	L	N/A	1, 3, 5, 7	N/A	H	H	Z	N/A	H
L	H	L	H	0, 2, 4, 6, 8	N/A	L	N/A	N/A	L	H	Z
L	H	L	H	1, 3, 5, 7	N/A	L	N/A	N/A	H	L	Z
L	H	L	H	0, 2, 4, 6, 8	N/A	H	N/A	N/A	H	H	Z
L	H	L	H	1, 3, 5, 7	N/A	H	N/A	N/A	L	L	Z
L	L	H	H	N/A	0, 2, 4, 6, 8	N/A	L	H	Z	N/A	L
L	L	H	H	N/A	1, 3, 5, 7	N/A	L	L	Z	N/A	H
L	L	H	H	N/A	0, 2, 4, 6, 8	N/A	H	H	Z	N/A	H
L	L	H	H	N/A	1, 3, 5, 7	N/A	H	H	L	Z	L
L	H	H	L	0, 2, 4, 6, 8	0, 2, 4, 6, 8	L	L	Z	H	Z	H
L	H	H	L	1, 3, 5, 7	1, 3, 5, 7	L	L	Z	L	Z	L
L	H	H	L	0, 2, 4, 6, 8	0, 2, 4, 6, 8	H	H	Z	L	Z	L
L	H	H	L	1, 3, 5, 7	1, 3, 5, 7	H	H	Z	H	Z	H
L	H	H	L	0, 2, 4, 6, 8	0, 2, 4, 6, 8	L	L	Z	L	Z	L
L	H	H	L	1, 3, 5, 7	1, 3, 5, 7	L	L	Z	H	Z	H
L	H	H	L	0, 2, 4, 6, 8	0, 2, 4, 6, 8	H	H	Z	H	Z	H
L	H	H	L	1, 3, 5, 7	1, 3, 5, 7	H	H	Z	L	Z	L
L	L	L	L	N/A	N/A	N/A	N/A	PE <sup>(1)</sup>	Z	PE <sup>(1)</sup>	Z
L	L	L	H	N/A	N/A	N/A	N/A	PO <sup>(2)</sup>	Z	PO <sup>(2)</sup>	Z

(1) Parity output is set to the level so that the specific bus side is set to even parity.

(2) Parity output is set to the level so that the specific bus side is set to odd parity.

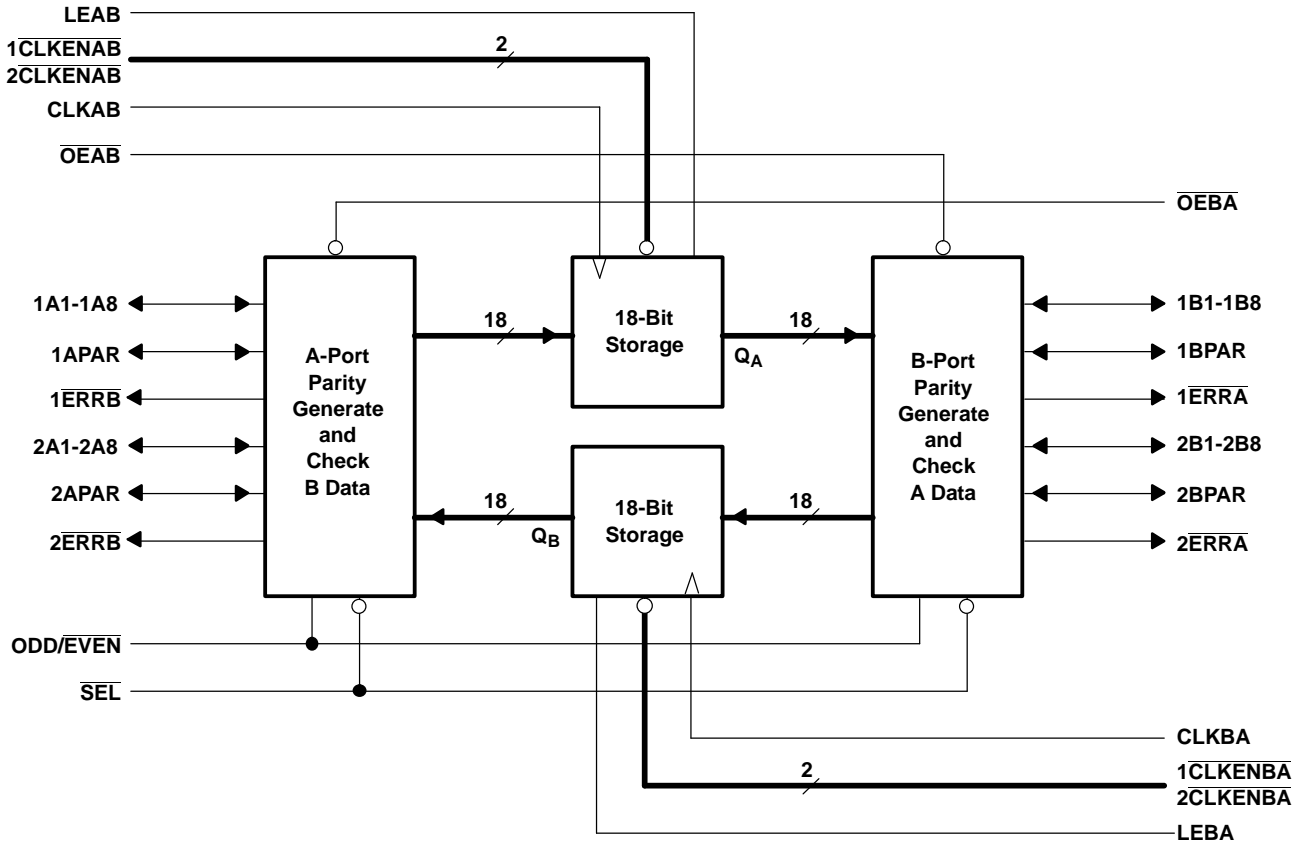
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**FUNCTIONAL BLOCK DIAGRAM**



**Absolute Maximum Ratings<sup>(1)</sup>**

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage range	-0.5	6.5	V
$V_I$	Input voltage range <sup>(2)</sup>	-0.5	6.5	V
$V_O$	Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup>	-0.5	6.5	V
$V_O$	Voltage range applied to any output in the high or low state <sup>(2)(3)</sup>	-0.5	$V_{CC} + 0.5$	V
$I_{IK}$	Input clamp current		-50	mA
		$V_I < 0$		
$I_{OK}$	Output clamp current		-50	mA
		$V_O < 0$		
$I_O$	Continuous output current		±50	mA
	Continuous current through each $V_{CC}$ or GND		±100	mA
$\theta_{JA}$	Package thermal impedance <sup>(4)</sup>		55	°C/W
$T_{stg}$	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of  $V_{CC}$  is provided in the recommended operating conditions table.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

**Recommended Operating Conditions<sup>(1)</sup>**

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	Operating	1.65	3.6	V
		Data retention only	1.5		
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V	0.65 × V <sub>CC</sub>		V
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.7		
		V <sub>CC</sub> = 2.7 V to 3.6 V	2		
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V		0.35 × V <sub>CC</sub>	V
		V <sub>CC</sub> = 2.3 V to 2.7 V		0.7	
		V <sub>CC</sub> = 2.7 V to 3.6 V		0.8	
V <sub>I</sub>	Input voltage		0	5.5	V
V <sub>O</sub>	Output voltage	High or low state	0	V <sub>CC</sub>	V
		3-state	0	5.5	
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 1.65 V		–4	mA
		V <sub>CC</sub> = 2.3 V		–8	
		V <sub>CC</sub> = 2.7 V		–12	
		V <sub>CC</sub> = 3 V		–24	
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 1.65 V		4	mA
		V <sub>CC</sub> = 2.3 V		8	
		V <sub>CC</sub> = 2.7 V		12	
		V <sub>CC</sub> = 3 V		24	
Δt/Δv	Input transition rise or fall rate			5	ns/V
T <sub>A</sub>	Operating free-air temperature		–40	85	°C

(1) All unused control inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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**Electrical Characteristics**

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP <sup>(1)</sup>	MAX	UNIT
V <sub>OH</sub>		I <sub>OH</sub> = -100 μA	1.65 V to 3.6 V	V <sub>CC</sub> - 0.2			V
		I <sub>OH</sub> = -4 mA	1.65 V	1.2			
		I <sub>OH</sub> = -8 mA	2.3 V	1.7			
		I <sub>OH</sub> = -12 mA	2.7 V	2.2			
			3 V	2.4			
	I <sub>OH</sub> = -24 mA	3 V	2.2				
V <sub>OL</sub>		I <sub>OL</sub> = 100 μA	1.65 V to 3.6 V			0.2	V
		I <sub>OL</sub> = 4 mA	1.65 V			0.45	
		I <sub>OL</sub> = 8 mA	2.3 V			0.7	
		I <sub>OL</sub> = 12 mA	2.7 V			0.4	
		I <sub>OL</sub> = 24 mA	3 V			0.55	
I <sub>I</sub>	Control inputs	V <sub>I</sub> = 0 to 5.5 V	3.6 V			±5	μA
I <sub>I(hold)</sub>	A or B ports	V <sub>I</sub> = 0.58 V	1.65 V	25		μA	
		V <sub>I</sub> = 1.07 V		-25			
		V <sub>I</sub> = 0.7 V	2.3 V	45			
		V <sub>I</sub> = 1.7 V		-45			
		V <sub>I</sub> = 0.8 V	3 V	75			
		V <sub>I</sub> = 2 V		-75			
	V <sub>I</sub> = 0 to 3.6 V <sup>(2)</sup>	3.6 V	±600				
I <sub>off</sub>		V <sub>I</sub> or V <sub>O</sub> = 5.5 V	0	±10		μA	
I <sub>OZ</sub> <sup>(3)</sup>		V <sub>O</sub> = 0 to 5.5 V	3.6 V	±10		μA	
I <sub>CC</sub>		V <sub>I</sub> = V <sub>CC</sub> or GND	3.6 V	20		μA	
		3.6 V ≤ V <sub>I</sub> ≤ 5.5 V <sup>(4)</sup>		20			
ΔI <sub>CC</sub>		One input at V <sub>CC</sub> - 0.6 V, Other inputs at V <sub>CC</sub> or GND	2.7 V to 3.6 V	500		μA	
C <sub>i</sub>	Control inputs	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V	7		pF	
C <sub>io</sub>	A or B ports	V <sub>O</sub> = V <sub>CC</sub> or GND	3.3 V	9.5		pF	

- (1) All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.
- (2) This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.
- (3) For I/O ports, the parameter I<sub>OZ</sub> includes the input leakage current, but not I<sub>I(hold)</sub>.
- (4) This applies in the disabled state only.

## Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		$V_{CC} = 1.8\text{ V}^{(1)}$		$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$f_{\text{clock}}$	Clock frequency	125		125		125		125		MHz
$t_w$	Pulse duration	CLK $\uparrow$	4	3	3	3	3	3	3	ns
		LE high	3	3	3	3	3	3	3	
$t_{\text{su}}$	Setup time	A, APAR or B, BPAR before CLK $\uparrow$	4.7	2.7	2.8	2.5	2.5	2.5	2.5	ns
		$\overline{\text{CLKEN}}$ before CLK $\uparrow$	4.5	2.9	2.9	2.5	2.5	2.5	2.5	
		A, APAR or B, BPAR before LE $\downarrow$	0	2.2	2.1	2	2	2	2	
$t_h$	Hold time	A, APAR or B, BPAR after CLK $\uparrow$	0	1.2	1.2	1.3	1.3	1.3	1.3	ns
		$\overline{\text{CLKEN}}$ after CLK $\uparrow$	0	1.3	1.3	1.5	1.5	1.5	1.5	
		A, APAR or B, BPAR after LE $\downarrow$	1	1.7	1.9	1.7	1.7	1.7	1.7	

(1) Texas Instruments SPICE simulation data

## Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 1.8\text{ V}^{(1)}$		$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		UNIT
			MIN	TYP	MIN	MAX	MIN	MAX	MIN	MAX	
$f_{\text{max}}$			125		125		125		125		MHz
$t_{\text{pd}}$	A or B	B or A	5.9	1	6.2	5.8	1	5.4	5.4	5.4	ns
		BPAR or APAR	12.7	2	9.9	8.6	2	7.7	7.7	7.7	
	APAR or BPAR	BPAR or APAR	7	1	6.7	6.2	1	5.7	5.7	5.7	
		$\overline{\text{ERRA}}$ or $\overline{\text{ERRB}}$	13	2	10.7	9.7	2	8.5	8.5	8.5	
	ODD/EVEN	$\overline{\text{ERRA}}$ or $\overline{\text{ERRB}}$	9.9	1.5	9.7	8.9	1.5	7.8	7.8	7.8	
		BPAR or APAR	10.4	1.5	9.3	8.6	1.5	7.5	7.5	7.5	
	$\overline{\text{SEL}}$	BPAR or APAR	6.9	1	7.1	6.9	1	6.1	6.1	6.1	
	CLKAB or CLKBA	A or B	6.9	1	7.4	6.8	1	6.1	6.1	6.1	
		BPAR or APAR parity feedthrough	8.5	1.5	8.1	7.3	1.5	6.6	6.6	6.6	
		BPAR or APAR parity generated	14.1	2.5	11.2	9.7	2	8.7	8.7	8.7	
		$\overline{\text{ERRA}}$ or $\overline{\text{ERRB}}$	14.3	2.5	11.5	9.9	2	8.9	8.9	8.9	
	LEAB or LEBA	A or B	6.8	1	7	6.5	1	5.8	5.8	5.8	
		BPAR or APAR parity feedthrough	7.9	1.5	7.7	7	1.5	6.3	6.3	6.3	
		BPAR or APAR parity generated	13.6	2.5	10.8	9.3	2	8.4	8.4	8.4	
		$\overline{\text{ERRA}}$ or $\overline{\text{ERRB}}$	13.5	2.5	10.9	9.5	2	8.5	8.5	8.5	
	$t_{\text{en}}$	$\overline{\text{OEAB}}$ or $\overline{\text{OEBA}}$	B, BPAR or A, APAR	6.8	1.4	7.3	7.1	1	6.3	6.3	
$t_{\text{dis}}$	$\overline{\text{OEAB}}$ or $\overline{\text{OEBA}}$	B, BPAR or A, APAR	6.9	1.3	7.1	6.2	1.5	5.9	5.9	ns	
$t_{\text{en}}$	$\overline{\text{OEAB}}$ or $\overline{\text{OEBA}}$	$\overline{\text{ERRA}}$ or $\overline{\text{ERRB}}$	7.4	1.4	7.2	6.5	1	5.9	5.9	ns	
$t_{\text{dis}}$	$\overline{\text{OEAB}}$ or $\overline{\text{OEBA}}$	$\overline{\text{ERRA}}$ or $\overline{\text{ERRB}}$	9.3	1.3	8.3	7.5	1	6.7	6.7	ns	
$t_{\text{en}}$	$\overline{\text{SEL}}$	$\overline{\text{ERRA}}$ or $\overline{\text{ERRB}}$	7.6	1.4	7.7	7.5	1	6.5	6.5	ns	
$t_{\text{dis}}$	$\overline{\text{SEL}}$	$\overline{\text{ERRA}}$ or $\overline{\text{ERRB}}$	7.8	1.3	7.4	6.4	1.5	5.9	5.9	ns	

(1) Texas Instruments SPICE simulation data

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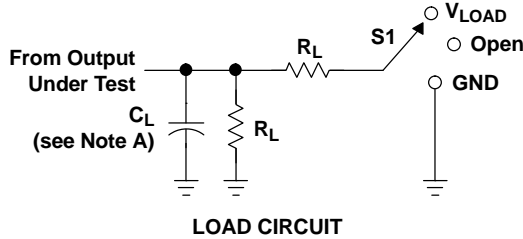
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**Operating Characteristics**

$T_A = 25^\circ\text{C}$

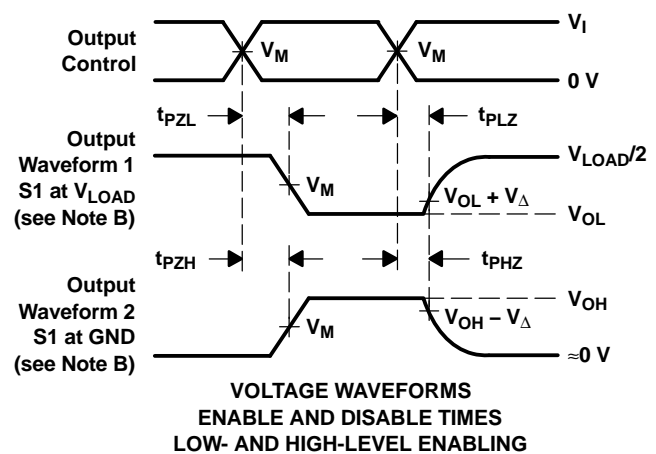
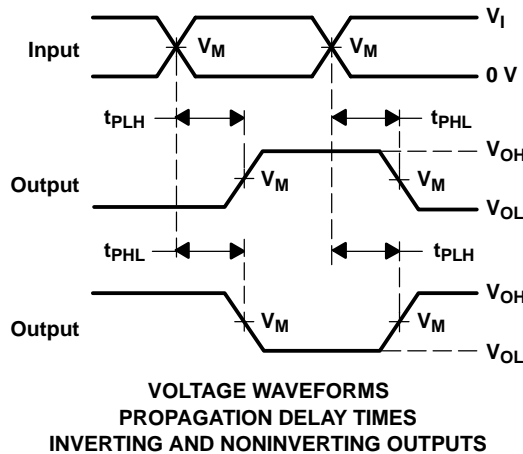
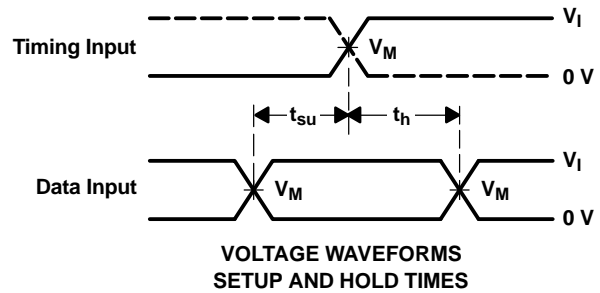
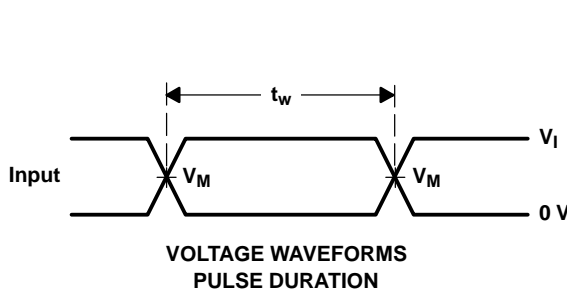
PARAMETER		TEST CONDITIONS	$V_{CC} = 1.8\text{ V}$	$V_{CC} = 2.5\text{ V}$	$V_{CC} = 3.3\text{ V}$	UNIT
			TYP	TYP	TYP	
$C_{pd}$	Power dissipation capacitance per transceiver	Outputs enabled	37	52	68	$\mu\text{F}$
		Outputs disabled	16	22	28	

PARAMETER MEASUREMENT INFORMATION



TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$V_{LOAD}$
$t_{PHZ}/t_{PZH}$	GND

$V_{CC}$	INPUTS		$V_M$	$V_{LOAD}$	$C_L$	$R_L$	$V_{\Delta}$
	$V_I$	$t_r/t_f$					
$1.8\text{ V} \pm 0.15\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k $\Omega$	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 $\Omega$	0.15 V
2.7 V	2.7 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V
$3.3\text{ V} \pm 0.3\text{ V}$	2.7 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V



- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ .
  - D. The outputs are measured one at a time, with one transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
  - H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
74LVCH16901DGGRE4	NRND	TSSOP	DGG	64		TBD	Call TI	Call TI	-40 to 85		
74LVCH16901DGGRG4	NRND	TSSOP	DGG	64		TBD	Call TI	Call TI	-40 to 85		
SN74LVCH16901DGGR	OBSOLETE	TSSOP	DGG	64		TBD	Call TI	Call TI	-40 to 85		

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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DGG (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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