## FEATURES

- **Meets or Exceeds the Requirements of IBM® 360/370 Input/Output Interface Specification for 4.5-Mb/s Operation**
- **Single 5-V Supply**
- **Uncommitted Emitter-Follower Output Structure for Party-Line Operation**
- **Driver Output Short-Circuit Protection**
- **Driver Input/Receiver Output Compatible With TTL**
- **Receiver Input Resistance . . . 7.4 kΩ to 20 kΩ**
- **Ratio Specification for Propagation Delay Time, Low to High/High to Low**

## DESCRIPTION/ ORDERING INFORMATION

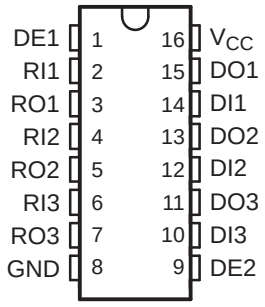
The SN751730 triple line driver/receiver is specifically designed to meet the input/output interface specifications for IBM System 360/370. It also is compatible with standard TTL logic and supply voltage levels.

The low-impedance emitter-follower driver outputs of the SN751730 drive terminated lines, such as coaxial cable or twisted pair. Having the outputs uncommitted allows wired-OR logic to be performed in party-line applications. Output short-circuit protection is provided by an internal clamping network that turns on when the output voltage drops below approximately 2.5 V.

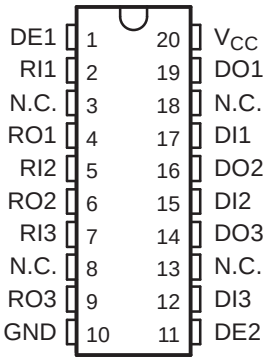
An open line affects the receiver input as does a low-level input voltage.

All the driver inputs and receiver outputs are in conventional TTL configuration and the gating can be used during power-up and power-down sequences to ensure that no noise is introduced to the line by pulling either DE1 or DE2 to a low level.

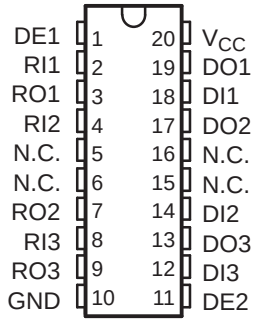
**D OR N PACKAGE**
**(TOP VIEW)**




**DW PACKAGE**
**(TOP VIEW)**




**NS PACKAGE**
**(TOP VIEW)**




N.C. – No internal connection

## ORDERING INFORMATION

| $T_A$ | PACKAGE(1)(2) | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|
| 0°C to 70°C | PDIP – N | Tube | SN751730N | SN751730N |
| | SOIC – D | Tube | SN751730D | SN751730 |
| | | Tape and reel | SN751730DR | |
| | SOIC – DW | Tube | SN751730DW | SN751730 |
| | | Tape and reel | SN751730DWR | |
| | SOP – NS | Tape and reel | SN751730NSR | SN751730 |

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

## FUNCTION TABLES

### EACH DRIVER

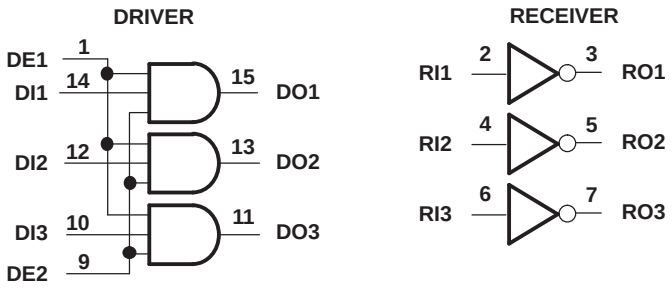
| INPUTS | | | OUTPUT DO |
|---|---|---|---|
| DI | DE1 | DE2 | |
| L | X | X | L |
| X | L | X | L |
| X | X | L | L |
| H | H | H | H |

### EACH DRIVER(1)

| INPUT RI | OUTPUT RO |
|---|---|
| L | H |
| H | L |
| Open | H |

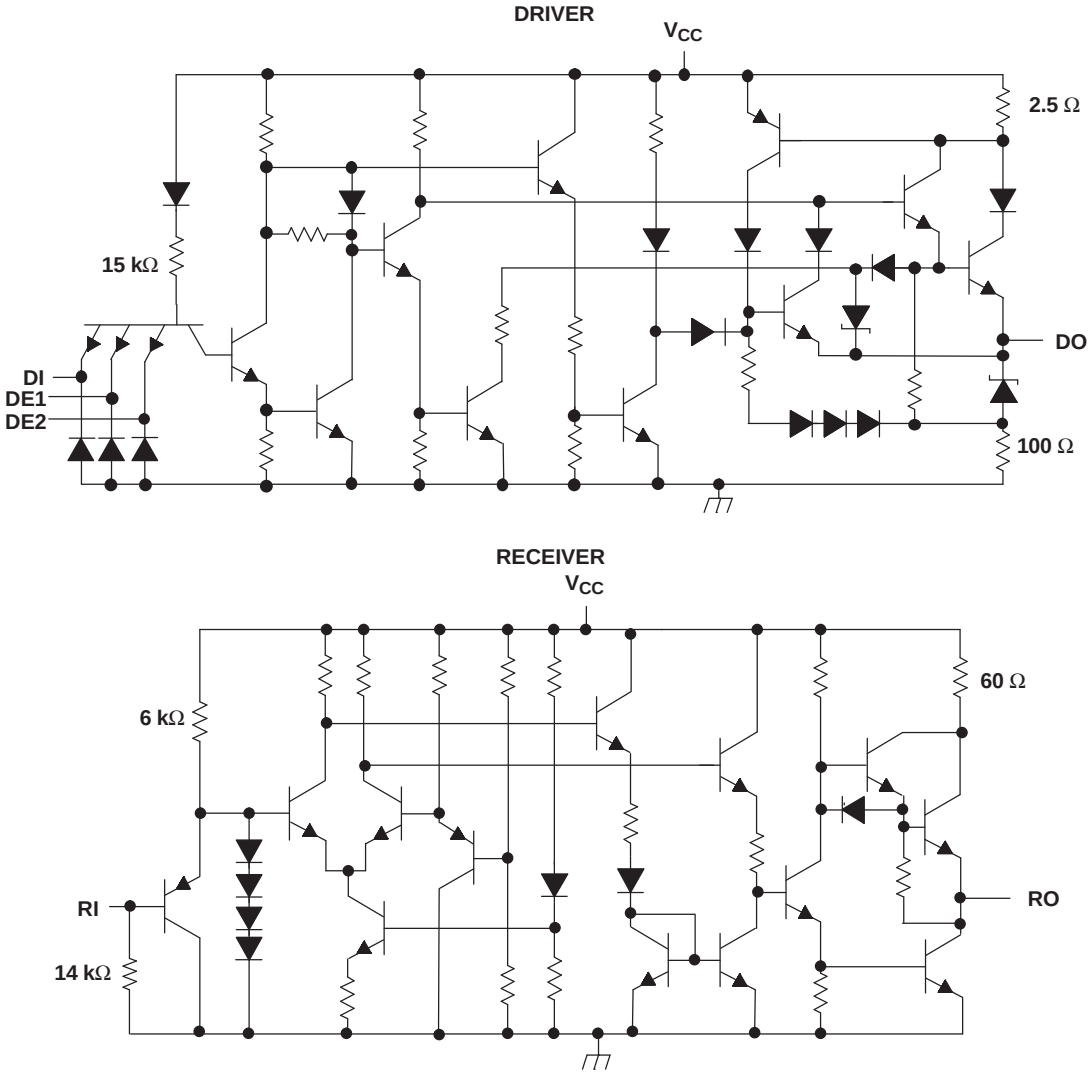
(1) H = high level, L = low level, X = irrelevant

### LOGIC DIAGRAM (POSITIVE LOGIC)




Pin numbers shown are for the D and N package only.

## EQUIVALENT SCHEMATICS OF DRIVER AND RECEIVER(1)




(1) All resistor values are nominal.

## Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage(2) | | | 7 | V |
| $V_I$ | Input voltage range | Driver | –0.5 | 7 | V |
| | | Receiver | –0.5 | 7 | V |
| $V_O$ | Output voltage range | Driver | –0.5 | 7 | V |
| | Enable input voltage range | | –0.5 | 7 | V |
| $\theta_{JA}$ | Package thermal impedance(3) | D package | | 73 | °C/W |
| | | DW package | | 58 | |
| | | N package | | 67 | |
| | | NS package | | 60 | |
| $T_J$ | Operating virtual junction temperature | | | 150 | °C |
| | Lead temperature 1,6 mm (1/16 inch) from case for 10 s | | | 260 | °C |
| $T_{stg}$ | Storage temperature range | | –65 | 150 | °C/W |

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.

## Recommended Operating Conditions

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 4.75 | 5 | 5.25 | V |
| $V_{IH}$ | High-level input voltage | Driver, Enable | 2 | | | V |
| | | Receiver | 1.55 | | | |
| $V_{IL}$ | Low-level input voltage | Driver, Enable | | | 0.8 | V |
| | | Receiver | | | 1.15 | |
| $T_A$ | Operating free-air temperature | | 0 | | 70 | °C |

## DRIVER SECTION

### Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IK}$ | Input clamp voltage | | $V_{CC}$ = 4.75 V, | $I_{IL}$ = –18 mA | | –1.5 | V |
| $V_{OH}$ | High–level output voltage | | $V_{CC}$ = 4.75 V, $I_{OH}$ = –59.3 mA | $V_{IH}$ = 2 V, $T_A$ = 25°C | 3.11 | | V |
| | | | $V_{CC}$ = 5.25 V, $I_{OH}$ = - 78.1 mA | $V_{IH}$ = 2 V, | | 4.1 | |
| | | | $V_{CC}$ = 4.75 V, $R_L$ = 51.4 Ω | $V_{IH}$ = 2 V, | 3.05 | | |
| | | | $V_{CC}$ = 5.25 V, $R_L$ = 56.9 Ω | $V_{IH}$ = 2 V, | | 4.2 | |
| $V_{ODH}$ | Differential high-level output voltage | | $R_L$ = 46.3 Ω or 56.9 Ω | | | 0.5 | V |
| $V_{OL}$ | Low-level output voltage | | $V_{CC}$ = 5.25 V, $V_{IL}$ = 0.8 V, $V_{IH}$ = 4.5 V | $I_{OL}$ = –0.24 mA | | 0.15 | V |
| | | | | $R_L$ = 56.9 Ω | | 0.15 | |
| $I_{IH}$ | High-level input current | DI | $V_{CC}$ = 5.25 V, | $V_{IH}$ = 2.7 V | | 20 | µA |
| | | DE | | | | 60 | |
| $I_{IL}$ | Low-level input current | DI | $V_{CC}$ = 5.25 V, | $V_{IH}$ = 0.4 V | | –400 | µA |
| | | DE | | | | –1200 | |
| $I_{OH}$ | High-level output current | | $V_{CC}$ = 4.75 V, $V_{OH}$ = 5 V | $V_{IL}$ = 0 | | 100 | µA |
| | | | | $V_{IH}$ = 4.5 V | | 100 | |
| $I_{OS}$ | Short-circuit output current(1) | | $V_{CC}$ = 5.25 V | $V_{IH}$ = 4.5 V | | –30 | mA |
| $I_{CCH}$ | Supply current (total package) | | $V_{CC}$ = 5.25 V, No load | $V_{I(D)}$ = 4.5 V, $V_{I(R)}$ = 0 | | 47 | mA |
| $I_{CCL}$ | | | | $V_{I(D)}$ = 0, $V_{I(R)}$ = 4.5 V | | 80 | |

(1) Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

### Switching Characteristics

$V_{CC}$ = 5 V + 5%, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay time, low- to high-level output | $R_L$ = 47.5 Ω, | See Figure 1 | 6.5 | 12 | 18.5 | ns |
| $t_{PHL}$ | Propagation delay time, high- to low-level output | | | 6.5 | 12 | 18.5 | ns |
| $\Delta t_{pd}$ | Differential propagation delay time(1) | | | | | 10 | ns |
| $t_r$ | Output rise time | $V_{CC}$ = 5 V, $R_L$ = 47.5 Ω, See Figure 1 | $V_O$ = 0.15 V to 3.05 V, $C_L$ = 10.2 pF, | 5 | 10 | | ns |
| $t_f$ | Output fall time | | | 5 | 13 | | ns |
| SR | Slew rate | $V_O$ = 1 V to 3 V average, $R_L$ = 47.5 Ω, See Figure 1 | $C_L$ = 10.2 pF, | | | 0.65 | V/ns |

(1) $\Delta t_{pd} = |t_{PLH} - t_{PHL}|$

## RECEIVER SECTION

### Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage | $V_{CC}$ = 4.75 V, $I_{OH}$ = –400 µA | $V_I$ = 1.15 V, | 2.7 | | V |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$ = 4.75 V, $V_{IH}$ = 1.55 V | $I_{OL}$ = 8 mA | | 0.5 | V |
| | | | $I_{OL}$ = 4 mA | | 0.4 | |
| $r_I$ | Input resistance | $V_{CC}$ = 0, | $V_I$ = 0.15 V to 3.9 V | 7.4 | 20 | kΩ |
| $I_{IH}$ | High-level input current | $V_{CC}$ = 4.75 V, | $V_{IH}$ = 3.11 V | | 0.42 | mA |
| $I_{IL}$ | Low-level input current | $V_{CC}$ = 5.25 V, | $V_{IL}$ = 0.15 V | –0.24 | 0.04 | mA |
| $I_{OS}$ (1) | Short-circuit output current | $V_{CC}$ = 5.25 V, | $V_{IL}$ = 0 | –20 | –100 | mA |
| $I_{CCH}$ | Supply current (total package) | $V_{CC}$ = 5.25 V, No load | $V_{I(D)}$ = 4.5 V, $V_{I(R)}$ = 0 | | 47 | mA |
| $I_{CCL}$ | | | $V_{I(D)}$ = 0, $V_{I(R)}$ = 4.5 V | | 80 | |

(1) Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

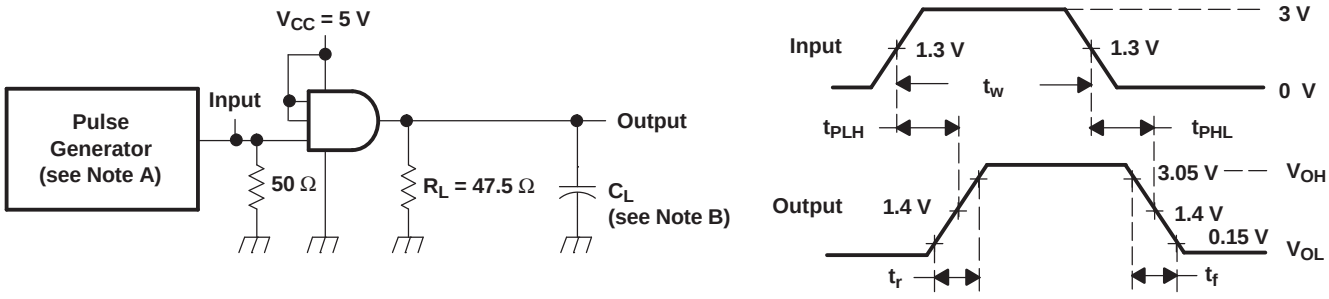
### Switching Characteristics

$V_{CC}$ = 5 V + 5%, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay time, low- to high-level output | $R_L$ = 2 kΩ, $C_L$ = 15 pF, See Figure 2 | 7.5 | 12 | 19.5 | ns |
| $t_{PHL}$ | Propagation delay time, high- to low-level output | | 7.5 | 12 | 19.5 | ns |
| $\Delta t_{pd}$ (1) | Differential propagation delay time | | | | 10 | ns |

(1) $\Delta t_{pd} = |t_{PLH} - t_{PHL}|$

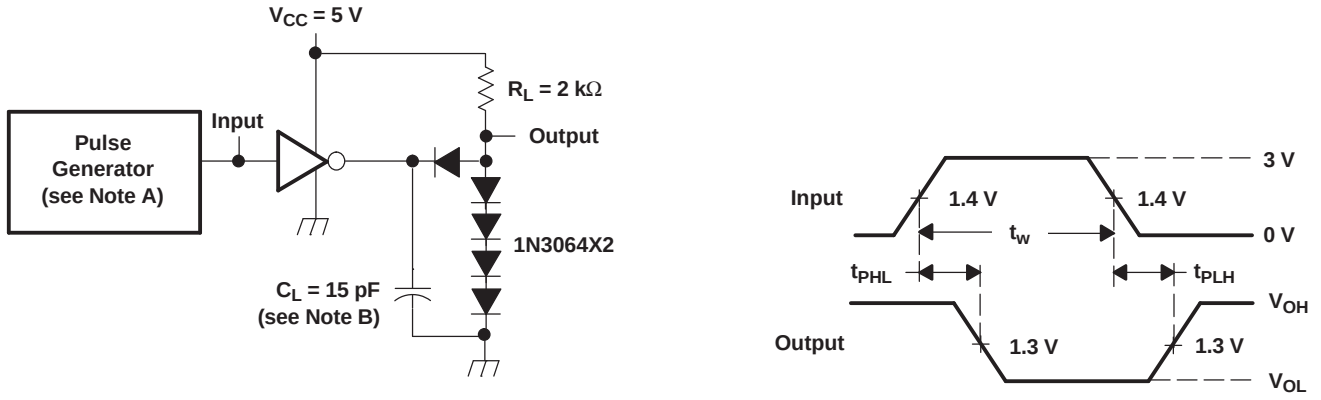
## PARAMETER MEASUREMENT INFORMATION




**TEST CIRCUIT** **VOLTAGE WAVEFORMS**

NOTES: A. The pulse generator has the following characteristics: $Z_O \approx 50\ \Omega$, $t_w \le 500$ ns, PRR ≤ 1 MHz, $t_f \le 6$ ns, $t_r \le 15$ ns.
B. $C_L$ includes probe and jig capacitance.

**Figure 1. Driver Test Circuit and Voltage Waveforms**




**TEST CIRCUIT** **VOLTAGE WAVEFORMS**

NOTES: A. The pulse generator has the following characteristics: $Z_O \approx 50\ \Omega$, $t_w \le 500$ ns, PRR ≤ 1 MHz, $t_f \le 10$ ns, $t_r \le 10$ ns.
B. $C_L$ includes probe and jig capacitance.

**Figure 2. Receiver Test Circuit and Voltage Waveforms**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SN751730D | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | SN751730 | Samples |
| SN751730DE4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | SN751730 | Samples |
| SN751730DWR | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | | SN751730 | Samples |
| SN751730N | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | 0 to 70 | SN751730N | Samples |
| SN751730PWR | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | | A1730 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

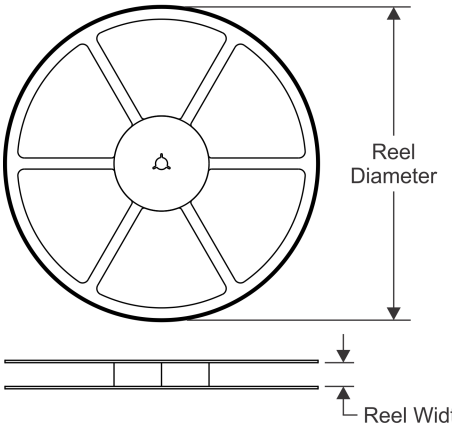
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

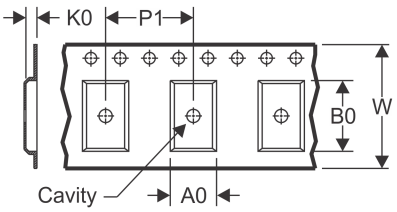
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

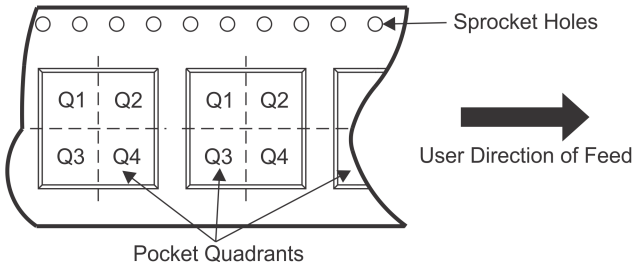



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

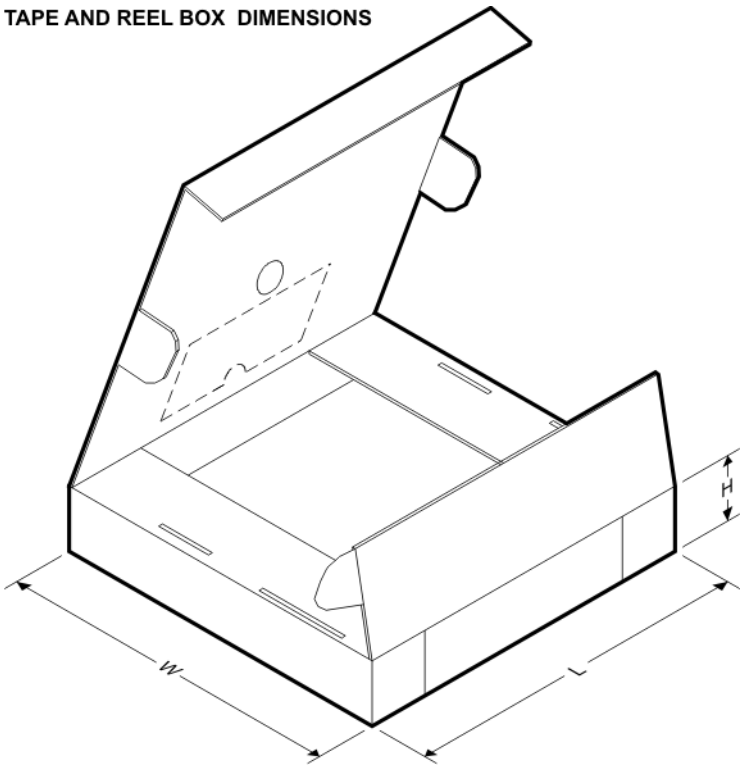
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN751730DWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |
| SN751730PWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



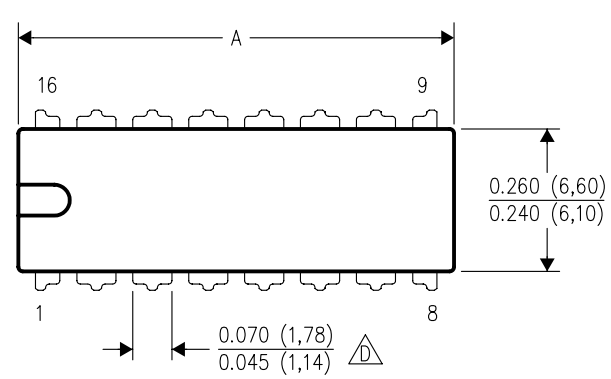

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN751730DWR | SOIC | DW | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| SN751730PWR | TSSOP | PW | 16 | 2000 | 367.0 | 367.0 | 35.0 |

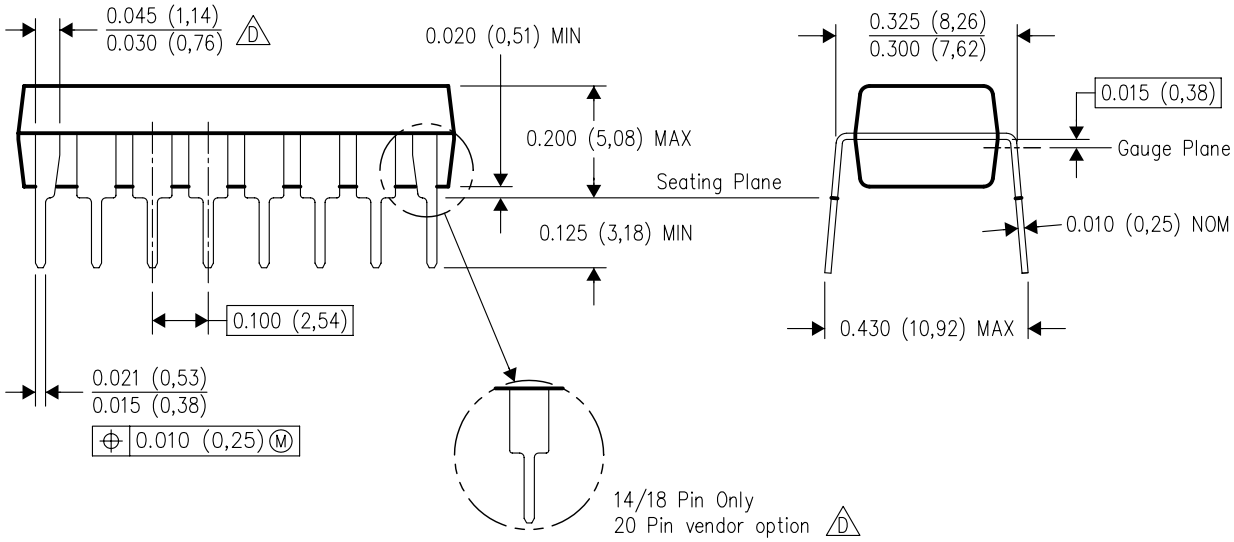
## N (R–PDIP–T**)

## PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |

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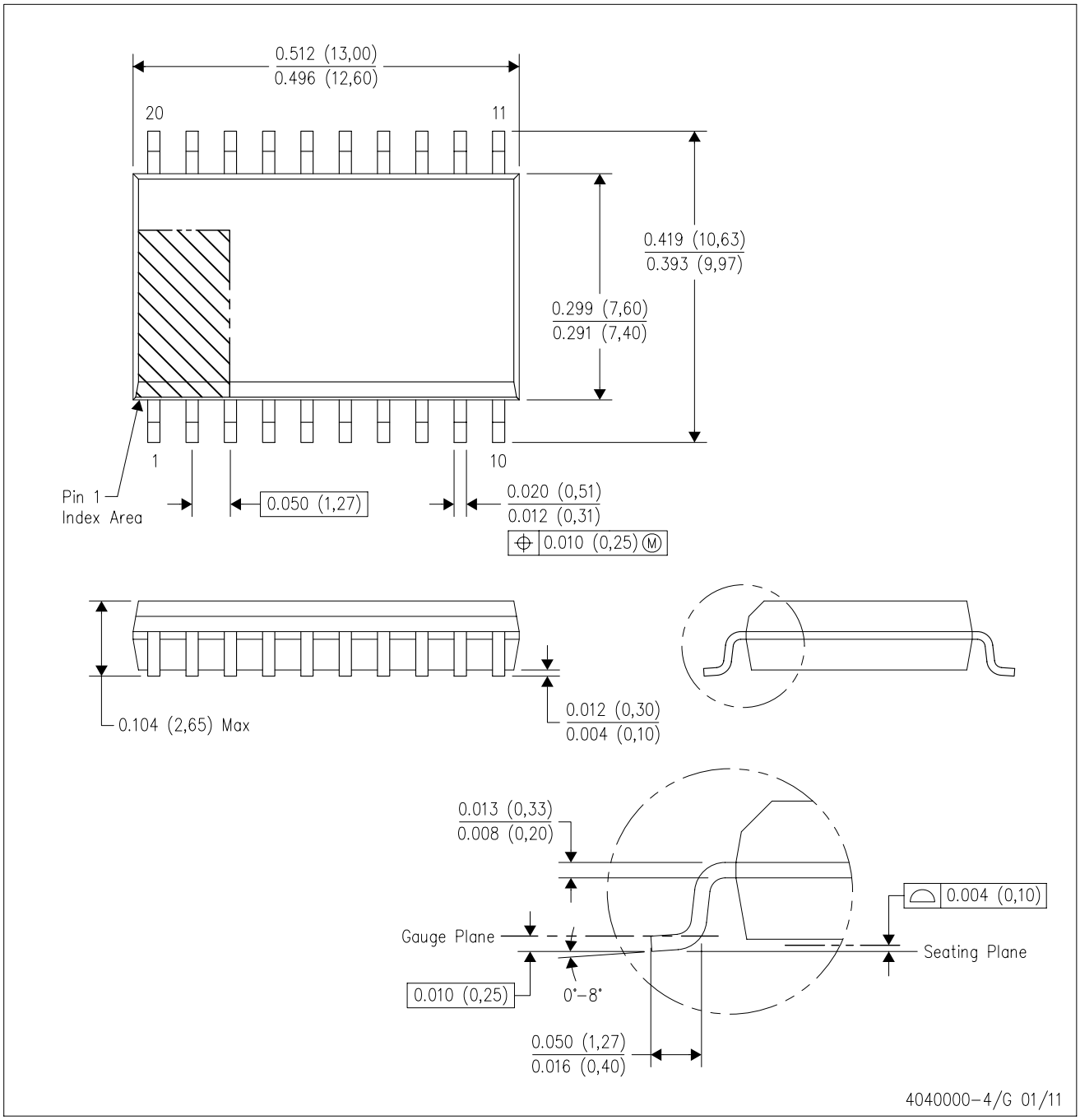
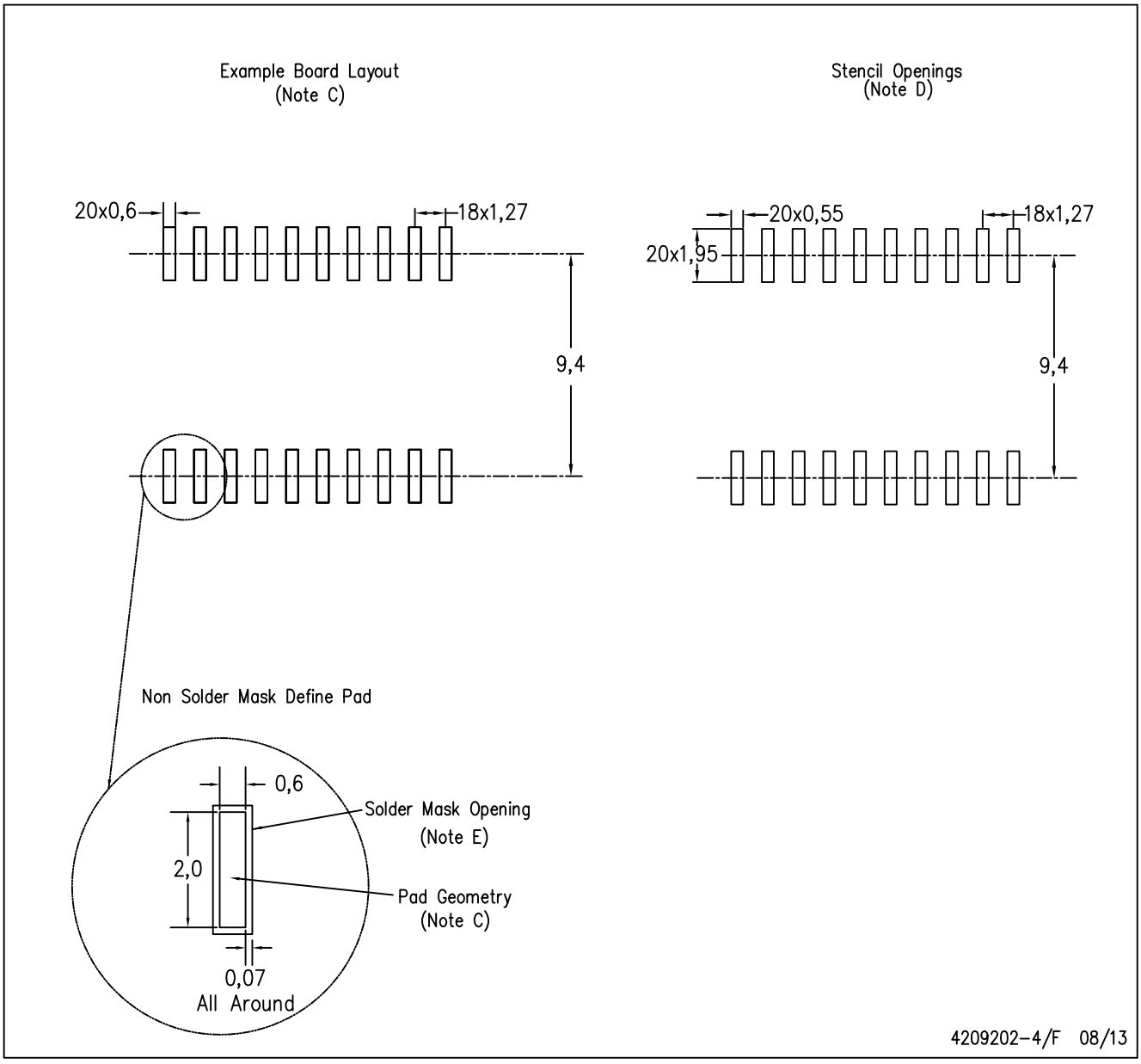
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW (R–PDSO–G20) PLASTIC SMALL OUTLINE



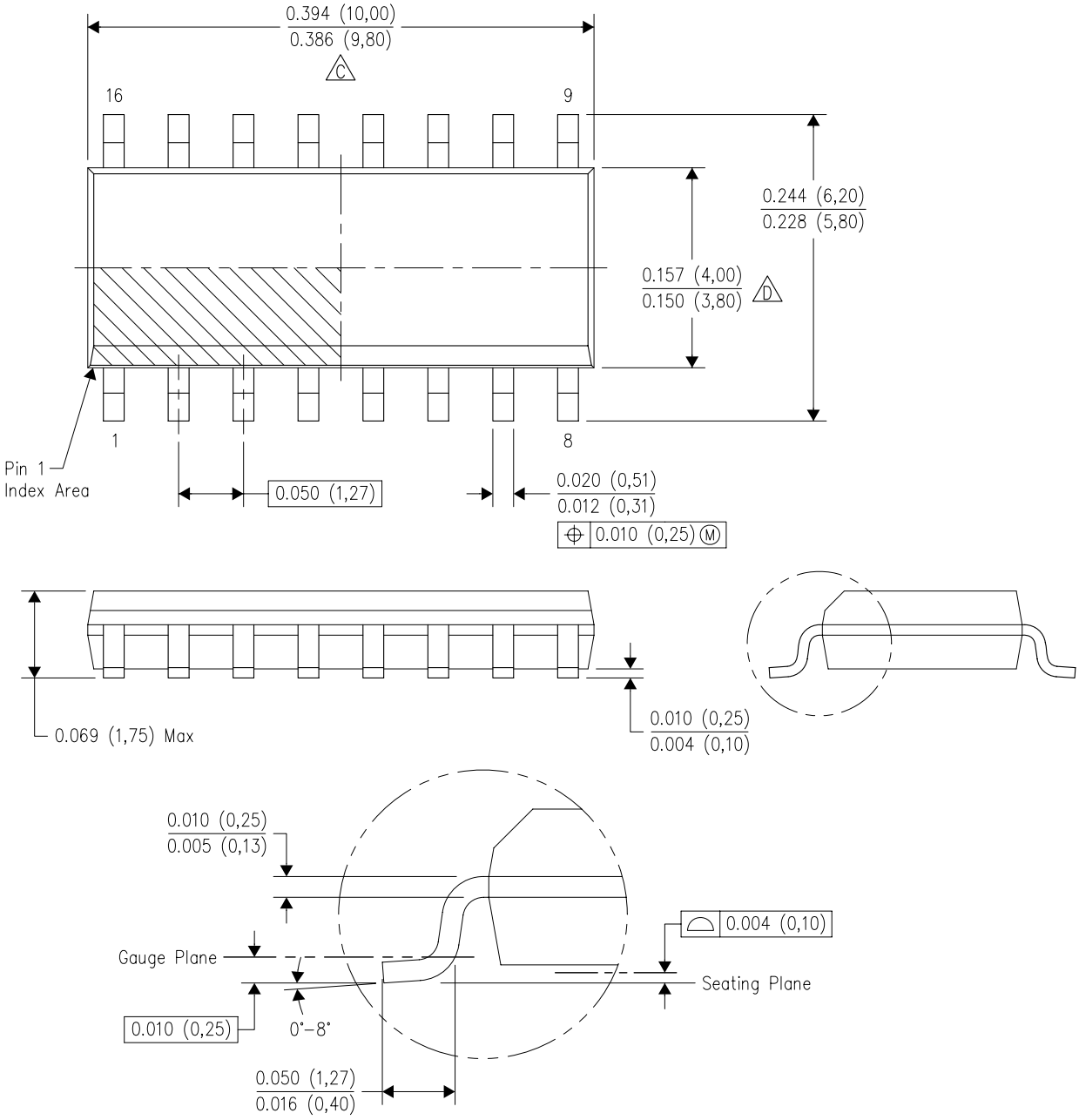

NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AC.

DW (R–PDSO–G20) PLASTIC SMALL OUTLINE



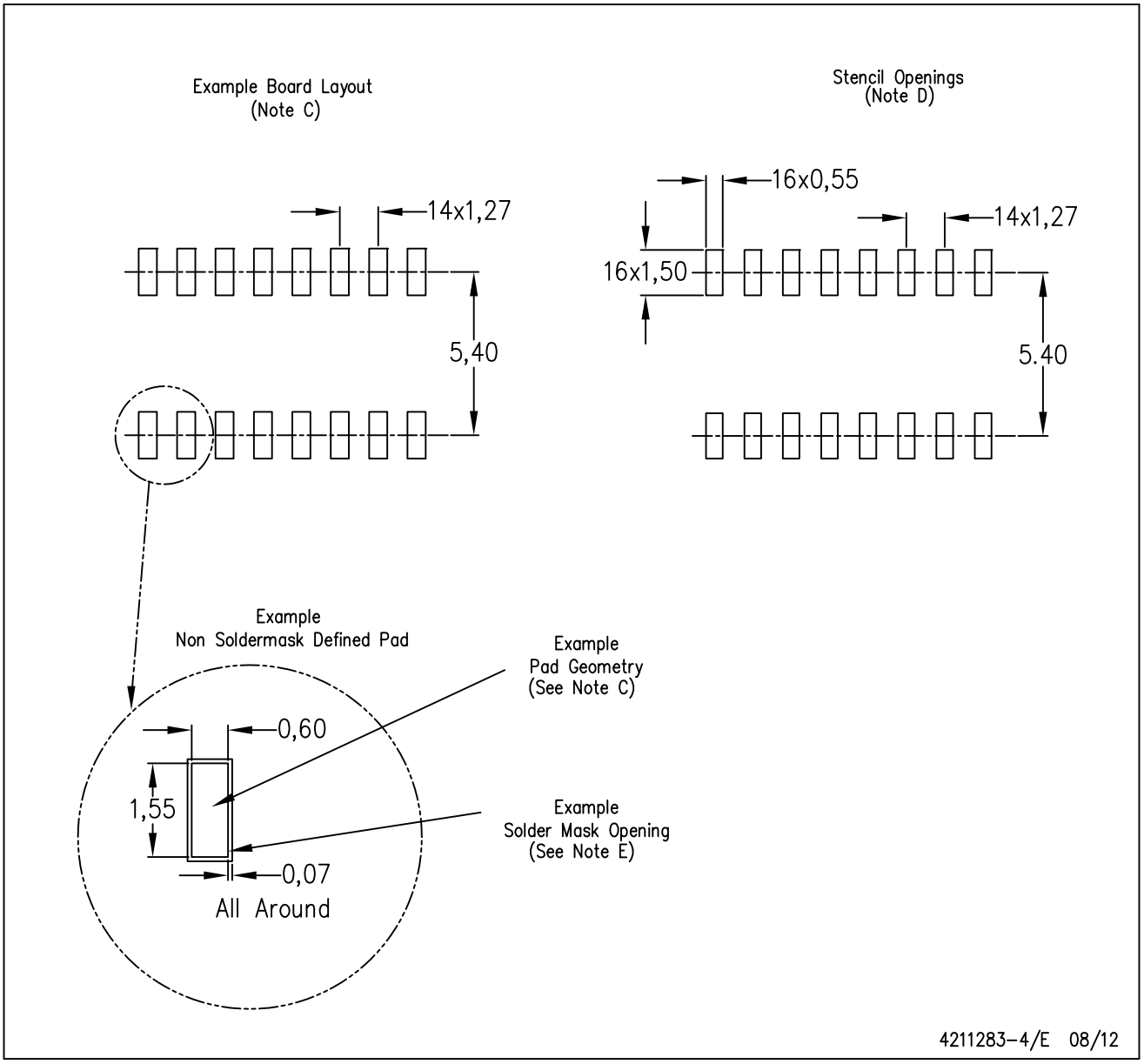

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Refer to IPC7351 for alternate board design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



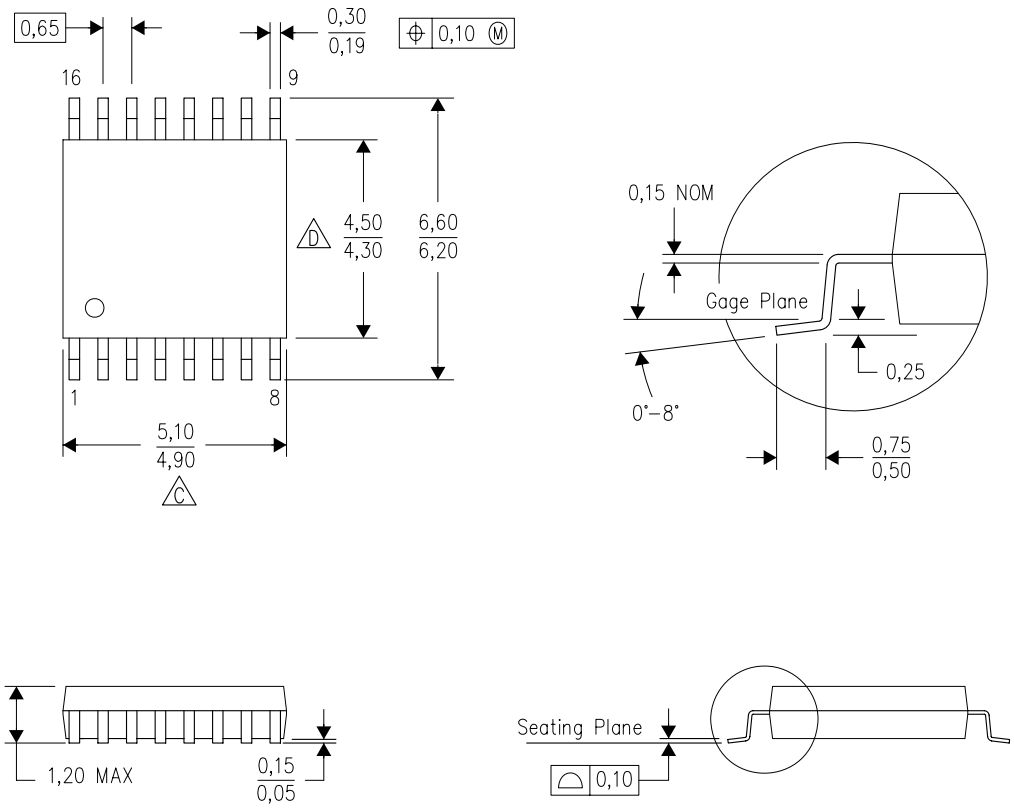

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

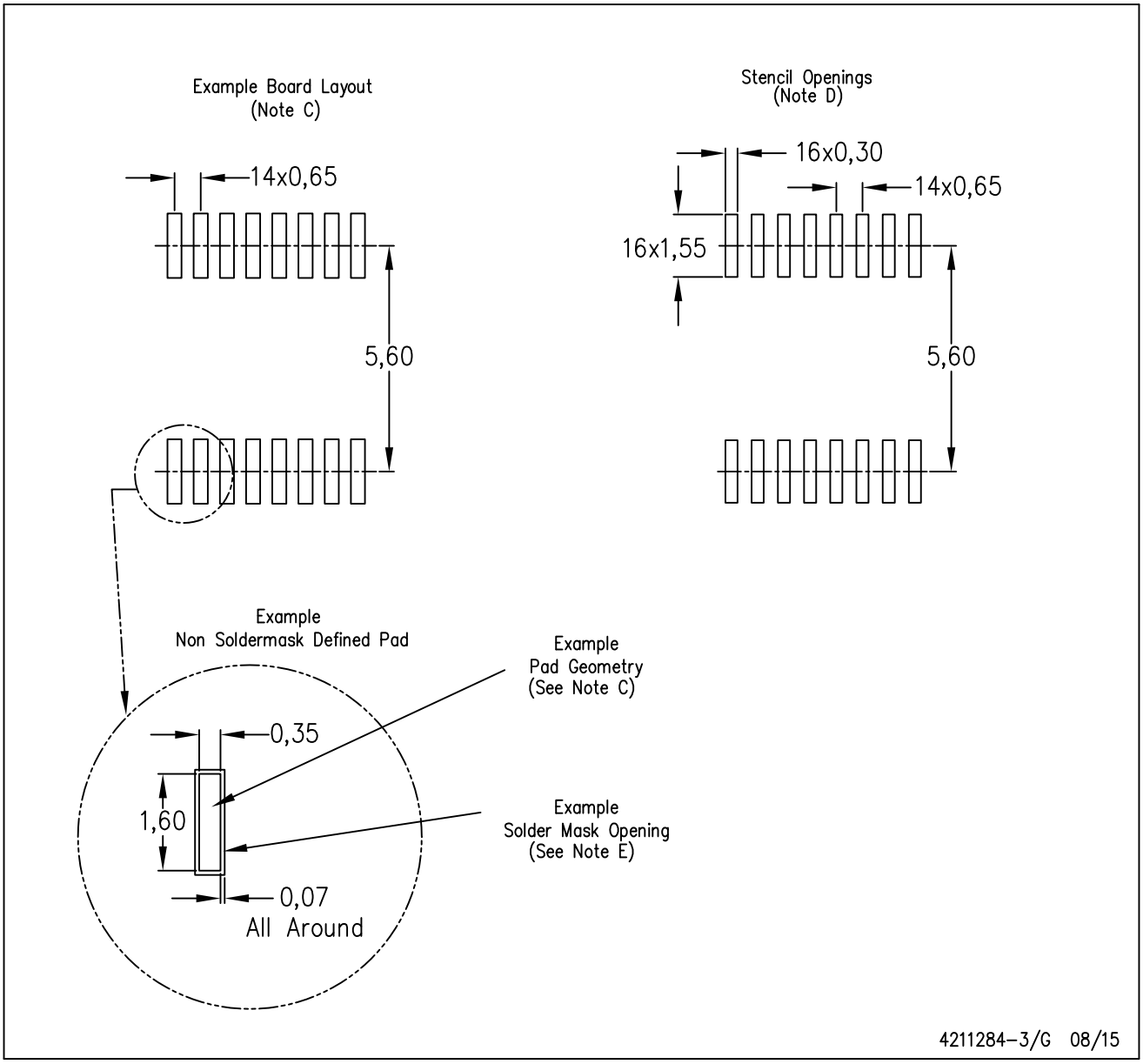
PW (R–PDSO–G16) PLASTIC SMALL OUTLINE




4040064–4/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G16) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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