



# STF12NK65Z

N-channel 650 V, 0.57  $\Omega$ , 10 A, TO-220FP  
Zener-protected SuperMESH™ Power MOSFET

## Features

| Order code | V <sub>DSS</sub> | R <sub>DS(on)</sub> max. | I <sub>D</sub> | P <sub>W</sub> |
|------------|------------------|--------------------------|----------------|----------------|
| STF12NK65Z | 650 V            | < 0.7 $\Omega$           | 10 A           | 35 W           |

- Extremely high dv/dt capability
- 100% avalanche tested
- Gate charge minimized
- Very low intrinsic capacitance
- Very good manufacturing repeatability

## Application

Switching applications

## Description

This N-channel SuperMESH™ Power MOSFET is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications. Such series complements ST full range of high voltage Power MOSFETs including revolutionary MDmesh™ products.

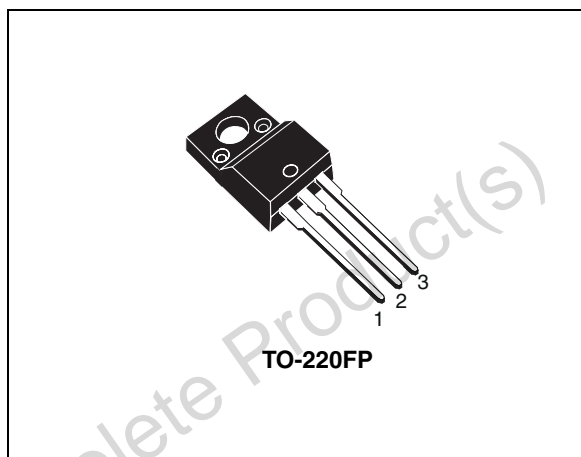


Figure 1. Internal schematic diagram

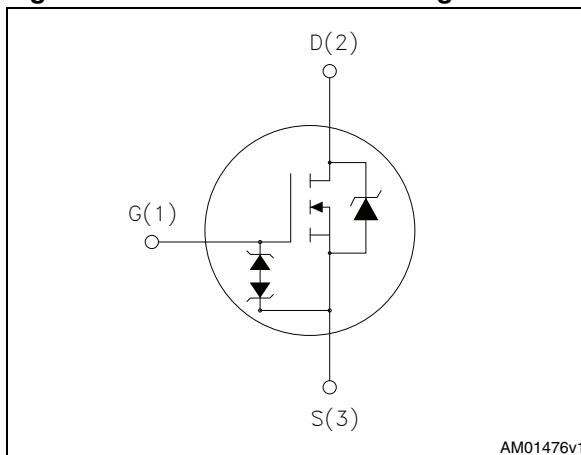


Table 1. Device summary

| Order code | Marking | Package  | Packaging |
|------------|---------|----------|-----------|
| STF12NK65Z | 12NK65Z | TO-220FP | Tube      |

# Contents

|          |   |           |
|----------|---|-----------|
| <b>1</b> | <b>Electrical ratings</b> .....           | <b>3</b>  |
| <b>2</b> | <b>Electrical characteristics</b> .....   | <b>4</b>  |
| 2.1      | Electrical characteristics (curves) ..... | 6         |
| <b>3</b> | <b>Test circuits</b> .....                | <b>8</b>  |
| <b>4</b> | <b>Package mechanical data</b> .....      | <b>9</b>  |
| <b>5</b> | <b>Revision history</b> .....             | <b>11</b> |

Obsolete Product(s) - Obsolete Product(s)

# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

| Symbol         | Parameter   | Value       | Unit |
|----------------|---|-------------|------|
| $V_{DS}$       | Drain-source voltage ( $V_{GS} = 0$ )   | 650         | V    |
| $V_{GS}$       | Gate- source voltage  | $\pm 30$    | V    |
| $I_D$          | Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$  | 10          | A    |
| $I_D$          | Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$   | 6.3         | A    |
| $I_{DM}^{(1)}$ | Drain current (pulsed)  | 40          | A    |
| $P_{TOT}$      | Total dissipation at $T_C = 25\text{ }^\circ\text{C}$   | 35          | W    |
|                | Derating factor   | 1.2         | W/°C |
| $V_{ISO}$      | Insulation withstand voltage (RMS) from all three leads to external heat sink ( $t = 1\text{ s}$ ; $T_C = 25\text{ }^\circ\text{C}$ ) | 2500        | V    |
| $dv/dt^{(2)}$  | Peak diode recovery voltage slope   | 4.5         | V/ns |
| $T_{stg}$      | Storage temperature   | - 55 to 150 | °C   |
| $T_j$          | Max operating junction temperature  | 150         | °C   |

1. Pulse width limited by safe operating area

2.  $I_{SD} \leq 10\text{ A}$ ,  $di/dt \leq 200\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  $T_j \leq T_{JMAX}$ .

**Table 3. Thermal data**

| Symbol         | Parameter                                      | Value | Unit |
|----------------|--|-------|------|
| $R_{thj-case}$ | Thermal resistance junction-case max           | 3.6   | °C/W |
| $R_{thj-amb}$  | Thermal resistance junction-ambient max        | 62.5  | °C/W |
| $T_l$          | Maximum lead temperature for soldering purpose | 300   | °C   |

**Table 4. Avalanche characteristics**

| Symbol   | Parameter  | Value | Unit |
|----------|--|-------|------|
| $I_{AR}$ | Avalanche current, repetitive or not-repetitive (pulse width limited by $T_j$ Max)                             | 10    | A    |
| $E_{AS}$ | Single pulse avalanche energy (starting $T_j=25\text{ }^\circ\text{C}$ , $I_D=I_{AR}$ , $V_{DD}=50\text{ V}$ ) | 225   | mJ   |

## 2 Electrical characteristics

( $T_{CASE} = 25\text{ °C}$  unless otherwise specified)

**Table 5. On/off states**

| Symbol        | Parameter  | Test conditions  | Min. | Typ. | Max.     | Unit                           |
|---------------|--|--|------|------|----------|--------------------------------|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage                   | $I_D = 1\text{ mA}$ , $V_{GS} = 0$   | 650  |      |          | V                              |
| $I_{DSS}$     | Zero gate voltage drain current ( $V_{GS} = 0$ ) | $V_{DS} = \text{max rating}$<br>$V_{DS} = \text{max rating}$ , $T_C = 125\text{ °C}$ |      |      | 1<br>50  | $\mu\text{A}$<br>$\mu\text{A}$ |
| $I_{GSS}$     | Gate-body leakage current ( $V_{DS} = 0$ )       | $V_{GS} = \pm 20\text{ V}$   |      |      | $\pm 10$ | $\mu\text{A}$                  |
| $V_{GS(th)}$  | Gate threshold voltage                           | $V_{DS} = V_{GS}$ , $I_D = 100\text{ }\mu\text{A}$                                   | 3    | 3.75 | 4.5      | V                              |
| $R_{DS(on)}$  | Static drain-source on resistance                | $V_{GS} = 10\text{ V}$ , $I_D = 10\text{ A}$   |      | 0.57 | 0.7      | $\Omega$                       |

**Table 6. Dynamic**

| Symbol                     | Parameter                     | Test conditions  | Min. | Typ. | Max. | Unit     |
|----------------------------|-------------------------------|--|------|------|------|----------|
| $g_{fs}^{(1)}$             | Forward transconductance      | $V_{DS} = 15\text{ V}$ , $I_D = 5\text{ A}$  | -    | 9.5  | -    | S        |
| $C_{iss}$                  | Input capacitance             | $V_{DS} = 25\text{ V}$ , $f = 1\text{ MHz}$ ,<br>$V_{GS} = 0$  | -    | 1837 | -    | pF       |
| $C_{oss}$                  | Output capacitance            |  |      | 208  |      | pF       |
| $C_{rss}$                  | Reverse transfer capacitance  |  |      | 48.8 |      | pF       |
| $C_{oss\text{ eq.}}^{(2)}$ | Equivalent output capacitance | $V_{DS} = 0$ , $V_{DS} = 0$ to $520\text{ V}$  | -    | 122  | -    | pF       |
| $t_{d(on)}$                | Turn-on delay time            | $V_{DD} = 325\text{ V}$ , $I_D = 5\text{ A}$ ,<br>$R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$<br>(see <a href="#">Figure 14</a> ) | -    | 25   | -    | ns       |
| $t_r$                      | Rise time                     |  |      | 14   |      | ns       |
| $t_{d(off)}$               | Turn-off delay time           |  |      | 55   |      | ns       |
| $t_f$                      | Fall time                     |  |      | 11.5 |      | ns       |
| $Q_g$                      | Total gate charge             | $V_{DD} = 520\text{ V}$ , $I_D = 10\text{ A}$ ,<br>$V_{GS} = 10\text{ V}$<br>(see <a href="#">Figure 15</a> )                            | -    | 62.6 | -    | nC       |
| $Q_{gs}$                   | Gate-source charge            |  |      | 9.6  |      | nC       |
| $Q_{gd}$                   | Gate-drain charge             |  |      | 36   |      | nC       |
| $R_G$                      | Intrinsic gate resistance     | $f = 1\text{ MHz}$ open drain  | -    | 1    | -    | $\Omega$ |

1. Pulsed: pulse duration=300 $\mu\text{s}$ , duty cycle 1.5%

2.  $C_{oss\text{ eq.}}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$ .

**Table 7. Source drain diode**

| Symbol          | Parameter                     | Test conditions  | Min. | Typ. | Max. | Unit          |
|-----------------|-------------------------------|--|------|------|------|---------------|
| $I_{SD}$        | Source-drain current          |  | -    |      | 10   | A             |
| $I_{SDM}^{(1)}$ | Source-drain current (pulsed) |  | -    |      | 38   | A             |
| $V_{SD}^{(2)}$  | Forward on voltage            | $I_{SD} = 10 \text{ A}$ , $V_{GS} = 0$   | -    |      | 1.6  | V             |
| $t_{rr}$        | Reverse recovery time         | $I_{SD} = 10 \text{ A}$ ,<br>$di/dt = 100 \text{ A}/\mu\text{s}$<br>$V_{DD} = 60 \text{ V}$<br>(see <a href="#">Figure 16</a> )                                      | -    | 436  |      | ns            |
| $Q_{rr}$        | Reverse Recovery Charge       |  |      | 3.4  |      | $\mu\text{C}$ |
| $I_{RRM}$       | Reverse Recovery Current      |  |      | 15.4 |      | A             |
| $t_{rr}$        | Reverse recovery time         | $I_{SD} = 10 \text{ A}$ ,<br>$di/dt = 100 \text{ A}/\mu\text{s}$<br>$V_{DD} = 60 \text{ V}$ , $T_J = 150 \text{ }^\circ\text{C}$<br>(see <a href="#">Figure 16</a> ) | -    | 518  |      | ns            |
| $Q_{rr}$        | Reverse recovery charge       |  |      | 4.1  |      | $\mu\text{C}$ |
| $I_{RRM}$       | Reverse recovery current      |  |      | 15.9 |      | A             |

1. Pulsed: pulse duration=300 $\mu\text{s}$ , duty cycle 1.5%
2. Pulse width limited by safe operating area

**Table 8. Gate-source Zener diode**

| Symbol           | Parameter                     | Test conditions                          | Min. | Typ. | Max. | Unit |
|------------------|-------------------------------|--|------|------|------|------|
| $BV_{GSO}^{(1)}$ | Gate-source breakdown voltage | $I_{GS} = \pm 1 \text{ mA}$ (open drain) | 30   |      | -    | V    |

1. The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

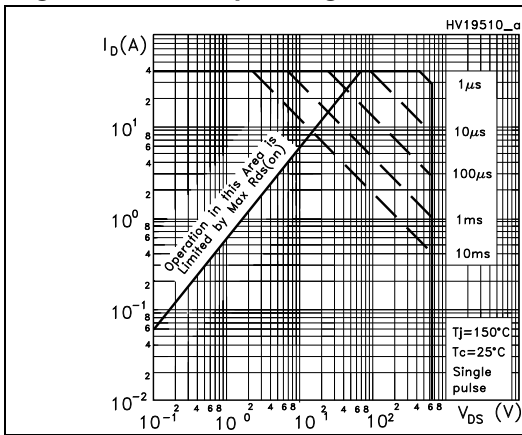


Figure 3. Thermal impedance

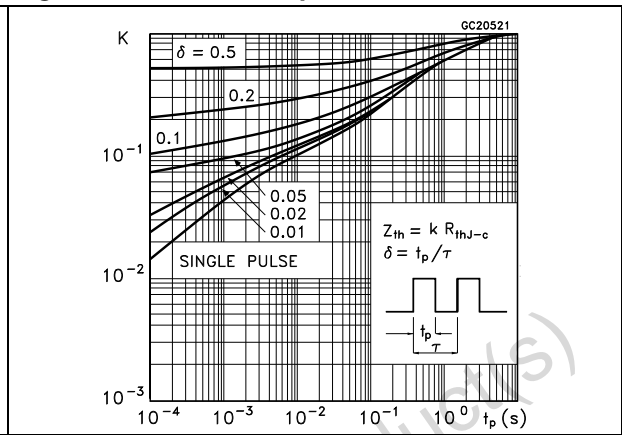


Figure 4. Output characteristics

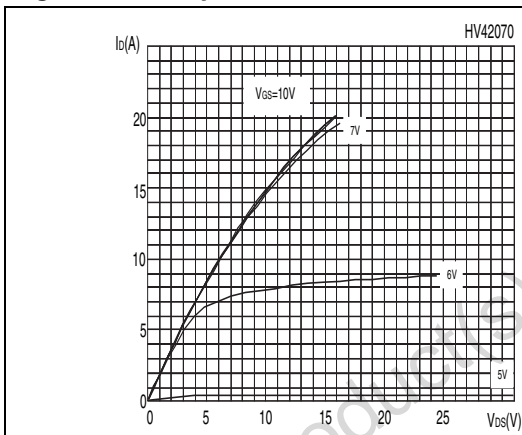


Figure 5. Transfer characteristics

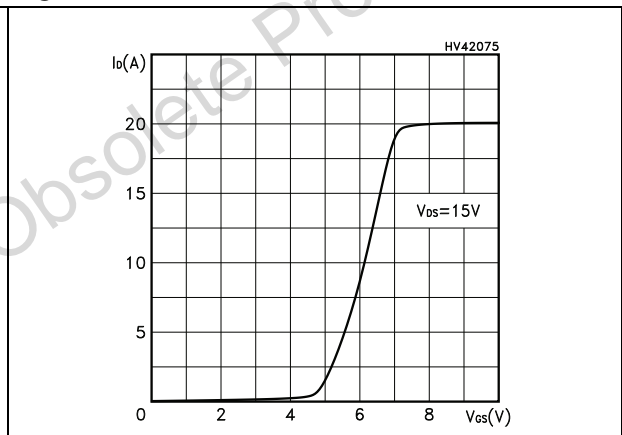


Figure 6. Normalized  $B_{V_{DS}}$  vs temperature

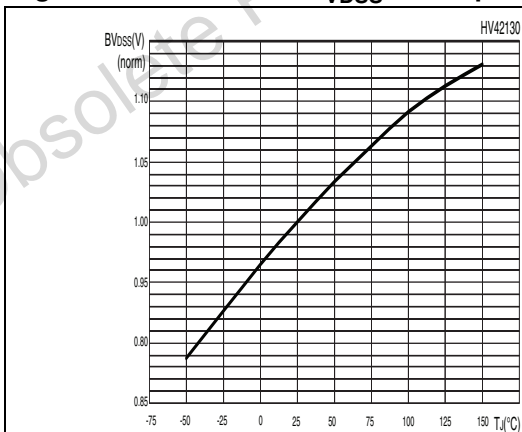


Figure 7. Static drain-source on resistance

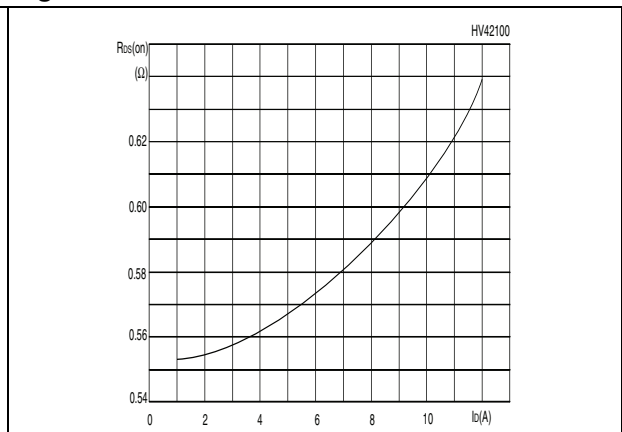


Figure 8. Gate charge vs. gate-source voltage Figure 9. Capacitance variations

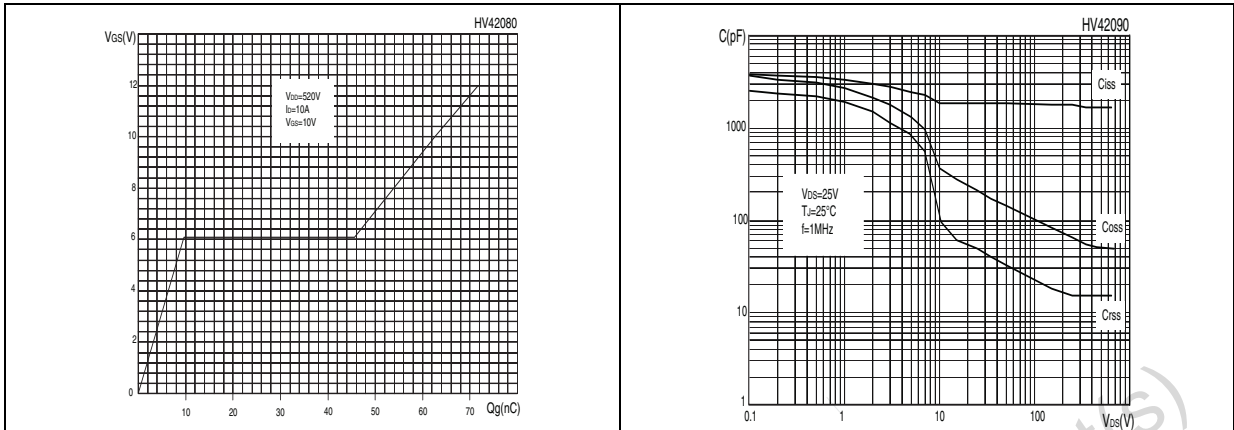


Figure 10. Normalized gate threshold voltage vs temperature

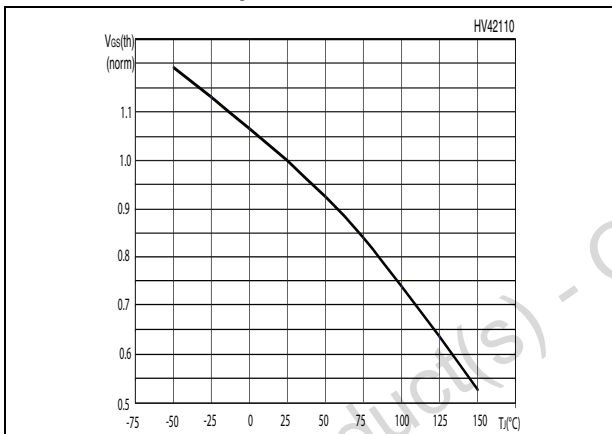


Figure 11. Normalized on resistance vs temperature

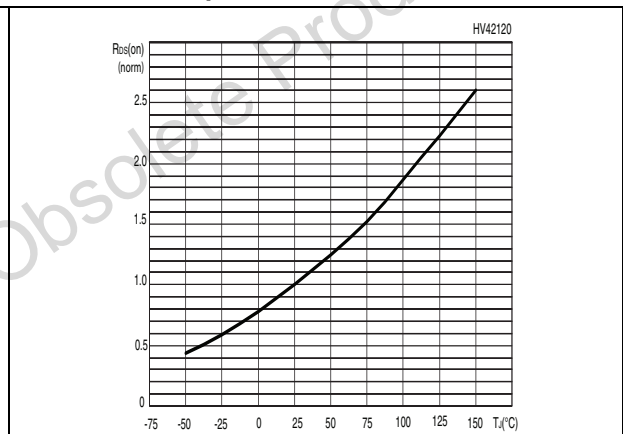


Figure 12. Maximum avalanche energy vs temperature

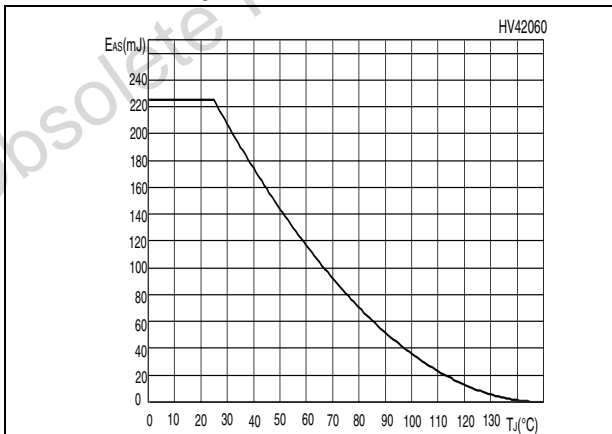
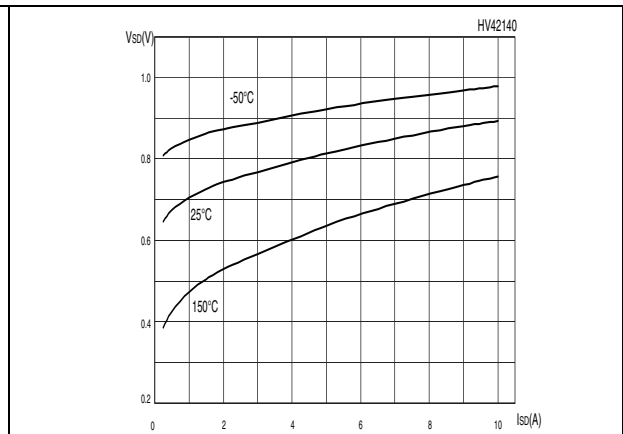
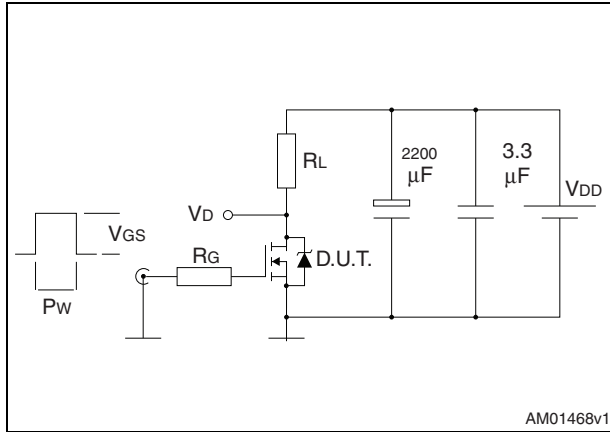


Figure 13. Source-drain diode forward characteristic

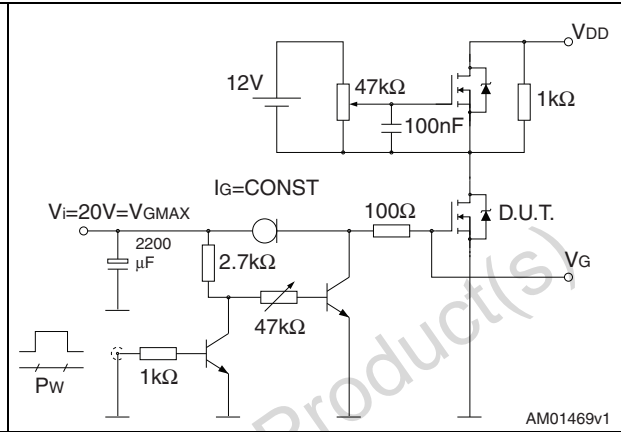


### 3 Test circuits

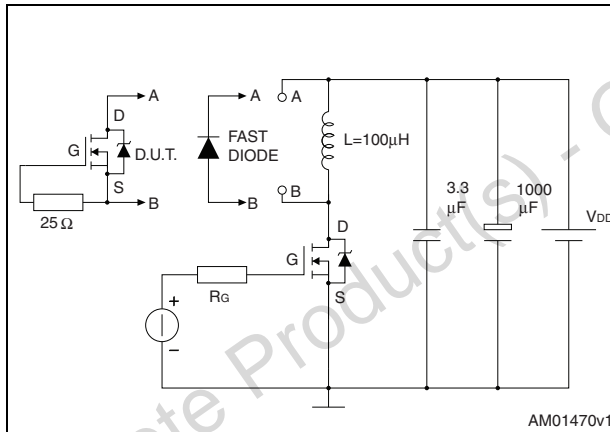
**Figure 14. Switching times test circuit for resistive load**



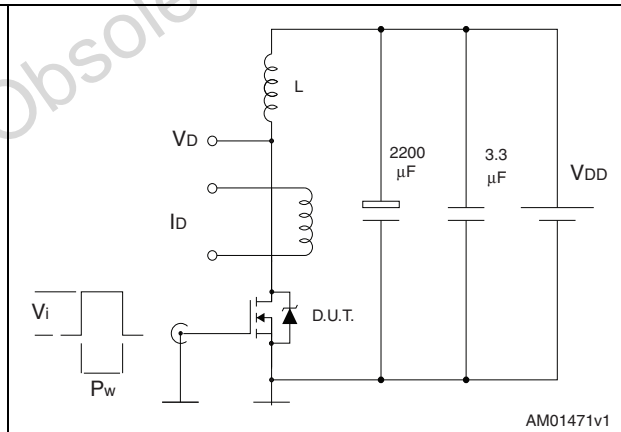
**Figure 15. Gate charge test circuit**



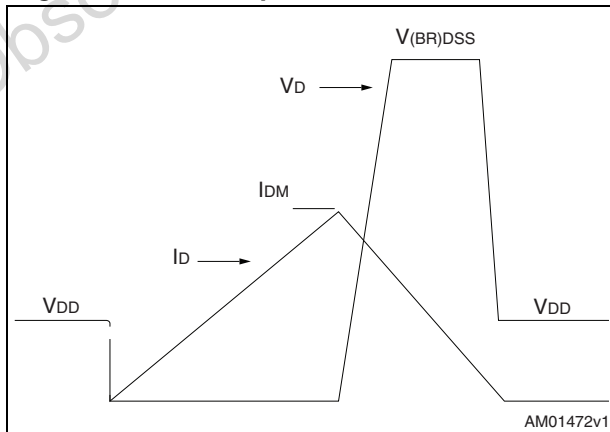
**Figure 16. Test circuit for inductive load switching and diode recovery times**



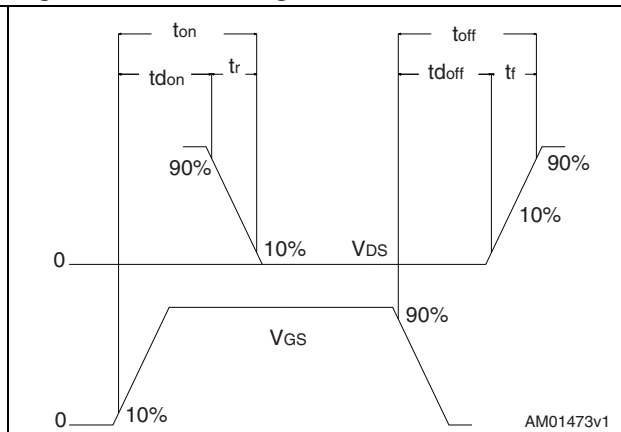
**Figure 17. Unclamped inductive load test circuit**



**Figure 18. Unclamped inductive waveform**



**Figure 19. Switching time waveform**



## 4 Package mechanical data

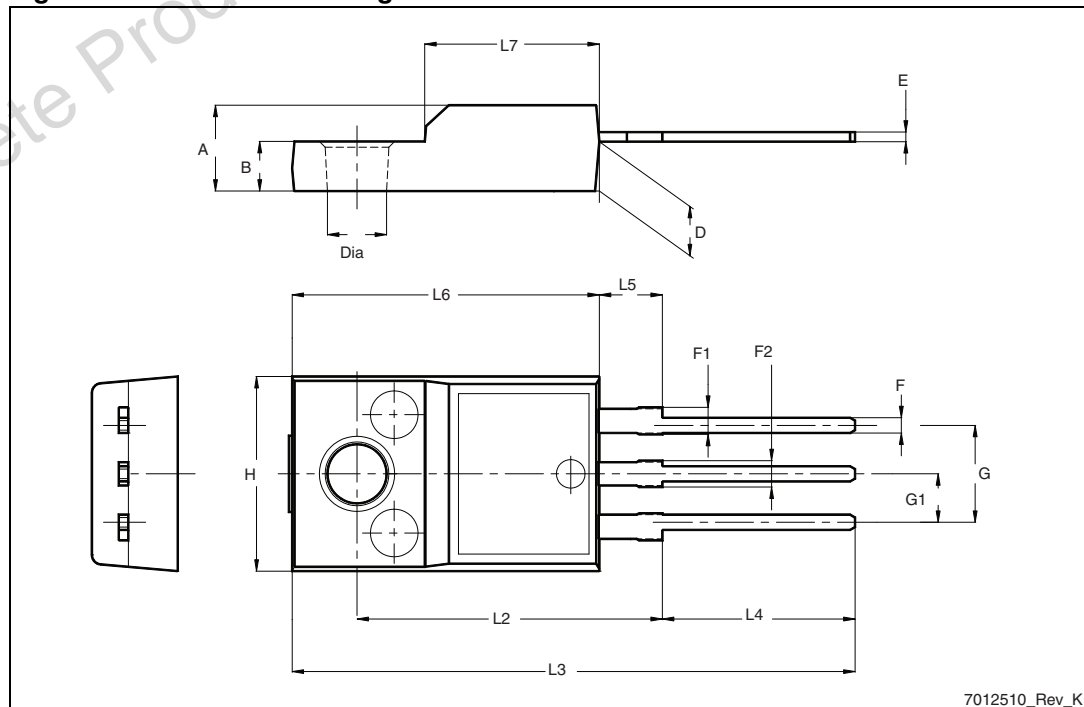
In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

Obsolete Product(s) - Obsolete Product(s)

Table 9. TO-220FP mechanical data

| Dim. | mm   |      |      |
|------|------|------|------|
|      | Min. | Typ. | Max. |
| A    | 4.4  |      | 4.6  |
| B    | 2.5  |      | 2.7  |
| D    | 2.5  |      | 2.75 |
| E    | 0.45 |      | 0.7  |
| F    | 0.75 |      | 1    |
| F1   | 1.15 |      | 1.70 |
| F2   | 1.15 |      | 1.70 |
| G    | 4.95 |      | 5.2  |
| G1   | 2.4  |      | 2.7  |
| H    | 10   |      | 10.4 |
| L2   |      | 16   |      |
| L3   | 28.6 |      | 30.6 |
| L4   | 9.8  |      | 10.6 |
| L5   | 2.9  |      | 3.6  |
| L6   | 15.9 |      | 16.4 |
| L7   | 9    |      | 9.3  |
| Dia  | 3    |      | 3.2  |

Figure 20. TO-220FP drawing



7012510\_Rev\_K

## 5 Revision history

Table 10. Document revision history

| Date        | Revision | Changes         |
|-------------|----------|-----------------|
| 01-Oct-2010 | 1        | Initial release |

Obsolete Product(s) - Obsolete Product(s)

**Please Read Carefully:**

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST's terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

**UNLESS OTHERWISE SET FORTH IN ST'S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.**

**UNLESS EXPRESSLY APPROVED IN WRITING BY AN AUTHORIZED ST REPRESENTATIVE, ST PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE. ST PRODUCTS WHICH ARE NOT SPECIFIED AS "AUTOMOTIVE GRADE" MAY ONLY BE USED IN AUTOMOTIVE APPLICATIONS AT USER'S OWN RISK.**

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2010 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

[www.st.com](http://www.st.com)