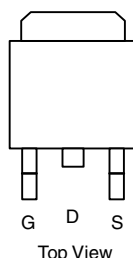


N-Channel 30 V (D-S) MOSFET

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A) ^{a, e}	Q_g (Typ.)
30	0.0022 at $V_{GS} = 10$ V	90	82 nC
	0.0027 at $V_{GS} = 4.5$ V	90	

TO-263



Ordering Information: SUM90N03-2m2P-E3 (Lead (Pb)-free)

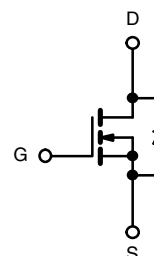
FEATURES

- TrenchFET[®] Power MOSFET
- 100 % R_g and UIS Tested
- Material categorization:
For definitions of compliance please see www.vishay.com/doc?99912


RoHS
COMPLIANT

APPLICATIONS

- OR-ing
- Server



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ($T_J = 175$ °C)	I_D	$T_C = 25$ °C	A
		$T_C = 70$ °C	
		$T_A = 25$ °C	
		$T_A = 70$ °C	
Pulsed Drain Current	I_{DM}	200	mJ
Avalanche Current Pulse	I_{AS}	36	
Single Pulse Avalanche Energy	E_{AS}	64.8	
Continuous Source-Drain Diode Current	I_S	$T_C = 25$ °C	A
		$T_A = 25$ °C	
Maximum Power Dissipation	P_D	$T_C = 25$ °C	W
		$T_C = 70$ °C	
		$T_A = 25$ °C	
		$T_A = 70$ °C	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 175	°C

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{b, d}	R_{thJA}	32	40	°C/W
Maximum Junction-to-Case	R_{thJC}	0.5	0.6	

Notes:

a. Based on $T_C = 25$ °C.

b. Surface mounted on 1" x 1" FR4 board.

c. $t = 10$ s.

d. Maximum under steady state conditions is 90 °C/W.

e. Calculated based on maximum junction temperature. Package limitation current is 90 A.

SPECIFICATIONS ($T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

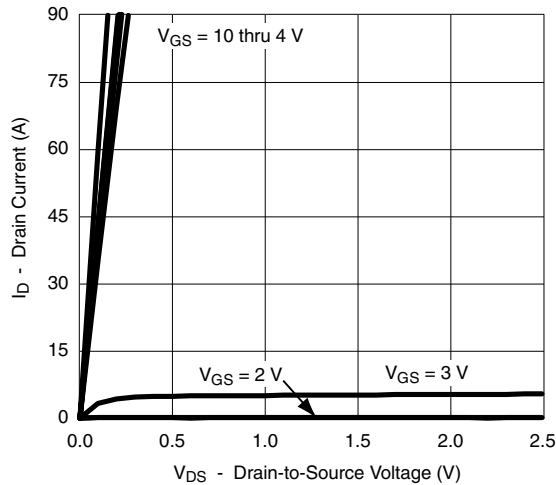
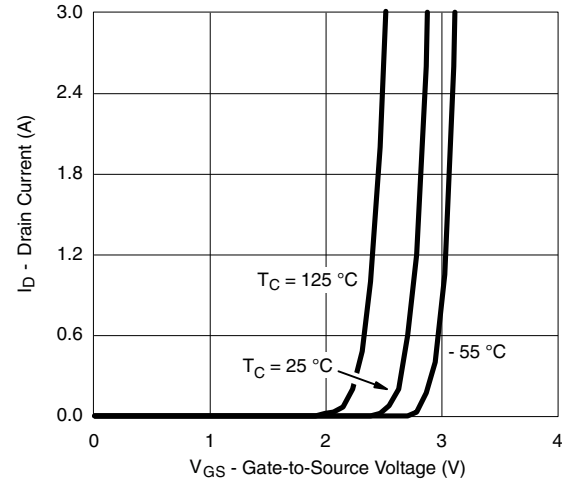
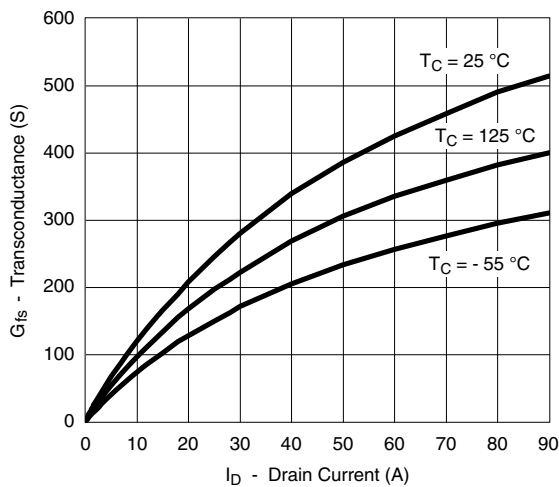
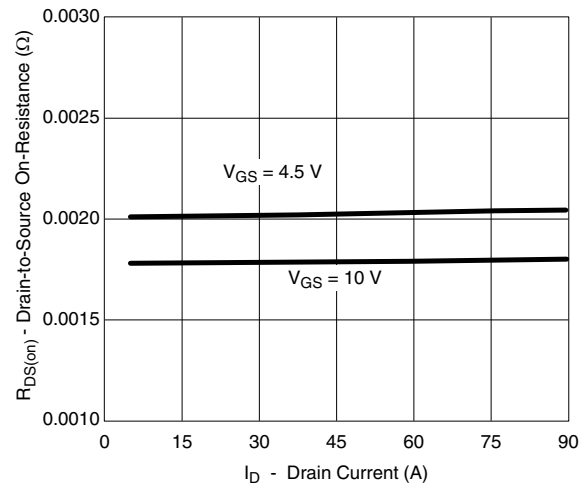
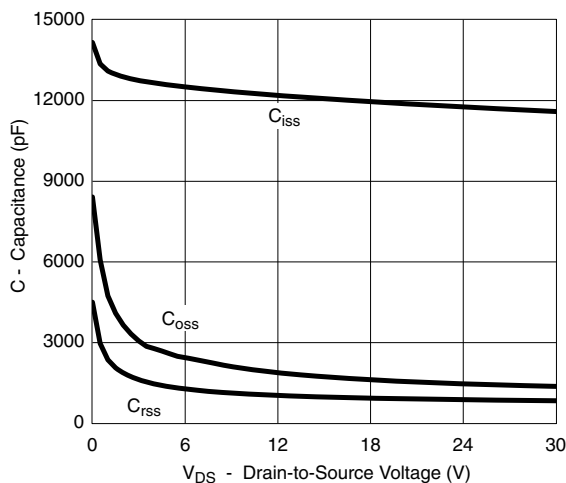
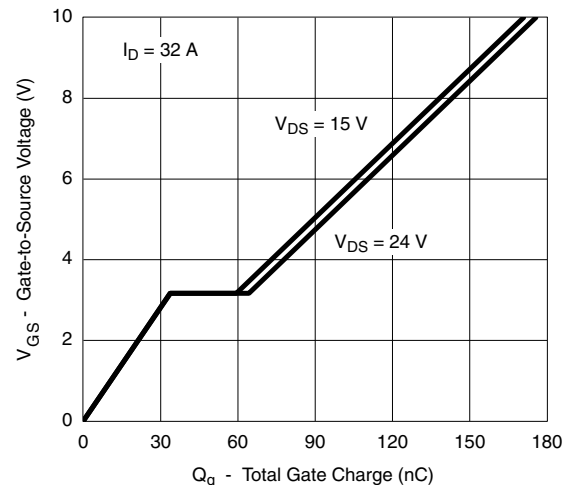
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$	30			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\text{ }\mu\text{A}$		35		mV/ $^{\circ}\text{C}$
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			- 7.5		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	1.5		2.5	V
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 20\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 30\text{ V}$, $V_{GS} = 0\text{ V}$			1	μA
		$V_{DS} = 30\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 55\text{ }^{\circ}\text{C}$			10	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}$, $V_{GS} = 10\text{ V}$	90			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$, $I_D = 32\text{ A}$		0.0018	0.0022	Ω
		$V_{GS} = 4.5\text{ V}$, $I_D = 29\text{ A}$		0.0022	0.0027	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15\text{ V}$, $I_D = 32\text{ A}$		160		S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{DS} = 15\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$		12065		pF
Output Capacitance	C_{oss}			1725		
Reverse Transfer Capacitance	C_{rss}			970		
Total Gate Charge	Q_g	$V_{DS} = 15\text{ V}$, $V_{GS} = 10\text{ V}$, $I_D = 32\text{ A}$		171	257	nC
		$V_{DS} = 15\text{ V}$, $V_{GS} = 4.5\text{ V}$, $I_D = 29\text{ A}$		81.5	123	
Gate-Source Charge	Q_{gs}			34		
Gate-Drain Charge	Q_{gd}			29		
Gate Resistance	R_g	$f = 1\text{ MHz}$		1.4	2.1	Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 15\text{ V}$, $R_L = 0.555\text{ }\Omega$ $I_D \cong 27\text{ A}$, $V_{GEN} = 10\text{ V}$, $R_g = 1\text{ }\Omega$		18	27	ns
Rise Time	t_r			11	17	
Turn-Off Delay Time	$t_{d(off)}$			70	105	
Fall Time	t_f			10	15	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 15\text{ V}$, $R_L = 0.625\text{ }\Omega$ $I_D \cong 24\text{ A}$, $V_{GEN} = 4.5\text{ V}$, $R_g = 1\text{ }\Omega$		55	83	
				180	270	
Rise Time	t_r			55	83	
Turn-Off Delay Time	$t_{d(off)}$			12	18	
Fall Time	t_f					
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^{\circ}\text{C}$			90	A
Pulse Diode Forward Current ^a	I_{SM}				200	
Body Diode Voltage	V_{SD}	$I_S = 22\text{ A}$		0.8	1.2	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = 20\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $T_J = 25\text{ }^{\circ}\text{C}$		52	78	ns
Body Diode Reverse Recovery Charge	Q_{rr}			70.2	105	nC
Reverse Recovery Fall Time	t_a			27		ns
Reverse Recovery Rise Time	t_b			25		

Notes:

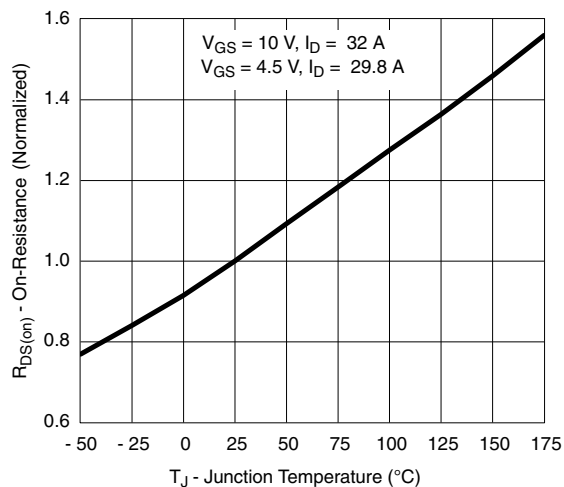
a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

b. Guaranteed by design, not subject to production testing.

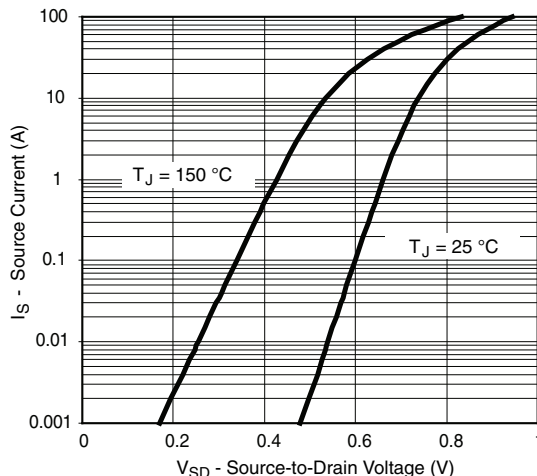
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)**Output Characteristics****Transfer Characteristics****Transconductance** **$R_{DS(on)}$ vs. Drain Current****Capacitance****Gate Charge**

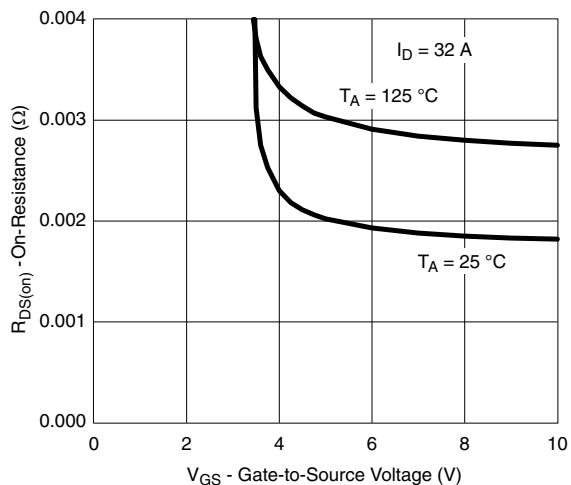
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



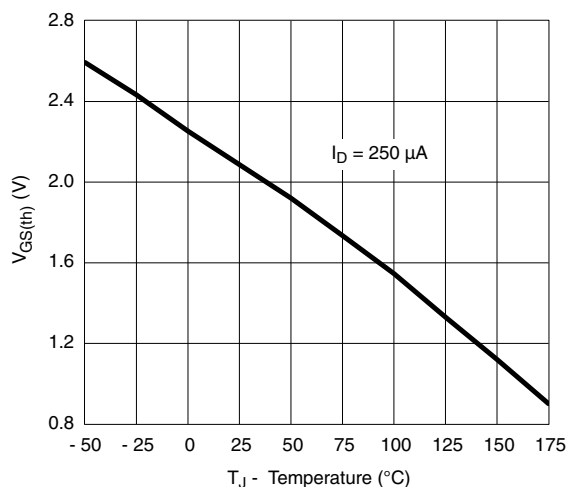
On-Resistance vs. Junction Temperature



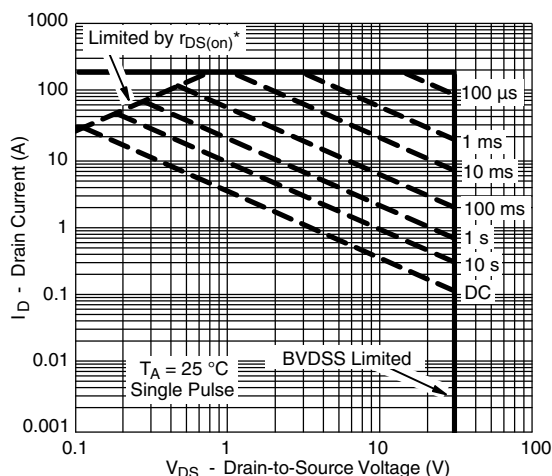
Forward Diode Voltage vs. Temperature



$R_{DS(on)}$ vs. V_{GS} vs. Temperature

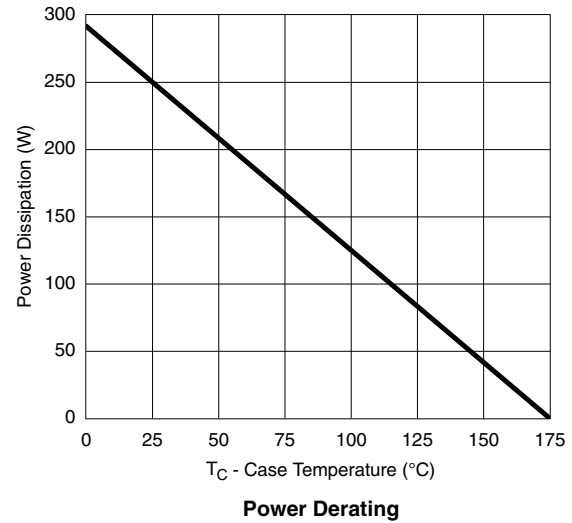
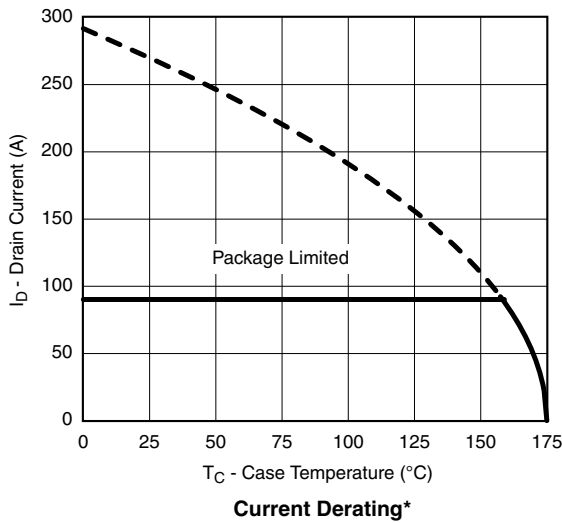


Threshold Voltage

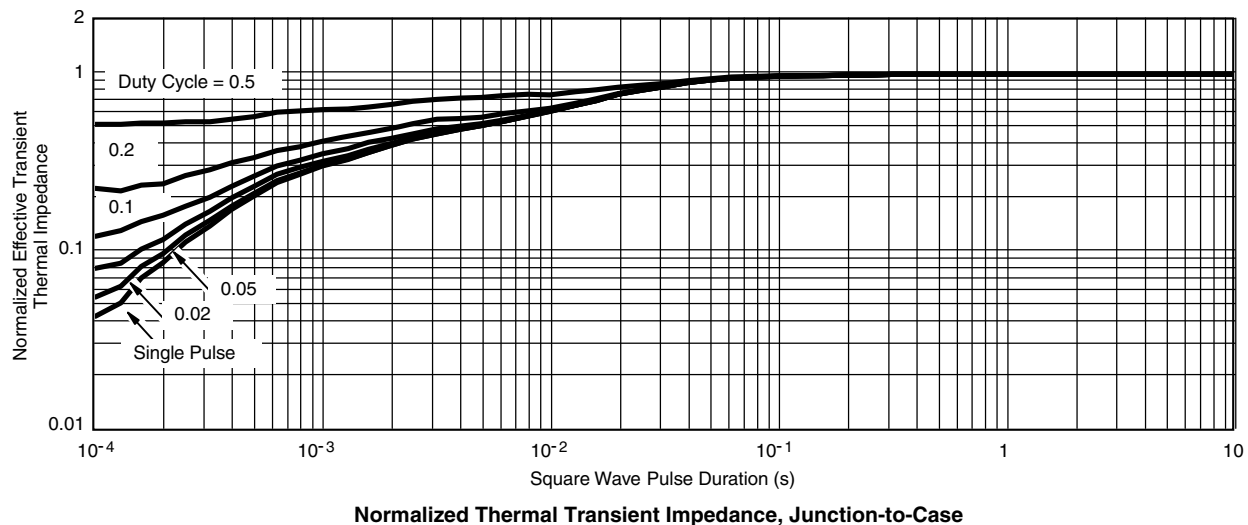


* $V_{GS} >$ minimum V_{GS} at which $r_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

* The power dissipation P_D is based on $T_{J(max)} = 175$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?74342

TO-263 (D²PAK): 3-LEAD



DETAIL A (ROTATED 90°)



SECTION A-A

Notes

- Plane B includes maximum features of heat sink tab and plastic.
- No more than 25 % of L1 can fall above seating plane by max. 8 mils.
- Pin-to-pin coplanarity max. 4 mils.
- *: Thin lead is for SUB, SYB.
Thick lead is for SUM, SYM, SQM.
- Use inches as the primary measurement.
-  This feature is for thick lead.

DIM.		INCHES		MILLIMETERS	
		MIN.	MAX.	MIN.	MAX.
A		0.160	0.190	4.064	4.826
b		0.020	0.039	0.508	0.990
b1		0.020	0.035	0.508	0.889
b2		0.045	0.055	1.143	1.397
c*	Thin lead	0.013	0.018	0.330	0.457
	Thick lead	0.023	0.028	0.584	0.711
c1	Thin lead	0.013	0.017	0.330	0.431
	Thick lead	0.023	0.027	0.584	0.685
c2		0.045	0.055	1.143	1.397
D		0.340	0.380	8.636	9.652
D1		0.220	0.240	5.588	6.096
D2		0.038	0.042	0.965	1.067
D3		0.045	0.055	1.143	1.397
D4		0.044	0.052	1.118	1.321
E		0.380	0.410	9.652	10.414
E1		0.245	-	6.223	-
E2		0.355	0.375	9.017	9.525
 E3		0.072	0.078	1.829	1.981
e		0.100 BSC		2.54 BSC	
K		0.045	0.055	1.143	1.397
L		0.575	0.625	14.605	15.875
L1		0.090	0.110	2.286	2.794
L2		0.040	0.055	1.016	1.397
L3		0.050	0.070	1.270	1.778
L4		0.010 BSC		0.254 BSC	
M		-	0.002	-	0.050
ECN: T13-0707-Rev. K, 30-Sep-13					
DWG: 5843					

RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

[Return to Index](#)



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