

Complementary N- and P-Channel 20 V (D-S) MOSFET

PRODUCT SUMMARY

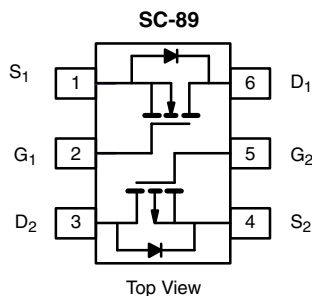
	V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (mA)
N-Channel	20	5 at $V_{GS} = 4.5$ V	200
		7 at $V_{GS} = 2.5$ V	175
		9 at $V_{GS} = 1.8$ V	150
		10 at $V_{GS} = 1.5$ V	50
P-Channel	- 20	8 at $V_{GS} = - 4.5$ V	- 150
		12 at $V_{GS} = - 2.5$ V	- 125
		15 at $V_{GS} = - 1.8$ V	- 100
		20 at $V_{GS} = - 1.5$ V	- 30

FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET® Power MOSFET: 1.5 V Rated
- Very Small Footprint
- High-Side Switching
- Low On-Resistance:
N-Channel, 5 Ω
P-Channel, 8 Ω
- Low Threshold: ± 0.9 V (typ.)
- Fast Switching Speed: 45 ns (typ.)
- 1.5 V Operation
- Gate-Source ESD Protected: 2000 V
- Compliant to RoHS Directive 2002/95/EC



RoHS
COMPLIANT
HALOGEN
FREE



Marking Code: M

Ordering Information: Si1035X-T1-GE3 (Lead (Pb)-free and Halogen-free)

BENEFITS

- Ease in Driving Switches
- Low Offset (Error) Voltage
- Low-Voltage Operation
- High-Speed Circuits
- Low Battery Voltage Operation

APPLICATIONS

- Replace Digital Transistor, Level-Shifter
- Battery Operated Systems
- Power Supply Converter Circuits
- Load/Power Switching Cell Phones, Pagers

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)

ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C, unless otherwise noted)							
Parameter		Symbol	N-Channel		P-Channel		Unit
			5 s	Steady State	5 s	Steady State	
Drain-Source Voltage		V _{DS}	20		- 20		V
Gate-Source Voltage		V _{GS}	± 5				
Continuous Drain Current (T _J = 150 °C) ^a	T _A = 25 °C	I _D	190	180	- 155	- 145	mA
	T _A = 85 °C		140	130	- 110	- 105	
Pulsed Drain Current ^b		I _{DM}	650		- 650		
Continuous Source Current (Diode Conduction)		I _S	450	380	- 450	- 380	
Maximum Power Dissipation ^a	T _A = 25 °C	P _D	280	250	280	250	mW
	T _A = 85 °C		145	130	145	130	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150				°C
Gate-Source ESD Rating (HBM, Method 3015)		ESD	2000				V

Notes:

a. Surface mounted on FR4 board.

b. Pulse width limited by maximum junction temperature.

SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)							
Parameter	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
Static							
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	N-Ch	0.40			V
		V _{DS} = V _{GS} , I _D = - 250 μA	P-Ch	- 0.40			
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 2.8 V	N-Ch		± 0.5	± 1.0	μA
			P-Ch		± 0.5	± 1.0	
		V _{DS} = 0 V, V _{GS} = ± 4.5 V	N-Ch		± 1.5	± 3.0	
			P-Ch		± 1.0	± 3.0	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 16 V, V _{GS} = 0 V	N-Ch		1	500	nA
		V _{DS} = - 16 V, V _{GS} = 0 V	P-Ch		- 1	- 500	
		V _{DS} = 16 V, V _{GS} = 0 V, T _J = 85 °C	N-Ch			10	μA
		V _{DS} = - 16 V, V _{GS} = 0 V, T _J = 85 °C	P-Ch			- 10	
On-State Drain Current ^a	I _{D(on)}	V _{DS} = 5 V, V _{GS} = 4.5 V	N-Ch	250			mA
		V _{DS} = - 5 V, V _{GS} = - 4.5 V	P-Ch	- 200			
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 4.5 V, I _D = 200 mA	N-Ch			5	Ω
		V _{GS} = - 4.5 V, I _D = - 150 mA	P-Ch			8	
		V _{GS} = 2.5 V, I _D = 175 mA	N-Ch			7	
		V _{GS} = - 2.5 V, I _D = 125 mA	P-Ch			12	
		V _{GS} = 1.8 V, I _D = 150 mA	N-Ch			9	
		V _{GS} = - 1.8 V, I _D = - 100 mA	P-Ch			15	
		V _{DS} = 1.5 V, I _D = 40 mA	N-Ch			10	
		V _{DS} = - 1.5 V, I _D = - 30 mA	P-Ch			20	
Forward Transconductance ^a	g _{fs}	V _{DS} = 10 V, I _D = 200 mA	N-Ch		0.5		S
		V _{DS} = - 10 V, I _D = - 150 mA	P-Ch		0.4		
Diode Forward Voltage ^a	V _{SD}	I _S = 150 mA, V _{GS} = 0 V	N-Ch			1.2	V
		I _S = - 150 mA, V _{GS} = 0 V	P-Ch			- 1.2	
Dynamic ^b							
Total Gate Charge	Q _g	N-Channel V _{DS} = 10 V, V _{GS} = 4.5 V, I _D = 150 mA P-Channel V _{DS} = - 10 V, V _{GS} = - 4.5 V, I _D = - 150 mA	N-Ch		750		pC
Gate-Source Charge	Q _{gs}		P-Ch		1500		
			N-Ch		75		
			P-Ch		150		
Gate-Drain Charge	Q _{gd}	N-Ch		225			
		P-Ch		450			
Turn-On Time	t _{ON}	N-Channel V _{DD} = 10 V, R _L = 47 Ω I _D ≅ 250 mA, V _{GEN} = 4.5 V, R _g = 10 Ω	N-Ch			75	ns
			P-Ch			80	
Turn-Off Time	t _{OFF}	P-Channel V _{DD} = - 10 V, R _L = 65 Ω I _D ≅ - 150 mA, V _{GEN} = - 4.5 V, R _g = 10 Ω	N-Ch			75	
			P-Ch			90	

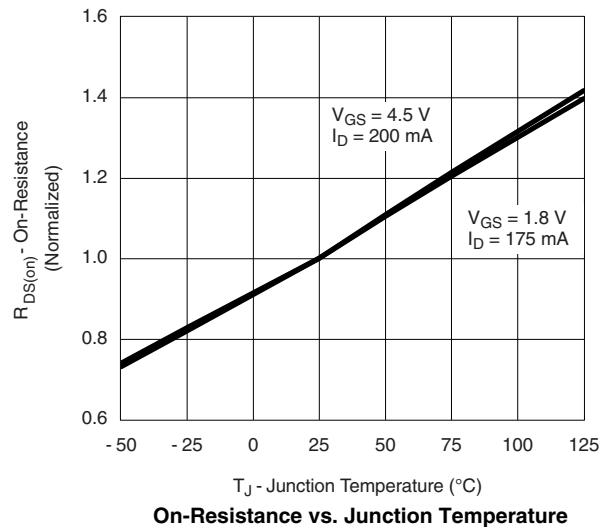
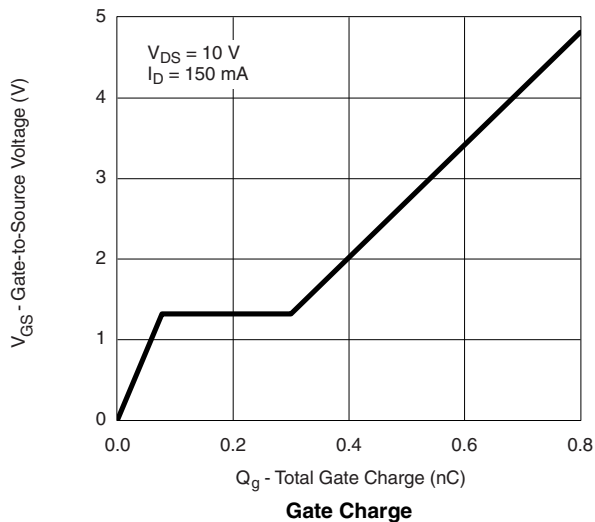
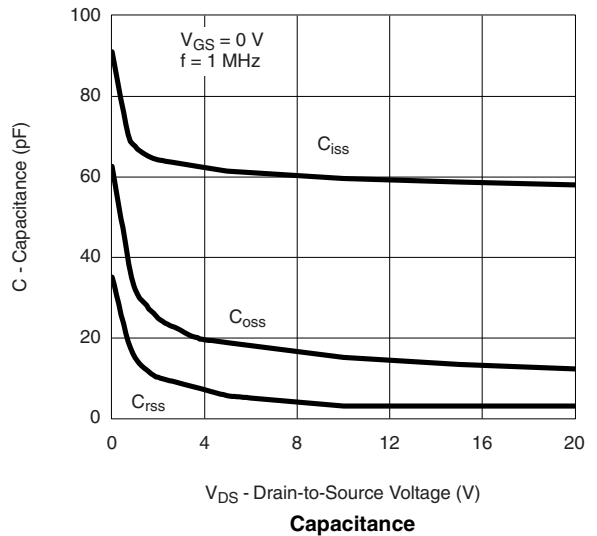
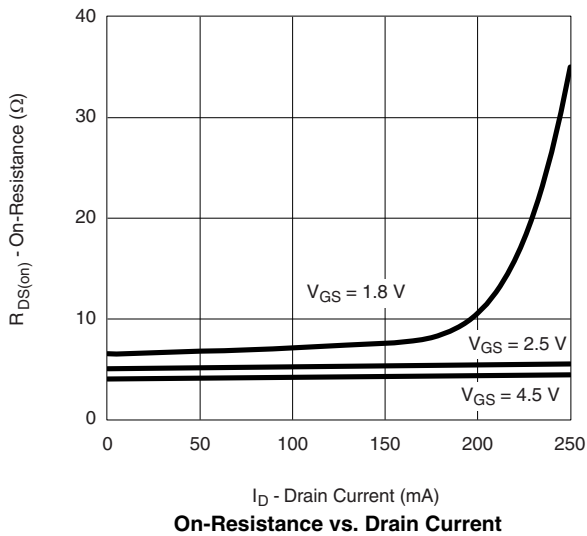
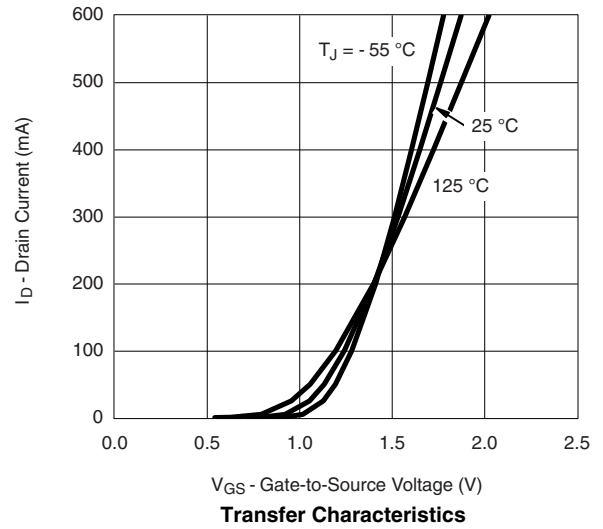
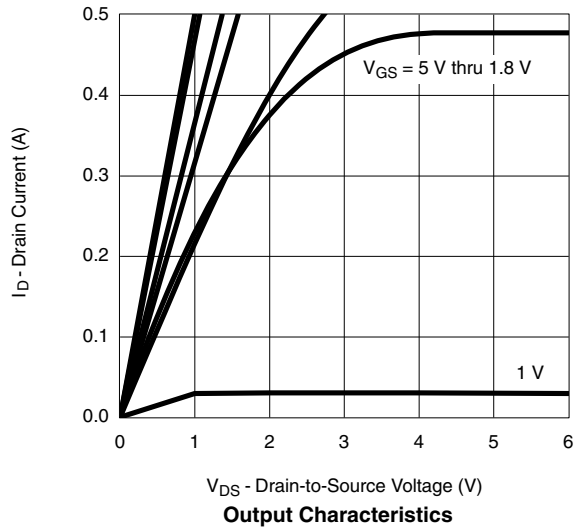
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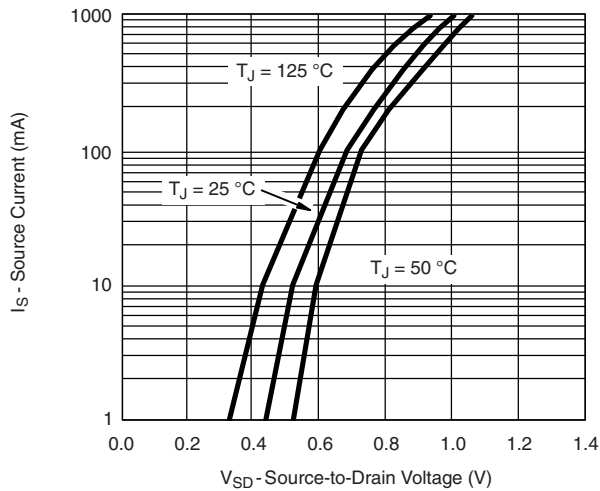
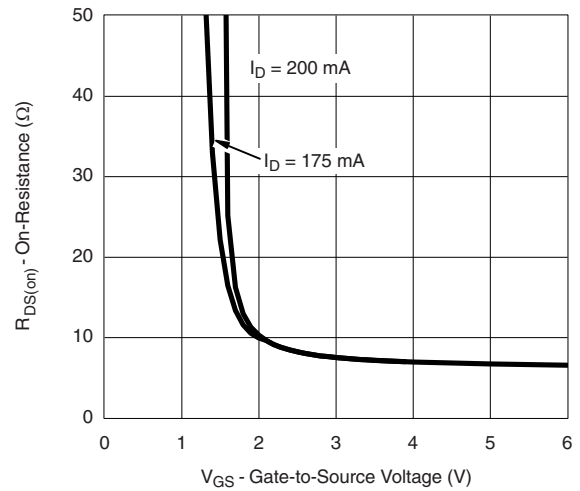
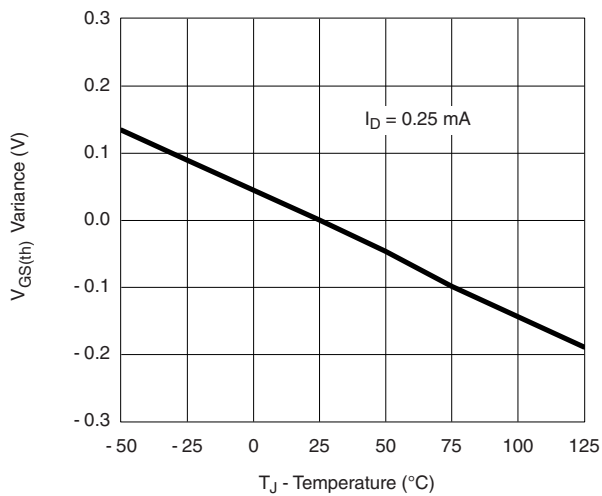
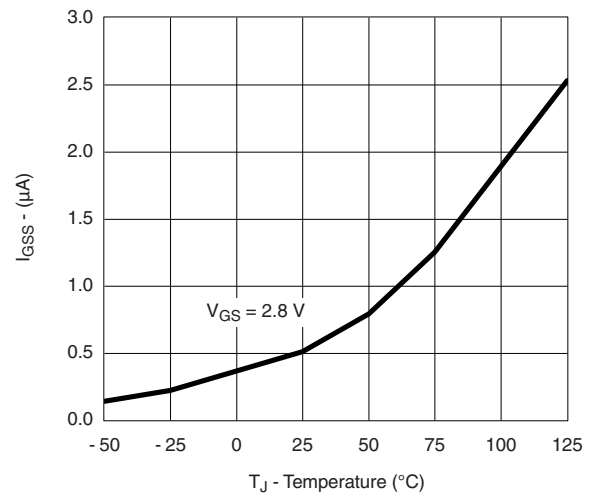
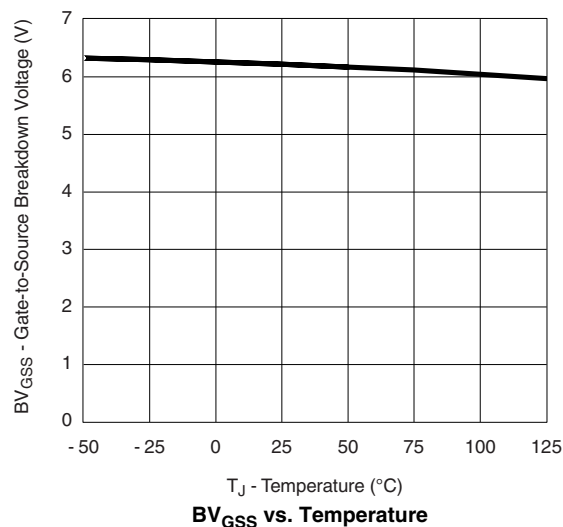
a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

b. Guaranteed by design, not subject to production testing.

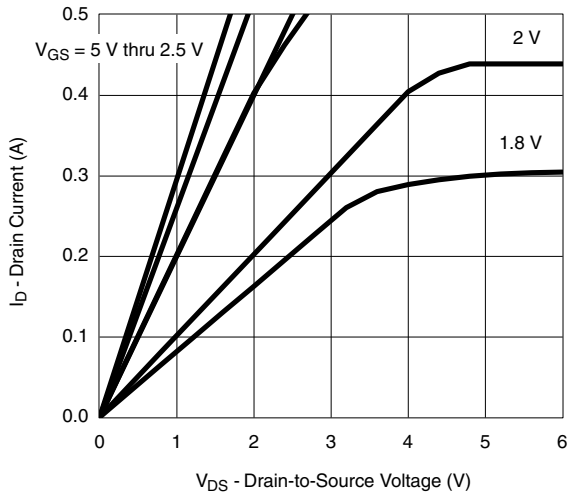
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

N-CHANNEL TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, unless otherwise noted)

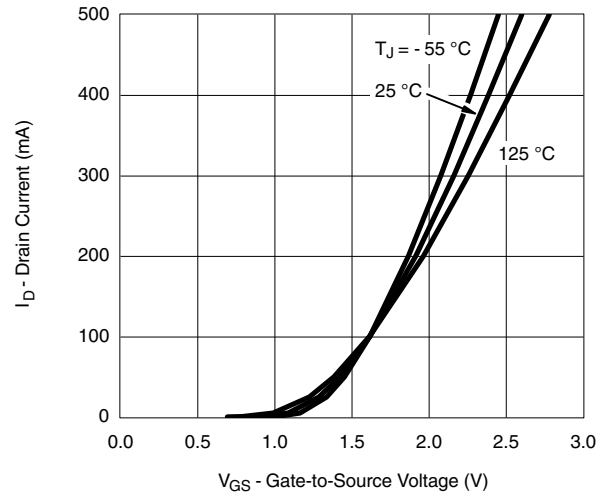


N-CHANNEL TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, unless otherwise noted)**Source-Drain Diode Forward Voltage****On-Resistance vs. Gate-to-Source Voltage****Threshold Voltage Variance vs. Temperature** **I_{GSS} vs. Temperature** **BV_{GSS} vs. Temperature**

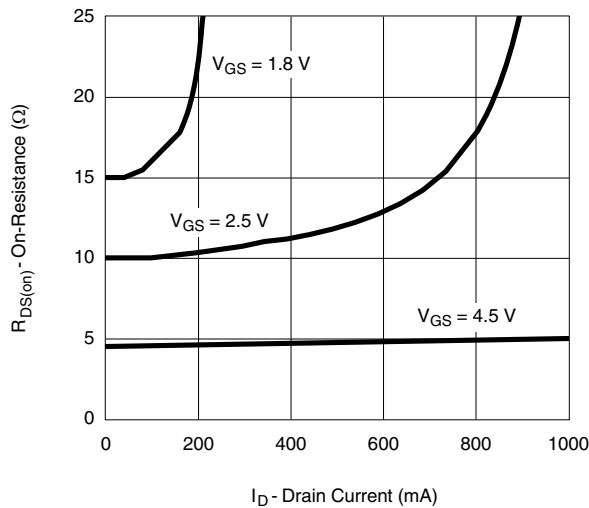
P-CHANNEL TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, unless otherwise noted)



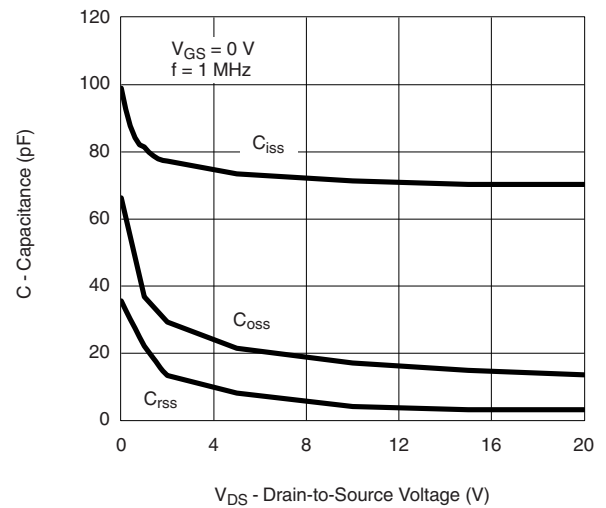
Output Characteristics



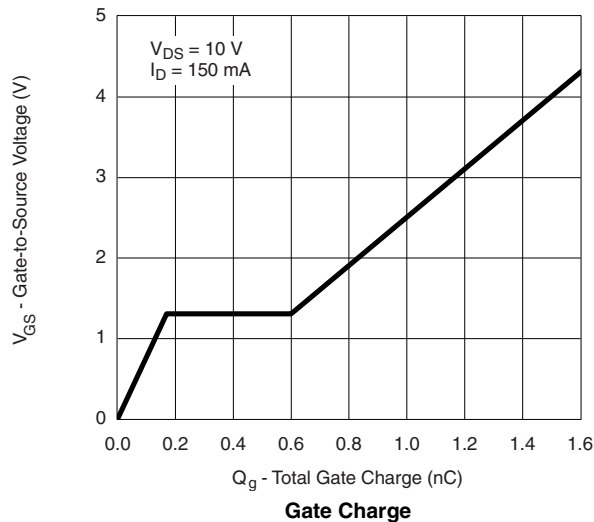
Transfer Characteristics



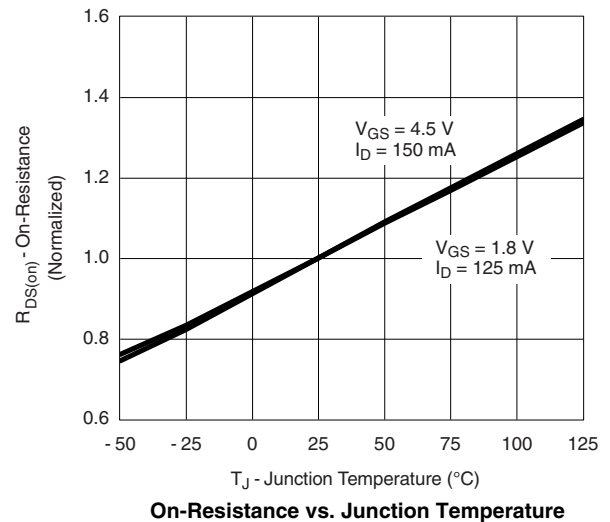
On-Resistance vs. Drain Current



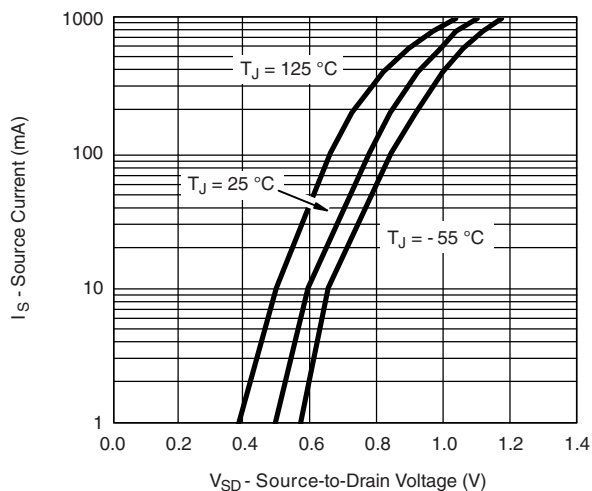
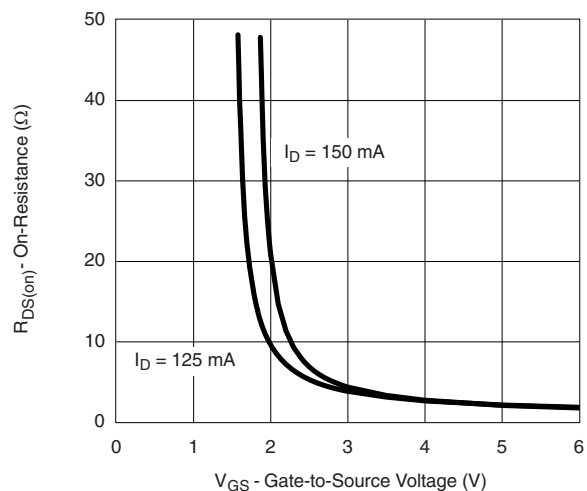
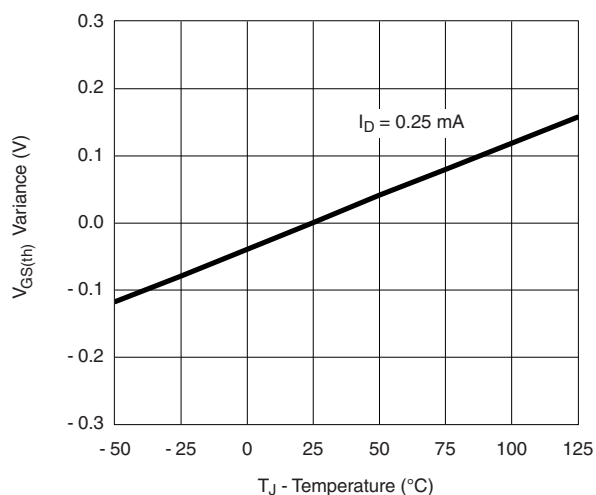
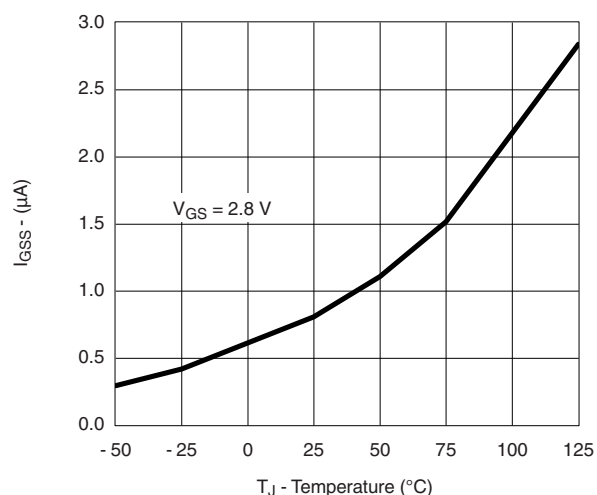
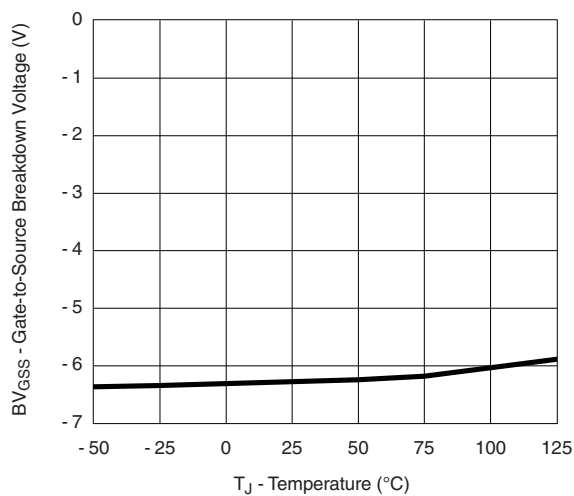
Capacitance

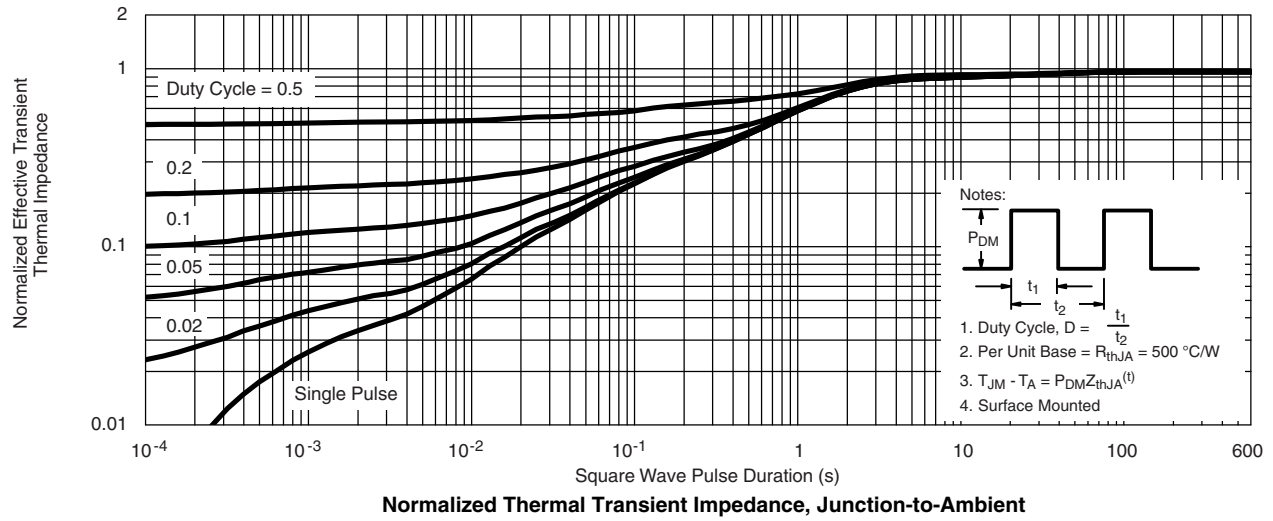


Gate Charge



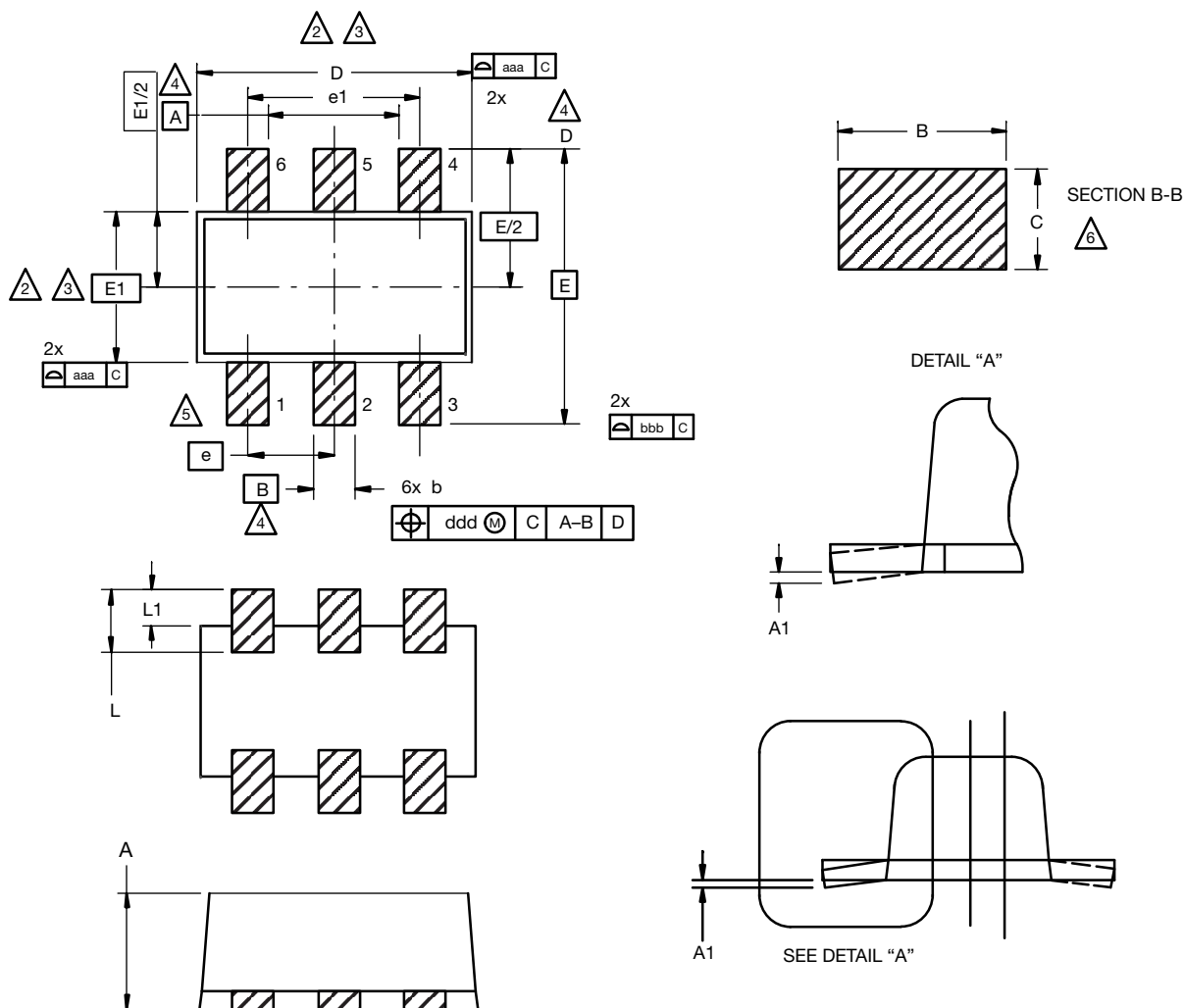
On-Resistance vs. Junction Temperature

P-CHANNEL TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)**Source-Drain Diode Forward Voltage****On-Resistance vs. Gate-to-Source Voltage****Threshold Voltage Variance vs. Temperature** **I_{GSS} vs. Temperature** **BV_{GSS} vs. Temperature**

N- OR P-CHANNEL TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)


Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?71426.

SC-89 6-Leads (SOT-563F)



Notes

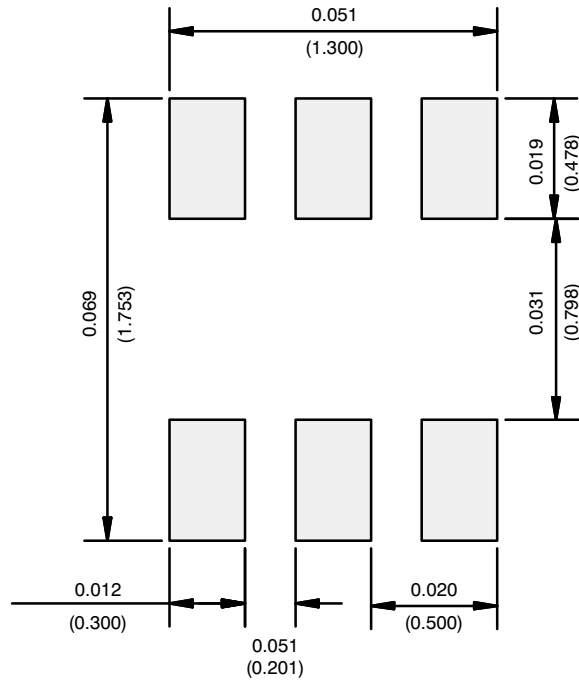
1. Dimensions in millimeters.

- ② Dimension D does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per dimension E1 does not include interlead flash or protrusion, interlead flash or protrusion shall not exceed 0.15 mm per side.
- ③ Dimensions D and E1 are determined at the outmost extremes of the plastic body exclusive of mold flash, the bar burrs, gate burrs and interlead flash, but including any mismatch between the top and the bottom of the plastic body.
- ④ Datums A, B and D to be determined 0.10 mm from the lead tip.
- ⑤ Terminal numbers are shown for reference only.
- ⑥ These dimensions apply to the flat section of the lead between 0.08 mm and 0.15 mm from the lead tip.

DIM.	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.56	0.58	0.60
A1	0	0.02	0.10
b	0.15	0.22	0.30
c	0.10	0.14	0.18
D	1.50	1.60	1.70
E	1.50	1.60	1.70
E1	1.15	1.20	1.25
e	0.45	0.50	0.55
e1	0.95	1.00	1.05
L	0.25	0.35	0.50
L1	0.10	0.20	0.30

C14-0439-Rev. C, 11-Aug-14
DWG: 5880

RECOMMENDED MINIMUM PADS FOR SC-89: 6-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

[Return to Index](#)



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