High Efficiency Low-Side Controller with True Shutdown

Check for Samples: LM3017

FEATURES

- **Fully Compliant to Thunderbolt™ Technology Specifications**
- **True Shutdown for Short Circuit Protection**
- **Input Side Current Limit**
- **Single Enable Pin with Three Modes of Operation: Boost, Pass Through, or Shutdown**
- **Built-in Charge Pump for High-side NFET Disconnect Switch**
- **1A Push-pull Driver for Low-side NFET**
- **Peak Current Mode Control**
- **Simple Slope Compensation**
- **Protection Features: Thermal Shutdown, Cycle-by-cycle Current Limit, Short Circuit Protection, Output Overvoltage Protection, and Latch-off**
- **Internal Soft-start**
- **2.4mm × 2.7mm × 0.8mm 10-pin QFN Package**

APPLICATIONS

- **Thunderbolt Technology™ Host Ports**
- **Notebook and Desktop Computers, Tablets, and Other Portable Consumer Electronics**
- **Hard Disc Drives, Solid State Drives**
- **Offline Power Supplies**
- **Set-Top Boxes**

KEY SPECIFICATION

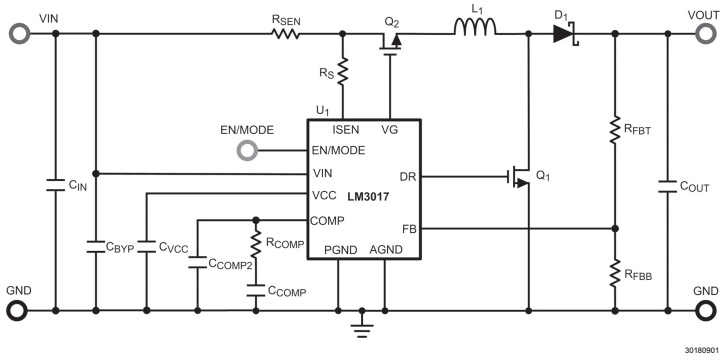
- **Input Voltage Range of 5V to 18V**
- **600 kHz fixed Frequency Operation**
- **±1% Reference Voltage Accuracy Over Temperature**
- **Low Shutdown Current (< 1µA), 40nA Typical**

DESCRIPTION

The LM3017 is a versatile low-side NFET controller incorporating true shutdown and input side current limiting. It is designed for simple implementation of boost conversions in Thunderbolt™ Technology. The LM3017 can also be configured for flyback or SEPIC designs. The input voltage range of 5V to 18V accommodates a two or three cell lithium ion battery or a 12V rail. The enable pin accepts a single input to drive three different modes of operation: boost, pass through, or shutdown mode. The LM3017 draws very low current in shutdown mode, typically 40nA from the input supply.

The LM3017 provides an adjustable output in order to drive the Power Load Switch or Mux for the host Thunderbolt™ port. The ability to drive an external high-side NMOS provides for true isolation of the load from the input. Current limiting on the input ensures that inrush and short-circuit currents are always under control. The LM3017 incorporates built in thermal shutdown, cycle-by-cycle current limit, short-circuit protection, output overvoltage protection, and soft-start. It is available in a 10-pin QFN package.

TYPICAL APPLICATION CIRCUIT



Typical Boost Converter Application

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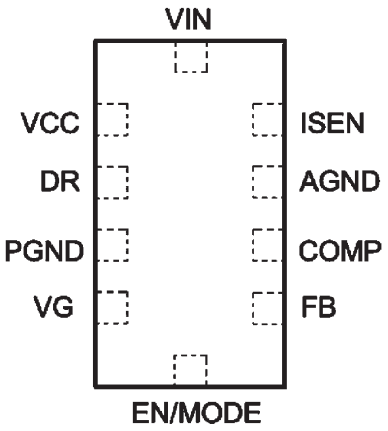
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

CONNECTION DIAGRAM

10-PIN VQFN
TOP VIEW



30180903

PIN DESCRIPTIONS

PIN		DESCRIPTION	FUNCTION
NAME	NO.		
VCC	1	Driver supply voltage pin	Output of internal regulator powering low side NMOS driver. A minimum of 0.47µF must be connected from this pin to PGND for proper operation.
DR	2	Low-side NMOS gate driver output	Output gate drive to low side NMOS gate.
PGND	3	Power Ground	Ground for power section. External power circuit reference. Should be connected to AGND at a single point.
VG	4	High side NMOS gate driver output	Output gate drive to high side NMOS gate.
EN/MODE	5	Multi-function input pin	This input provides for chip enable, and mode selection. See functional description for details.
FB	6	Feed-back input pin	Negative input to error amplifier. Connect to feed-back resistor tap to regulate output.
COMP	7	Compensation pin	A resistor and capacitor combination connected to this pin provides frequency compensation for the regulator control loop.
AGND	8	Analog Ground	Ground for analog control circuitry. Reference point for all stated voltages.
ISEN	9	Current sense input	Current sense input, with respect to Vin, for all current limit functions.
VIN	10	Power Supply input pin	Input supply to regulator. See applications section for recommendations on bypass capacitors on this pin.

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ABSOLUTE MAXIMUM RATINGS(1)(2)

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
VIN to PGND, AGND	–0.3	20	V
FB, COMP, VCC,DR to PGND, AGND	–0.2	6	V
EN/MODE	-0.2	5.5	V
VG	-0.3	VIN+6	V
ISEN to PGND, AGND	VIN-0.3	VIN	V
Peak low side driver output current		1.0	A
Power Dissipation	Internally Limited		
Storage Temperature Range	–65	150	°C
Junction Temperature		150	°C
ESD Susceptibility, Human Body Model(3)		1.5	kV

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings indicates conditions for which the device is intended to be functional, but does not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions.
(2) If Military/Aerospace specified devices are required, contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) The human body model is a 100 pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method is per JESD-22-114.

OPERATING RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Supply Voltage, VIN		5.4		18	V
T_J	Junction Temperature Range		–40		+125	°C

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings indicates conditions for which the device is intended to be functional, but does **NOT** guarantee specific performance limits. For specifications and test conditions, see the Electrical Characteristics. The specifications apply only for the test conditions.

ELECTRICAL CHARACTERISTICS

Limits in standard type are for T_J = 25°C only; limits apply over the junction temperature (T_J) range of –40°C to +125°C. Minimum and Maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{IN} = 12V.

SYMBOLS	PARAMETER	TEST CONDITIONS	MIN(1)	TYP(2)	MAX(1)	UNIT
V_{FB}	Feedback Voltage	Vcomp = 1.4V	1.256	1.27	1.282	V
ΔV_{LINE}	Feedback Voltage Line Regulation	5V ≤ Vin ≤ 18V		0.33		%
V_{UVLO}	Input Under Voltage Lock-Out Voltage	Rising	4.6	4.82	4.9	V
	Input Under Voltage Lock-Out Hysteresis	Falling; below V_{UVLO}		280		mV
F_{SW}	Nominal Switching Frequency	EN/MODE = 1.6 V	550	600	635	kHz
$R_{DS(ON)}$	Low side NMOS driver resistance; top driver FET	V_{IN} = 5V, I_{DR} = 0.2 A		3.4		Ω
	Low side NMOS driver resistance; bottom driver FET			1		
VCC	Driver Voltage Supply	V_{IN} < 6 V		V_{IN}		V
		V_{IN} ≥ 6 V		5.6		
D_{max}	Maximum Duty Cycle			86		%
$T_{min(on)}$	Minimum On Time			125		ns

(1) All limits are specified at room temperature (standard type face) and at **temperature extremes (bold type face)**. All room temperatures are 100% production tested. All limits at **temperature extremes** are specified via correlation using Statistical Quality Control (SQD) methods. All limits are used to calculate Average Outgoing Quaity Level (AOQL).
(2) Typical numbers are at 25°C and represent the most likely parametric norm.

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ELECTRICAL CHARACTERISTICS (continued)

Limits in standard type are for T_J = 25°C only; limits apply over the junction temperature (T_J) range of –40°C to +125°C. Minimum and Maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{IN} = 12V.

SYMBOLS	PARAMETER	TEST CONDITIONS	MIN(1)	TYP(2)	MAX(1)	UNIT
$I_{Q\text{-}boost}$	Supply Current in Boost Mode - No switching	EN/MODE = 1.6V, FB = 1.4V		5.2	9	mA
$I_{Q\text{-}SD}$	Supply Current in Shutdown Mode	EN/MODE pin = 0.4V		0.025	1	µA
$I_{Q\text{-}pass}$	Supply Current in Pass-Through mode	EN/MODE = 2.6V, FB = 1.4V		1.4	2.3	mA
$V_{en\text{-}pass}$	Pass-Through Mode Threshold (3)	Rising	2.19	2.4	2.56	V
$V_{mode\text{-}hyst}$	Mode change hysteresis, falling(3)	Falling	65	107	165	V
$V_{en\text{-}shutdown}$	Shut-down Mode Threshold (3)	Falling	0.2	0.4	0.59	V
$V_{en\text{-}boost}$	Boost Mode Enable Window(3)	Rising	0.65	1.22	1.6	V
I_{en}	EN/MODE pin bias current (4)	EN/MODE = 1.6V		±1.0		µA
V_{SENSE}	Cycle-by-Cycle Current Limit Threshold during boost mode	EN/MODE = 1.6V FB = 50V	142	170	182	mV
ΔV_{SC}	Short Circuit Current Limit Threshold during boost mode	EN/MODE = 1.6 V, FB = 0 V	18	30	42	mV
V_{SL}	Internal Ramp Compensation Voltage			90		mV
V_{LIM1}	Input Current Limit Threshold Voltage in Pass-Through mode during T_{LIM1}(3)	EN/MODE = 2.6V	70	85	95	mV
ΔV_{LIM2}	Input Current Limit Threshold Voltage in Pass-Through mode during T_{LIM2}(3)	EN/MODE = 2.6V	14.5	18	21	mV
T_{LIM1}	Curent Limit Time at T_{LIM1}(3)			900		µs
T_{LIM2}	Current Limit Time at T_{LIM2}(3)			3.6		ms
T_{SC}	Current Limit Time at T_{SC}(3)			900		µs
V_{OVP}	Upper Output-Over Voltage Protection Threshold	Rising threshold measured at FB pin with respect to FB pin, VCOMP = 1.45V		40		mV
	Lower Output-Over Voltage Protection Threshold	Falling threshold measured at FB pin with respect to FB pin, VCOMP = 1.45V		26		mv
$V_{GS\text{-}on}$	On State Drive voltage at VG pin (5)	V_{IN} = 5V, ISEN = 5V, I_G = 0A	3.8	4.9		V
$V_{GS\text{-}off}$	Off State Drive voltage at VG pin(6)	Vin = 5V, ISEN = V_{IN} – 200mV I_G = 0A		5		mV
I_G	Maximum Drive current at VG pin	V_{IN} = 5V, ISEN = 5V V_G = V_{IN}		20		µA
G_m	Error Amplifier Transconductance	V_{COM} = 1.4 V, I_{COMP} = ±50µA	340	522	900	µA/V
A_{VOL}	Error Amplifier Open Loop Voltage Gain	V_{COM} = 1.2 V to 1.8V, I_{COMP} = 0A	190	313	450	V/V
R_O	Error Amplifier Open Loop Output Resistance (7)			600		kΩ
I_{EAO}	Error Amplifier Output Current Swings	SOURCING: V_{COMP} = 1.4V, V_{FB} = 1.1V	27	66	115	µA
		SINKING: V_{COMP} = 1.4V, V_{FB} = 1.4V	49	68	125	µA

(3) See sections on operational modes and short circuit protection.
(4) The bias current flowing through this pin is compensated and can flow either into or out-of this pin.
(5) This is the gate-to-source voltage drive of Q2, when the controller turns on this FET.
(6) This voltage is measured from the VG pin to AGND, when the controller fully turns off Q2.
(7) This parameter is calculated from the error amplified G_m and A_{VOL}, and is not tested.

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ELECTRICAL CHARACTERISTICS (continued)

Limits in standard type are for T_J = 25°C only; limits apply over the junction temperature (T_J) range of –40°C to +125°C. Minimum and Maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{IN} = 12V.

SYMBOLS	PARAMETER	TEST CONDITIONS	MIN(1)	TYP(2)	MAX(1)	UNIT
V_{EAO}	Error Amplifier Output Voltage Limits	UPPER: V_{FB} = 0V, COMP pin floating		2.3		V
		LOWER: V_{FB} = 1.4V		0.82		V
T_r	Drive Pin Rise Time	C_{load} = 3nF, V_{DR} = 0V to 3V		25		ns
T_f	Drive Pin Fall Time	C_{load} = 3nF, V_{DR} = 3V to 0V		25		ns
T_{SD}	Thermal Shutdown Threshold			165		°C
$T_{SD\text{-}hyst}$	Thermal Shutdown Threshold Hysteresis			10		°C
θ_{JA}	Thermal Resistance from Junction to Ambient	10-Lead QFN LEK10A		36		°C/W

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TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise specified, V_{IN} = 12V, T_J = 25°C, circuit of Figure 29

Switching Frequency vs Temperature

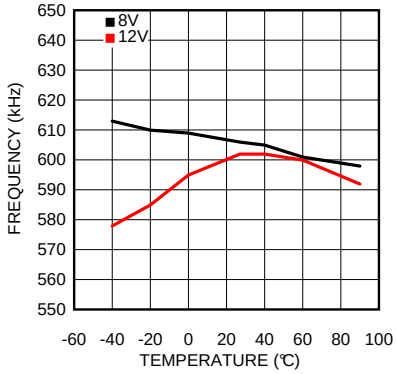

Figure 1.

Supply current in Pass-through Mode (I_{G-pass})

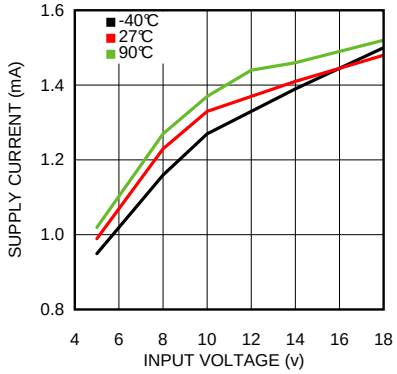

Figure 2.

Supply Current in Boost Mode ($I_{Q-boost}$)

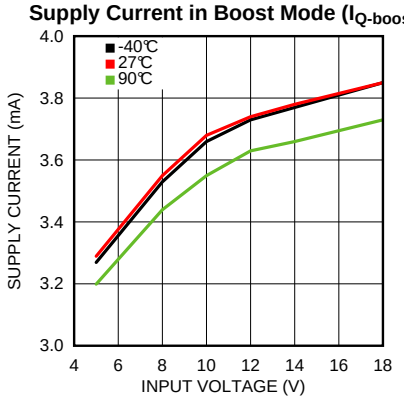

Figure 3.

Minimum On-Time vs Temperature

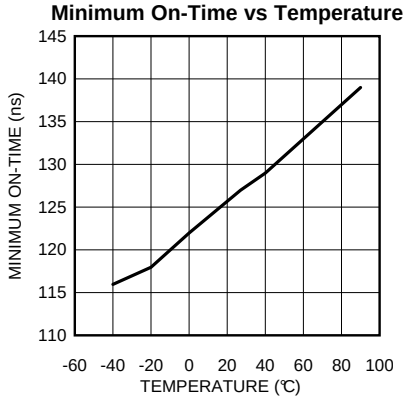

Figure 4.

Current Limit Timing vs Temperature

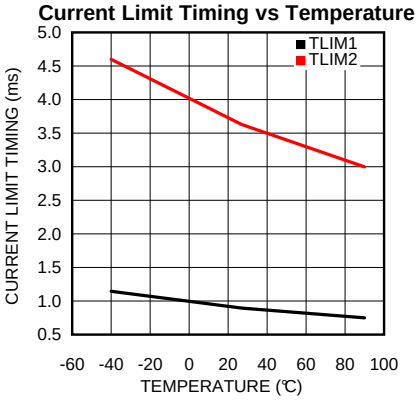

Figure 5.

Pass FET Drive Voltage vs Input Voltage (V_{GS-on})

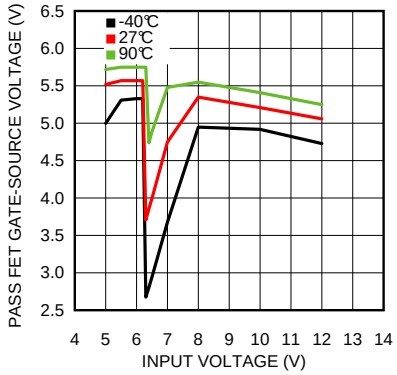

Figure 6.

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TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified, V_{IN} = 12V, T_J = 25°C, circuit of Figure 29

Pass FET Drive Current vs Temperature

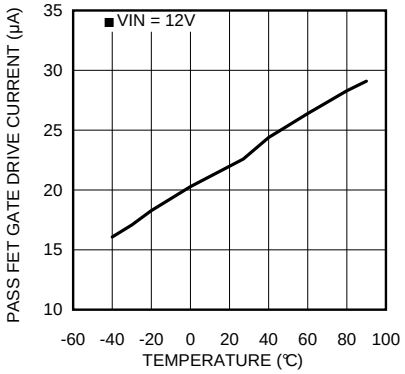


Figure 7.

VCC Voltage vs Input Voltage

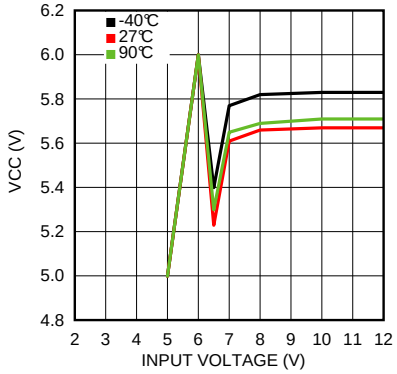


Figure 8.

Efficiency, V_{OUT} = 15 V

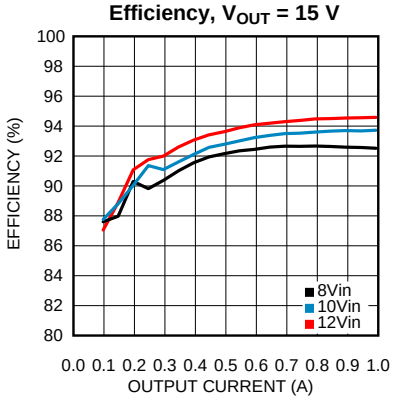


Figure 9.

Load Regulation

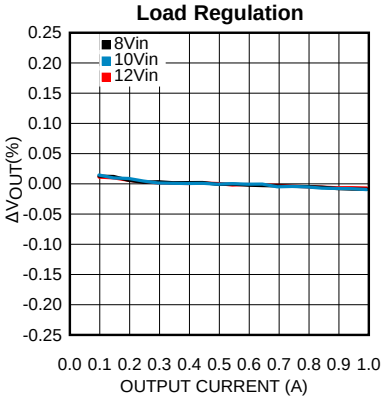


Figure 10.

Line Regulation

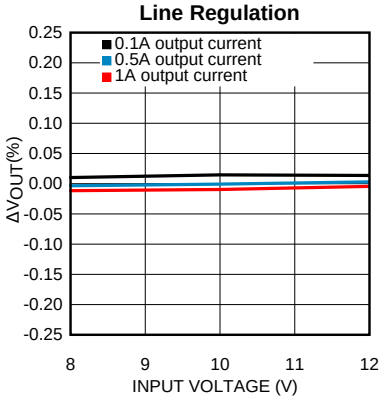


Figure 11.

Startup Waveforms, V_{IN} = 8 V

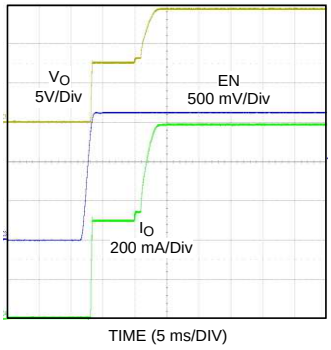
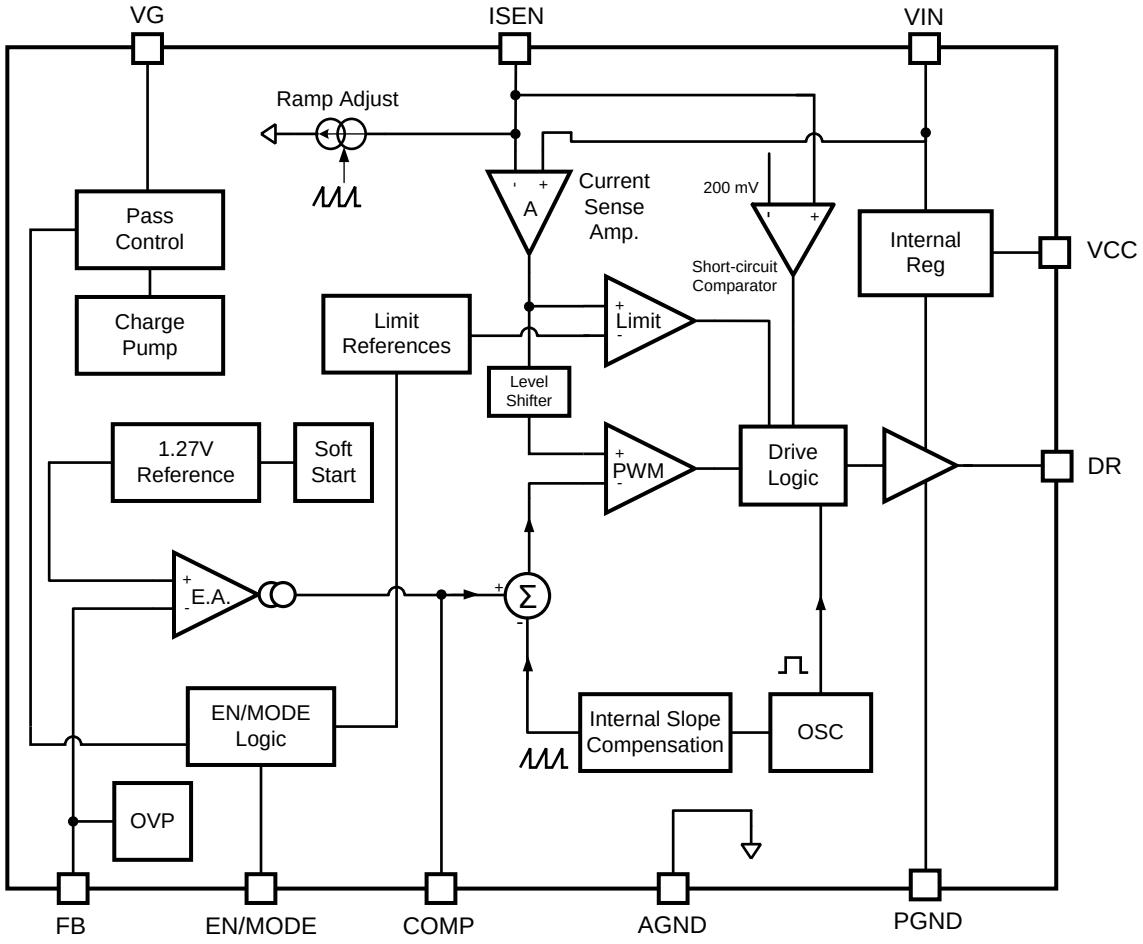


Figure 12.

FUNCTIONAL BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The LM3017 uses a fixed frequency, Pulse Width Modulated (PWM), current mode control architecture. A high-side current sense amplifier provides inductor current information by sensing the voltage drop across R_{SEN}. The voltage across this resistor is fed into the I_{SEN} pin. This voltage is then level shifted and fed into the positive input of the PWM comparator. As with all architectures of this type, a compensation ramp is required to ensure stability of the current control loop under all operating conditions. A nominal value of the ramp is provided internally while additional ramp can be added through the ISEN pin. The output voltage is sensed through an external feedback resistor divider network and fed into the error amplifier (EA) negative input (feedback pin, FB). The output of the error amplifier (COMP pin) is added to the slope compensation ramp and fed into the negative input of the PWM comparator.

At the start of any switching cycle, the oscillator sets a high signal on the DR pin (gate of the external MOSFET) and the external MOSFET turns on. When the voltage on the positive input of the PWM comparator exceeds the negative input, the Drive Logic is reset and the external MOSFET turns off.

Under extremely light load or no-load conditions, the energy delivered to the output capacitor when the external MOSFET is on during the minimum on time is more than what is delivered to the load. An over-voltage comparator inside the LM3017 prevents the output voltage from rising under these conditions by sensing the feedback (FB pin) voltage and resetting the RS latch. The latch remains in a reset state until the output decays to the nominal value. Thus the operating frequency decreases at light loads, resulting in excellent efficiency.

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TRUE SHUTDOWN

The LM3017 incorporates circuitry to control a high side NMOS transistor in series with the inductor. This feature is used to dis-connect the load from the input supply and protect the system from shorts on the output. Using an NMOS, rather than a PMOS transistor, saves the use of a diode from the inductor to ground. When the NMOS is turned-off, the inductor brings the source belowground, keeping it on until the current is safely brought to zero. A built-in charge pump supplies typically V_{IN}+5V to drive the gate of this NMOS.

OPERATION OF THE EN/MODE PIN

The EN/MODE pin is used to control the modes of the regulator by driving the high side gate (VG pin) to enable or disable the output through the pass MOSFET. Furthermore it defines the current limit for each operation mode (see next section). The following table shows the modes versus the voltage on the EN/MODE pin:

EN/MODE PIN VOLTAGE	MODE
≤ 0.4V	Shutdown
1.6 V to 2.2 V	Boost
≥2.6 V	Pass-through

Figure 13 shows the output voltage behavior in the various operation modes.

SHUTDOWN MODE

Pulling the EN/MODE pin to less than 0.4V (typ.), during any mode of operation, will place the part in full shutdown mode. The boost regulator and the pass FET will be off and the load will be disconnected from the input supply. In this mode, the regulator will draw a maximum of 1µA from the input supply.

BOOST MODE

The boost regulator can be turned on by bringing the EN/MODE pin to greater than 1.6V, but less than 2.2V. This is the run mode for the boost regulator. Note that the LM3017 will always start in pass-through and transition to boost mode.

STANDBY MODE

Setting the EN/MODE pin to greater than 2.6V (typ.), will place the part in pass-through mode. The boost regulator will be off and the pass MOSFET will be on. During this mode, the load is connected to the input supply through the inductor and power diode, and is fully protected from output short circuits.

EN/MODE CONTROL

As stated previously, the EN/MODE pin controls the state of the LM3017. As with any digital input , the voltage on this pin must not be allowed to slowly cross the various thresholds. Although hysteresis is used on this input, slowly varying signal may cause unpredictable behavior. Also, the EN/MODE pin must not be allowed to float. One way to control the LM3017, from digital logic, is to use the circuit shown in Figure 14. The resistor values are adjusted based on the above table and the logic supply used. The MOSFET can be any small signal device, such as the 2N7002.

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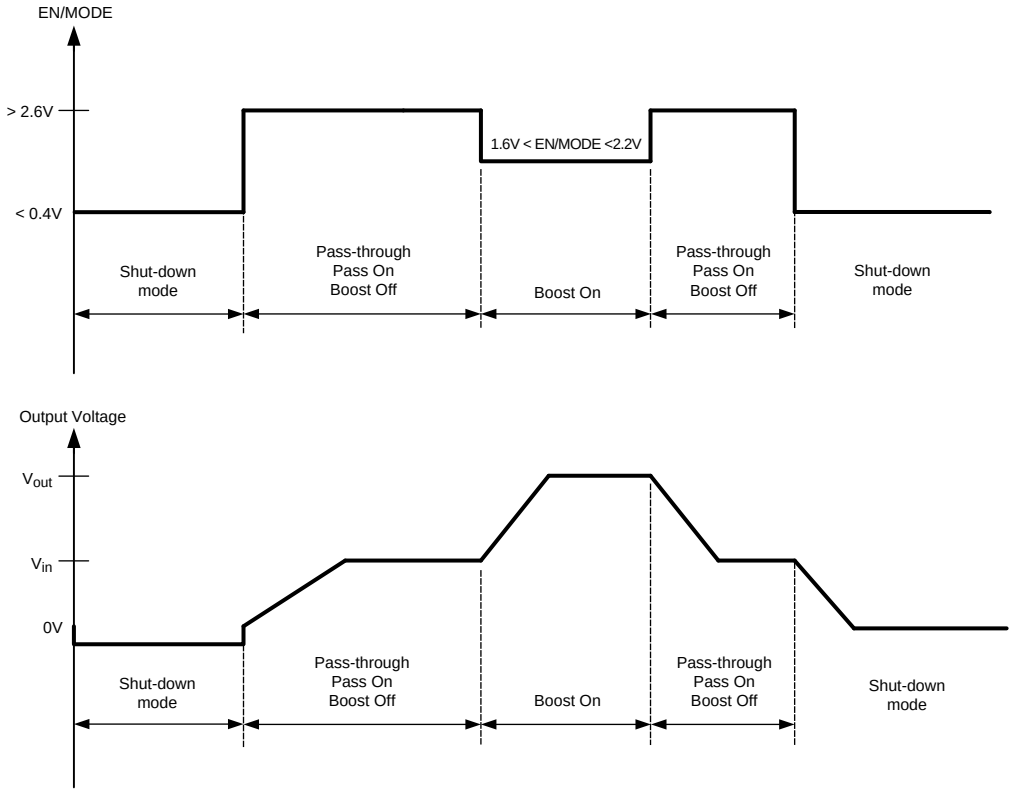

Figure 13. Typical EN/MODE Operation

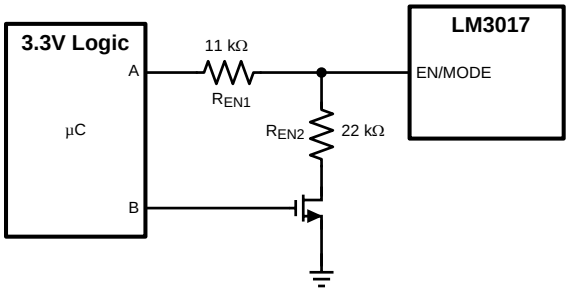

Figure 14. Typical EN/MODE Control Circuit

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CURRENT LIMIT AND SHORT CIRCUIT PROTECTION

Boost Mode

The LM3017 implements current limit protection by controlling the pass FET, Q2.

In boost mode the LM3017 features both cycle-by-cycle current limit and short circuit protection. Unlike most boost regulators, the LM3017 can protect itself from short circuits on the output by shutting off the pass FET. The boost current limit, defined by V_{CL}=170mV in the electrical characteristics table, turns off the boost FET for normal overloads on a cycle-by-cycle basis. The current is limited to V_{CL}/R_{SEN} until the overload is removed. Should the output be shorted, or otherwise pulled below V_{IN}, the inductor current will have a tendency to "run-away". This is prevented by the short circuit protection feature, defined as V_{SC} = 200mV in the electrical characteristics table. When this current limit is tripped, the current is limited to V_{SC}/R_{SEN} by controlling the pass FET. If the short persists for T_{SC} > 450µs the pass FET will be latched off. In this way, the current is limited to V_{SC}/R_{sen} until the short is removed or the time of T_{SC} = 450µs is completed. Pulling the EN/MODE pin low (<0.4V, typ) is required to reset this short circuit latch-off mode. The delay of T_{SC} = 450µs helps to prevent nuisance latch-off during a momentary short on the output.

Start-up Boost Mode

During start-up in boost mode, peak inductor current may be higher compared to normal operation. To allow for this, current limit levels and timing are different during startup. The current limit is defined by V_{LIM2} = 100mV (typ.) in the electrical characteristics table, for the first T_{LIM2} = 3.6ms (typ.). The current is limited to V_{LIM2}/R_{SEN}, for this period . Once the T_{LIM2} = 3.6ms (typ.) timer has finished, the current limit is increased to V_{SC} = 200mV (typ.). For the first T_{LIM2} = 3.6ms (typ.) of the start-up, the latch-off feature is not enabled, however the current will always be limited to V_{LIM2}/R_{SEN}. This allows the part to start-up normally. If the current limit is still tripped at the end of T_{LIM2} = 3.6ms (typ.) , the T_{SC} = 900µs (typ.) timer is started. Once the T_{SC} = 900µs (typ.) time has expired, the pass FET (Q2) is latched off. This gives a total current-limited time of T_{SC} + T_{LIM2} = 4.05ms (typ.), in cases where the LM3017 is started into a short circuit at the output.

Pass-Through Mode

In pass-through mode the power path is protected from shorts and overloads by the current limit defined as V_{LIM1} = 85mV (typ.) in the electrical characteristics table. When this current limit is tripped, the current is limited to V_{LIM1}/R_{SEN} by controlling the pass FET. If the short persists for T_{LIM1} > 900µs (typ.) the pass FET (Q2) will be latched off. In this way, the current is limited to V_{LIM1}/R_{SEN} until the short is removed or the time of T_{LIM1} = 900µs (typ.) is completed. Pulling the EN/MODE pin low (0.4V, typ.) is required to reset this latch-off mode.

Start-up Pass-Through Mode

During start-up in pass mode, the current limit is defined by V_{LIM2} = 100mV (typ.) in the electrical characteristics table, for the first T_{LIM2} = 3.6ms (typ.). The current is limited to V_{LIM2}/R_{SEN}, for this period . Once the T_{LIM2} = 3.6ms (typ.) timer has finished, the current limit is reduced to V_{LIM1} = 85mV (typ.). For the first T_{LIM2} = 3.6ms (typ.) of the start-up, the latch-off feature is not enabled, however the current will always be limited to V_{LIM2}/R_{SEN}. This higher limit allows the part to start-up normally. If the current limit is still tripped at the end of T_{LIM2} = 3.6ms (typ.), the T_{LIM1} = 900µs (typ.) timer is started. Once the T_{LIM1}= 900µs time has expired, the pass FET(Q2) is latched off. This gives a total current-limited time of T_{LIM1}+ T_{LIM2} = 4.5ms (typ.), in cases where the LM3017 is started into a short circuit at the output.

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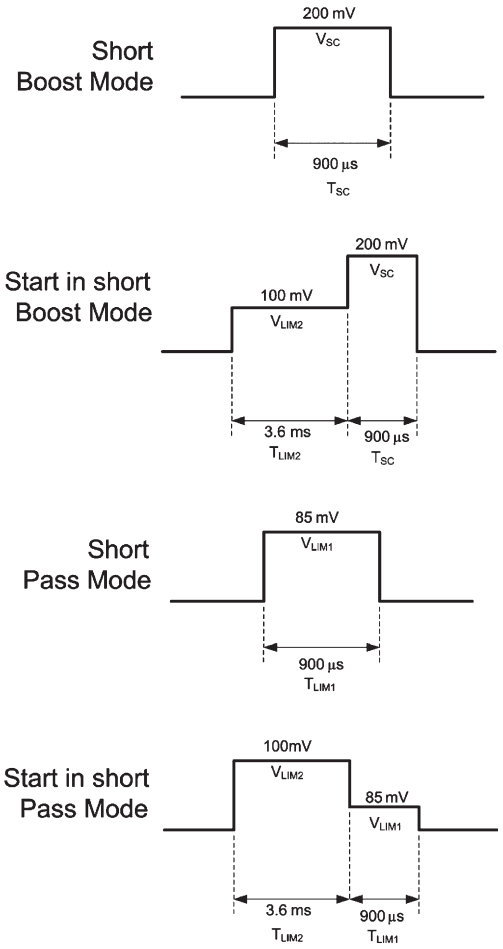

Figure 15. REPLACE THIS FIGURE. Current Limit/Short Circuit Protection

OVER VOLTAGE PROTECTION

The LM3017 incorporates output over-voltage protection (OVP). At light, or no load the minimum switch on-time may not be short enough to allow regulation in constant frequency PWM mode. In these cases the output voltage (and therefore the voltage on the FB pin) will try to rise. When the voltage on the FB pin reaches approximately 20mV higher than the regulation point, the power switch (Q1) is turned off. Q1 will remain off until the FB voltage drops back to the regulation point, at which time normal switching will begin again. In this way the LM3017 will prevent the output voltage from rising too high with no load on the output.

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APPLICATION INFORMATION

he LM3017 may be operated in either continuous or discontinuous conduction mode. The following descriptions assume continuous conduction operation (CCM). This mode of operation has higher efficiency and lower EMI characteristics than the discontinuous mode.

BOOST CONVERTER

The most common topology for the LM3017 is the boost or step-up topology. The boost converter converts a low input voltage into a higher output voltage. The basic configuration for a boost regulator is shown in Figure 16. In continuous conduction mode (when the inductor current never reaches zero at steady state), the boost regulator operates in two cycles. In the first cycle of operation, MOSFET Q is turned on and energy is stored in the inductor. During this cycle, diode D1 is reverse biased and load current is supplied by the output capacitor, COUT.

In the second cycle, MOSFET Q is off and the diode is forward biased. The energy stored in the inductor is transferred to the load and output capacitor. The ratio of these two cycles determines the output voltage. The output voltage is defined as:

$$V_{OUT} = \frac{V_{IN}}{1-D};\ D = 1 - \frac{V_{IN}}{V_{OUT}}$$

including the voltage drop of the diode:

$$V_{OUT} + V_{D1} = \frac{V_{IN}}{1-D};\ D = \frac{V_{OUT} - V_{IN} + V_{D1}}{V_{OUT} + V_{D1}}$$

where D is the duty cycle of the switch, V_{D1} is the forward voltage drop of the diode. The following sections describe selection of components for a boost converter.

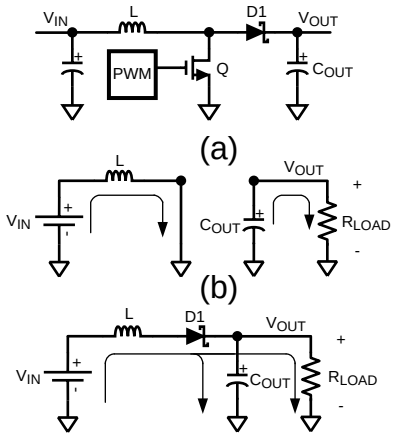

Figure 16. 4 Simplified Boost Converter Diagram (a) First cycle of operation. (b) Second cycle of operation

Programming the Output Voltage

The output voltage can be programmed using a resistor divider between the output and the feedback pins, as shown in Figure 19. The resistors are selected such that the voltage at the feedback pin is equal to V_{FB} (refer to Electrical Characteristic). R_{FBT} and R_{FBB} can be selected using the equation,

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R_{FBT}}{R_{FBB}}\right)$$

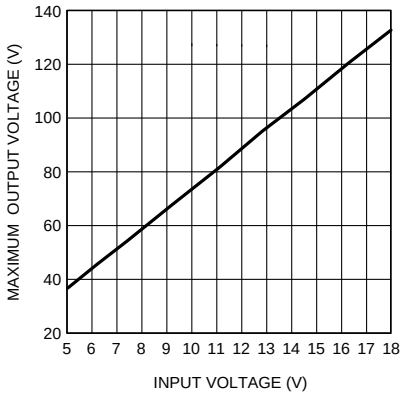

Figure 17. Maximum Output Voltage

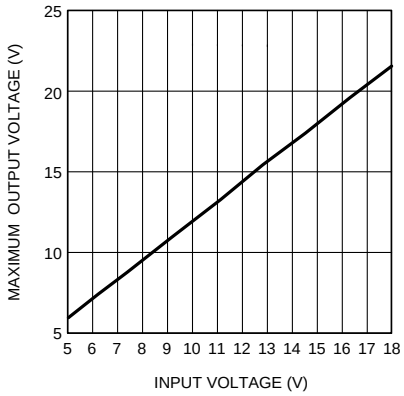

Figure 18. Minimum Output Voltage

Figure 17 shows maximum regulated output voltage based on maximum duty cycle value of 85% and by assuming a voltage drop on the output diode of 0.5V and 90% efficiency. Figure 18 shows the minimum regulated output voltage, the calculation is based on minimum on time of 126ns (typ.) that generates a minimum duty cycle equal to:

$$D_{MIN} = t_{ON(min)} \times f_S = 0.076$$

where f_S is the switching frequency and it equal to 600kHz and by assuming 90% efficiency.

Power Inductor Selection

The inductor is one of the two energy storage elements in a boost converter.

Choose the minimum I_{OUT} to determine the minimum inductance L. A common choice is to set (2 x Δi_L) from 30% to 50% of I_L. Choosing an appropriate core size for the inductor involves calculating the average and peak currents expected through the inductor. In a boost converter the inductor current I_L, the peak of the inductor current and the inductor current ripple Δi_L are equal to:

$$I_L = \frac{I_{OUT}}{1-D}$$

$$I_{Lpeak} = I_L(max) + \Delta i_L(max)$$

$$\Delta i_L = \frac{D \times V_{IN}}{2 \times L \times f_S}$$

The inductance used is a tradeoff between size and cost. Larger inductance means lower input ripple current, however because the inductor is connected to the output during the off-time only, there is a limit to the reduction in output voltage ripple. Lower inductance results in smaller, less expensive magnetics.

All the analysis in this datasheet assumes operation in continuous conduction mode. To operate in continuous conduction mode, the following conditions must be met:

$$I_L = \Delta i_L$$

$$\frac{I_{OUT}}{1-D} = \frac{D \times V_{IN}}{2 \times f_S \times L}$$

$$L \geq \frac{(1-D) \times D \times V_{IN}}{2 \times f_S \times I_{OUT}}$$

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A core size with ratings higher than these values should be chosen. If the core is not properly rated, saturation will dramatically reduce overall efficiency or damage the power stage. Choose an inductor with a saturation current value higher than I_{Lpeak}. The LM3017 senses the peak current through the switch. The peak current through the switch is the same as the peak current calculated above.

Losses due to DCR of the inductance can be easily calculated as:

$$P_L = DCR \times \left[\left(\frac{I_{OUT}}{1-D} \right)^2 + \frac{\Delta i_L^2}{12} \right]$$

No core losses have been considered.

Setting the Output Current

The maximum amount of current that can be delivered at the output can be controlled by the sense resistor, R_{SEN}. Current limit occurs when the voltage that is generated across the sense resistor equals the current sense threshold voltage, V_{SENSE}. Limits for V_{SENSE} have been specified in the electrical characteristics section. This can be expressed as:

$$I_{sw(peak)} \times R_{SEN} = V_{SENSE}$$

The peak current through the switch is equal to the peak inductor current:

$$I_{sw(peak)} = I_L(max) + \Delta i_L$$

Therefore for a boost converter:

$$I_{SW_{peak}} = \frac{I_{OUT}}{1-D} + \frac{D \times V_{IN}}{2 \times f_S \times L}$$

Combining the two equations yields an expression for R_{SEN} and includes a 20% margin on the peak of the switching current:

$$R_{SEN} = \frac{V_{SENSE}}{1.2 \times \left(\frac{I_{OUT}}{1-D} + \frac{D \times V_{IN}}{2 \times f_S \times L} \right)}$$

Evaluate R_{SEN} at the maximum and minimum V_{IN} values and choose the smallest R_{SEN} calculated.

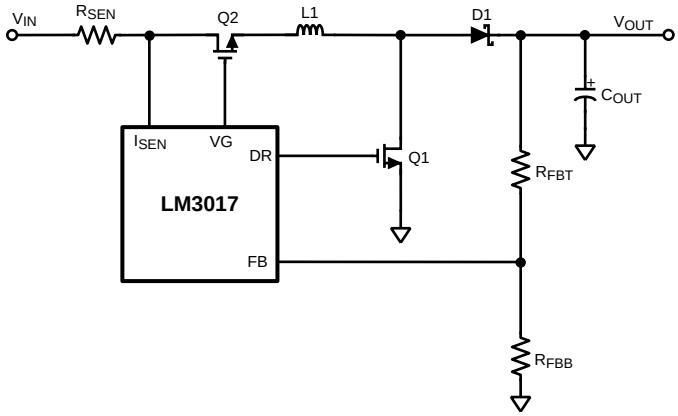

Figure 19. Adjusting the Output Voltage

Additional Slope Compensation

It is good design practice to only add as much slope compensation as needed to avoid instability. Additional slope compensation (see Figure 23) minimizes the influence of the sensed current in the control loop. With very large slope compensation the control loop characteristics are similar to a voltage mode regulator which compares the error voltage to a saw tooth waveform rather than the inductor current. It is possible to calculate the minimum value of RS in order to meet the equation (see CONTROL LOOP COMPENSATION IN DETAIL section):

$M_C > M_2/2$

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Hense:

$$R_S \geq \frac{1}{K} \times \left[\frac{R_{SEN} \times (V_{OUT} - V_{IN}(min))}{2 \times L \times f_S} - V_{SL} \right]$$

Where K = 40 µA.

If the result of the previous equation is negative it means that no additional slope compensation is needed, anyway a 100Ω resistor is recommended. For details see SLOPE COMPENSATION RAMP section.

Current Limit with Additional Slope Compensation

If an external slope compensation resistor is used then the internal control signal will be modified and this will have an effect on the current limit.

If R_S is used, then this will add to the existing slope compensation. The command voltage, V_{CS}, will then be given by:

$V_{CS} = V_{SL} + \Delta V_{SL}$

Where V_{SENSE} is a defined parameter in the electrical characteristics section, V_{SL} is the amplitude of the internal compensation ramp and $\Delta V_{SL} = R_S$ x K is the additional slope compensation generated as discussed in the SLOPE COMPENSATION RAMP section. This changes the equation for R_{SEN} to:

$$R_{SEN} = \frac{V_{SENSE} - D \times V_{CS}}{\left(\frac{I_{OUT}}{1-D} + \frac{D \times V_{IN}}{2 \times f_S \times L} \right)}$$

Note that since $\Delta V_{SL} = R_S$ x K as defined earlier, R_S can be used to provide an additional method for setting the current limit. In some designs R_S can also be used to help filter noise to keep the I_{SEN} pin quiet. Dissipation due to R_{SEN} resistor is equal to:

$$P_{SEN} = R_{SEN} \times \left[\left(\frac{I_{OUT}}{1-D} \right)^2 + \frac{\Delta i_{Lpp}^2}{12} \right]$$

Power Diode Selection

Observation of the boost converter circuit shows that the average current through the diode is the average output current, and the peak current through the diode is the peak current through the inductor. The peak diode current can be calculated using the formula:

$I_{D(Peak)} = [I_{OUT} / (1-D)] + \Delta i_L$

The peak reverse voltage for a boost converter is equal to the regulator output voltage. The diode must be capable of handling this peak reverse voltage as well as the output rms current. To improve efficiency, a low forward drop Schottky diode is recommended due to low forward drop and near-zero reverse recovery time. The overall efficiency becomes more dependent on the selection of D at low duty cycles, where the boost diode carries the load current for an increasing percentage of the time. This power dissipation can be calculated by checking the typical diode forward voltage VD, from the I-V curve on the diode's datasheet and the multiplying it by IO. Diode data sheets will also provide a typical junction-to-ambient thermal resistance, θJ_A, which can be used to estimate the operating die temperature of the Schottky. Multiplying the power dissipation ($P_D = I_O$ x V_D) by θ_{JA} gives the temperature rise. The diode case size can then be selected to maintain the Schottky diode temperature below the operational maximum.

Low Side MOSFET Selection (switching MOSFET)

The drive pin, DR, of the LM3017 must be connected to the gate of an external MOSFET. In a boost topology, the drain of the external N-Channel MOSFET is connected to the inductor and the source is connected to the ground. The drive pin voltage, V_{DR}, depends on the input voltage (see typical performance characteristics).

The selected MOSFET directly affects the efficiency. The critical parameters for selection of a MOSFET are:

1. Minimum threshold voltage, $V_{TH(MIN)}$
2. On-resistance, $R_{DS(ON)}$
3. Total gate charge, Q_g
4. Reverse transfer capacitance, C_{RSS}

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5. Maximum drain to source voltage, $V_{DS(MAX)}$

The off-state voltage of the MOSFET is approximately equal to the output voltage. $V_{DS(MAX)}$ of the MOSFET must be greater than the output voltage plus the voltage drop across the output diode (20% margin recommended).

The power losses in the MOSFET can be categorized into conduction losses, gate charging losses and switching losses. $R_{DS(ON)}$ is needed to estimate the conduction losses. The conduction loss, P_{COND}, is the I2R loss across the MOSFET. The maximum conduction loss is given by:

$$P_{COND} = \left(\frac{I_{OUT}}{1 - D_{MAX}} \right)^2 \times D_{MAX} \times R_{DS(on)}$$

where D_{MAX} is the maximum duty cycle.

$$D_{MAX} = 1 - \frac{V_{IN}(min)}{V_{OUT}}$$

To take in account the increase in MOSFET on resistance due to heating, a factor of 1.3 is introduced, hence:

$$P_{COND\_real} = P_{COND(max)} \text{ x } 1.3$$

Gate charging loss, P_G, results from the current required to charge and discharge the gate capacitance of the power MOSFET and is approximated as:

$$P_G = VCC \text{ x } Q_G \text{ } f_S$$

Q_G is the total gate charge of the MOSFET. Gate charge loss differs from conduction and switching losses because the actual dissipation occurs in the LM3017 and not in the MOSFET itself. This loss, P_{VCC}, is estimated as:

$$P_{VCC} = (V_{IN} - VCC) \text{ x } Q_G \text{ x } f_S$$

The switching losses are very difficult to calculate due to changing parasitics of a given MOSFET in operation. Often, the individual MOSFET datasheet does not give enough information to yield a useful result. The following formulas give a rough idea how the switching losses are calculated:

$$P_{SW} = \frac{I_L \times V_{OUT}}{2} \times f_S \times (t_{LH} + t_{HL})$$

Where t_{LH} and t_{HL} are rise and fall times of the MOSFET.

Pass MOSFET Selection (High Side MOSFET)

The VG pin drives the gate of the high side MOSFET (Pass FET Q2). This requires special considerations. When the output is shorted, this FET must sustain the full input voltage and the short circuit current simultaneously. This is due to the fact that the controller regulates the short circuit current in a quasi-linear manner, through Q2. This power pulse will only last for T_{LIM2} or T_{SC}, depending on the operational mode. Therefore, the designer must carefully examine the SOA curve for the desired FET before committing to the design. The following equations give the maximum energy pulses that Q2 is required to survive:

$$E_1 \geq (V_{in} + 2) \times \left(\frac{V_{LIM2}}{R_{sen}} \right) \times T_{LIM2}$$

$$E_2 \geq (V_{in} + 2) \times \left(\frac{V_{SC}}{R_{sen}} \right) \times T_{SC}$$

These two energy points must fall within the SOA of the selected FET. In addition, Q2 should have a low threshold voltage and low $R_{DS(on)}$ for high efficiency. Power dissipation during boost mode is given by:

$$P_{Q2} = R_{DS(on)} \times \left[\left(\frac{I_{OUT}}{1 - D} \right)^2 + \frac{\Delta i_{Lpp}^2}{12} \right]$$

Input Capacitor Selection

Due to the presence of an inductor at the input of a boost converter, the input current waveform is continuous and triangular. The inductor ensures that the input capacitor sees fairly low ripple currents. However, as the input capacitor gets smaller, the input ripple goes up. The rms current in the input capacitor is given by:

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$$I_{C_{IN}(rms)} = \frac{\Delta i_L}{\sqrt{3}} = \frac{(V_{OUT} - V_{IN}) \times V_{IN}}{\sqrt{12} \times V_{OUT} \times f_S}$$

The input capacitor must be capable of handling this rms current. Although the input capacitor is not as critical in a boost application, low values can cause impedance interactions. Therefore a good quality capacitor should be chosen in the range of 10 µF to 20 µF. Furthermore, a low ESR 0.1µF ceramic bypass capacitor is recommended in order to avoid transients and ringing due to parasitics. Bypass capacitors must be placed as close as possible to the V_{IN} pin and grounded close to the GND pin on the IC to minimize additional ESR and ESL. The following formula can be used to define the input voltage ripple:

$$\Delta V_{ipp} = \Delta i_{LPP} \times \sqrt{ESR^2 + \left(\frac{1}{8 \times f_S \times C_i}\right)^2}$$

Where $\Delta i_{Lpp} = 2 \times \Delta i_L$ is the peak-to-peak inductor current ripple and ΔV_{ipp} is the peak-to-peak input voltage ripple. Many times it is necessary to use an electrolytic capacitor on the input in parallel with the ceramics. The ESR of this capacitor can help to damp any ringing on the input supply caused by long power leads.

Output Capacitor Selection

The output capacitor in a boost converter provides all the output current when the inductor is charging and it determines the steady state output voltage ripple ΔV_{Opp}. As a result it sees very large ripple currents. The output capacitor should be selected based on its capacitance C_O, its equivalent series resistance ESR and its RMS current rating. The rms current in the output capacitor is:

$$I_{C_{OUT}(rms)} = \sqrt{(1-D) \times \left[I_{OUT}^2 \times \frac{D}{(1-D)^2} + \frac{\Delta i_L^2}{3}\right]}$$

Where Δi_L is the inductor ripple current and D is the duty cycle.

The magnitude of the output voltage ripple during the on-time is equal to the ripple voltage during the off-time and it is composed of two parts. For simplicity the analysis will be performed for off-time only.

The first part of the ripple voltage is the surge created as the output diode D turns on. At this point inductor/diode current is at the peak value, and the ripple voltage increase can be calculated as:

$\Delta V_{O1} = I_{PK} \times ESR$

Where $I_{PK} = I_{OUT} / (1-D)$.

The second portion of the ripple voltage is the increase due to the charging of CO through the output diode. This portion can be approximated as:

$\Delta V_{O2} = (I_O / C_O) \times (D / f_S)$

The following formula can be used to define the output voltage ripple:

$$\Delta V_{Opp} = ESR \times \left(\frac{I_{OUT}}{1-D} + \Delta i_L\right) + \frac{I_{OUT} \times D}{C_o \times f_S}$$

The ESR of the output capacitor(s) has a strong influence on the slope and direction of the output voltage ripple. Capacitors with high ESR such as tantalum and aluminum electrolytic create an output voltage ripple that is dominated by ΔV_{O1} with a shape shown in Figure 20. Ceramic capacitors, in contrast, have a very low ESR and lower capacitance and the shape of the output voltage ripple is dominated by ΔV_{O2} with a shape shown in Figure 21.

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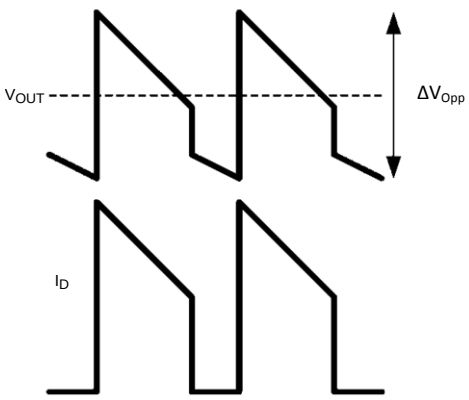

Figure 20. ΔV_{Opp} Using High ESR Capacitors

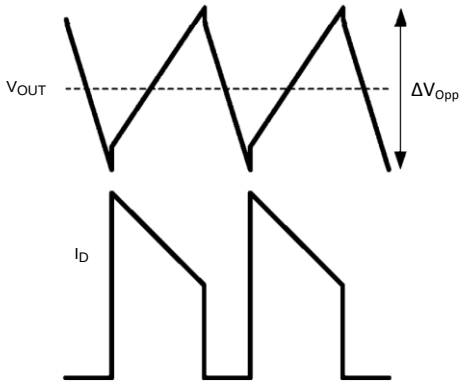

Figure 21. ΔV_{Opp} Using Low ESR Capacitors

Ceramic capacitors are recommended with a typical value between 10µF and 100µF. The minimum quality dielectric that is suitable for switching power supply output capacitors is X5R, while X7R (or better) is preferred. Careful attention must be paid to the DC voltage rating and case size, as ceramic capacitors can lose 60% or more of their rated capacitance at the maximum DC voltage. This is the reason that ceramic capacitors are often de-rated to 50% of their capacitance at their working voltage.

VCC Decoupling Capacitor

The internal bias of the LM3017 comes from either the internal bias voltage generator as shown in the block diagram or directly from the voltage at the VIN pin. At input voltages lower than 6V the internal IC bias is the input voltage and at voltages above 6V the internal bias voltage generator of the LM3017 provides the bias. A good quality ceramic bypass capacitor must be connected from the VCC pin to the PGND pin for proper operation. This capacitor supplies the transient current required by the internal MOSFET driver, as well as filtering the internal supply voltage for the controller. A value of between 0.47µF and 4.7µF is recommended.

Thermal Considerations

The majority of power dissipation and heat generation comes from FETs and diode. Selecting MOSFETs with exposed pads will aid the power dissipation of these devices. Careful attention to RDS(on) at high temperature should be observed. Diode data sheets will provide a typical junction-to-ambient thermal resistance θ_{JA}, which can be used to estimate the operating die temperature of the Schottky. Multiplying the power dissipation by θ_{JA} gives the temperature rise. The diode case size can then be selected to maintain the Schottky diode temperature below the operational maximum. Larger case sizes generally have lower θ_{JA} and lower forward voltage drop.

Thermal Protection

Internal thermal shutdown circuitry is provided to protect the LM3017 in the event that the maximum junction temperature is exceeded. When activated, typically at 165°C, the controller is forced into a low power standby state, disabling the output driver and the VCC regulator. After the temperature is reduced (typical hysteresis is 10°C) the VCC regulator will be re-enabled and the LM3017 will perform a soft-start.

SLOPE COMPENSATION RAMP

The LM3017 uses a current mode control scheme. The main advantages of current mode control are inherent cycle-by-cycle current limit for the switch, simpler control loop characteristics and excellent line and load transient response. However there is a natural instability due to sub-harmonic oscillations that will occur for duty cycles, D, greater than 50% if slope compensation is not addressed.

$$M_C > M_2/2$$

For best **input noise immunity:**

$$M_C = M_2$$

For best **sub-harmonic suppression:**

$$M_C = M_2/2$$

Where:

- $\mathbf{M_C}$ is the slope of the compensation ramp.

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- **M_1** is the slope of the inductor current during the ON time.
- **M_2** is the slope of the inductor current during the OFF time.
- **R_{SEN}** is the sensing resistor value.
- **V_{OUT}** represents the output voltage.
- **V_{IN}** represents the input voltage.
- **A** is equal to 0.86 and it is the internal sensing amplification of the LM3017.

In the case of the boost topology:

$$M_1 = [V_{IN} / L] \times R_{SEN} \times A$$
$$M_2 = [(V_{OUT} - V_{IN}) / L] \times R_{SEN} \times A$$

The compensation ramp has been added internally in the LM3017. The slope of this compensation ramp has been selected to satisfy most applications, and its value depends on the switching frequency. This slope can be calculated using the formula:

$$M_C = V_{SL} \times f_S$$

In the above equation, V_{SL} is the amplitude of the internal compensation ramp and f_S is the controller's switching frequency. Limits for V_{SL} have been specified in the electrical characteristics section.

In order to provide the user additional flexibility, a patented scheme has been implemented inside the IC to increase the slope of the compensation ramp externally, if the need arises. Adding a single external resistor, R_S (as shown in Figure 23) increases the amplitude of the compensation ramp as shown in Figure 22.

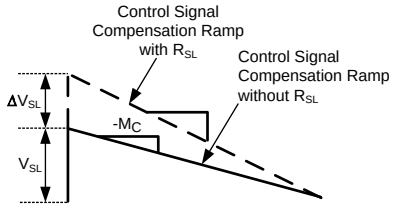

Figure 22. Additional Slope Compensation Added Using External Resistor R_S

Where,

$\Delta V_{SL} = K \times R_s$

K = 40 µA typically and changes slightly as the switching frequency changes.

A more general equation for the slope compensation ramp, MC, is shown below to incluse ΔV_{SL} cause by the resistor R_s.

$M_C = (V_{SL} + \Delta V_{SL}) \times f_s$

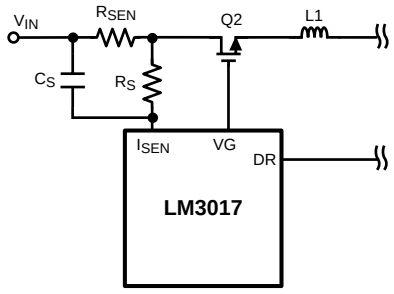

Figure 23. Increasing the Slope of the Compensation Ramp

An additional capacitor C_S could be added if the sensing signal generated by R_{SEN} is very noisy (parasitic circuit capacitance, inductance and gate drive current create a spike in the current sense voltage at the point where Q1 turns on.) The time constant R_{SEN} x C_S should be long enough to reduce the parasitics spike without significantly affecting the shape of the actual current sense voltage (a typical range is from 100pF to 2.2nF).

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CONTROL LOOP COMPENSATION IN DETAIL

The LM3017 uses peak current-mode PWM control to correct changes in output voltage due to line and load transients. Peak current-mode provides inherent cycle-by-cycle current limiting, improved line transient response, and easier control loop compensation. The control loop is comprised of two parts. The first is the power stage, which consists of the pulse width modulator, output filter, and the load. The second part is the error amplifier. Figure 24 shows the regulator control loop components.

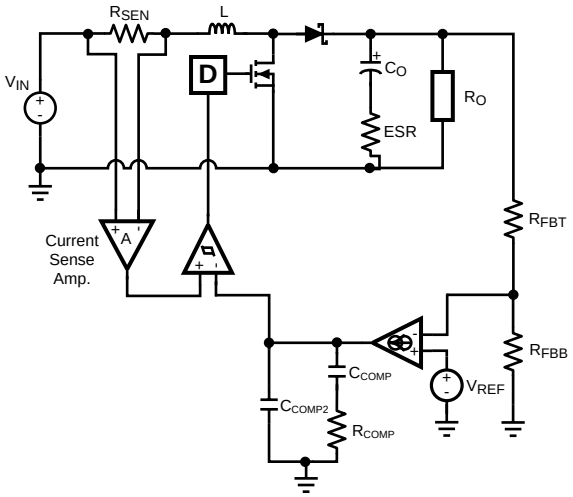

Figure 24. Power Stage and Error Amp

The power stage in a CCM peak current mode boost converter consists of the DC gain, G_{VC0}, a single low frequency pole, f_P, the ESR zero, f_Z, a right-half plane zero, f_R, and a double pole resulting from the sampling of the peak current. The power stage transfer function (also called the Control-to-Output transfer function) can be written:

$$G_{VC}(s) = G_{VC0} \times \frac{\left(1 - \frac{s}{\omega_R}\right)\left(1 + \frac{s}{\omega_Z}\right)}{\left(1 + \frac{s}{\omega_P}\right)\left(1 + \frac{s}{\omega_n} + \frac{s^2}{\omega_n^2}\right)}$$

The DC gain is defined as:

$$G_{VC0} = \frac{R_O(1-D)}{2 \times A \times R_{SEN}}$$

Where: $R_O = V_{OUT} / I_{OUT}$

In the equation for G_{VC0}, DC gain is highest when input voltage and output current are at the maximum. The system ESR zero is:

$$f_Z = \frac{\omega_Z}{2\pi} = \frac{1}{2\pi \times C_O \times ESR}$$

The low frequency pole is:

$$f_P = \frac{\omega_P}{2\pi} = \frac{2}{2\pi \times C_O \times (ESR + R_O)}$$

The right-half plane zero is:

$$f_R = \frac{\omega_R}{2\pi} = \frac{R_O \times (1-D)^2}{2\pi \times L}$$

The sampling double pole quality factor is:

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$$Q_n = \frac{1}{\pi \times \left[(1-D) \times \left(1 + \frac{M_C}{M_1} \right) - 0.5 \right]}$$

The sampling double corner frequency is: $\omega_n = \pi \times f_S$

The natural inductor current slope is: $M_1 = R_{SEN} \times V_{IN} / L$

The external ramp slope is: $M_C = (V_{SL} + \Delta V_{SL}) \times f_S$

A step-up converter produces an undesirable right-half plane zero in the regulation feedback loop. This requires compensating the regulator such that the crossover frequency occurs well below the frequency of the right-half plane zero

COMPENSATION NETWORK COMPONENTS CALCULATIONS

As shown in Figure 24, the LM3017 uses a compensation network base on a transconductance amplifier. The closed loop transfer function is defined as:

$T(s) = G_{VA}(s) \times G_{VC}(s)$

Where $G_{VA}(s)$ is the transfer function implemented by the compensation network:

$$G_{VA}(s) = \frac{\omega_{P1}\left(1 + \frac{s}{\omega_{Z1}}\right)}{s\left(1 + \frac{s}{\omega_{P2}}\right)}$$

$$\omega_{Z1} = \frac{1}{C_{COMP} \times R_{COMP}}$$

$$\omega_{P1} = \frac{G_m \times \frac{R_{FBB}}{R_{FBB} + R_{FBT}}}{C_{COMP} + C_{COMP2}}$$

$$\omega_{P2} = \frac{C_{COMP} + C_{COMP2}}{C_{COMP} \times C_{COMP2} \times R_{COMP}}$$

To stabilize the regulator, ensure that the regulator crossover frequency is less than or equal to one-fifth of the right-half plane zero:

$$f_C \leq \frac{f_R}{5}$$

To determine the crossover frequency it is important to note that, at that frequency, the compensation impedance (Z_{COMP}) is dominated by a resistor, and the output impedance (Z_{OUT}) is dominated by the impedance of an output capacitor. Therefore, when solving for the crossover frequency, the equation (by definition of the crossover frequency) of the loop gain is simplified to:

$$|T| = \frac{V_{FB}}{V_{OUT}} \times \frac{V_{IN}}{V_{OUT}} \times G_m \times \frac{1}{2\pi \times f_C \times C_O} \times R_{COMP} \times \frac{1}{A \times R_{SEN}} = 1$$

Where:

- **|T|** is the loop gain magnitude.
- $\mathbf{V_{FB}}$ is feedback voltage, 1.275V.
- $\mathbf{V_{OUT}}$ is the output voltage.
- $\mathbf{V_{IN}}$ is the input voltage
- $\mathbf{G_m}$ is the error amplifier transconductance.
- $\mathbf{Z_{COMP}}$ is the impedance of the compensation network from the COMP pin to ground.
- $\mathbf{R_{SEN}}$ is the current sensing resistor.
- **A** is equal to 0.86 and it is the internal sensing amplification of the LM3017.

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- **C_O** is the output capacitor value.

Solve for R_{COMP}:

$$R_{COMP} = \frac{2\pi \times f_C \times C_O \times V_{OUT}^2}{V_{FB} \times V_{IN} \times G_m} \times A \times R_{SEN}$$

Once the compensation resistor is known, set the zero formed by the compensation capacitor and resistor to one-fourth of the crossover frequency:

$$C_{COMP} = \frac{2}{\pi \times f_C \times R_{COMP}}$$

Where C_{COMP} is the compensation capacitor.

he high frequency capacitor C_{COMP2}, is chosen to cancel the zero introduced by output capacitance ESR:

$$C_{COMP2} = \frac{ESR \times C_O}{R_{COMP}}$$

For optimal transient performance, R_{COMP} and C_{COMP} might need to be adjusted by observing the load transient response.

For detailed explanation on how to select the right compensation components for a boost topology please see Application Note 1286 and Application Note 1994.

COMPENSATION DESIGN EXAMPLE

Referring to Figure 29:

input voltage **V_{IN}**	8 V to 12 V
output voltage **V_{OUT}**	15 V
output current **I_{OUT}**	1 A
switching frequency **f_S**	600 kHz
duty cycle **D** (considering losses)	0.482 with VIN = 8 V
	0.223 with VIN = 12 V
right-half plane zero **f_R**	136.187 kHz when V_{IN} = 8 V
	306.421 kHz when V_{IN} = 12 V
inductor **L**	4.7 µH
output capacitance **C_O** (consireding derating due to applied voltage)	33 µF

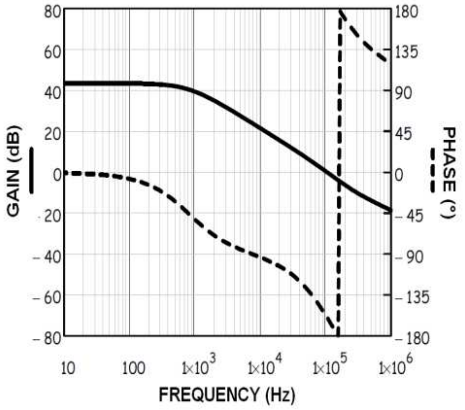

Figure 25. Control-to-output Transfer Function Bode Plot $G_{VC}(s)$, V_{IN}=8V, V_{OUT}=15V, I_{OUT}=1A

By choosing the crossover frequency as:

f_C = 20 kHz = f_S / 20 f_R / 5

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PARAMETER	CALCULATED VALUE	ACTUAL VALUE
R_{COMP}	3.42 kΩ	3.4 kΩ
C_{COMP}	9.306 nF	10 nF
C_{COMP2}	96.48 pF	100 pF

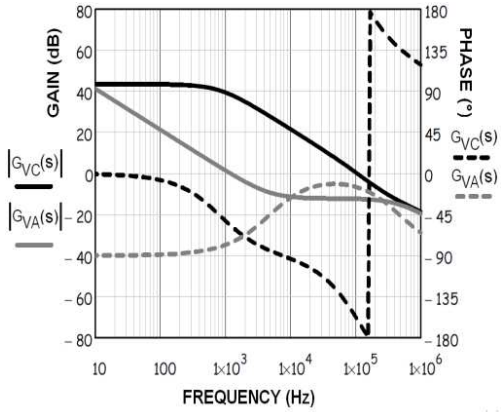

Figure 26. $G_{VC}(s)$ and Compensation Network $G_{VA}(s)$ Bode Plots, V_{IN}=8V, V_{OUT}=15V, I_{OUT}=1A

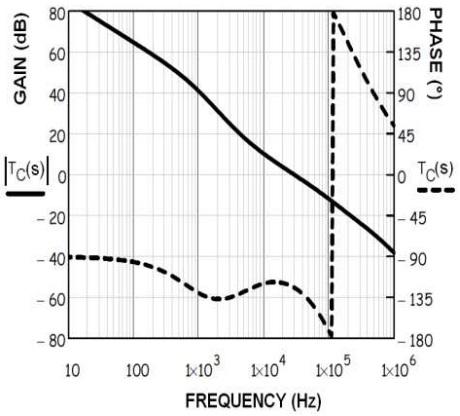

Figure 27. Closed Loop Bode Plot T(s), V_{IN}=8V, V_{OUT}=15V, I_{OUT}=1A

LAYOUT GUIDELINES

Good board layout is critical for switching controllers such as the LM3017. First the ground plane area must be sufficient for thermal dissipation purposes and second, appropriate guidelines must be followed to reduce the effects of switching noise. Switch mode converters are very fast switching devices. In such devices, the rapid increase of input current combined with the parasitic trace inductance generates unwanted voltage noise spikes. The magnitude of this noise tends to increase as the output current increases. This parasitic spike noise may create electromagnetic interference (EMI), and can also cause problems in device performance. Therefore, care must be taken in layout to minimize the effect of this switching noise.

FILTER CAPACITORS

Ceramic filter capacitors are most effective when the inductance of the current loops that they filter is minimized. Place C_{BYP} as close as possible to the VIN and GND pins of the LM3017. Place C_{VCC} next to the VCC and GND pins of the LM3017 (refer to Figure 29 for designators).

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SENSE LINES

The current sensing circuit in current mode devices can be easily effected by switching noise. This noise can cause duty cycle jitter which leads to increased spectral noise. R_{SEN} should be connected to the ISEN pin with a separate trace made as short as possible, it is also recommended to route the trace the connects the VIN pin to the input voltage as close as possible to R_{SEN}. Route this trace away from the inductor and the switch node (where D1, Q1, and L1 connect). For the voltage loop, keep $R_{FBB/T}$ close to the LM3017 and run a trace as close as possible to the positive side of C_O. As with the ISEN line, the FB line should be routed away from the inductor and the switch node. These measures minimize the length of high impedance lines and reduce noise pickup.

COMPACT LAYOUT

The most important layout rule is to keep the AC current loops as small as possible. Figure 28 shows the current flow of a boost converter. The top schematic shows a dotted line which represents the current flow during on-state and the middle schematic shows the current flow during off-state. The bottom schematic shows the currents we refer to as AC currents. They are the most critical ones since current is changing in very short time periods. The dotted line traces of the bottom schematic are the ones to make as short as possible. In a boost regulator the primary switching loop consists of the output capacitor, diode and MOSFET. Minimizing the area of this loop reduces the stray inductances and minimizes noise and possible erratic operation (see Figure 28 for a layout example). The output capacitor(s) should be placed as close as possible to the diode cathode and MOSFET GND.

GROUND PLANE AND VIAS

A ground plane in the printed circuit board is recommended as a means to connect the quiet end (input voltage ground side) of the input filter capacitor to the output filter capacitors and the PGND pin of the controller. Connect all the low power ground connections directly to the regulator AGND. Connect the AGND and PGND pins together through a copper area covering the entire underside of the device. Place several vias in this underside copper area to ground plane. If a via is needed to connect the sensing resistor to the ISEN pin, then place that via in the inner side of the sensing resistor such that no current flow occurs. Place several vias from the ground side of the output capacitor(s) to ground place, that will minimize the path for AC current. The PGND and AGND pins have to be connected to the same ground very close to the IC. To avoid ground loop currents attach all the grounds of the system only at one point.

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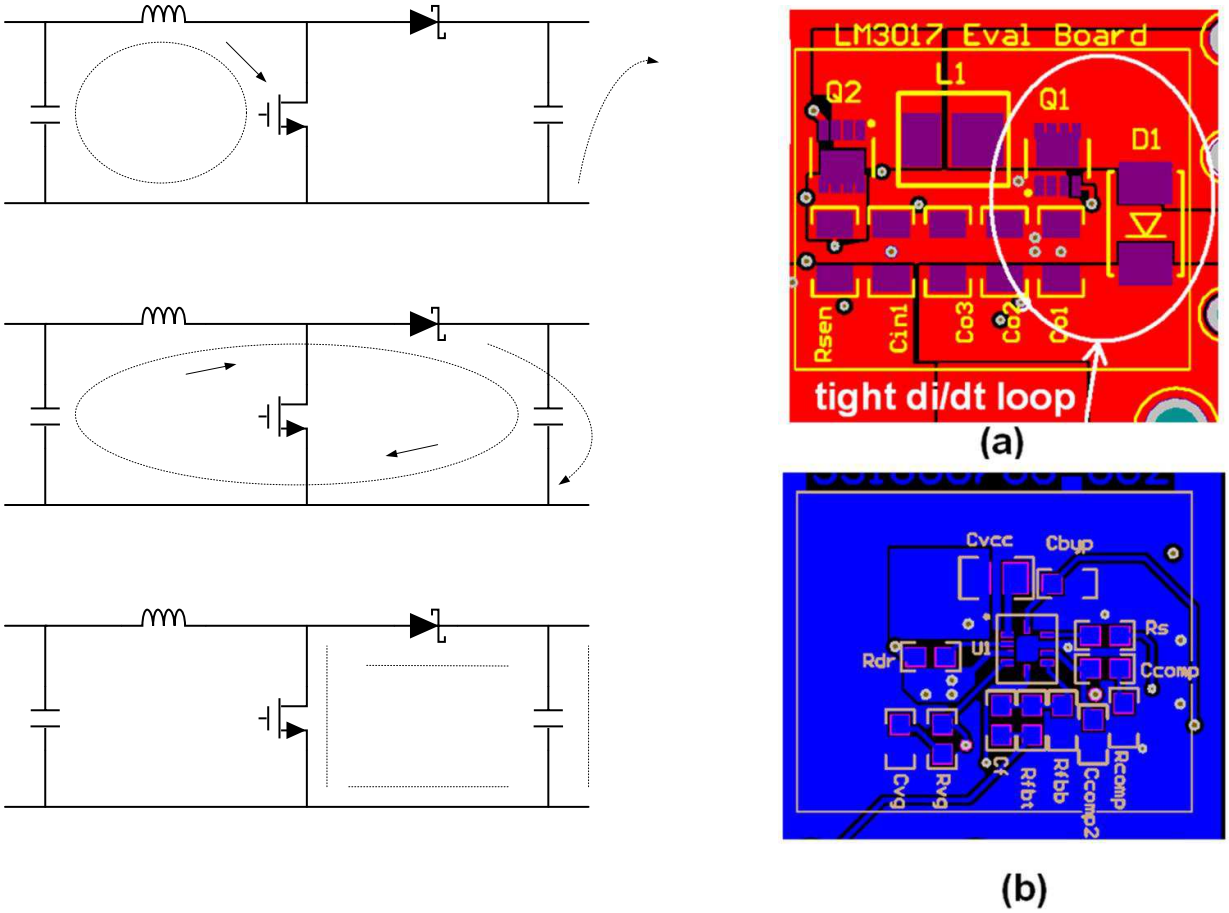

Figure 28. Current Flow in a Boost Application (left) and Layout Example (right) (a) top layer (b) bottom layer

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APPLICATION CIRCUITS

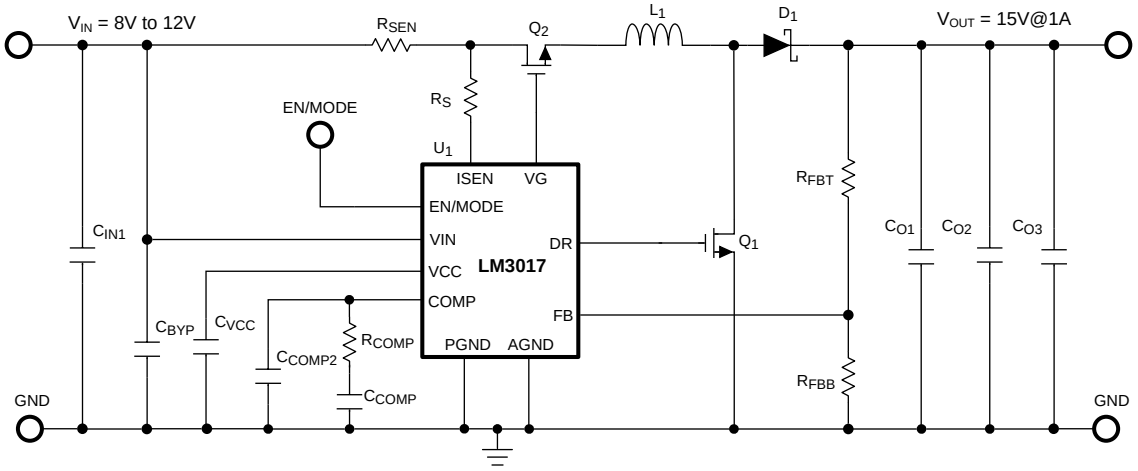

Figure 29. Example 1A High Efficiency Step-Up (Boost) Converter

Bill of Materials (BOM) LM3017

Designation	Description	Size	Manufacturer Part #	Vendor
C_{IN1}	Cap 22µF 25V X5R	1206	GRM31CR61E226KE15L	Murata
C_{O1},C_{O2}, C_{O3}	Cap 22µF 25V X5R	1206	GRM31CR61E226KE15L	Murata
C_{COMP}	Cap 0.022µF	0603	C0603C103J1RACTU	Kemet
C_{COMP2}	Cap 1000pF	0603	C1608C0G1H101J	TDK
C_{BYP}	Cap 0.1µF 25V X7R	0603	06033C104KAT2A	AVX
C_{VCC}	Cap 0.47µF 16V X7R	0805	C2012X7R1C474K	TDK
R_{COMP}	RES, 3.4k ohm, 1%, 0.1W	0603	CRCW06033K40FKEA	Vishay
R_{FBT}	RES, 21.5k ohm, 1%, 0.1W	0603	CRCW060321K5FKEA	Vishay
R_{FBB}	RES, 2k ohm, 1%, 0.1W	0603	CRCW06032K00FKEA	Vishay
R_S	RES, 100 ohm, 1%, 0.1W	0603	CRCW0603100RFKEA	Vishay
R_{SEN}	RES, 0.03 ohm, 1%, 1W	1206	WSLP1206R0300FEA	Vishay
Q_1	NexFET™ N-CH, 25V, 60A, $R_{DS(on)}$= 4.4mohm	8-SON	CSD16323Q3	TI
Q_2	NexFET™ N-CH, 25V, 60A, $R_{DS(on)}$= 4.3mohm	8-SON	CSD16340Q3	TI
D_1	Diode Schottky, 30V, 2A	SMB	20BQ030TRPBF	Vishay
L_1	Shielded Inductor, 4.7µH, 2.3A	4mm L × 4mm W × 1.85mm H	MPI4040R3-4R7-R	Cooper
U_1	LM3017			TI

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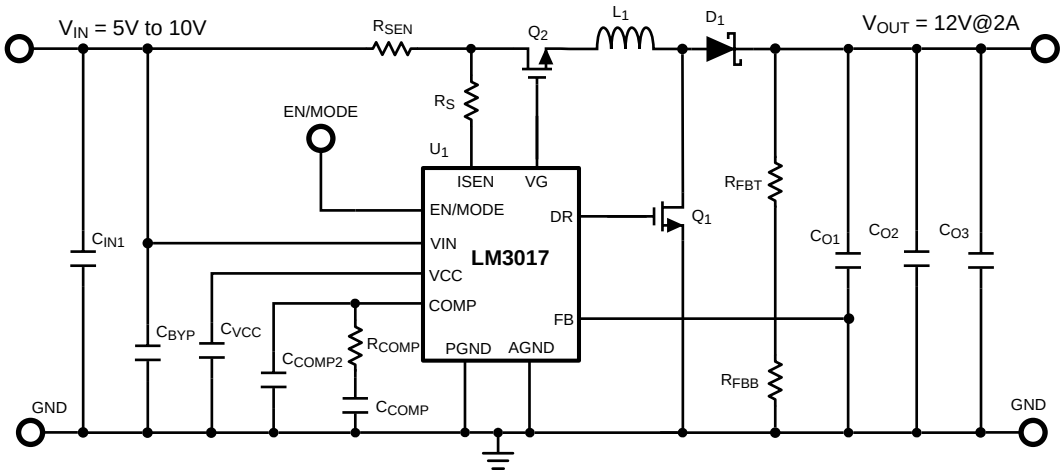

Figure 30. Example 2A High Efficiency Step-Up (Boost) Converter

Bill of Materials (BOM) LM3017

Designation	Description	Size	Manufacturer Part #	Vendor
C_{IN1}	Cap 220µF 16V	Radial	EEE-FC1C221P	Panasonic
C_{O1},C_{O2}, C_{O3}	Cap 22µF 25V X5R	1206	GRM31CR61E226KE15L	Murata
C_{COMP}	Cap 0.047µF	0603	06033C473JAT2A	AVX
C_{COMP2}	Cap 470pF	0603	06031C471JAT2A	AVX
C_{BYP}	Cap 0.1µF 25V X7R	0603	06033C104KAT2A	AVX
C_{VCC}	Cap 0.47µF 16V X7R	0805	C2012X7R1C474K	TDK
R_{COMP}	RES, 1kΩ, 1%, 0.1W	0603	CRCW06031K00FKEA	Vishay
R_{FBT}	RES,16.9kΩ, 1%, 0.1W	0603	CRCW060316K9FKEA	Vishay
R_{FBB}	RES, 2kΩ, 1%, 0.1W	0603	CRCW06032K00FKEA	Vishay
R_S	RES, 100Ω, 1%, 0.1W	0603	CRCW0603100RFKEA	Vishay
R_{SEN}	RES, 0.01Ω, 1%, 1W	1206	WSLP1206R0100FEA	Vishay
Q_1	NexFET™ N-CH, 25V, 60A, $R_{DS(on)}$= 4.4mΩ	8-SON	CSD16323Q3	TI
Q_2	NexFET™ N-CH, 25V, 60A, $R_{DS(on)}$= 4.3mΩ	8-SON	CSD16340Q3	TI
D_1	Diode Schottky, 30V, 5A	SOD128	PMEG3050BEP	NXP
L_1	Shielded Inductor, 2.2µH, 10A	6.36mm L × 6.56mm W × 3.1mm H	XAL6030-182ME	Coilcraft
U_1	LM3017			TI

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM3017LE/NOPB	ACTIVE	WQFN	NKL	10	1000	Green (RoHS & no Sb/Br)	SN	Level-3-260C-168 HR	-40 to 125	SK6B	Samples
LM3017LEX/NOPB	ACTIVE	WQFN	NKL	10	4500	Green (RoHS & no Sb/Br)	SN	Level-3-260C-168 HR	-40 to 125	SK6B	Samples

(1) The marketing status values are defined as follows:
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NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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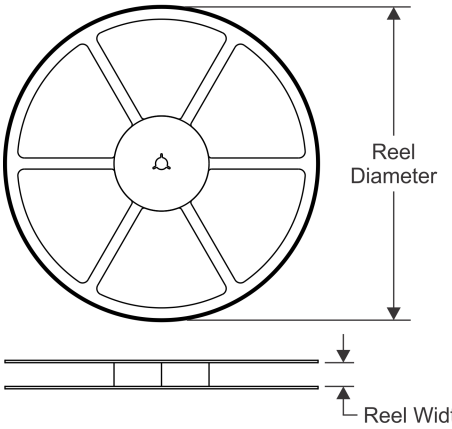

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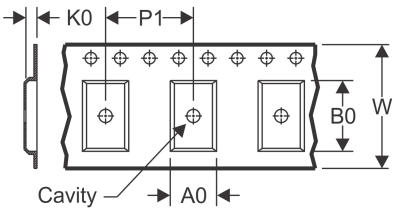
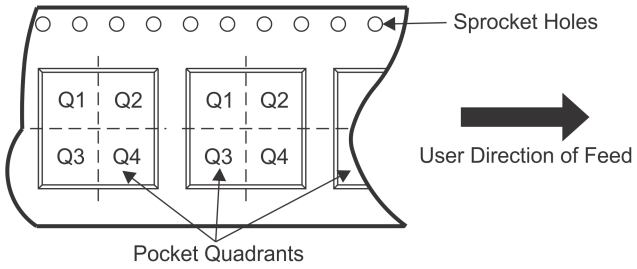


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

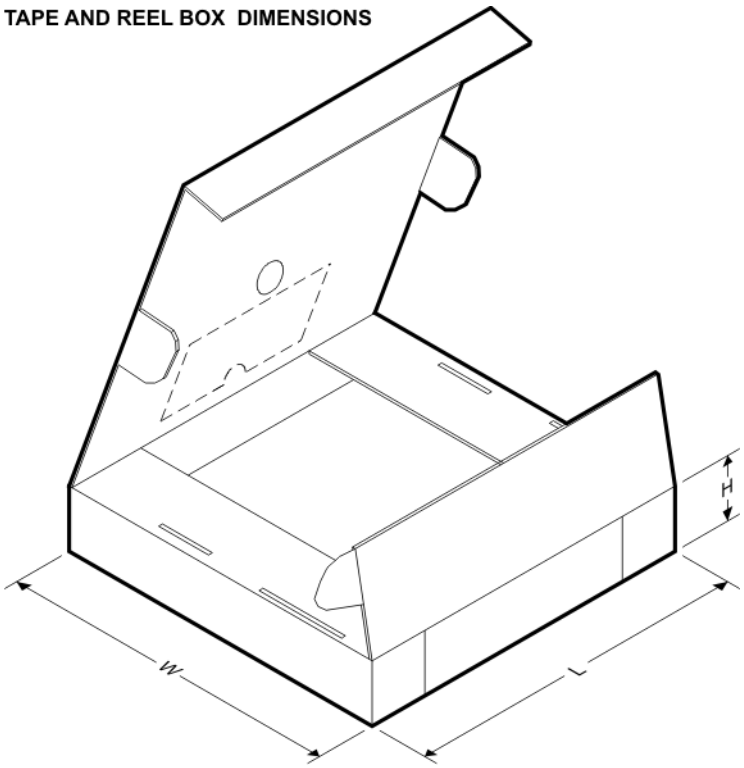
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM3017LE/NOPB	WQFN	NKL	10	1000	178.0	12.4	2.7	3.0	1.0	8.0	12.0	Q1
LM3017LEX/NOPB	WQFN	NKL	10	4500	330.0	12.4	2.7	3.0	1.0	8.0	12.0	Q1

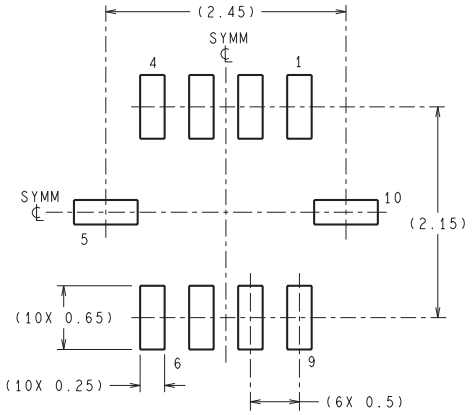
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM3017LE/NOPB	WQFN	NKL	10	1000	213.0	191.0	55.0
LM3017LEX/NOPB	WQFN	NKL	10	4500	367.0	367.0	35.0

NKL0010A



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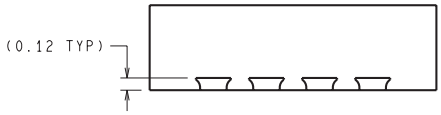

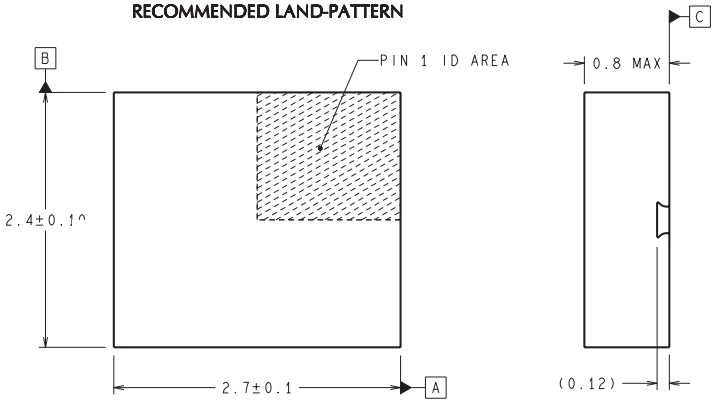

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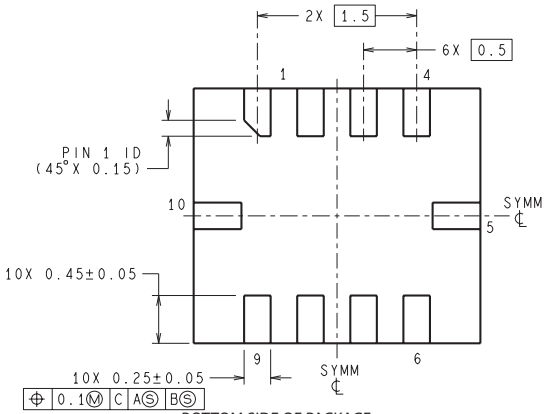

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Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
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