Hysteretic PFET Buck Controller With Enable Pin

Check for Samples: LM3489, LM3489-Q1

FEATURES

- **Easy to use control methodology**
- **No control loop compensation required**
- **Wide 4.5V to 35V input range**
- **1.239V to V_{IN} adjustable output range**
- **High efficiency 93%**
- **±1.3% (±2% over temp) internal reference**
- **100% duty cycle operation**
- **Maximum operation frequency > 1MHz**
- **Current limit protection**
- **Dedicated enable pin (on if unconnected)**
- **Shutdown mode draws only 7µA supply current**
- **VSSOP-8**
- **LM3489 is AEC-Q100 Grade 1 qualified**

APPLICATIONS

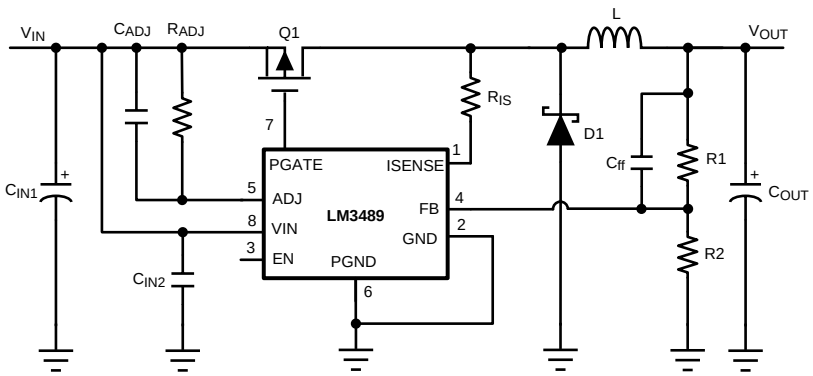
- **Set-Top Box**
- **DSL or Cable Modem**
- **PC/IA**
- **Auto PC**
- **TFT Monitor**
- **Battery Powered Portable Applications**
- **Distributed Power Systems**
- **Always On Power**
- **High Power LED Driver**
- **Automotive**

DESCRIPTION

The LM3489 is a high efficiency PFET switching regulator controller that can be used to quickly and easily develop a small, cost effective, switching buck regulator for a wide range of applications. The hysteretic control architecture provides for simple design without any control loop stability concerns using a wide variety of external components. The PFET architecture also allows for low component count as well as ultra-low dropout, 100% duty cycle operation. Another benefit is high efficiency operation at light loads without an increase in output ripple. A dedicated Enable Pin provides a shutdown mode drawing only 7µA. Leaving the Enable Pin unconnected defaults to on.

Current limit protection can be implemented by measuring the voltage across the PFET's $R_{DS(ON)}$, thus eliminating the need for a sense resistor. A sense resistor may be used to improve current limit accuracy if desired. The cycle-by-cycle current limit can be adjusted with a single resistor, ensuring safe operation over a range of output currents.

TYPICAL APPLICATION CIRCUIT



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CONNECTION DIAGRAM

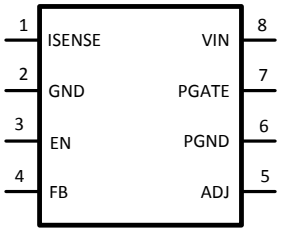


Figure 1. Top View
8-Lead Plastic VSSOP-8
Package Number (DGK)

PIN DESCRIPTIONS

Pin No.	Name	Description
1	ISENSE	The current sense input pin. This pin should be connected to the PFET drain terminal directly or through a series resistor up to 600 ohm for 28V>Vin>35V.
2	GND	Signal ground.
3	EN	Enable pin. Connect EN pin to ground to shutdown the part or float to enable operation (Internally pulled high). This pin can also be used to perform UVLO function.
4	FB	The feedback input. Connect the FB to a resistor voltage divider between the output and GND for an adjustable output voltage.
5	ADJ	Current limit threshold adjustment. Connected to an internal 5.5µA current source. A resistor is connected between this pin and VIN. The voltage across this resistor is compared with the ISENSE pin voltage to determine if an over-current condition has occurred.
6	PGND	Power ground.
7	PGATE	Gate Drive output for the external PFET. PGATE swings between VIN and VIN-5V.
8	VIN	Power supply input pin.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)

VIN Voltage		−0.3V to 36V
PGATE Voltage		−0.3V to 36V
FB Voltage		−0.3V to 5V
ISENSE Voltage		−1.0V to 36V
		-1V (<100ns)
ADJ Voltage		−0.3V to 36V
EN Voltage(2)		−0.3V to 6V
Maximum Junction Temperature		150°C
Power Dissipation, T_A = 25°C (3)		417mW
ESD Susceptibility	Human Body Model(4)	2kV
Lead Temperature	Vapor Phase (60 sec.)	215°C
	Infrared (15 sec.)	220°C
Storage Temperature		−65°C to 150°C

(1) Absolute maximum ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions for which the device is intended to be functional, but device parameter specifications may not be ensured. For specifications and test conditions, see the Electrical Characteristics.
(2) This pin is internally pulled high and clamped at 8V typical. The absolute maximum and operating maximum rating specifies the input level allowed for an external voltage source applied to this pin without triggering the internal clamp with margin.
(3) The maximum allowable power dissipation is a function of the maximum junction temperature, T_{J_MAX}, the junction-to-ambient thermal resistance, θ_{JA} = 240°C/W, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is calculated using: $P_{D\_MAX} = (T_{J\_MAX} - T_A)/\theta_{JA}$. Exceeding the maximum allowable power dissipation will cause excessive die temperature.
(4) The human body model is a 100 pF capacitor discharged through a 1.5kΩ resistor into each pin. The machine model is a 200pF capacitor discharged directly into each pin. MIL-STD-883 3015.7

Operating Ratings(1)

Supply Voltage Range (V_{IN})	4.5V to 35V
EN Voltage (maximum) (2)	5.5V
Operating Junction Temperature (T_J)	−40°C to +125°C

(1) Absolute maximum ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions for which the device is intended to be functional, but device parameter specifications may not be ensured. For specifications and test conditions, see the Electrical Characteristics.
(2) This pin is internally pulled high and clamped at 8V typical. The absolute maximum and operating maximum rating specifies the input level allowed for an external voltage source applied to this pin without triggering the internal clamp with margin.

Electrical Characteristics (1)(2)

Specifications in Standard type face are for T_J = 25°C, and in **bold type face** apply over the full **Operating Temperature Range** (T_J = −40°C to +125°C). Unless otherwise specified, V_{IN} = 12V, V_{ISNS} = V_{IN} − 1V, and V_{ADJ} = V_{IN} − 1.1V. Datasheet min/max specification limits are specified by design, test, or statistical analysis.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{SHDN}	Shutdown input supply current	EN = 0V		7	**15**	µA
V_{EN}	Enable threshold voltage	Enable rising	**1.15**	1.5	**1.85**	V
V_{EN_HYST}	Enable threshold hysteresis			130		mV
I_Q	Quiescent Current at ground pin	FB = 1.5V (Not Switching)		280	**400**	µA
V_{FB} (3)	Feedback Voltage		1.223 **1.214**	1.239	1.255 **1.264**	V
V_{HYST}	Comparator Hysteresis			10 **14**	15 **20**	mV
V_{CL_OFFSET}	Current limit comparator offset	V_{FB} = 1.0V	**-20**	0	**+20**	mV
I_{CL_ADJ}	Current limit ADJ current source	V_{FB} = 1.5V	**3.0**	5.5	**7.0**	µA
T_{CL}	Current limit one shot off time	V_{ADJ} = 11.5V V_{ISNS} = 11.0V V_{FB} = 1.0V	**6**	9	**14**	µs
R_{PGATE}	Driver resistance	Source I_{SOURCE} = 100mA		5.5		Ω
		Sink I_{SINK} = 100mA		8.5		
I_{PGATE}	Driver Output current	Source V_{IN} = 7V, PGATE = 3.5V		0.44		A
		Sink VIN = 7V, PGATE = 3.5V		0.1		
I_{FB} (4)	FB pin Bias Current	V_{FB} = 1.0V		300	**750**	nA
T_{ONMIN_NOR}	Minimum on time in normal operation	V_{ISNS} = V_{ADJ} + 0.1V C_{load} on OUT = 1000pF (5)		100		ns
T_{ONMIN_CL}	Minimum on time in current limit	V_{ISNS} = V_{ADJ} - 0.1V V_{FB} = 1.0V C_{load} on OUT = 1000pF (5)		200		ns
$\%V_{FB}/\Delta V_{IN}$	Feedback Voltage Line Regulation	4.5 ≤ V_{IN} ≤ 35V		0.01		%/V

(1) All limits are specified at room temperature (standard type face) and at **temperature extremes (bold type face)**. All room temperature limits are 100% tested. All limits at **temperature extremes** are specified via correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).
(2) Typical numbers are at 25°C and represent the most likely norm.
(3) The V_{FB} is the trip voltage at the FB pin when PGATE switches from high to low.
(4) Bias current flows out from the FB pin.
(5) A 1000pF capacitor is connected between V_{IN} and PGATE.

Typical Performance Characteristics

All curves taken at VIN = 12V with configuration in Design Information. T_J = 25°C, unless otherwise specified.

Quiescent Current vs Input Voltage

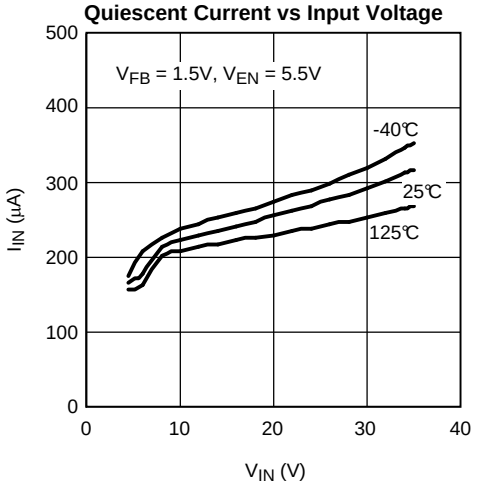


Figure 2.

Shutdown Current vs Input Voltage

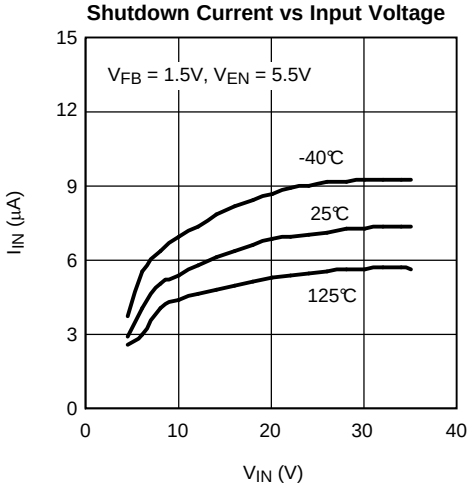


Figure 3.

Feedback Voltage vs Temperature

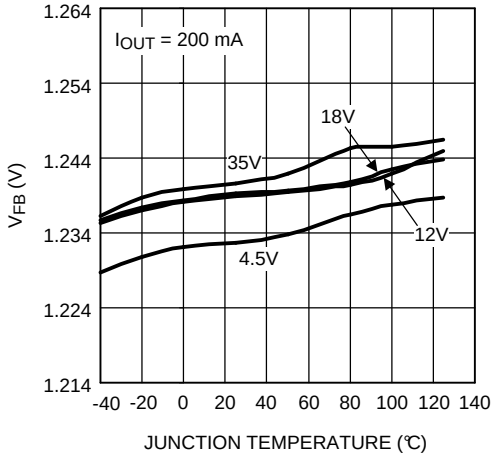


Figure 4.

Feedback Voltage Hysteresis vs Input Voltage

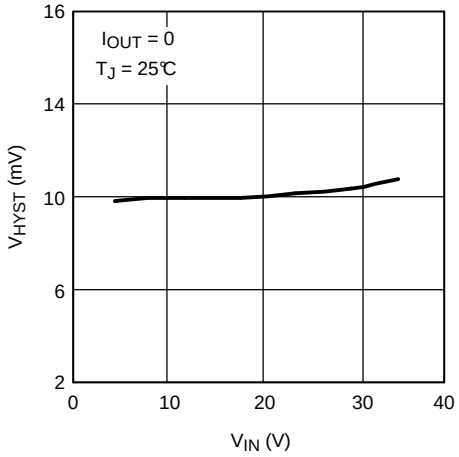


Figure 5.

Feedback Voltage Hysteresis vs Temperature

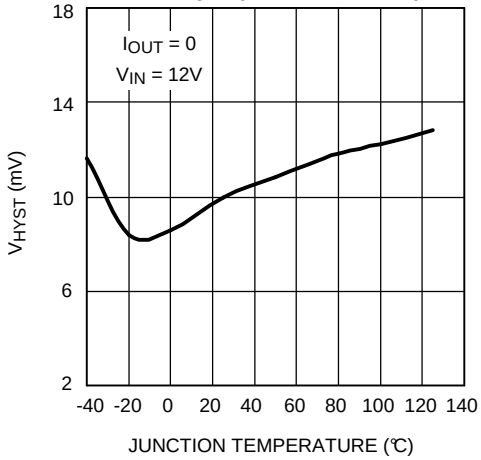


Figure 6.

Current Limit ADJ Current vs Temperature

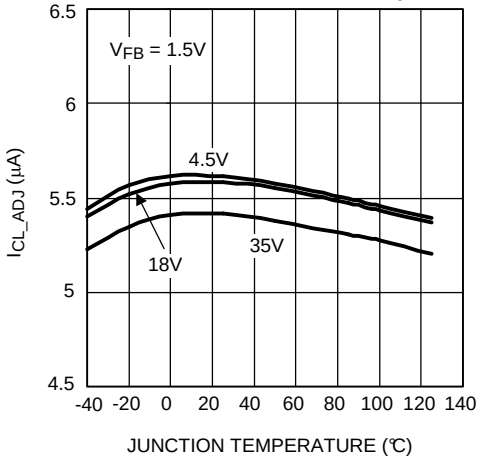


Figure 7.

Typical Performance Characteristics (continued)

All curves taken at VIN = 12V with configuration in Design Information. T_J = 25°C, unless otherwise specified.

Current Limit One Shot OFF Time vs Temperature

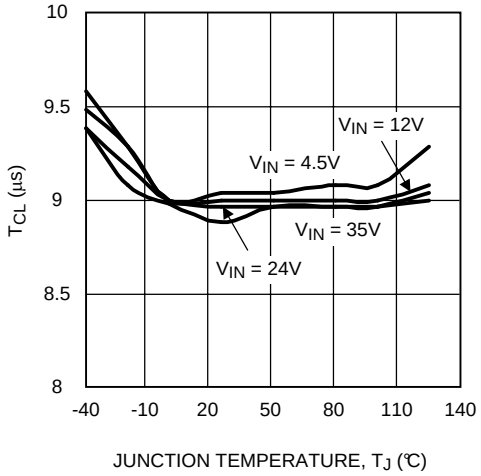


Figure 8.

V_{IN} - V_{PGATE} vs V_{IN}

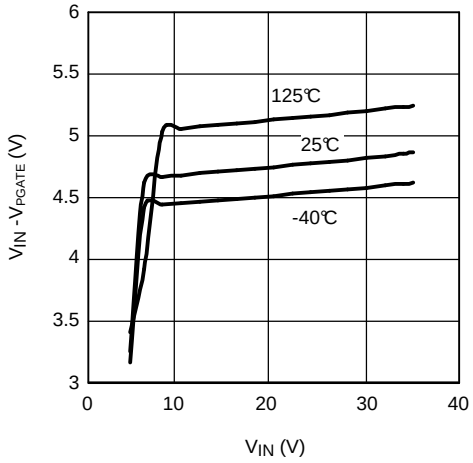


Figure 9.

Minimum ON Time vs Temperature (Normal Operation)

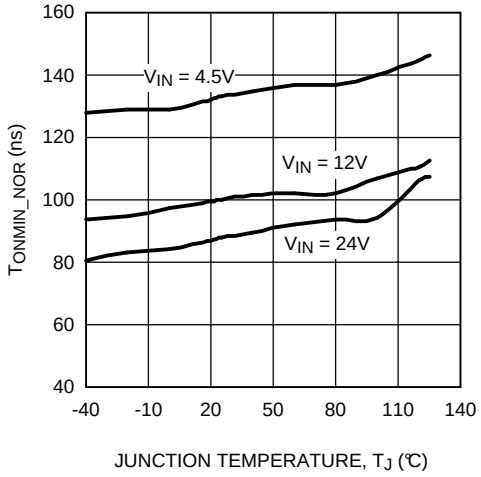


Figure 10.

Minimum ON Time vs Temperature (Current Limit)

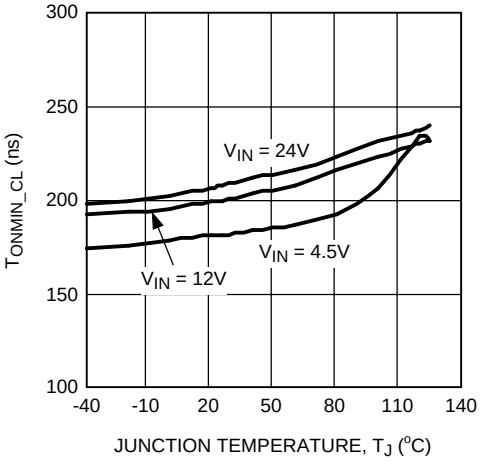


Figure 11.

Operating ON Time vs Load Current

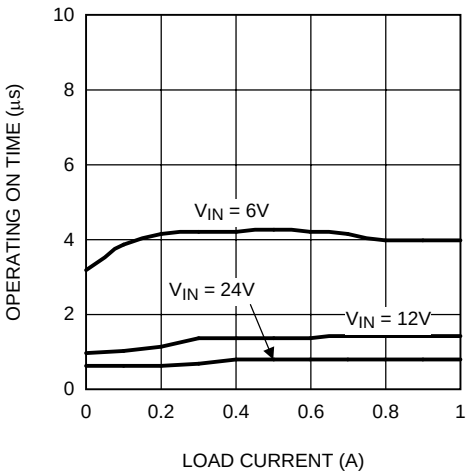


Figure 12.

Operating Frequency vs Input Voltage

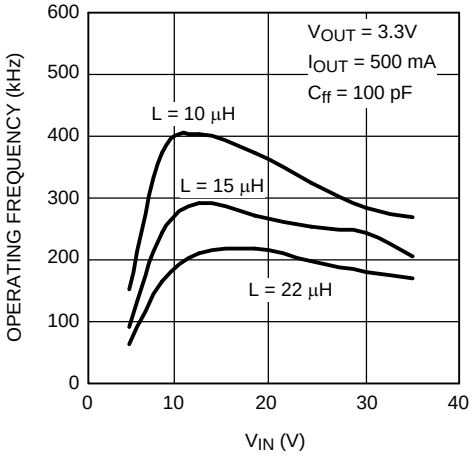


Figure 13.

Typical Performance Characteristics (continued)

All curves taken at VIN = 12V with configuration in Design Information. T_J = 25°C, unless otherwise specified.

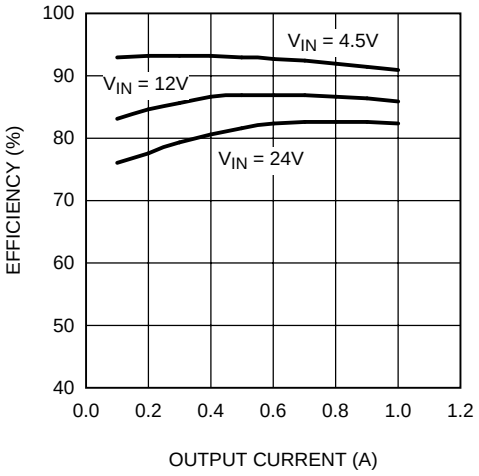


Figure 14.

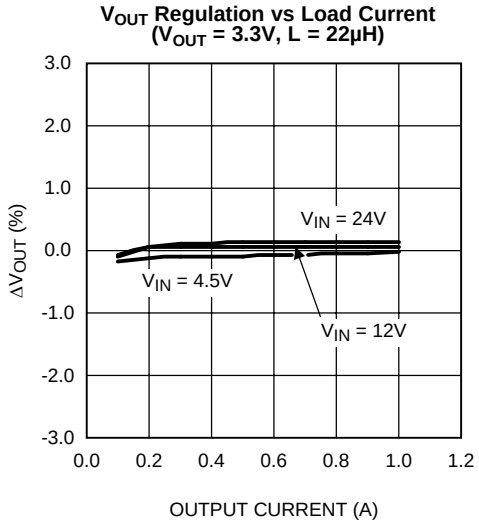


Figure 15.

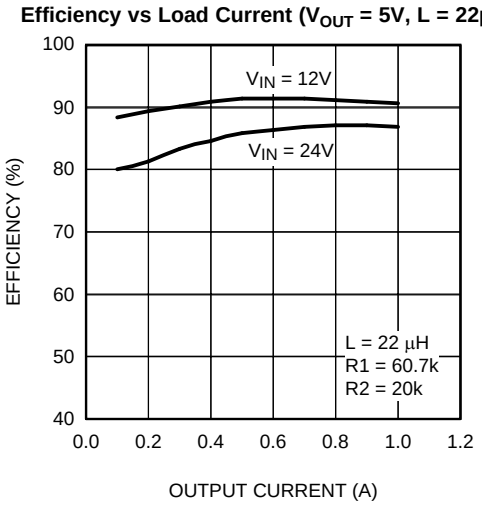


Figure 16.

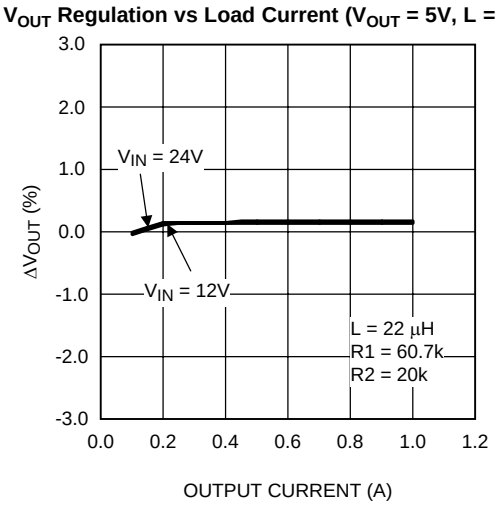


Figure 17.

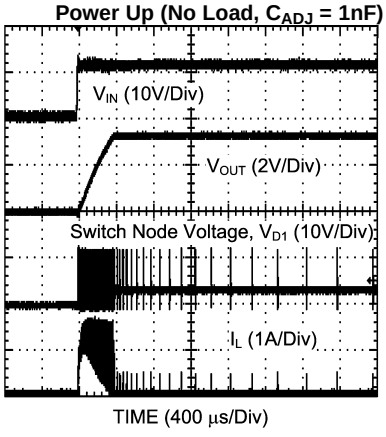


Figure 18.

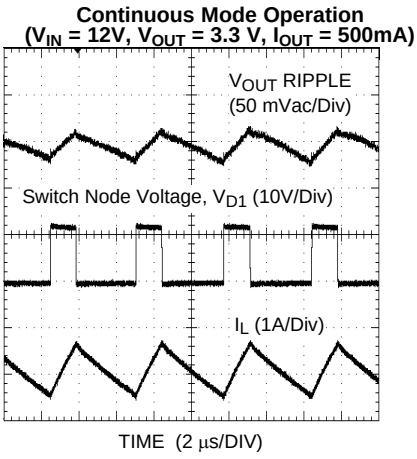


Figure 19.

Typical Performance Characteristics (continued)

All curves taken at VIN = 12V with configuration in Design Information. T_J = 25°C, unless otherwise specified.

Discontinuous Mode Operation
(V_{IN} = 12V, V_{OUT} =3.3 V, I_{OUT} = 50mA)

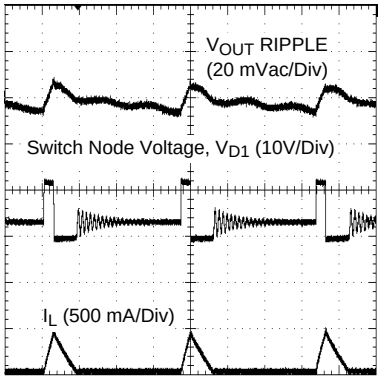


Figure 20.

Load Transient
(V_{OUT} = 3.3 V, 50 mA - 500 mA Load)

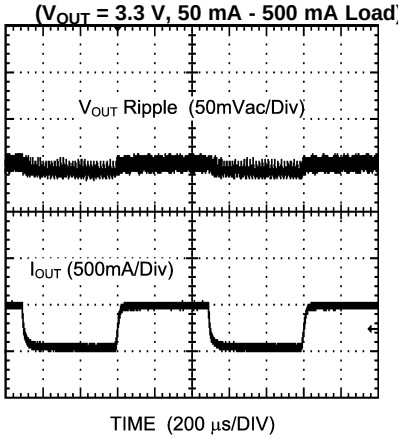


Figure 21.

Enable Transient
(V_{OUT} = 3.3 V, 500 mA Loaded)

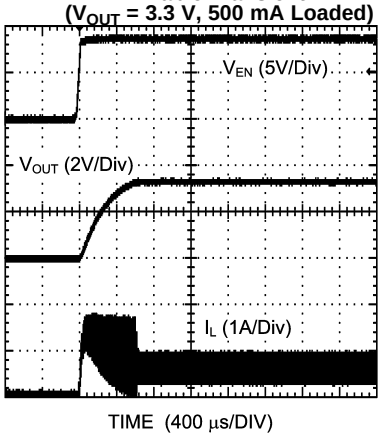


Figure 22.

Shutdown Transient
(V_{OUT} = 3.3 V, 500 mA Loaded)

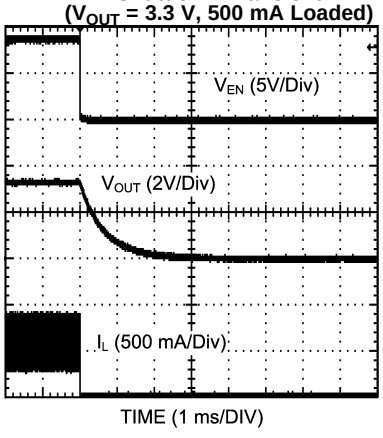
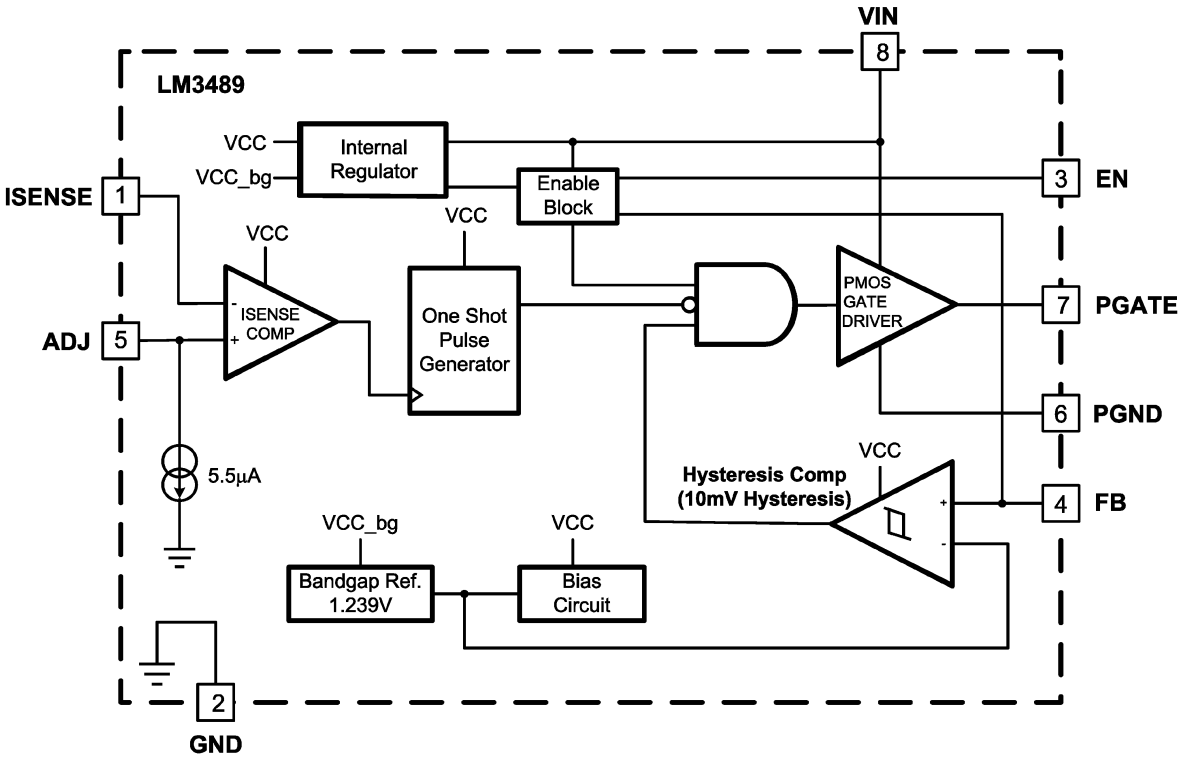


Figure 23.

SIMPLIFIED FUNCTIONAL BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

OVERVIEW

The LM3489 is a buck (step-down) DC-DC controller that uses a hysteretic control scheme. The control comparator is designed with approximately 10mV of hysteresis. In response to the voltage at the FB pin, the gate drive (PGATE pin) turns the external PFET on or off. When the inductor current is too high, the current limit protection circuit engages and turns the PFET off for approximately 9µs.

Hysteretic control does not require an internal oscillator. Switching frequency depends on the external components and operating conditions. The operating frequency reduces at light loads resulting in excellent efficiency compared to other architectures.

The output voltage can be programmed by two external resistors. The output can be set in a wide range from 1.239V (typical) to V_{IN}.

HYSTERETIC CONTROL CIRCUIT

When the FB input to the control comparator falls below the reference voltage (1.239V), the output of the comparator switches to a low state. This results in the driver output, PGATE, pulling the gate of the PFET low and turning on the PFET. With the PFET on, the input supply charges C_{OUT} and supplies current to the load via the series path through the PFET and the inductor. Current through the Inductor ramps up linearly and the output voltage increases. As the FB voltage reaches the upper threshold, which is the internal reference voltage plus 10mV, the output of the comparator changes from low to high, and the PGATE responds by turning the PFET off. As the PFET turns off, the inductor voltage reverses, the catch diode turns on, and the current through the inductor ramps down. Then, as the output voltage reaches the internal reference voltage again, the next cycle starts.

The LM3489 operates in discontinuous conduction mode at light load current or continuous conduction mode at heavy load current. In discontinuous conduction mode, current through the inductor starts at zero and ramps up to the peak, then ramps down to zero. The next cycle starts when the FB voltage reaches the reference voltage. Until then, the inductor current remains zero and the output capacitor supplies the load. The operating frequency is lower and switching losses reduced. In continuous conduction mode, current always flows through the inductor and never ramps down to zero.

The output voltage (V_{OUT}) can be programmed by 2 external resistors. It can be calculated as follows:

$$V_{OUT} = 1.239 \times (R1 + R2) / R2 \quad (1)$$

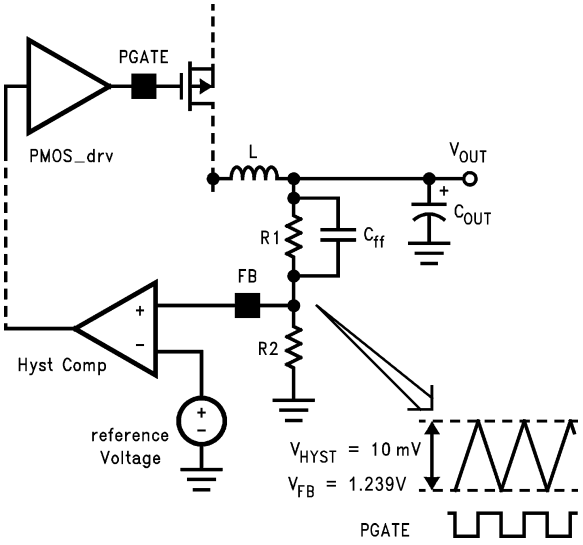


Figure 24. Hysteretic Window

The minimum output voltage ripple (V_{OUT_PP}) can be calculated in the same way.

$$V_{OUT\_PP} = V_{HYST} (R1 + R2) / R2 \quad (2)$$

For example, with V_{OUT} set to 3.3V, V_{OUT_PP} is 26.6mV

$$V_{OUT\_PP} = 0.01 \times (33K + 20k) / 20k = 0.0266V \quad (3)$$

Operating frequency (F) is determined by knowing the input voltage, output voltage, inductor, V_{HYST}, ESR (Equivalent Series Resistance) of output capacitor, and the delay. It can be approximately calculated using the formula:

$$F = \frac{V_{OUT}}{V_{IN}} * \frac{(V_{IN} - V_{OUT}) * ESR}{(V_{HYST} * \alpha * L) + (V_{IN} * delay * ESR)} \quad (4)$$

where:

α: (R1 + R2) / R2

delay: It includes the LM3489 propagation delay time and the PFET delay time. The propagation delay is 90ns typically (see Figure 25).

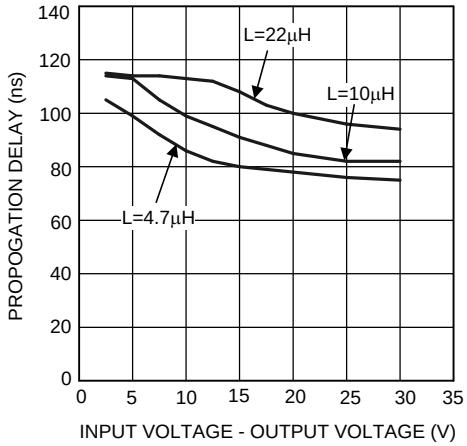


Figure 25. Propagation Delay

The operating frequency and output ripple voltage can also be significantly influenced by the speed up capacitor (Cff). Cff is connected in parallel with the high side feedback resistor, R1. The location of this capacitor is similar to where a phase lead capacitor would be located in a PWM control scheme. However it's effect on hysteretic operation is much different. Cff effectively shorts out R1 at the switching frequency and applies the full output ripple to the FB pin without dividing by the R2/R1 ratio. The end result is a reduction in output ripple and an increase in operating frequency. When adding Cff, calculate the formula above with α = 1. The value of Cff depend on the desired operating frequency and the value of R2. A good starting point is 470pF ceramic at 100kHz decreasing linearly with increased operating frequency. Also note that as the output voltage is programmed below 2.5V, the effect of Cff will decrease significantly.

CURRENT LIMIT OPERATION

The LM3489 has a cycle-by-cycle current limit. Current limit is sensed across the V_{DS} of the PFET or across an additional sense resistor. When current limit is activated, the LM3489 turns off the external PFET for a period of 9µs(typical). The current limit is adjusted by an external resistor, R_{ADJ}.

The current limit circuit is composed of the ISENSE comparator and the one-shot pulse generator. The positive input of the ISENSE comparator is the ADJ pin. An internal 5.5µA current sink creates a voltage across the external R_{ADJ} resistor. This voltage is compared to the voltage across the PFET or sense resistor. The ADJ voltage can be calculated as follows:

$$V_{ADJ} = V_{IN} - (R_{ADJ} \times 3.0\mu A) \quad (5)$$

Where 3.0µA is the minimum $I_{CL\text{-}ADJ}$ value.

The negative input of the ISENSE comparator is the ISENSE pin that should be connected to the drain of the external PFET. The inductor current is determined by sensing the V_{DS}. It can be calculated as follows.

$$V_{ISENSE} = V_{IN} - (R_{DSON} \times I_{IND\_PEAK}) = V_{IN} - V_{DS} \quad (6)$$

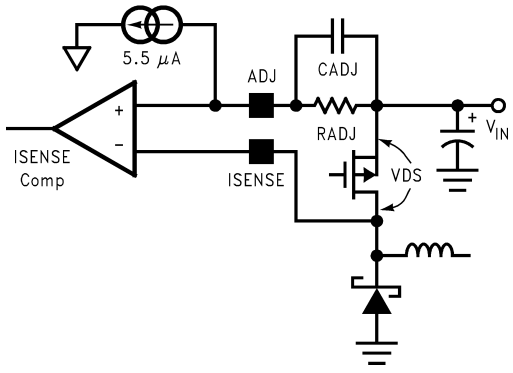


Figure 26. Current Sensing by V_{DS}

The current limit is activated when the voltage at the ADJ pin exceeds the voltage at the I_{SENSE} pin. The ISENSE comparator triggers the 9µs one shot pulse generator forcing the driver to turn the PFET off. The driver turns the PFET back on after 9µs. If the current has not reduced below the set threshold, the cycle will repeat continuously.

A filter capacitor, C_{ADJ}, should be placed as shown in Figure 26. C_{ADJ} filters unwanted noise so that the ISENSE comparator will not be accidentally triggered. A value of 100pF to 1nF is recommended in most applications. Higher values can be used to create a soft-start function (See Start Up section).

The current limit comparator has approximately 100ns of blanking time. This ensures that the PFET is fully on when the current is sensed. However, under extreme conditions such as cold temperature, some PFETs may not fully turn on within the blanking time. In this case, the current limit threshold must be increased. If the current limit function is used, the on time must be greater than 100ns. Under low duty cycle operation, the maximum operating frequency will be limited by this minimum on time.

During current limit operation, the output voltage will drop significantly as will operating frequency. As the load current is reduced, the output will return to the programmed voltage. However, there is a current limit fold back phenomenon inherent in this current limit architecture. See Figure 27.

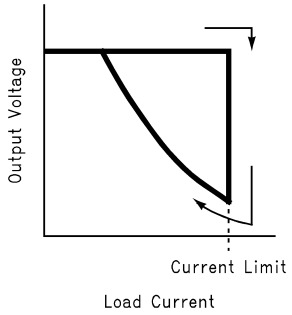


Figure 27. Current Limit Fold Back Phenomenon

At high input voltages (>28V) increased undershoot at the switch node can cause an increase in the current limit threshold. To avoid this problem, a low Vf Schottky catch diode must be used (See Catch Diode Selection). Additionally, a resistor can be placed between the ISENSE pin and the switch node. Any value in the range of 220Ω to 600Ω is recommended.

START UP

The current limit circuit is active during start-up. During start-up the PFET will stay on until either the current limit or the feedback comparator is tripped

If the current limit comparator is tripped first then the fold back characteristic should be taken into account. Start-up into full load may require a higher current limit set point or the load must be applied after start-up.

One problem with selecting a higher current limit is inrush current during start-up. Increasing the capacitance (C_{ADJ}) in parallel with R_{ADJ} results in a soft-start characteristic. C_{ADJ} and R_{ADJ} create an RC time constant forcing current limit to activate at a lower current. The output voltage will ramp more slowly when using this technique. There is example start-up plot for C_{ADJ} equal to 1nF in the Typical Performance Characteristics. Lower values for C_{ADJ} will have little to no effect on soft-start.

EXTERNAL SENSE RESISTOR

The V_{DS} of a PFET will tend to vary significantly over temperature. This will result an equivalent variation in current limit. To improve current limit accuracy an external sense resistor can be connected from V_{IN} to the source of the PFET, as shown in Figure 28. The current sense resistor, R_{CS} should have value comparable with R_{DSON} of the PFET used, typically in the range of 50mΩ to 200 mΩ. The equation in CURRENT LIMIT OPERATION can be used by replacing the R_{DSON} with R_{CS}.

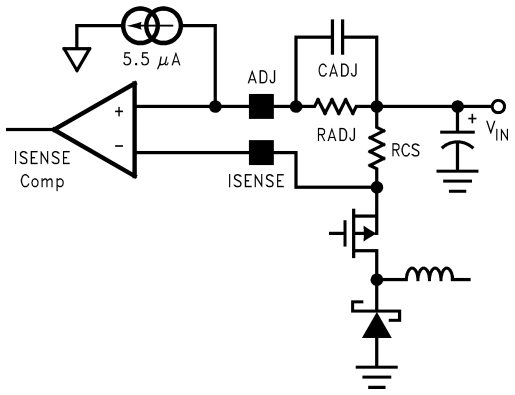


Figure 28. Current Sensing by External Resistor

PGATE

When switching, the PGATE pin swings from VIN (off) to some voltage below VIN (on). How far the PGATE will swing depends on several factors including the capacitance, on time, and input voltage.

PGATE voltage swing will increase with decreasing gate capacitance. Although PGATE voltage will typically be around VIN-5V, with very small gate capacitances, this value can increase to a typical maximum of VIN-8.3V.

Additionally, PGATE swing voltage will increase as on time increases. During long on times, such as when operating at 100% duty cycle, the PGATE voltage will eventually fall to its maximum voltage of VIN-8.3V (typical) regardless of the PFET gate capacitance.

The PGATE voltage will not fall below 0.4V (typical). Therefore, when the input voltage falls below approximately 9V, the PGATE swing voltage range will be reduced. At an input voltage of 7V, for instance, PGATE will swing from 7V to a minimum of 0.4V.

DEVICE ENABLE, SHUTDOWN

The LM3489 can be remotely shutdown by forcing the enable pin to ground. With EN pin grounded, the internal blocks other than the enable logic are de-activated and the shutdown current of the device will be lowered to only 7µA (typical). Releasing the EN pin allows for normal operation to resume. The EN pin is internally pulled high with the voltage clamped at 8V typical. For normal operation this pin should be left open. In case an external voltage source is applied to this pin for enable control, the applied voltage should not exceed the maximum operating voltage level specified in this datasheet, i.e. 5.5V.

ADJUSTABLE UVLO

The under-voltage-lockout function can be implemented as shown in Figure 29. By incorporating the feature of the internal enable threshold, the lockout level can be programmed through an external potential divider formed with R3 and R4. The input voltage information is detected and compared with the enable threshold and the device operation will be inhibited when V_{IN} drops below the preset UVLO level. The UVLO and hysteresis voltage can be calculated as follows:

$$V_{IN(UVLO)} = V_{EN}\left(1 + \frac{R4}{R3}\right) \quad (7)$$

$$V_{IN(UVLO\_HYST)} = V_{EN\_HYST} \times \left(1 + \frac{R4}{R3}\right) \quad (8)$$

where V_{EN} is the enable rising threshold voltage and V_{EN_HYST} is the enable threshold hysteresis.

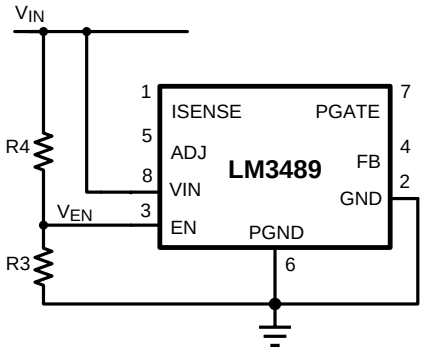


Figure 29. Adjustable UVLO

DESIGN INFORMATION

Hysteretic control is a simple control scheme. However the operating frequency and other performance characteristics highly depend on external conditions and components. If either the inductance, output capacitance, ESR, V_{IN}, or Cff is changed, there will be a change in the operating frequency and output ripple. The best approach is to determine what operating frequency is desirable in the application and then begin with the selection of the inductor and C_{OUT} ESR.

INDUCTOR SELECTION (L)

The important parameters for the inductor are the inductance and the current rating. The LM3489 operates over a wide frequency range and can use a wide range of inductance values. A rule of thumb is to use the equations used for **Simple Switchers**®. The equation for inductor ripple (Δi) as a function of output current (I_{OUT}) is:

for I_{out} < 2.0Amps

$\Delta i \leq I_{out} \times I_{out}^{-0.366726}$

for I_{out} > 2.0Amps

$\Delta i \leq I_{out} \times 0.3$

The inductance can be calculated based upon the desired operating frequency where:

$$L = \frac{V_{IN} - V_{DS} - V_{OUT}}{\Delta i} \bullet \frac{D}{f} \tag{9}$$

And

$$I_{pk} = \left(I_{OUT} + \frac{\Delta i}{2}\right) \times 1.1 \tag{10}$$

where D is the duty cycle, V_D is the diode forward voltage, and V_{DS} is the voltage drop across the PFET.

The inductor should be rated to the following:

$$I_{pk} = \left(I_{OUT} + \frac{\Delta i}{2}\right) \times 1.1 \tag{11}$$

The inductance value and the resulting ripple is one of the key parameters controlling operating frequency. The second is the inductor ESR that contribute to the steady state power loss due to current flowing through the inductor.

OUTPUT CAPACITOR SELECTION (C_{OUT})

The ESR of the output capacitor times the inductor ripple current is equal to the output ripple of the regulator. However, the V_{HYST} sets the first order value of this ripple. As ESR is increased with a given inductance, operating frequency increases as well. If ESR is reduced then the operating frequency reduces.

The use of ceramic capacitors has become a common desire of many power supply designers. However, ceramic capacitors have a very low ESR resulting in a 90° phase shift of the output voltage ripple. This results in low operating frequency and increased output ripple. To fix this problem a low value resistor should be added in series with the ceramic output capacitor. Although counter intuitive, this combination of a ceramic capacitor and external series resistance provides highly accurate control over the output voltage ripple. Other types capacitor, such as Sanyo POS CAP and OS-CON, Panasonic SP CAP, and Nichicon "NA" series, are also recommended and may be used without additional series resistance.

For all practical purposes, any type of output capacitor may be used with proper circuit verification.

INPUT CAPACITOR SELECTION (C_{IN})

A bypass capacitor is required between the input source and ground. It must be located near the source pin of the external PFET. The input capacitor prevents large voltage transients at the input and provides the instantaneous current when the PFET turns on.

The important parameters for the input capacitor are the voltage rating and the RMS current rating. Follow the manufacturer's recommended voltage derating. For high input voltage applications, low ESR electrolytic, Nichicon "UD" series or the Panasonic "FK" series are available. The RMS current in the input capacitor can be calculated as follows:

$$I_{RMS\_CIN} = I_{OUT} \times \frac{\sqrt{V_{OUT}(V_{IN} - V_{OUT})}}{V_{IN}} \tag{12}$$

The input capacitor power dissipation can be calculated as follows.

$$P_{D(CIN)} = I_{RMS\_CIN}^2 \times ESR_{CIN} \tag{13}$$

The input capacitor must be able to handle the RMS current and the dissipation. Several input capacitors may be connected in parallel to handle large RMS currents. In some cases it may be much cheaper to use multiple electrolytic capacitors than a single low ESR, high performance capacitor such as OS-CON or Tantalum. The capacitance value should be selected such that the ripple voltage created by the switch current pulses is less than 10% of the total DC voltage across the capacitor.

For high VIN conditions (> 28V), the fast switching, high swing of the internal gate drive introduces unwanted disturbance to the VIN rail and the current limit function can be affected. In order to eliminate this potential problem, a high quality ceramic capacitor of 0.1 µF is recommended to filter out the internal disturbance at the VIN pin. This capacitor should be placed right next to the VIN pin for best performance.

PROGRAMMING THE CURRENT LIMIT (R_{ADJ})

The current limit is determined by connecting a resistor (R_{ADJ}) between input voltage and the ADJ pin, pin 5.

$$R_{ADJ} = I_{IND\_PEAK} \times \frac{R_{DSON}}{I_{CL\_ADJ}} \tag{14}$$

where:

R_{DSON} : Drain-Source ON resistance of the external PFET

I_{CL_ADJ} : 3.0µA minimum

$I_{IND\_PEAK} = I_{LOAD} + I_{RIPPLE}/2$

Using the minimum value for I_{CL_ADJ} (3.0µA) ensures that the current limit threshold will be set higher than the peak inductor current.

The R_{ADJ} value must be selected to ensure that the voltage at the ADJ pin does not fall below 3.5V. With this in mind, $R_{ADJ\_MAX} = (V_{IN}\text{-}3.5)/7\mu A$. If a larger R_{ADJ} value is needed to set the desired current limit, either use a PFET with a lower R_{DSON}, or use a current sense resistor as shown in Figure 28.

The current limit function can be disabled by connecting the ADJ pin to ground and ISENSE to VIN.

CATCH DIODE SELECTION (D1)

The important parameters for the catch diode are the peak current, the peak reverse voltage, and the average power dissipation. The average current through the diode can be calculated as following.

$$I_{D\_AVE} = I_{OUT} \times (1 - D) \quad (15)$$

The off state voltage across the catch diode is approximately equal to the input voltage. The peak reverse voltage rating must be greater than input voltage. In nearly all cases a Schottky diode is recommended. In low output voltage applications a low forward voltage provides improved efficiency. For high temperature applications, diode leakage current may become significant and require a higher reverse voltage rating to achieve acceptable performance.

P-CHANNEL MOSFET SELECTION (Q1)

The important parameters for the PFET are the maximum Drain-Source voltage (V_{DS}), the on resistance (R_{DSON}), Current rating, and the input capacitance.

The voltage across the PFET when it is turned off is equal to the sum of the input voltage and the diode forward voltage. The V_{DS} must be selected to provide some margin beyond the input voltage.

PFET drain current, Id, must be rated higher than the peak inductor current, $I_{IND\text{-}PEAK}$.

Depending on operating conditions, the PGATE voltage may fall as low as V_{IN} - 8.3V. Therefore, a PFET must be selected with a V_{GS} maximum rating greater than the maximum PGATE swing voltage.

As input voltage decreases below 9V, PGATE swing voltage may also decrease. At 5.0V input the PGATE will swing from V_{IN} to V_{IN} - 4.6V. To ensure that the PFET turns on quickly and completely, a low threshold PFET should be used when the input voltage is less than 7V.

Total power loss in the FET can be approximated using the following equation:

$$PD_{switch} = R_{DSON} \times I_{OUT}^2 \times D + F \times I_{OUT} \times V_{IN} \times (t_{on} + t_{off})/2 \quad (16)$$

where:

t_{on} = FET turn on time

t_{off} = FET turn off time

A value of 10ns to 20ns is typical for ton and toff.

A PFET should be selected with a turn on rise time of less than 100ns. Slower rise times will degrade efficiency, can cause false current limiting, and in extreme cases may cause abnormal spiking at the PGATE pin.

The R_{DSON} is used in determining the current limit resistor value, R_{ADJ}. Note that the R_{DSON} has a positive temperature coefficient. At 100°C, the R_{DSON} may be as much as 150% higher than the 25°C value. This increase in R_{DSON} must be considered when determining R_{ADJ} in wide temperature range applications. If the current limit is set based upon 25°C ratings, then false current limiting can occur at high temperature.

Keeping the gate capacitance below 2000pF is recommended to keep switching losses and transition times low. This will also help keep the PFET drive current low, which will improve efficiency and lower the power dissipation within the controller.

As gate capacitance increases, operating frequency should be reduced and as gate capacitance decreases operating frequency can be increased.

INTERFACING WITH THE ENABLE PIN

The enable pin is internally pulled high with clamping at 8V typical. For normal operation this pin should be left open. To disable the device, the enable pin should be connected to ground externally. If an external voltage source is applied to this pin for enable control, the applied voltage should not exceed the maximum operating voltage level specified in this datasheet, i.e. 5.5V. For most applications, an open drain or open collector transistor can be used to short this pin to ground to shutdown the device .

PCB Layout

The PCB board layout is very important in all switching regulator designs. Poor layout can cause switching noise into the feedback signal and generate EMI problems. For minimal inductance, the wires indicated by heavy lines in schematic diagram should be as wide and short as possible. Keep the ground pin of the input capacitor as close as possible to the anode of the catch diode. This path carries a large AC current. The switching node, the node with the diode cathode, inductor and FET drain should be kept short. This node is one of the main sources for radiated EMI since it sees a large AC voltage at the switching frequency. It is always a good practice to use a ground plane in the design, particularly for high current applications.

The two ground pins, PGND and GND, should be connected by as short a trace as possible. They can be connected underneath the device. These pins are resistively connected internally by approximately 50Ω. The ground pins should be tied to the ground plane, or to a large ground trace in close proximity to both the FB divider and C_{OUT} grounds.

The gate pin of the external PFET should be located close to the PGATE pin. However, if a very small FET is used, a resistor may be required between PGATE pin and the gate of the PFET to reduce high frequency ringing. Since this resistor will slow down the PFET's rise time, the current limit blanking time should be taken into consideration (refer to Current Limiting Operation). The feedback voltage signal line can be sensitive to noise. Avoid inductive coupling with the inductor or the switching node. The FB trace should be kept away from those areas. Also, the orientation of the inductor can contribute un-wanted noise coupling to the FB path. If noise problems are observed it may be worth trying a different orientation of the inductor and select the best for final component placement.

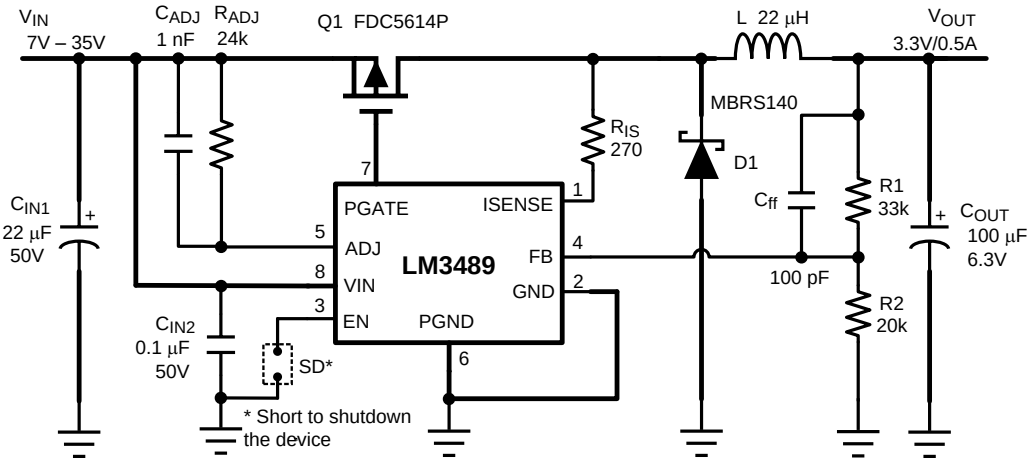


Figure 30. Typical Application Schematic for VOUT = 3.3V/500mA

REVISION HISTORY

Changes from Revision A (February 2013) to Revision B	Page
• Changed layout of National Data Sheet to TI format	17

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM3489MM	NRND	VSSOP	DGK	8	1000	TBD	Call TI	Call TI	-40 to 125	SKSB	
LM3489MM/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU NIPDAUAG | CU SN	Level-1-260C-UNLIM	-40 to 125	SKSB	Samples
LM3489MMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU NIPDAUAG | CU SN	Level-1-260C-UNLIM	-40 to 125	SKSB	Samples
LM3489QMM/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	STEB	Samples
LM3489QMMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	STEB	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF LM3489, LM3489-Q1 :

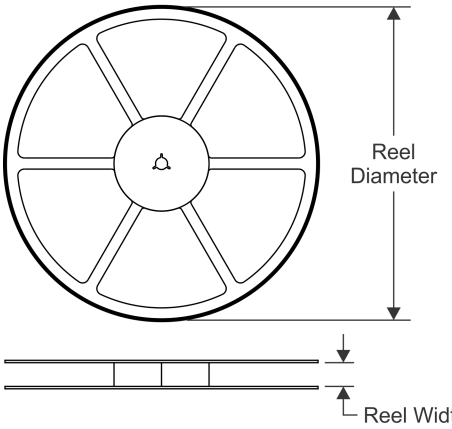
- Catalog: LM3489
- Automotive: LM3489-Q1

NOTE: Qualified Version Definitions:

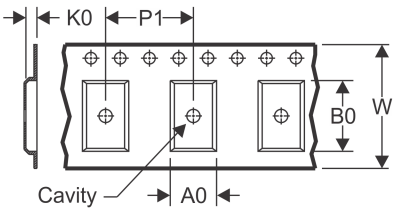
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

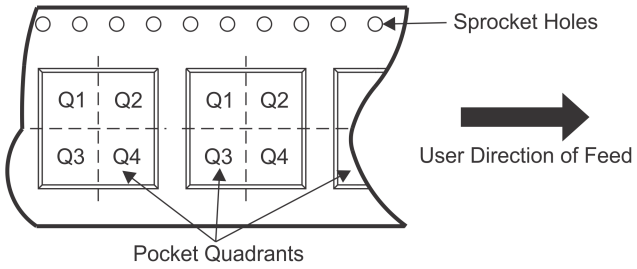


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

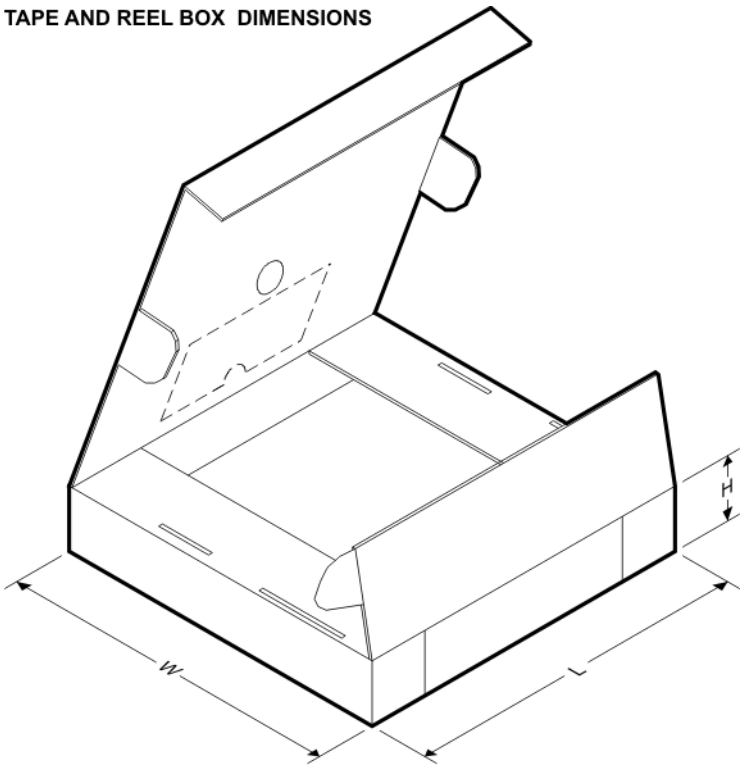
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM3489MM	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM3489MM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM3489MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM3489QMM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM3489QMMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

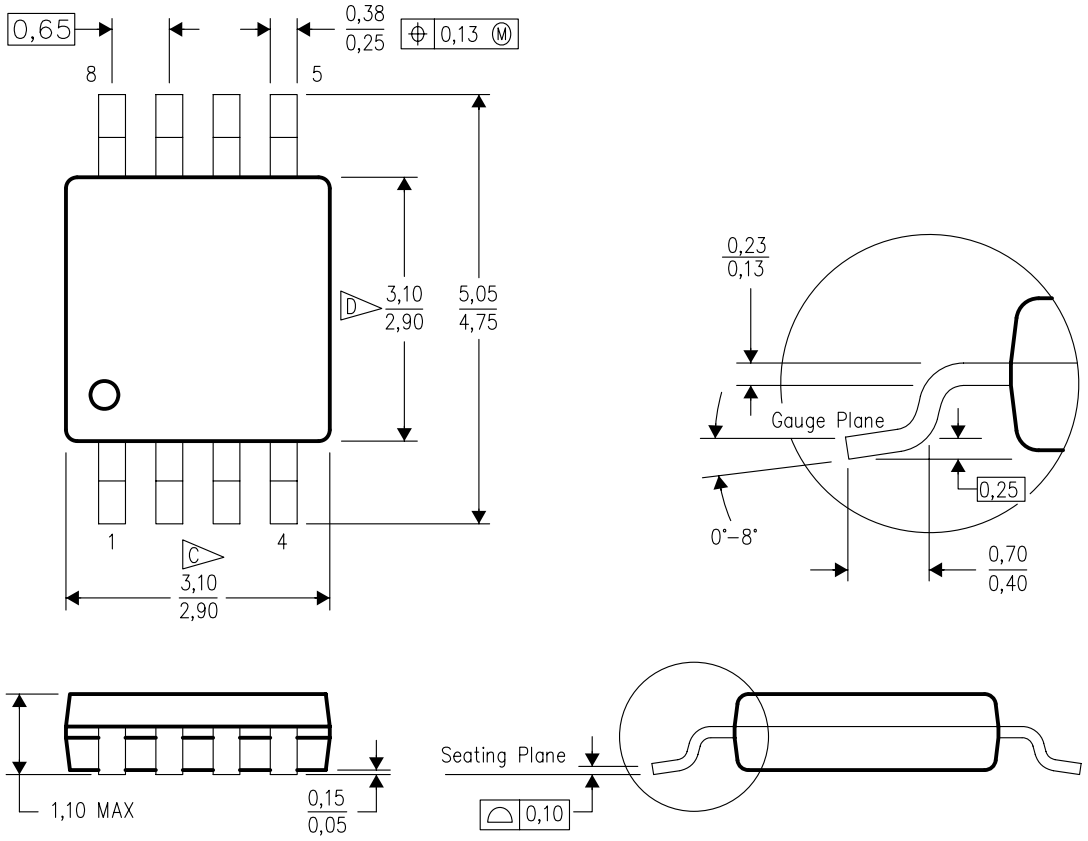
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM3489MM	VSSOP	DGK	8	1000	210.0	185.0	35.0
LM3489MM/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LM3489MMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LM3489QMM/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LM3489QMMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0

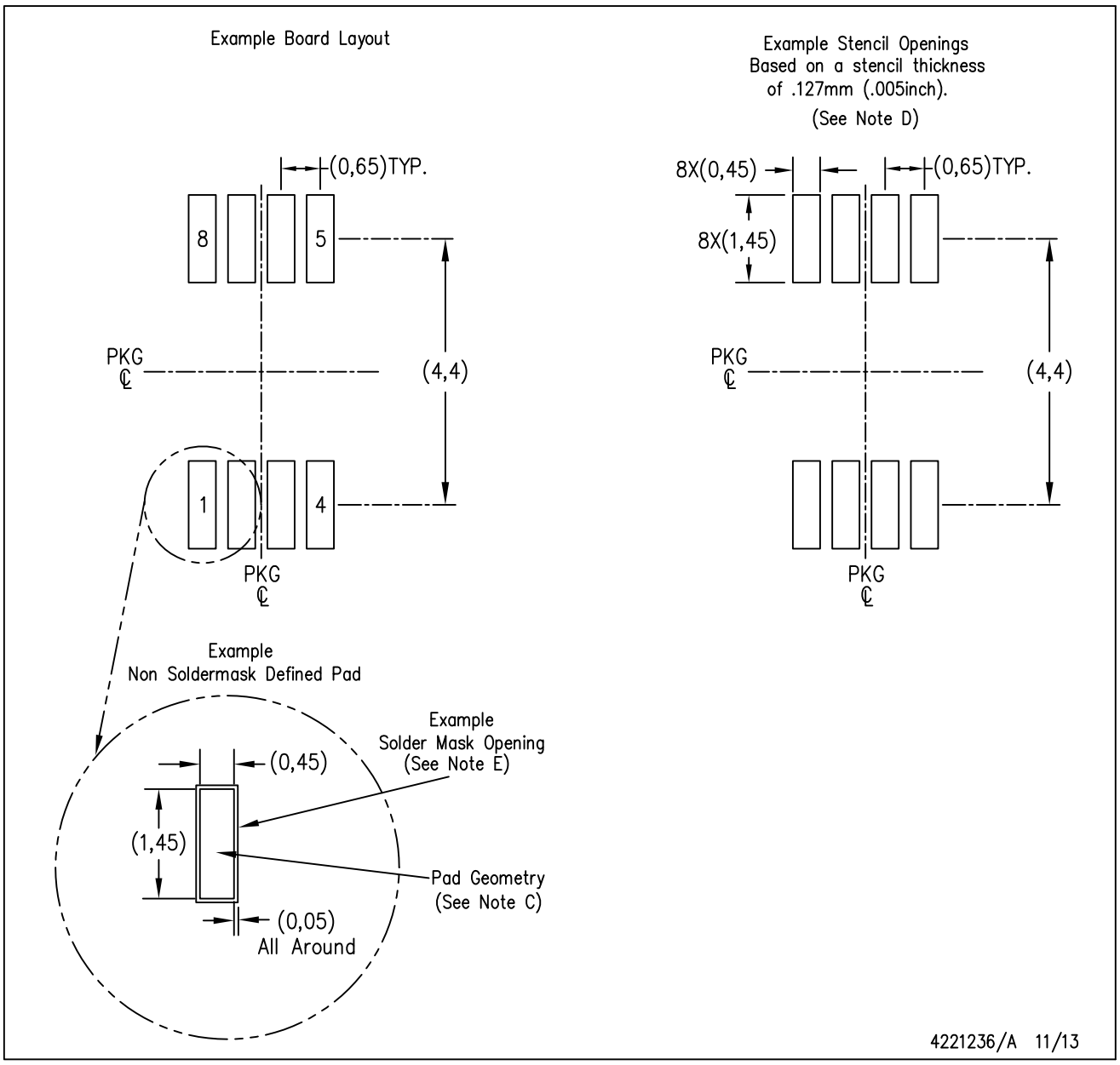
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

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