SNVS250E – NOVEMBER 2004 – REVISED FEBRUARY 2013

LM3670 Miniature Step-Down DC-DC Converter for Ultra Low Voltage Circuits

Check for Samples: LM3670

FEATURES

- **V_{OUT} = Adj (0.7V min), 1.2, 1.5, 1.6, 1.8, 1.875, 2.5, 3.3V**
- **2.5V ≤ V_{IN} ≤ 5.5V**
- **15 µA Typical Quiescent Current**
- **350 mA Maximum Load Capability**
- **1 MHz PWM Fixed Switching Frequency (typ.)**
- **Automatic PFM/PWM Mode Switching**
- **Available in Fixed Output Voltages as well as an Adjustable Version**
- **SOT-23-5 Package**
- **Low Drop Out Operation - 100% Duty Cycle Mode**
- **Internal Synchronous Rectification for High Efficiency**
- **Internal Soft Start**
- **0.1 µA Typical Shutdown Current**
- **Operates from a Single Li-Ion Cell or 3 Dell NiMH/NiCd Batteries**
- **Only Three Tiny Surface-Mount External Components Required (One Inductor, Two Ceramic Capacitors)**
- **Current Overload Protection**

APPLICATIONS

- **Mobile Phones**
- **HandHeld**
- **PDAs**
- **Palm-Top PCs**
- **Portable Instruments**
- **Battery Powered Devices**

DESCRIPTION

The LM3670 step-down DC-DC converter is optimized for powering ultra-low voltage circuits from a single Li-Ion cell or 3 cell NiMH/NiCd batteries. It provides up to 350 mA load current, over an input voltage range from 2.5V to 5.5V. There are several different fixed voltage output options available as well as an adjustable output voltage version.

The device offers superior features and performance for mobile phones and similar portable applications with complex power management systems. Automatic intelligent switching between PWM low-noise and PFM low-current mode offers improved system control. During full-power operation, a fixed-frequency 1 MHz (typ). PWM mode drives loads from ~70 mA to 350 mA max, with up to 95% efficiency. Hysteretic PFM mode extends the battery life through reduction of the quiescent current to 15 µA (typ) during light current loads and system standby. Internal synchronous rectification provides high efficiency (90 to 95% typ. at loads between 1 mA and 100 mA). In shutdown mode (Enable pin pulled low) the device turns off and reduces battery consumption to 0.1 µA (typ.).

Typical Application

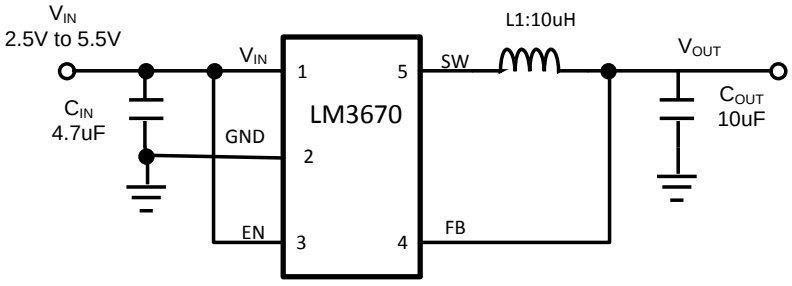
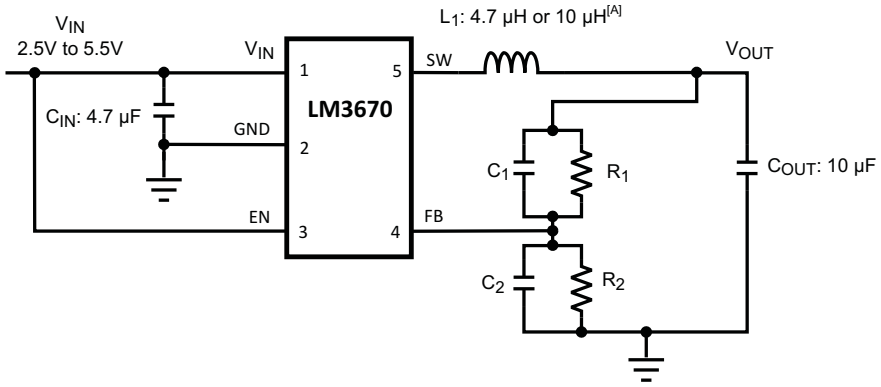


Figure 1. Fixed Output Voltage

DESCRIPTION (CONTINUED)

The LM3670 is available in a SOT-23-5 package. A high switching frequency - 1 MHz (typ) - allows use of tiny surface-mount components. Only three external surface-mount components, an inductor and two ceramic capacitors, are required.

Typical Application (continued)



A. See Table 3

Figure 2. Adjustable Output Voltage

Connection Diagram

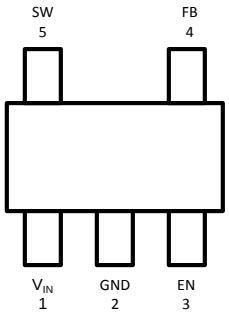


Figure 3. SOT-23-5 Package (Top View)

PIN DESCRIPTIONS

Pin #	Name	Description
1	V_{IN}	Power supply input. Connect to the input filter capacitor (Figure 1).
2	GND	Ground pin.
3	EN	Enable input.
4	FB	Feedback analog input. Connect to the output filter capacitor (Figure 1).
5	SW	Switching node connection to the internal PFET switch and NFET synchronous rectifier. Connect to an inductor with a saturation current rating that exceeds the 750 mA max. Switch Peak Current Limit specification.

ORDERING INFORMATION

ORDERABLE NUMBER	VOLTAGE OPTION (V)
LM3670MF-1.2	1.2
LM3670MFX-1.2	
LM3670MF-1.2/NOPB	
LM3670MFX-1.2/NOPB	
LM3670MF-1.5	1.5
LM3670MFX-1.5	
LM3670MF-1.5/NOPB	
LM3670MFX-1.5/NOPB	
LM3670MF-1.6	1.6
LM3670MFX-1.6	
LM3670MF-1.6/NOPB	
LM3670MFX-1.6/NOPB	
LM3670MF-1.8	1.8
LM3670MFX-1.8	
LM3670MF-1.8/NOPB	
LM3670MFX-1.8/NOPB	
LM3670MF-1.875	1.875
LM3670MFX-1.875	
LM3670MF-1.875/NOPB	
LM3670MFX-1.875/NOPB	
LM3670MF-2.5	2.5
LM3670MFX-2.5	
LM3670MF-2.5/NOPB	
LM3670MFX-2.5/NOPB	
LM3670MF-3.3	3.3
LM3670MFX-3.3	
LM3670MF-3.3/NOPB	
LM3670MFX-3.3/NOPB	
LM3670MF-ADJ	Adjustable
LM3670MFX-ADJ	
LM3670MF-ADJ/NOPB	
LM3670MFX-ADJ/NOPB	

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)

V_{IN} Pin: Voltage to GND	−0.2V to 6.0V
EN Pin: Voltage to GND	−0.2V to 6.0V
FB, SW Pin:	(GND−0.2V) to (V_{IN} + 0.2V)
Junction Temperature (T_{J-MAX})	−45°C to +125°C
Storage Temperature Range	−45°C to +150°C
Maximum Lead Temperature (Soldering, 10 sec.)	260°C
ESD Rating (3)	
Human Body Model:	
VIN, SW, FB, EN, GND	2.0kV
Machine Model:	200V

(1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
(3) The Human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. The machine model is a 200 pF capacitor discharged directly into each pin. MIL-STD-883 3015.7

Operating Ratings (1) (2)

Input Voltage Range	2.5V to 5.5V
Recommended Load Current	0A to 350 mA
Junction Temperature (T_J) Range	−40°C to +125°C
Ambient Temperature (T_A) Range	−40°C to +85°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) All voltages are with respect to the potential at the GND pin.

Thermal Properties

Juntion-to-Ambient Thermal Resistance (θ_{JA}) (1)	250°C/W

(1) Junction-to-ambient thermal resistance is highly dependent on application and board layout. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design.

Electrical Characteristics

Limits in standard typeface are for T_J = 25°C. Limits in **boldface** type apply over the full operating junction temperature range (−40°C ≤ T_J ≤ +125°C). Unless otherwise noted V_{IN} = 3.6V, V_{OUT} = 1.8V, I_O = 150mA, EN = V_{IN}

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IN}	Input Voltage Range	(1)	2.5		5.5	V
V_{OUT}	Fixed Output Voltage: 1.2V	2.5V ≤ V_{IN} ≤ 5.5V I_O = 10 mA	**-2.0**		**+4.0**	%
		2.5V ≤ V_{IN} ≤ 5.5V 0 mA ≤ I_O ≤ 150 mA	**-4.5**		**+4.0**	
	Fixed Output Voltage: 1.5V	2.5V ≤ V_{IN} ≤ 5.5V I_O = 10 mA	**-2.5**		**+4.0**	%
		2.5V ≤ V_{IN} ≤ 5.5V 0 mA ≤ I_O ≤ 350 mA	**-5.0**		**+4.0**	
	Fixed Output Voltage: 1.6V, 1.875V	2.5V ≤ V_{IN} ≤ 5.5V I_O = 10 mA	**-2.5**		**+4.0**	%
		2.5V ≤ V_{IN} ≤ 5.5V 0 mA ≤ I_O ≤ 350 mA	**-5.5**		**+4.0**	
	Fixed Output Voltage: 1.8V	2.5V ≤ V_{IN} ≤ 5.5V I_O = 10 mA	**-1.5**		**+3.0**	%
		2.5V ≤ V_{IN} ≤ 5.5V 0 mA ≤ I_O ≤ 350 mA	**−4.5**		**+3.0**	
	Fixed Output Voltage: 2.5V, 3.3V	3.6V ≤ V_{IN} ≤ 5.5V I_O = 10 mA	**-2.0**		**+4.0**	%
		3.6V ≤ V_{IN} ≤ 5.5V 0 mA ≤ I_O ≤ 350 mA	**-6.0**		**+4.0**	
	Adjustable Output Voltage (2)	2.5V ≤ V_{IN} ≤ 5.5V I_O = 10 mA	**-2.5**		**+4.5**	%
		2.5V ≤ V_{IN} ≤ 5.5V 0 mA ≤ I_O ≤ 150 mA	**-4.0**		**+4.5**	
Line_reg	Line Regulation	2.5V ≤ V_{IN} ≤ 5.5V I_O = 10 mA		0.26		%/V
Load_reg	Load Regulation	150 mA ≤ I_O ≤ 350 mA		0.0014		%/mA
V_{REF}	Internal Reference Voltage			0.5		V
I_{Q_SHDN}	Shutdown Supply Current	T_A=85ºC		0.1	1	µA
I_Q	DC Bias Current into V_{IN}	No load, device is not switching (V_{OUT} forced higher than programmed output voltage)		15	**30**	µA
V_{UVLO}	Minimum V_{IN} below which V_{OUT} will be disabled			**2.4**		V
$R_{DSON\ (P)}$	Pin-Pin Resistance for PFET	V_{IN}=V_{GS}=3.6V		360	**690**	mΩ
$R_{DSON\ (N)}$	Pin-Pin Resistance for NFET	V_{IN}=V_{GS}=3.6V		250	**660**	mΩ
$I_{LKG\ (P)}$	P Channel Leakage Current	V_{DS}=5.5V		0.1	1	µA
$I_{LKG\ (N)}$	N Channel Leakage Current	V_{DS}=5.5V		0.1	1.5	µA
I_{LIM}	Switch Peak Current Limit		**400**	620	**750**	mA
η	Efficiency (V_{IN} = 3.6V, V_{OUT} = 1.8V)	I_{LOAD} = 1 mA		91		%
		I_{LOAD} = 10 mA		94		
		I_{LOAD} = 100 mA		94		
		I_{LOAD} = 200 mA		94		
		I_{LOAD} = 300 mA		92		
		I_{LOAD} = 350 mA		90		
V_{IH}	Logic High Input		**1.3**			V
V_{IL}	Logic Low Input				**0.4**	V

(1) The input voltage range recommended for the specified output voltages are given below: V_{IN} = 2.5V to 5.5V for 0.7V ≤ V_{OUT} < 1.875VV_{IN} = (V_{OUT} + $V_{DROP\ OUT}$) to 5.5V for 1.875 ≤ V_{OUT}≤ 3.3VWhere $V_{DROP\ OUT}$ = I_{LOAD} * ($R_{DSON\ (P)}$ + $R_{INDUCTOR}$)

(2) Output voltage specification for the adjustable version includes tolerance of the external resistor divider.

Electrical Characteristics (continued)

Limits in standard typeface are for T_J = 25°C. Limits in **boldface** type apply over the full operating junction temperature range (−40°C ≤ T_J ≤ +125°C). Unless otherwise noted V_{IN} = 3.6V, V_{OUT} = 1.8V, I_O = 150mA, EN = V_{IN}

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{EN}	Enable (EN) Input Current			0.01	**1**	µA
F_{OSC}	Internal Oscillator Frequency	PWM Mode	**550**	1000	**1300**	kHz

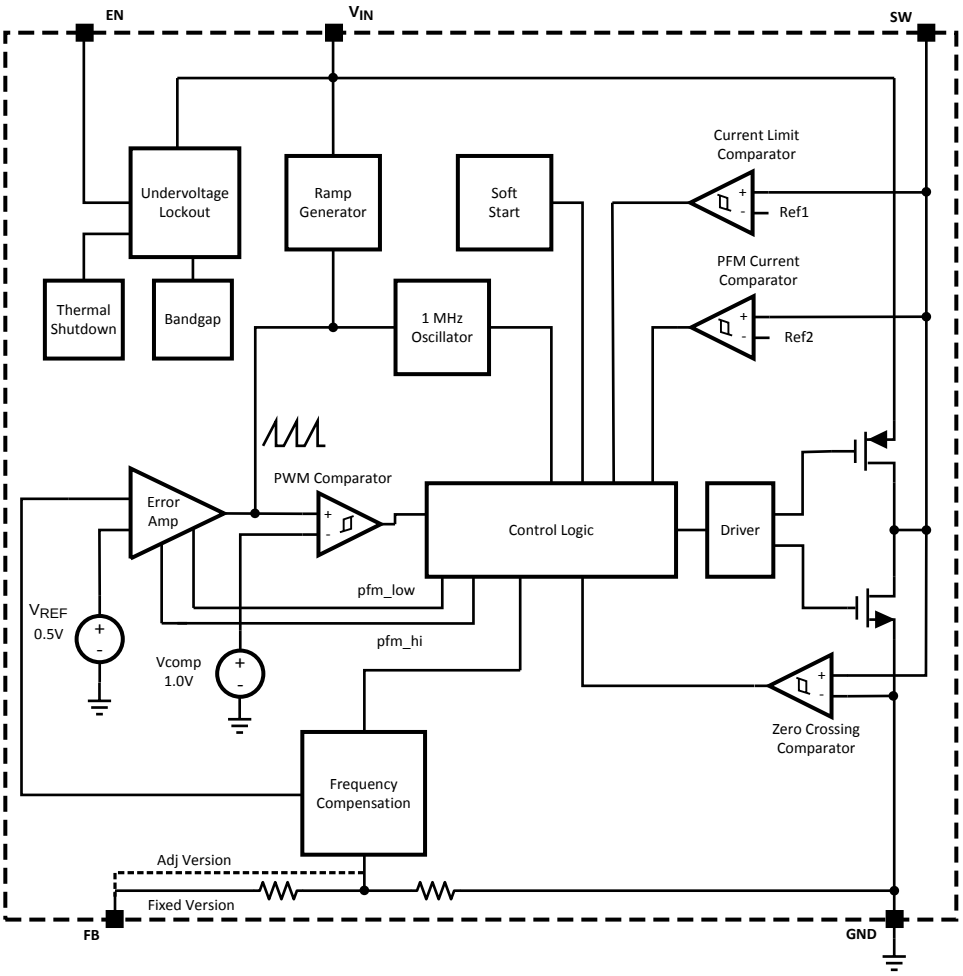


Figure 4. Simplified Functional Diagram

Typical Performance Characteristics

(unless otherwise stated: V_{IN}= 3.6V, V_{OUT}= 1.8V)

I_Q (Non-switching) vs. V_{IN}

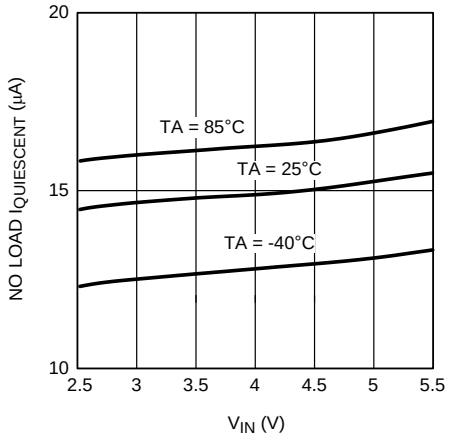


Figure 5.

I_Q vs. Temp

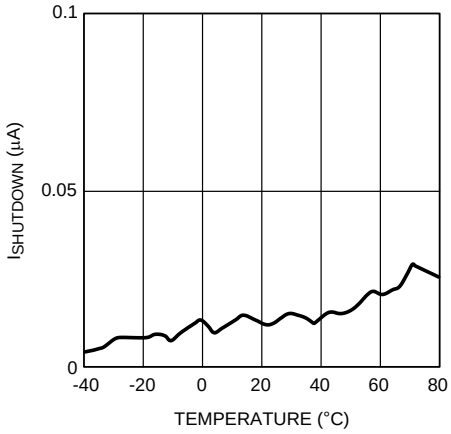


Figure 6.

V_{OUT} vs. V_{IN}

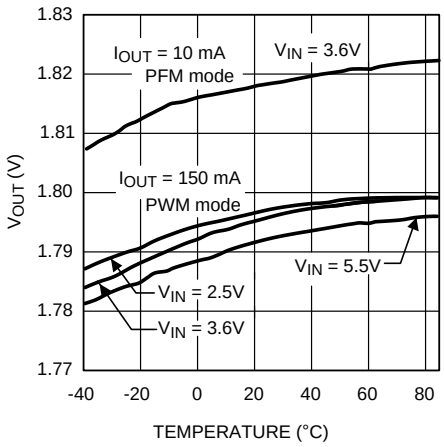


Figure 7.

V_{OUT} vs. I_{OUT}

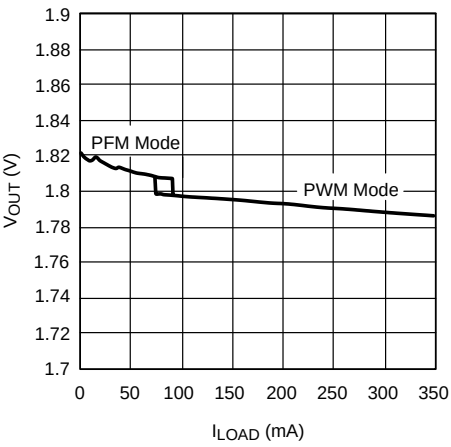


Figure 8.

Efficiency vs. I_{OUT}

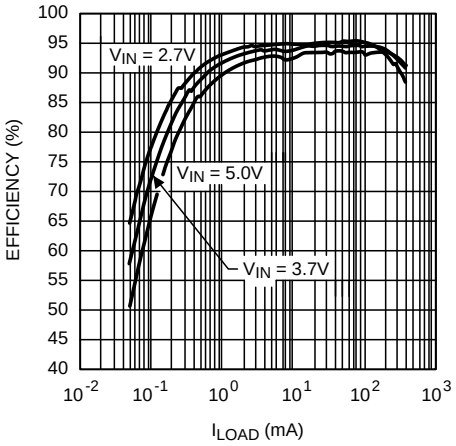


Figure 9.

Efficiency vs. V_{IN}

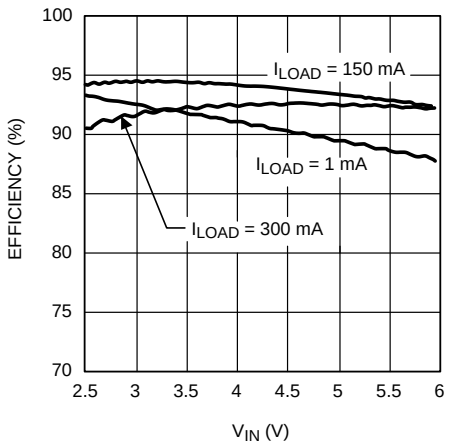


Figure 10.

Typical Performance Characteristics (continued)

(unless otherwise stated: V_{IN}= 3.6V, V_{OUT}= 1.8V)

Frequency vs. Temperature

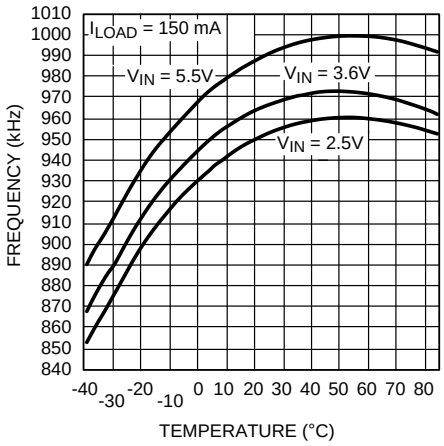


Figure 11.

R_{DSON} vs. V_{IN} P & N Channel

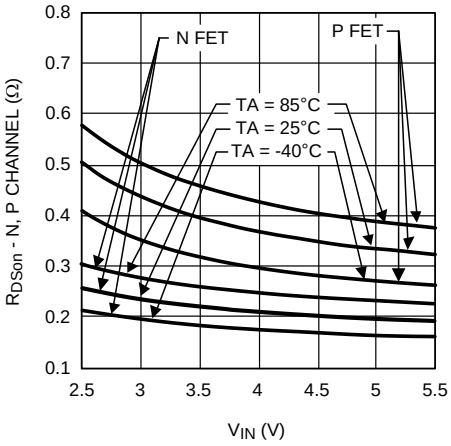


Figure 12.

Line Transient (V_{IN} = 2.6V to 3.6V, I_{LOAD} = 100 mA)

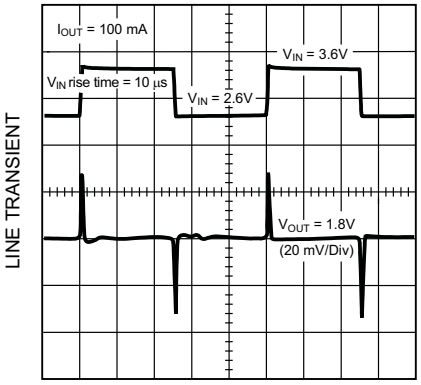


Figure 13.

Line Transient (V_{IN} = 3.6V to 4.6V , I_{LOAD} = 100 mA)

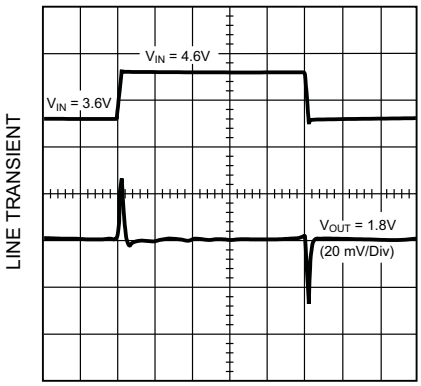


Figure 14.

Load Transient I_{LOAD} = 3mA to 280mA

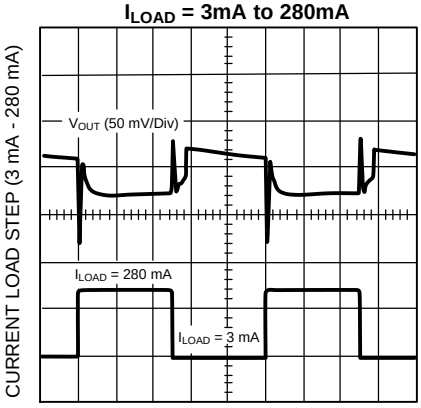


Figure 15.

Load Transient I_{LOAD} = 0mA to 70mA

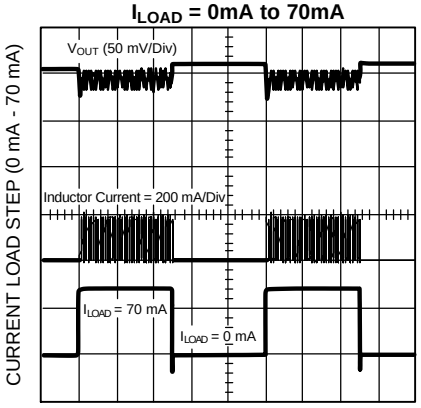


Figure 16.

Typical Performance Characteristics (continued)

(unless otherwise stated: V_{IN}= 3.6V, V_{OUT}= 1.8V)

Load Transient
I_{LOAD} = 0mA to 280mA

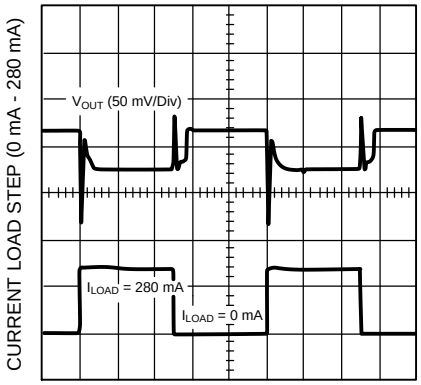


Figure 17.

Load Transient
I_{LOAD} = 0mA to 350mA

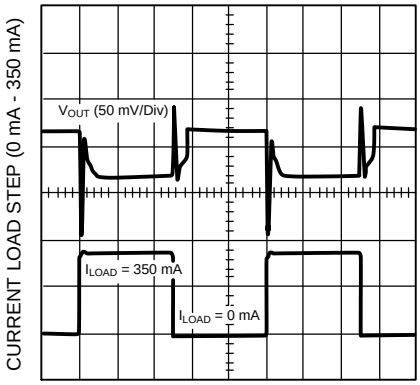


Figure 18.

Load Transient
I_{LOAD} = 50mA to 350mA

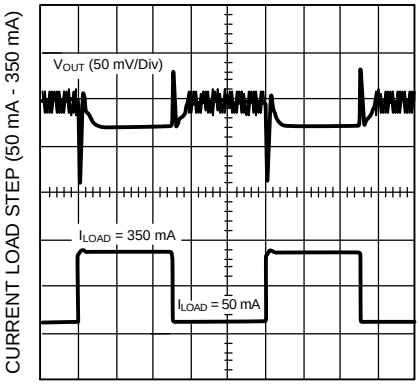


Figure 19.

Load Transient
I_{LOAD} = 100mA to 300mA

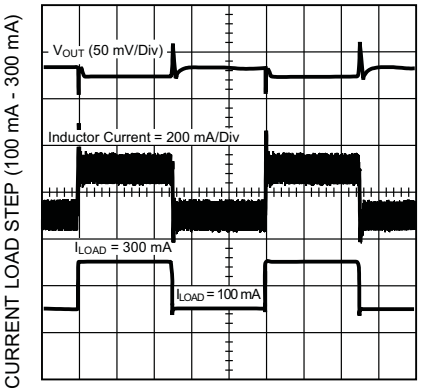


Figure 20.

PFM Mode
V_{SW}, V_{OUT}, $I_{INDUCTOR}$ vs. Time

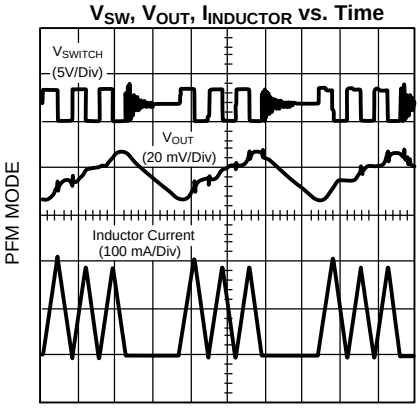


Figure 21.

PWM Mode
V_{SW}, V_{OUT}, $I_{INDUCTOR}$ vs. Time

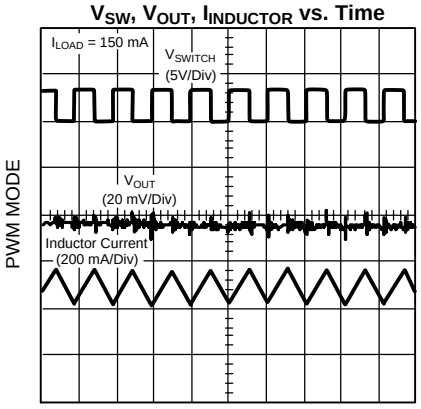


Figure 22.

Typical Performance Characteristics (continued)

(unless otherwise stated: V_{IN}= 3.6V, V_{OUT}= 1.8V)

Soft Start
V_{IN}, V_{OUT}, $I_{INDUCTOR}$ vs. Time
(I_{LOAD} = 350mA)

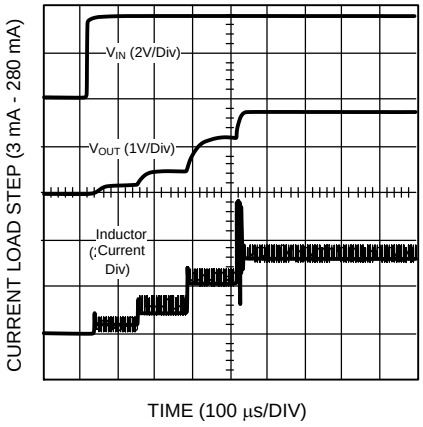


Figure 23.

OPERATION DESCRIPTION

Device Information

The LM3670, a high efficiency step down DC-DC switching buck converter, delivers a constant voltage from either a single Li-Ion or three cell NiMH/NiCd battery to portable devices such as cell phones and PDAs. Using a voltage mode architecture with synchronous rectification, the LM3670 has the ability to deliver up to 350 mA depending on the input voltage and output voltage (voltage head room), and the inductor chosen (maximum current capability).

There are three modes of operation depending on the current required - PWM (Pulse Width Modulation), PFM (Pulse Frequency Modulation), and shutdown. PWM mode handles current loads of approximately 70 mA or higher. Lighter output current loads cause the device to automatically switch into PFM for reduced current consumption (I_Q = 15 µA typ) and a longer battery life. Shutdown mode turns off the device, offering the lowest current consumption ($I_{SHUTDOWN}$ = 0.1 µA typ).

The LM3670 can operate up to a 100% duty cycle (PMOS switch always on) for low drop out control of the output voltage. In this way the output voltage will be controlled down to the lowest possible input voltage.

Additional features include soft-start, under voltage lock out, current overload protection, and thermal overload protection. As shown in Figure 1, only three external power components are required for implementation.

Circuit Operation

The LM3670 operates as follows. During the first portion of each switching cycle, the control block in the LM3670 turns on the internal PFET switch. This allows current to flow from the input through the inductor to the output filter capacitor and load. The inductor limits the current to a ramp with a slope of

$$\frac{V_{IN}-V_{OUT}}{L} \quad (1)$$

by storing energy in a magnetic field. During the second portion of each cycle, the controller turns the PFET switch off, blocking current flow from the input, and then turns the NFET synchronous rectifier on. The inductor draws current from ground through the NFET to the output filter capacitor and load, which ramps the inductor current down with a slope of

$$\frac{-V_{OUT}}{L} \quad (2)$$

The output filter stores charge when the inductor current is high, and releases it when low, smoothing the voltage across the load.

PWM Operation

During PWM operation the converter operates as a voltage-mode controller with input voltage feed forward. This allows the converter to achieve excellent load and line regulation. The DC gain of the power stage is proportional to the input voltage. To eliminate this dependence, feed forward inversely proportional to the input voltage is introduced.

Internal Synchronous Rectification

While in PWM mode, the LM3670 uses an internal NFET as a synchronous rectifier to reduce rectifier forward voltage drop and associated power loss. Synchronous rectification provides a significant improvement in efficiency whenever the output voltage is relatively low compared to the voltage drop across an ordinary rectifier diode.

Current Limiting

A current limit feature allows the LM3670 to protect itself and external components during overload conditions PWM mode implements cycle-by-cycle current limiting using an internal comparator that trips at 620 mA (typ).

PFM Operation

At very light load, the converter enters PFM mode and operates with reduced switching frequency and supply current to maintain high efficiency.

The part automatically transition into PFM mode when either of two conditions occurs for a duration of 32 or more clock cycles:

A. The inductor current becomes discontinuous

B. The peak PMOS switch current drops below the I_{MODE} level:

$$I_{MODE} < 26\ mA + \frac{V_{IN}}{50\Omega}\ (typ) \tag{3}$$

During PFM operation, the converter positions the output voltage slightly higher than the nominal output voltage in PWM operation, allowing additional headroom for voltage drop during a load transient from light to heavy load. The PFM comparator senses the output voltage via the feedback pin and control the switching of the output FETs such that the output voltage ramps between 0.8% and 1.6% (typ) above the nominal PWM output voltage. If the output voltage is below the 'high' PFM comparator threshold, the PMOS power switch is turned on. It remains on until the output voltage exceeds the 'high' PFM threshold or the peak current exceeds the I_{PFM} level set for PFM mode. The peak current in PFM mode is:

$$I_{PFM\ Peak} = 117\ mA + \frac{V_{IN}}{64\Omega}\ (typ) \tag{4}$$

Once the PMOS power switch is turned off, the NMOS power switch is turned on until the inductor current ramps to zero. When the NMOS zero-current condition is detected, the NMOS power switch is turned off. If the output voltage is below the 'high' PFM comparator threshold (see Figure 24), the PMOS switch is again turned on and the cycle is repeated until the output reaches the desired level. Once the output reaches the 'high' PFM threshold, the NMOS switch is turned on briefly to ramp the inductor current to zero and then both output switches are turned off and the part enters an extremely low power mode. Quiescent supply current during this 'sleep' mode is less than 30 µA, which allows the part to achieve high efficiencies under extremely light load conditions. When the output drops below the 'low' PFM threshold, the cycle repeats to restore the output voltage to ~1.6% above the nominal PWM output voltage.

If the load current should increase during PFM mode (see Figure 24) causing the output voltage to fall below the 'low2' PFM threshold, the part automatically transitions into fixed-frequency PWM mode.

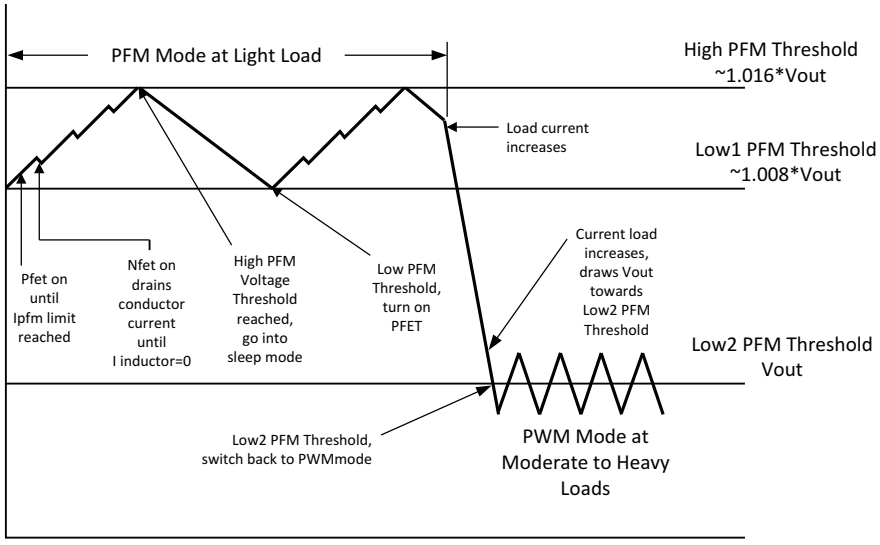


Figure 24. Operation in PFM Mode and Transition to PWM Mode

Soft-Start

The LM3670 has a soft-start circuit that limits in-rush current during start-up. Typical start-up times with a 10µF output capacitor and 350mA load is 400µs:

Inrush Current (mA)	Duration (µSec)
0	32
70	224
140	256
280	256
620	until soft start ends

LDO - Low Drop Out Operation

The LM3670 can operate at 100% duty cycle (no switching, PMOS switch is completely on) for low drop out support of the output voltage. In this way the output voltage is controlled down to the lowest possible input voltage.

The minimum input voltage needed to support the output voltage is

$$V_{IN,MIN} = I_{LOAD} * (R_{DSON,PFET} + R_{INDUCTOR}) + V_{OUT}$$

where

- I_{LOAD} is the load current
- $R_{DSON,\ PFET}$ is the drain to source resistance of PFET switch in the triode region
- $R_{INDUCTOR}$ is the Inductor resistance

(5)

Application Information

Output Voltage Selection for Adjustable LM3670

The output voltage of the adjustable parts can be programmed through the resistor network connected from V_{OUT} to V_{FB} then to GND. V_{OUT} is adjusted to make V_{FB} equal to 0.5V. The resistor from V_{FB} to GND (R2) should be at least 100KΩ to keep the current sunk through this network well below the 15µA quiescent current level (PFM mode with no switching) but large enough that it is not susceptible to noise. If R_2 is 200KΩ, and V_{FB} is 0.5V, then the current through the resistor feedback network is 2.5µA (I_{FB} =0.5V/R_2). The output voltage formula is:

$$V_{OUT} = V_{FB} * \left(\frac{R_1}{R_2} + 1\right)$$

where

- V_{OUT} Output Voltage (V)
- V_{FB} Feedback Voltage (0.5V typ)
- R_1 Resistor from V_{OUT} to V_{FB} (Ω)
- R_2 Resistor from V_{OUT} to GND (Ω)

(6)

For any output voltage greater than or equal to 0.7V a frequency zero must be added at 10kHz for stability. The formula is:

$$C_1 = \frac{1}{2 * \pi * R_1 * 10\ kHz}$$

(7)

For any output voltages below 0.7 and above or equal to 2.5V, a pole must also be placed at 10kHz as well. The lowest output voltage possible is 0.7V. At low output voltages the duty cycle is very small and, as the input voltage increases, the duty cycle decreases even further. Since the duty cycle is so low any change due to noise is an appreciable percentage. In other words, it is susceptible to noise. Capacitors C_1 and C_2 act as noise filters rather than frequency poles and zeros. If the pole and zero are at the same frequency the formula is:

$$C_2 = \frac{1}{2 * \pi * R_2 * 10\ kHz}$$

(8)

A pole can also be used at higher output voltages. For example, in Table 3, there is an entry for 1.24V with both a pole and zero at approximately 10kHz for noise rejection.

Inductor Selection

There are two main considerations when choosing an inductor; the inductor current should not saturate, and the inductor current ripple is small enough to achieve the desired output voltage ripple.

There are two methods to choose the inductor current rating.

Method 1:

The total current is the sum of the load and the inductor ripple current. This can be written as

$$I_{MAX} = I_{LOAD} + \frac{I_{RIPPLE}}{2} \tag{9}$$

$$V_{OUT} = I_{LOAD} + \left(\frac{V_{IN}-V_{OUT}}{2 * L}\right)\left(\frac{V_{OUT}}{V_{IN}}\right)\left(\frac{1}{f}\right)$$

where

- I_{LOAD} load current
- V_{IN} input voltage
- L inductor
- f switching frequency
- I_{RIPPLE} peak-to-peak (10)

Method 2:

A more conservative approach is to choose an inductor that can handle the current limit of 700 mA.

Given a peak-to-peak current ripple (I_{PP}) the inductor needs to be at least

$$L >= \left(\frac{V_{IN} - V_{OUT}}{I_{PP}}\right) * \left(\frac{V_{OUT}}{V_{IN}}\right) * \left(\frac{1}{f}\right) \tag{11}$$

A 10 µH inductor with a saturation current rating of at least 800 mA is recommended for most applications. The inductor's resistance should be less than around 0.3Ω for good efficiency. Table 1 lists suggested inductors and suppliers. For low-cost applications, an unshielded bobbin inductor is suggested. For noise critical applications, a toroidal or shielded-bobbin inductor should be used. A good practice is to lay out the board with overlapping footprints of both types for design flexibility. This allows substitution of a low-noise toroidal inductor, in the event that noise from low-cost bobbin models is unacceptable.

Input Capacitor Selection

A ceramic input capacitor of 4.7 µF is sufficient for most applications. A larger value may be used for improved input voltage filtering. The input filter capacitor supplies current to the PFET switch of the LM3670 in the first half of each cycle and reduces voltage ripple imposed on the input power source. A ceramic capcitor's low ESR provides the best noise filtering of the input voltage spikes due to this rapidly changing current. Select an input filter capacitor with a surge current rating sufficient for the power-up surge from the input power source. The power-up surge current is approximately the capacitor's value (µF) times the voltage rise rate (V/µs). The input current ripple can be calculated as:

$$I_{RMS} = I_{OUTMAX} * \sqrt{\frac{V_{OUT}}{V_{IN}} * \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

The worst case IRMS is:

$$IRMS = \frac{IRMS}{2} \qquad \text{(duty cycle = 50\%)} \tag{12}$$

Table 1. Suggested Inductors and Their Suppliers

Model	Vendor	Phone	FAX
IDC2512NB100M	Vishay	408-727-2500	408-330-4098
DO1608C-103	Coilcraft	847-639-6400	847-639-1469
ELL6RH100M	Panasonic	714-373-7366	714-373-7323
CDRH5D18-100	Sumida	847-956-0666	847-956-0702

Output Capacitor Selection

The output filter capacitor smoothes out current flow from the inductor to the load, maintaining a steady output voltage during transient load changes and reduces output voltage ripple. These capacitors must be selected with sufficient capacitance and sufficiently low ESR to perform these functions.

The output ripple current can be calculated as:

Voltage peak-to-peak ripple due to capacitance = $V_{PP\text{-}C} = \frac{I_{PP}}{f*8*C}$

Voltage peak-to-peak ripple due to ESR = $V_{OUT} = V_{PP\text{-}ESR} = I_{PP} * R_{ESR}$

Voltage peak-to-peak ripple, root mean squared = $V_{PP\text{-}RMS} = \sqrt{V_{PP\text{-}C}^2 + V_{PP\text{-}ESR}^2}$

Note that the output ripple is dependent on the current ripple and the equivalent series resistance of the output capacitor (R_{ESR}).

Because these two components are out of phase the rms value is used. The R_{ESR} is frequency dependent (as well as temperature dependent); make sure the frequency of the R_{ESR} given is the same order of magnitude as the switching frequency.

Table 2. Suggested Capacitors and Their Suppliers

Model	Type	Vendor	Phone	FAX
10 µF for C_{OUT}				
VJ1812V106MXJAT	Ceramic2	Vishay3	408-727-25004	408-330-4098 5
LMK432BJ106MM	Ceramic	Taiyo-Yuden	847-925-0888	847-925-0899
JMK325BJ106MM	Ceramic	Taiyo-Yuden	847-925-0888	847-925-0899
4.7 µF for C_{IN}				
VJ1812V475MXJAT	Ceramic	Vishay	408-727-2500	408-330-4098
EMK325BJ475MN	Ceramic	Taiyo-Yuden	847-925-0888	847-925-0899
C3216X5R0J475M	Ceramic	TDK	847-803-6100	847-803-6296

Table 3. Adjustable LM3670 Configurations for Various V_{OUT}

VOUT (V)	R1 (KΩ)	R2 (KΩ)	C1 (pF)	C2 (pF)	L (µH)	CIN (µF)	COUT (µF)
0.7	80.6	200	200	150	4.7	4.7	10
0.8	120	200	130	none	4.7	4.7	10
0.9	160	200	100	none	4.7	4.7	10
1.0	200	200	82	none	4.7	4.7	10
1.1	240	200	68	none	4.7	4.7	10
1.2	280	200	56	none	4.7	4.7	10
1.24	300	200	56	none	4.7	4.7	10
1.24	221	150	75	120	4.7	4.7	10
1.5	402	200	39	none	10	4.7	10
1.6	442	200	39	none	10	4.7	10
1.7	487	200	33	none	10	4.7	10
1.875	549	200	30	none	10	4.7	14.7 (1)
2.5	806	200	22	82	10	4.7	22

(1) (10 || 4.7)

Board Layout Considerations

PC board layout is an important part of DC-DC converter design. Poor board layout can disrupt the performance of a DC-DC converter and surrounding circuitry by contributing to EMI, ground bounce, and resistive voltage loss in the traces. These can send erroneous signals to the DC-DC converter IC, resulting in poor regulation or instability.

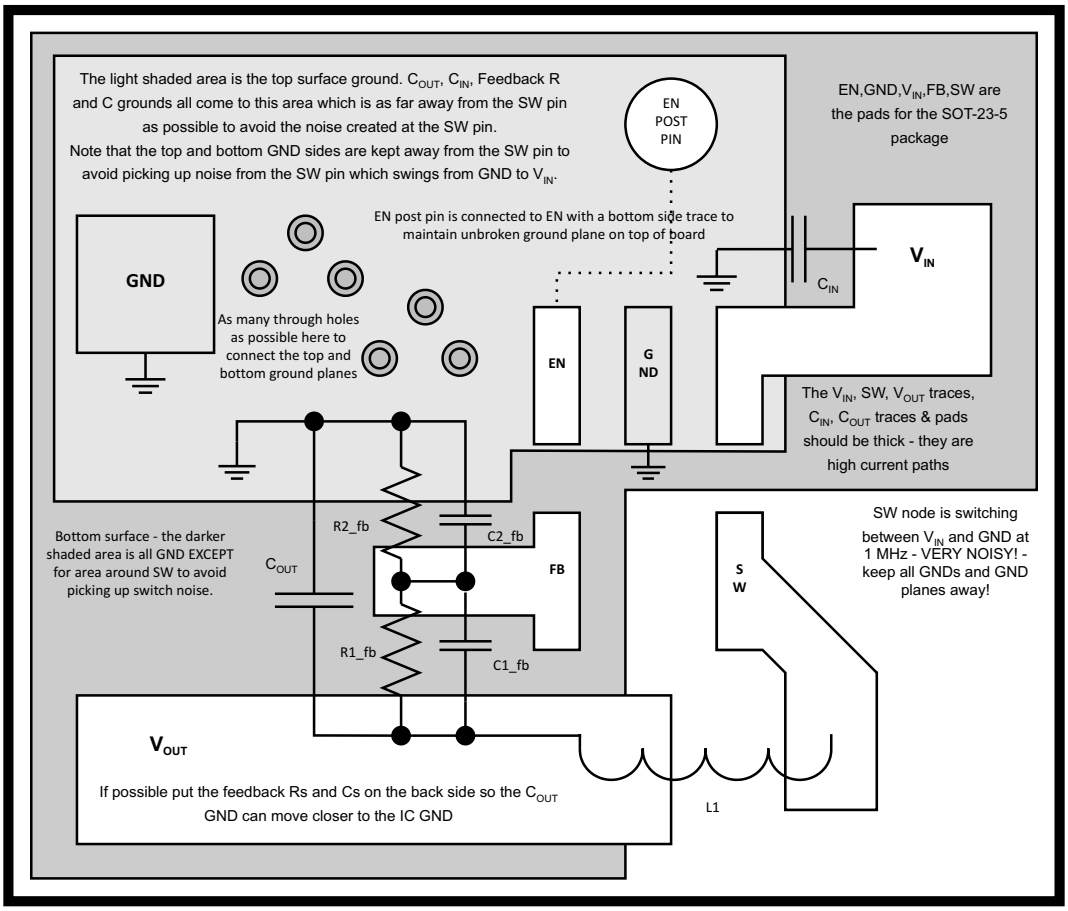


Figure 25. Board Layout Design Rules for the LM3670

Good layout for the LM3670 can be implemented by following a few simple design rules, as illustrated in Figure 25.

- *Place the LM3670, inductor and filter capacitors close together and make the traces short.* The traces between these components carry relatively high switching currents and act as antennas. Following this rule reduces radiated noise. Place the capacitors and inductor within 0.2 in. (5 mm) of the LM3670.
- *Arrange the components so that the switching current loops curl in the same direction.* During the first half of each cycle, current flows from the input filter capacitor, through the LM3670 and inductor to the output filter capacitor and back through ground, forming a current loop. In the second half of each cycle, current is pulled up from ground, through the LM3670 by the inductor, to the output filter capacitor and then back through ground, forming a second current loop. Routing these loops so the current curls in the same direction prevents magnetic field reversal between the two half-cycles and reduces radiated noise.
- *Connect the ground pins of the LM3670, and filter capacitors together using generous component-side copper fill as a pseudo-ground plane. Then, connect this to the ground-plane (if one is used) with several vias.* This reduces ground-plane noise by preventing the switching currents from circulating through the ground plane. It also reduces ground bounce at the LM3670 by giving it a low-impedance ground connection.
- *Use wide traces between the power components and for power connections to the DC-DC converter circuit.* This reduces voltage errors caused by resistive losses across the traces.
- *Route noise sensitive traces, such as the voltage feedback path, away from noisy traces between the power components.* The voltage feedback trace must remain close to the LM3670 circuit and should be direct but should be routed opposite to noisy components. This reduces EMI radiated onto the DC-DC converter's own voltage feedback trace.
- *Place noise sensitive circuitry, such as radio IF blocks, away from the DC-DC converter, CMOS digital blocks and other noisy circuitry.* Interference with noise-sensitive circuitry in the system can be reduced through distance.

In mobile phones, for example, a common practice is to place the DC-DC converter on one corner of the board, arrange the CMOS digital circuitry around it (since this also generates noise), and then place sensitive preamplifiers and IF stages on the diagonally opposing corner. Often, the sensitive circuitry is shielded with a metal pan and power to it is post-regulated to reduce conducted noise, using low-dropout linear regulators.

REVISION HISTORY

Changes from Revision D (February 2013) to Revision E	Page
• Changed layout of National Data Sheet to TI format	17

1-Nov-2015

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM3670MF-1.2/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	SCZB	Samples
LM3670MF-1.5/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	S82B	Samples
LM3670MF-1.6/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	SDBB	Samples
LM3670MF-1.8	NRND	SOT-23	DBV	5		TBD	Call TI	Call TI	-40 to 85	SDCB	
LM3670MF-1.8/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	SDCB	Samples
LM3670MF-1.875/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	SEFB	Samples
LM3670MF-3.3	NRND	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	-40 to 85	SDEB	
LM3670MF-3.3/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	SDEB	Samples
LM3670MF-ADJ/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	SDFB	Samples
LM3670MFX-1.2/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	SCZB	Samples
LM3670MFX-1.8/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	SDCB	Samples
LM3670MFX-ADJ/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	SDFB	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

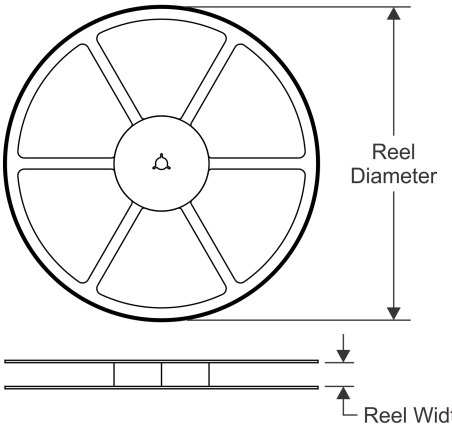
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

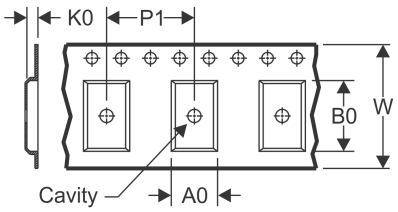
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

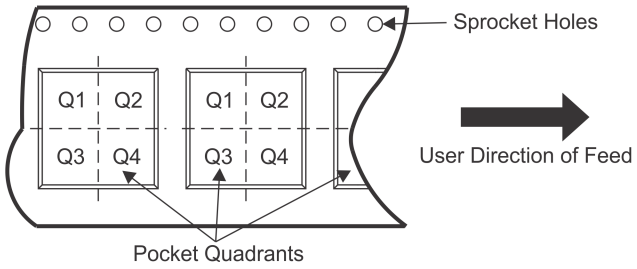


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



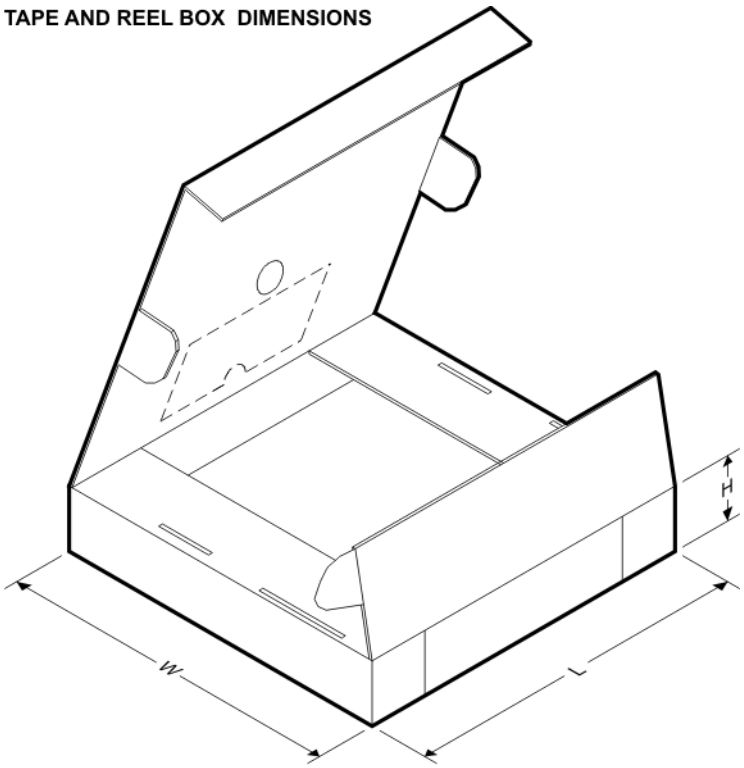
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM3670MF-1.2/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM3670MF-1.5/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM3670MF-1.6/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM3670MF-1.8/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM3670MF-1.875/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM3670MF-3.3	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM3670MF-3.3/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM3670MF-ADJ/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM3670MFX-1.2/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM3670MFX-1.8/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM3670MFX-ADJ/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

PACKAGE MATERIALS INFORMATION

2-Sep-2015

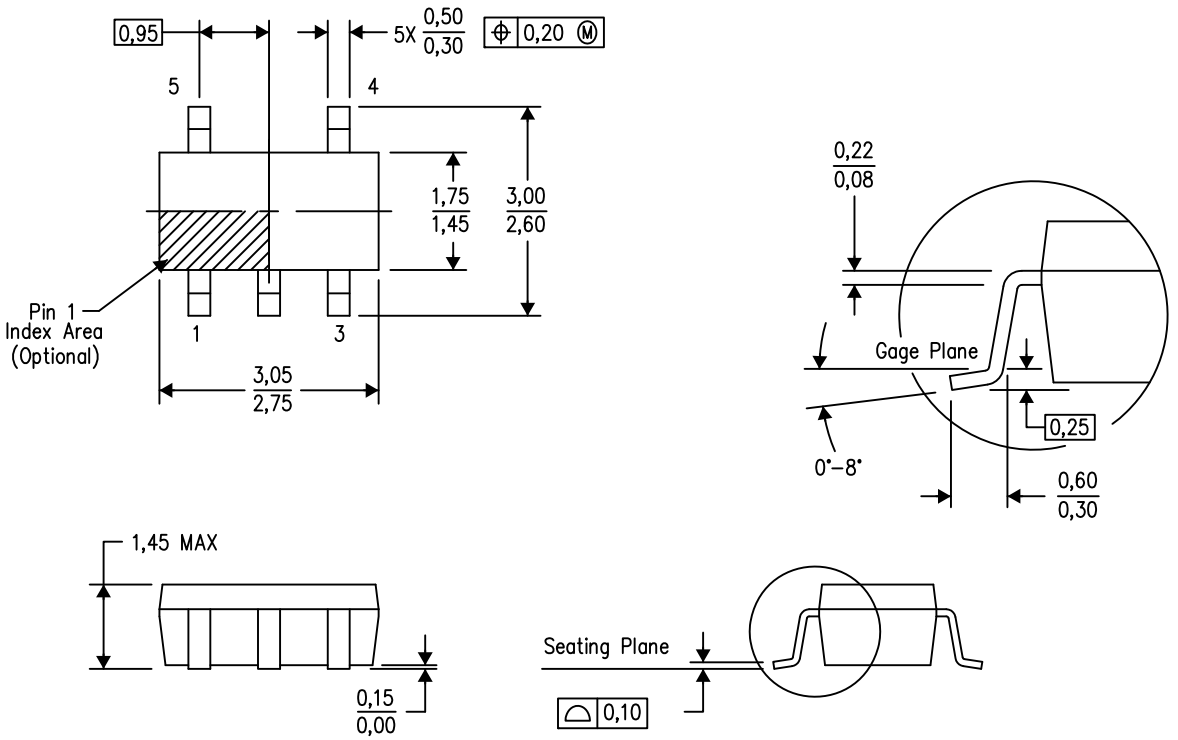
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM3670MF-1.2/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LM3670MF-1.5/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LM3670MF-1.6/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LM3670MF-1.8/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LM3670MF-1.875/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LM3670MF-3.3	SOT-23	DBV	5	1000	210.0	185.0	35.0
LM3670MF-3.3/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LM3670MF-ADJ/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LM3670MFX-1.2/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LM3670MFX-1.8/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LM3670MFX-ADJ/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0

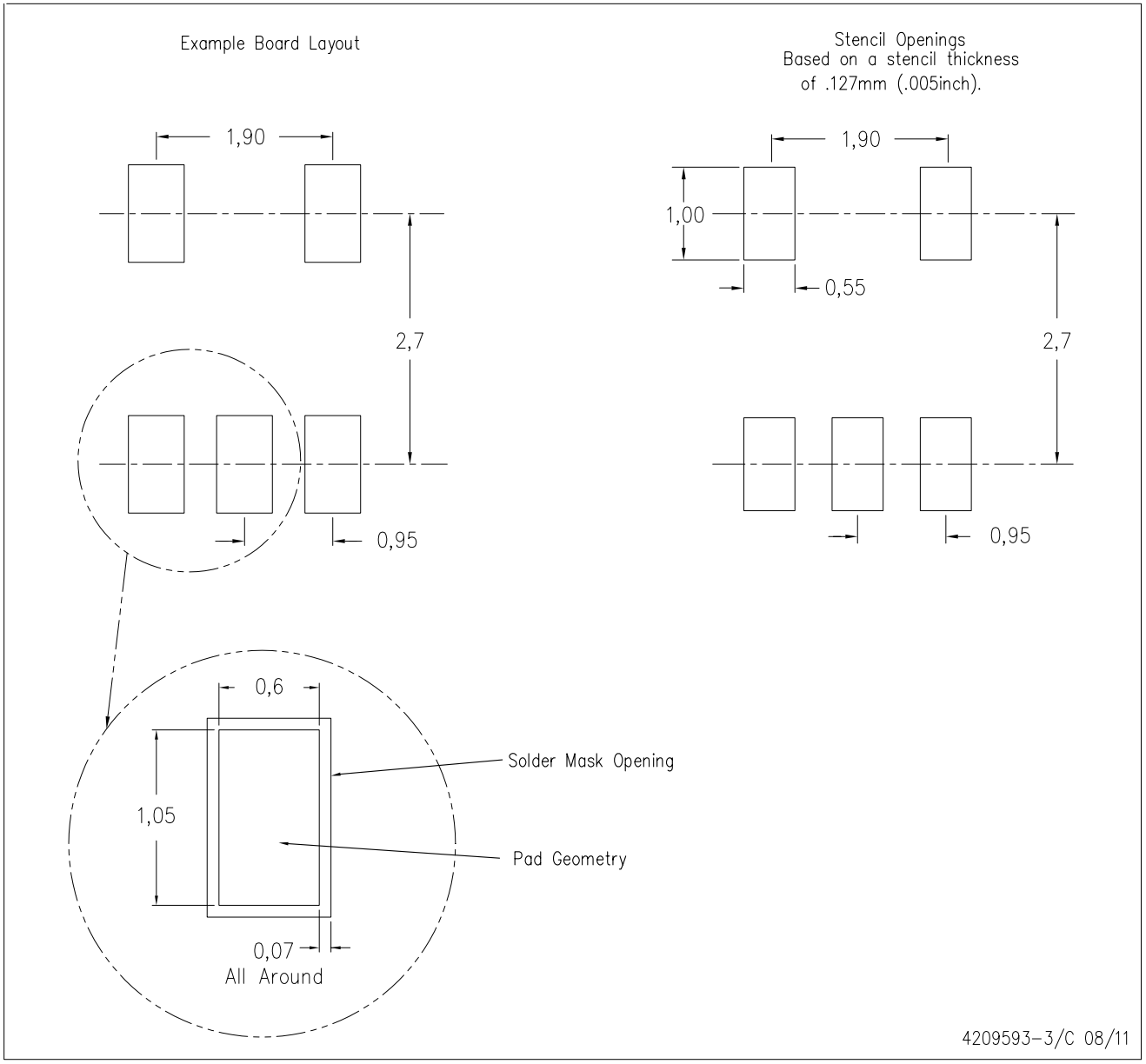
DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4073253–4/N 12/14

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

DBV (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.