LM49352 Boomer™ Mono Class D Audio Codec Subsystem with Ground Referenced Headphone Amplifiers, Earpiece Driver, and Audio DSP

Check for Samples: LM49352

FEATURES

- Ultra Efficient, Spread Spectrum Class D Loudspeaker Amplifier that Operates at 93% Efficiency
- Low Voltage, True Ground Headphone Amplifier Operation
- High Performance 103dB SNR Stereo DAC
- High Performance 97dB SNR Stereo ADC
- Up to 96kHz Stereo Audio Playback
- Up to 48kHz Stereo Recording
- Dual Bidirectional I^2S or PCM Compatible Audio Interfaces
- Read/Write I^2C Compatible Control Interface
- Flexible Digital Mixer with Sample Rate Conversion
- Sigma-Delta PLL Clock Network that Supports System Clocks up to 50MHz Including 13MHz, 19.2MHz, and 26MHz
- Dual stereo 5 band parametric equalizers
- Cascadable DSP Effects that Allow Stereo 10 Band Parametric Equalization
- ALC/Limiter/Compressor on Both DAC and ADC Paths
- Dedicated Earpiece Speaker Amplifier
- Stereo Auxiliary Inputs and Mono Differential Input
- Differential Microphone Input with Single-Ended Option
- Automatic Level Control for Digital Audio Inputs, Mono Differential Input, Microphone Input, and Stereo Auxiliary Inputs
- Flexible Audio Routing from Input to Output
- 16 Step Volume Control for Microphone with 2dB Steps
- 32 Step Volume Control for Auxiliary Inputs in 1.5dB Steps
- 4 Step Volume Control for Class D Loudspeaker Amplifier
- 8 Step Volume Control for Headphone Amplifier
- Micro-Power Shutdown Mode
- Available in the 3.3 x 3.3 mm 36 bump DSBGA package

APPLICATIONS

- Smart Phones
- Mobile Phones and VOIP Phones
- Portable GPS Navigator and Portable Gaming Devices
- Portable DVD/CD/AAC/MP3/MP4 Players
- Digital Cameras/Camcorders

KEY SPECIFICATIONS

- Class D Amplifier Efficiency 93% (Typ)
- P_{EP} at A_V_{DD} = 3.3V, 32Ω, 1% THD 58mW (Typ)
- P_{HP} at HP_V_{DD} = 2.8V, Stereo 32Ω, 1% THD 65mW/ch (Typ)
- P_{LS} at LS_V_{DD} = 5V, 8Ω, 1% THD 1.4W (Typ)
- P_{LS} at LS_V_{DD} = 4.2V, 8Ω, 1% THD 970 mW (Typ)
- P_{LS} at LS_V_{DD} = 3.3V, 8Ω, 1% THD 590 mW (Typ)
- SNR (Stereo DAC at 48kHz) 103 dB (Typ)
- PSRR at 217 Hz, A_V_{DD} = 3.3V, (HP from AUX) 100dB (Typ)

DESCRIPTION

The LM49352 is a high performance mixed signal audio subsystem. The LM49352 includes a high quality stereo DAC, a high quality stereo ADC, a stereo headphone amplifier, which supports True Ground operation, a low EMI Class D loudspeaker amplifier, and an earpiece speaker amplifier. It combines advanced audio processing, conversion, mixing, and amplification in the smallest possible footprint while extending the battery life of feature rich portable devices.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Boomer is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2009–2013, Texas Instruments Incorporated

DESCRIPTION (CONTINUED)

The LM49352 features dual bi-directional I^2S or PCM audio interfaces and an I^2C compatible interface for control. The stereo DAC path features an SNR of 103dB with 24-bit 48 kHz input. The headphone amplifier delivers $65mW_{RMS}$ (typ) to a 32Ω single-ended stereo load with less than 1% distortion (THD+N) when HP_V_{DD} = 2.8V. The loudspeaker amplifier delivers up to 970mW into an 8Ω load with less than 1% distortion when LS_V_{DD} = 4.2V.

The LM49352 employs advanced techniques to extend battery life, to reduce controller overhead, to speed development time, and to eliminate click and pop artifacts. Boomer audio power amplifiers are designed specifically for mobile devices and require minimal PCB area and external components.

LM49352 Overview

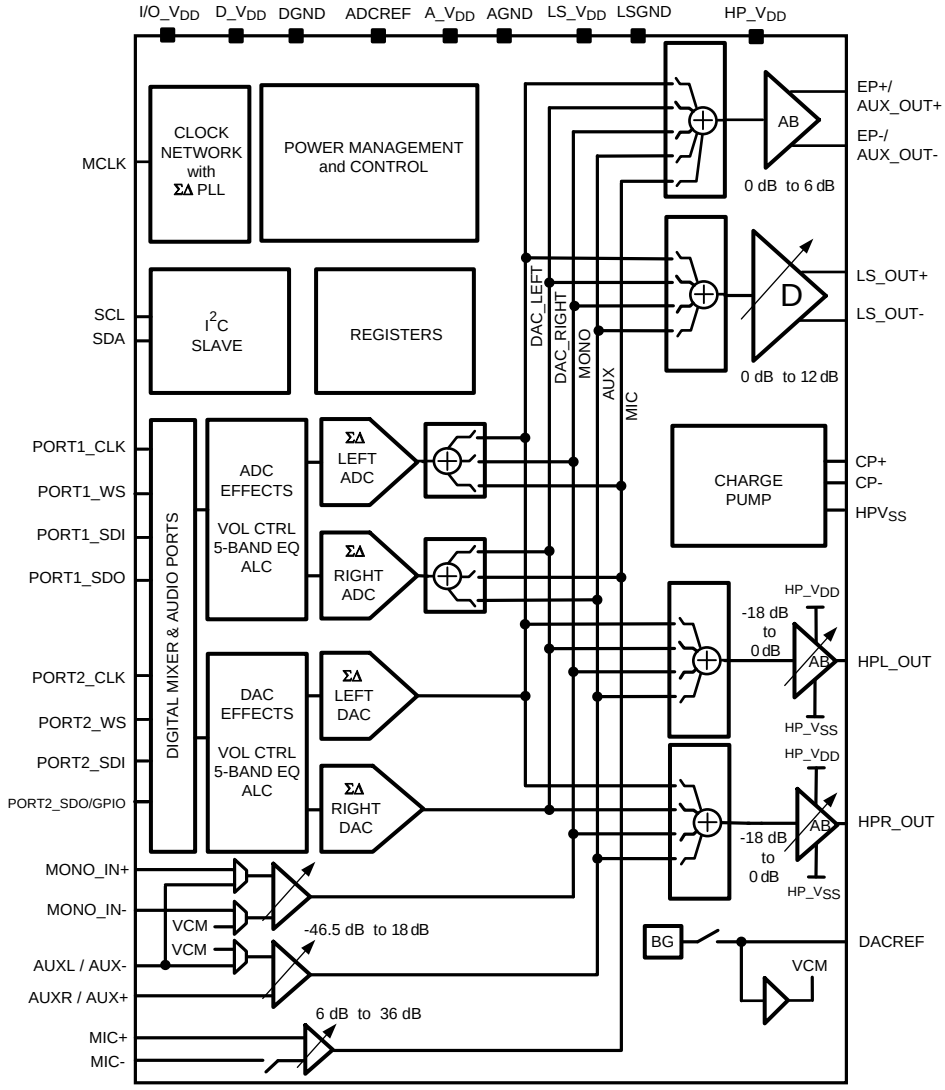


Figure 1. LM49352 Block Diagram

Copyright © 2009–2013, Texas Instruments Incorporated

Typical Application

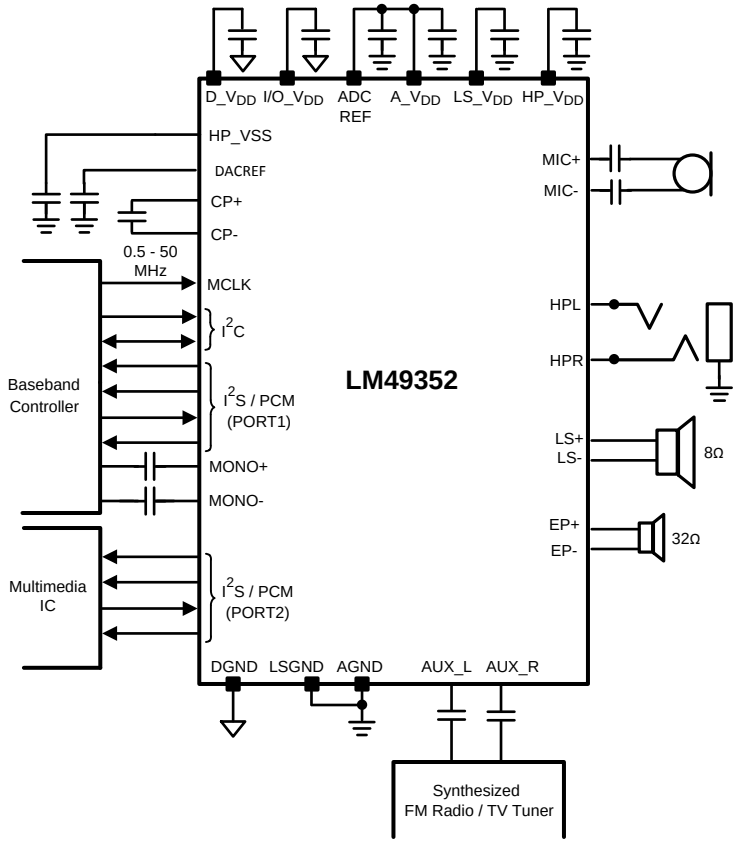


Figure 2. Example Application in Multimedia Phone with Dedicated Earpiece Speaker and Mono Loudspeaker

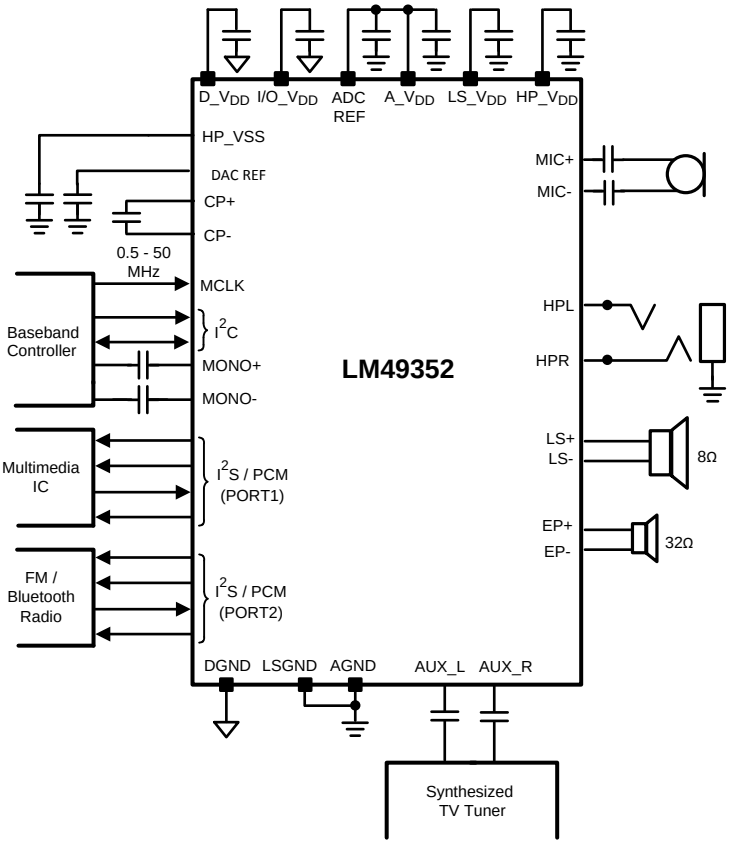


Figure 3. Example Application in Multimedia Phone Using Multiple Media Sources

Copyright © 2009–2013, Texas Instruments Incorporated

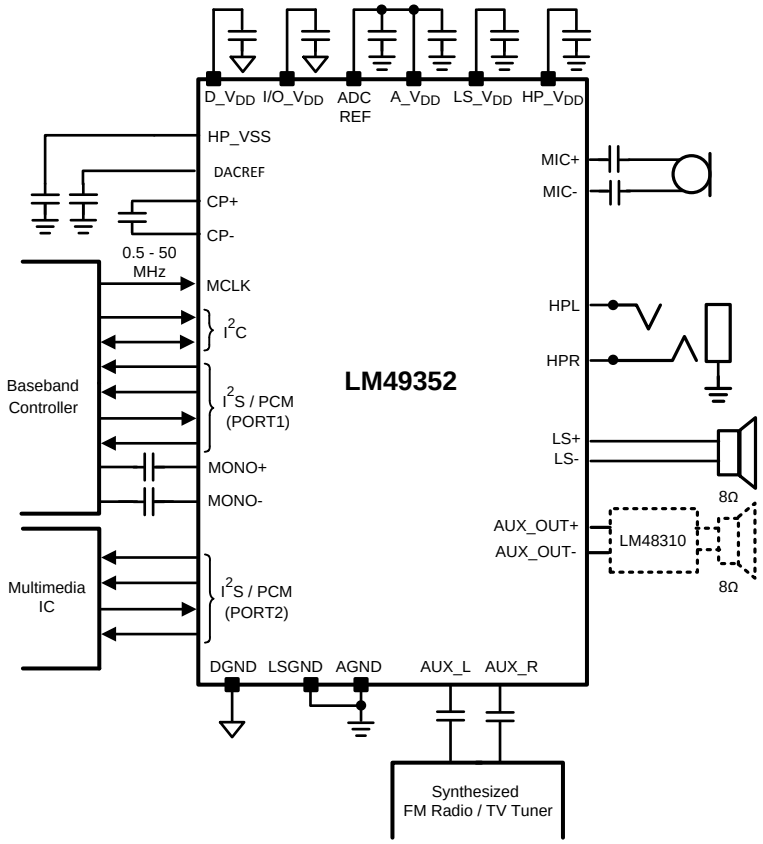


Figure 4. Example Application in a Multimedia Phone with Stereo Loudspeaker

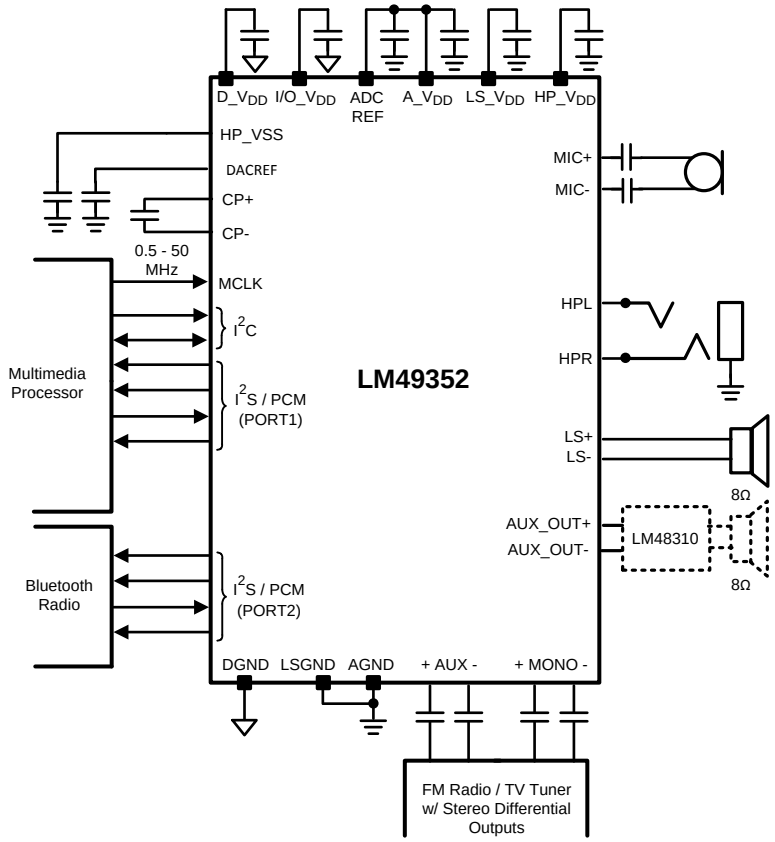


Figure 5. Example Application in a Portable Media Player with Stereo Loudspeakers

Connection Diagrams

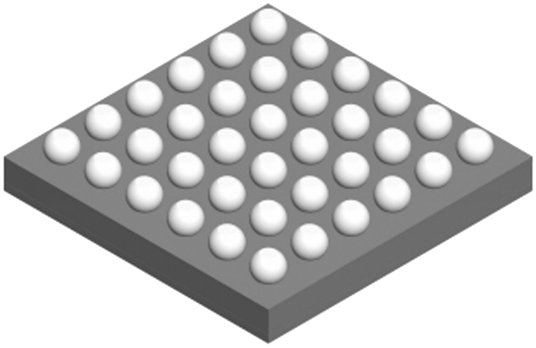


Figure 6. 36 Bump DSBGA

Copyright © 2009–2013, Texas Instruments Incorporated

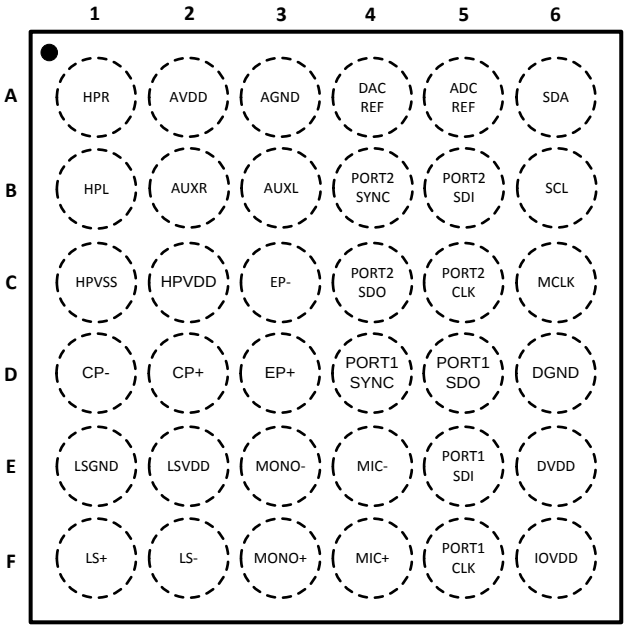


Figure 7. LM49352RL Pinout Diagram
Top View (Bump Side Down)

PIN DESCRIPTIONS

Pin	Pin Name	Type	Direction	Description
A1	HPR	Analog	Output	Headphone right output
A2	A_V_{DD}	Supply	Input	DAC (Analog), ADC (Analog), PLL (Analog), input stages, analog mixer (AUX and class D), and Earpiece amplifier power supply input
A3	AGND	Supply	Input	DAC (Analog), ADC (Analog), PLL (Analog), input stages, analog mixer (AUX and class D), and Earpiece amplifier ground
A4	DAC REF	Analog	Input/Output	Filter point for the DAC reference
A5	ADC REF	Analog	Input	Filter point for the ADC reference. Connect this pin to A_V_{DD}.
A6	SDA	Digital	Input/Output	I^2C interface data line
B1	HPL	Analog	Output	Headphone left output
B2	AUX_R/AUX+	Analog	Input	Right analog input or positive differential auxiliary input
B3	AUX_L/AUX-	Analog	Input	Left analog input or negative differential auxiliary input
B4	PORT2_SYNC	Digital	Input/Output	Audio Port 2 sync signal (can be master or slave)
B5	PORT2_SDI	Digital	Input	Audio Port 2 serial data input
B6	SCL	Digital	Input	I^2C interface clock line
C1	HP_V_{SS}	Analog	Output	Negative power supply pin for the headphone amplifier
C2	HP_V_{DD}	Supply	Input	Headphone amplifier power supply pin
C3	EP-/AUXOUT-	Analog	Output	Earpiece negative output or Auxiliary negative output
C4	PORT2_SDO / GPIO	Digital	Input / Output	Audio port 2 serial data output or General Purpose Input Output
C5	PORT2_CLK	Digital	Input/Output	Audio port 2 clock signal (can be master or slave)
C6	MCLK	Digital	Input	Input clock from 0.5MHz to 50 MHz
D1	CP-	Analog	Input/Output	Fly capacitor negative input
D2	CP+	Analog	Input/Output	Fly capacitor positive input
D3	EP+/AUXOUT+	Analog	Output	Earpiece positive output or Auxiliary positive output
D4	PORT1_SYNC	Digital	Input/Output	Audio Port 1 sync signal (can be master or slave)
D5	PORT1_SDO	Digital	Output	Audio Port 1 serial data output

Copyright © 2009–2013, Texas Instruments Incorporated

PIN DESCRIPTIONS (continued)

Pin	Pin Name	Type	Direction	Description
D6	DGND	Supply	Input	Digital ground
E1	LSGND	Supply	Input	Loudspeaker ground
E2	LS_V_{DD}	Supply	Input	Loudspeaker amplifier and analog mixer (headphone) supply input
E3	MONO-	Analog	Input	Mono differential negative input
E4	MIC-	Analog	Input	Microphone negative input
E5	PORT1_SDI	Digital	Input	Audio Port 1 serial data input
E6	D_V_{DD}	Supply	Input	DAC (Digital), ADC (Digital), PLL (Digital), digital mixer, DSP core, and I^2C register power supply input
F1	LS +	Analog	Output	Loudspeaker positive output
F2	LS -	Analog	Output	Loudspeaker negative output
F3	MONO+	Analog	Input	Mono differential positive input
F4	MIC +	Analog	Input	Microphone positive input
F5	PORT1_CLK	Digital	Input/Output	Audio Port 1 clock signal (can be master or slave)
F6	I/O_V_{DD}	Supply	Input	Digital I/O (MCLK, I^2S/PCM, I^2C) interface power supply input

PIN TYPE DEFINITIONS

Analog Input — A pin that is used by the analog and is never driven by the device. Supplies are part of this classification.

Analog Output — A pin that is driven by the device and should not be driven by external sources.

Analog Input/Output — A pin that is typically used for filtering a DC signal within the device. Passive components can be connected to these pins.

Digital Input — A pin that is used by the digital but is never driven by the device.

Digital Output — A pin that is driven by the device and should not be driven by another device to avoid contention.

Digital Input/Output — A pin that is either open drain (SDA) or a bidirectional CMOS in/out. In the latter case the direction is selected by a control register within the LM49352.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Copyright © 2009–2013, Texas Instruments Incorporated

Absolute Maximum Ratings[1][2][3]

Analog Supply Voltage (A_V_{DD} and LS_V_{DD})			6.0V
Digital Supply Voltage D_V_{DD}			2.2V
I/O Supply Voltage I/O_V_{DD}			5.5V
Headphone Supply Voltage HP_V_{DD}			3.0V
Storage Temperature			−65°C to +150°C
Power Dissipation[4]			Internally Limited
ESD Ratings	Human Body Model[5]	HPR and HPL pins	8kV
		All other pins	2.5kV
	Machine Model[6]		200V
Junction Temperature			150°C
Thermal Resistance		θ_{JA} – RLA36 (soldered down to PCB with $2in^2$ 1oz. copper plane)	60°C/W
Soldering Information		See Applications Note AN-1112 (Literature Number SNVA009).	

(1) *"Absolute Maximum Ratings"* indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the *Absolute Maximum Ratings* or other conditions beyond those indicated in the *Recommended Operating Conditions* is not implied. The *Recommended Operating Conditions* indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified.

(2) The *Electrical Characteristics* tables list ensured specifications under the listed *Recommended Operating Conditions* except as otherwise modified or specified by the *Electrical Characteristics Conditions* and/or Notes. Typical specifications are estimations only and are not ensured.

(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.

(4) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA}$ or the number given in *Absolute Maximum Ratings*, whichever is lower.

(5) Human body model, applicable std. JESD22-A114C.

(6) Machine model, applicable std. JESD22-A115-A.

Operating Ratings

Temperature Range		−40°C to +85°C
Supply Voltage	A_V_{DD}, LS_V_{DD}, and AV_{DD}_REF	2.7V to 5.5V
	D_V_{DD}	1.6V to 2.0V
	I/O_V_{DD}	1.6V to 4.5V
	HP_V_{DD}	1.7V to 2.8V

Copyright © 2009–2013, Texas Instruments Incorporated

Electrical Characteristics
A_V_{DD} = LS_V_{DD} = 3.3V; HP_V_{DD} = D_V_{DD} = I/O_V_{DD} = 1.8V(1)(2)

The following specifications apply for $R_{L(LS)}$ = 8Ω, $R_{L(HP)}$ = 32Ω, f = 1kHz, unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM49352		Units (Limit)
			Typical (3)	Limit (4)	
DC CHARACTERISTICS (Digital current combines D_V_{DD} and I/O_V_{DD}. Analog current combines A_V_{DD}, HP_V_{DD}, and LS_V_{DD})					
DI_{SD}	Digital Shutdown Current	Shutdown Mode, f_{MCLK} = 13MHz, PLL Off	2		µA
DI_{DD}	Digital Active Current (MP3 Mode)	f_{MCLK} = 11.2896MHz, f_S = 44.1kHz, Stereo DAC On, OSR_{DAC} = 64, PLL Off, HP On	1.2	1.4	mA (max)
	Digital Active Current (FM Mode)	f_{MCLK} = 13MHz Analog Audio modes	0.2	0.5	mA (max)
	Digital Active Current (FM Record Mode)	f_{MCLK} = 12.288MHz, f_S = 48kHz, Stereo ADC On, OSR_{ADC} = 128, PLL Off, Stereo Analog Inputs On	1.3	1.5	mA (max)
	Digital Active Current (CODEC Mode)	f_{MCLK} = 12.288MHz, f_S = 8kHz, Mono ADC On, Mono DAC On, OSR_{DAC} = 64 OSR_{ADC} = 128, PLL Off, MIC On	0.5	0.8	mA (max)
AI_{SD}	Analog Shutdown Current	Shutdown Mode	0.1	5	µA (max)
AI_{DD}	Analog Supply Current (MP3 Mode)	f_{MCLK} = 11.2896MHz, f_S = 44.1kHz Stereo DAC On, OSR_{DAC} = 64 PLL Off, Stereo HP On			
		From A_V_{DD}	4.3	6	mA (max)
		From HP_V_{DD}	1.5	2.7	mA (max)
	Analog Supply Current (FM Mode)	f_{MCLK} = 13MHz, PLL Off Stereo Auxiliary Inputs On, PLL Off, Stereo HP On			
		From A_V_{DD}	1.7	2.6	mA (max)
		From HP_V_{DD}	1.5	2.7	mA (max)
	Analog Supply Current (FM Record Mode)	f_{MCLK} = 12.288MHz, f_S = 48kHz, Stereo ADC On, OSR_{ADC} = 128, PLL Off, Stereo Analog Inputs On	7.2	9.3	mA (max)
	Analog Supply Current (CODEC Mode)	f_{MCLK} = 12.288MHz, f_S = 8kHz, Mono ADC On, Mono DAC On, OSR_{DAC} = 64 OSR_{ADC} = 128, PLL Off, MIC On, EP On	6.6	8.7	mA (max)
$PLLI_{DD}$	PLL Total Active Current	f_{MCLK} = 13MHz, f_{PLLOUT} = 12MHz, PLL On only			
		From A_V_{DD}	1.9	2.7	mA (max)
		From D_V_{DD}	1.4	2	mA (max)
HPI_{DD}	Headphone Quiescent Current	Stereo HP On only	1.5		mA
LSI_{DD}	Loudspeaker Quiescent Current	LS On only	2.2		mA
$MICI_{DD}$	Microphone Quiescent Current	Mono MIC	0.4		mA

(1) *"Absolute Maximum Ratings"* indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the *Absolute Maximum Ratings* or other conditions beyond those indicated in the *Recommended Operating Conditions* is not implied. The *Recommended Operating Conditions* indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified.

(2) The *Electrical Characteristics* tables list ensured specifications under the listed *Recommended Operating Conditions* except as otherwise modified or specified by the *Electrical Characteristics Conditions* and/or Notes. Typical specifications are estimations only and are not ensured.

(3) Typical values represent most likely parametric norms at T_A = +25ºC, and at the *Recommended Operation Conditions* at the time of product characterization and are not ensured.

(4) Datasheet min/max specification limits are specified by test or statistical analysis.

Copyright © 2009–2013, Texas Instruments Incorporated

Electrical Characteristics
A_V_{DD} = LS_V_{DD} = 3.3V; HP_V_{DD} = D_V_{DD} = I/O_V_{DD} = 1.8V[1][2] (continued)

The following specifications apply for $R_{L(LS)}$ = 8Ω, $R_{L(HP)}$ = 32Ω, f = 1kHz, unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM49352		Units (Limit)
			Typical (3)	Limit (4)	
$ADCI_{DD}$	ADC Total Active Current	f_S = 48kHz, Stereo			
		From A_V_{DD}	5.8		mA
		From D_V_{DD}	1.3		mA
$DACI_{DD}$	DAC Total Active Current	f_S = 48kHz, Stereo			
		From A_V_{DD}	3.1		mA
		From D_V_{DD}	1		mA
$AUXINI_{DD}$	Mono/Auxiliary Input Amplifier Quiescent Current	Mono and AUX Input Amplifiers enabled	0.6		mA
$AUXOUTI_{DD}$	Auxiliary Output Amplifier Quiescent Current	AUXOUT enabled	0.4		mA
		Earpiece Mode	1.1		mA
LOUDSPEAKER AMPLIFIER					
LS_{EFF}	Loudspeaker Efficiency	P_O = 970mW, R_L = 8Ω, LS_VDD = 4.2V	93		%
THD+N	Total Harmonic Distortion + Noise	P_O = 300mW, f = 1kHz, R_L = 8Ω, Mono Input Signal	0.03		%
P_O	Output Power	R_L = 8Ω, f = 1kHz, THD+N = 1%, Mono Input Signal			
		LS_V_{DD} = 5V	1.4		W
		LS_V_{DD} = 4.2V	970		mW
		LS_V_{DD} = 3.3V	590	510	mW (min)
		R_L = 4Ω, f = 1kHz, THD+N = 1%, Mono Input Signal			
		LS_V_{DD} = 5V	2.4		W
		LS_V_{DD} = 4.2V	1.65		W
		LS_V_{DD} = 3.3V	980		mW
PSRR	Power Supply Rejection Ratio	V_{RIPPLE} = 200mV_{P-P} f_{RIPPLE} = 217Hz Mono Input Terminated V_{REF} = 1.0µF, Input Referred LS Gain = 12dB	75	60	dB (min)
		V_{RIPPLE} = 200mV_{P-P} f_{RIPPLE} = 217Hz From DAC, DAC gain = 0dB	74		dB
SNR	Signal-to-Noise Ratio	Reference = V_{OUT} (1% THD+N) Mono gain = 0dB, A-weighted Mono Input Terminated, LS Gain = 8dB			
		LS_V_{DD} = 4.2V	95		dB
		LS_V_{DD} = 3.3V	93	88	dB (min)
		Reference = V_{OUT} (1% THD+N) DAC Gain = 0dB, A-weighted f_S = 48kHz, OSR = 128 LS Gain = 8dB			
		LS_V_{DD} = 4.2V	91		dB
		LS_V_{DD} = 3.3V	89		dB
e_{OS}	Output Noise	Mono gain = 0dB, A-weighted, Mono Input Terminated, Input Referred	43		µV
V_{OS}	Offset Voltage	Mono gain = 0dB, from Mono Input	10	50	mV (max)

Copyright © 2009–2013, Texas Instruments Incorporated

Electrical Characteristics
A_V_{DD} = LS_V_{DD} = 3.3V; HP_V_{DD} = D_V_{DD} = I/O_V_{DD} = 1.8V[1][2] (continued)

The following specifications apply for $R_{L(LS)}$ = 8Ω, $R_{L(HP)}$ = 32Ω, f = 1kHz, unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM49352		Units (Limit)
			Typical (3)	Limit (4)	
HEADPHONE AMPLIFIERS					
THD+N	Total Harmonic Distortion + Noise	P_O = 15mW, f = 1kHz, R_L = 32Ω Stereo Analog Input Signal	0.025	0.1	% (max)
P_O	Headphone Output Power	R_L = 32Ω, f = 1kHz, THD+N = 1%, Stereo Analog Input Signal, In phase			
		HP_V_{DD} = 2.8V	65		mW
		HP_V_{DD} = 1.8V	24	20	mW (min)
		R_L = 16Ω, f = 1kHz, THD+N = 1%, Stereo Analog Input Signal, In phase			
		HP_V_{DD} = 2.8V	73		mW
		HP_V_{DD} = 1.8V	24		mW
PSRR	Power Supply Rejection Ratio	V_{RIPPLE} = 200mV_{P-P}, f_{RIPPLE} = 217Hz Mono Input Terminated, Mono gain = 0dB V_{REF} = 1.0µF, Mono Differential Input Mode,			
		Ripple applied to AV_{DD} only	100	85	dB (min)
		Ripple applied to AV_{DD} and HPV_{DD}	88		dB
		V_{RIPPLE} = 200mV_{P-P}, f_{RIPPLE} = 217Hz From DAC, DAC gain = 0dB			
		Ripple applied to AV_{DD} HPV_{DD}, and DV_{DD}	81		dB
SNR	Signal to Noise Ratio	Reference = V_{OUT} (1% THD+N) Gain = 0dB, A-weighted Stereo Inputs Terminated	98	93	dB (min)
		Reference = V_{OUT} (1% THD+N) Gain = 0dB, A-weighted, I^2S Input = Digital Zero	97	93	dB (min)
e_{OS}	Output Noise	Gain = 0dB, A-weighted, Stereo Inputs Terminated	11		µV
		Gain = 0dB, A-weighted, I^2S Input = Digital Zero	12		µV
X_{TALK}	Crosstalk	P_O = 7.5mW, f = 1kHz, R_L = 32Ω Stereo Analog Input Signal	85		dB
ΔA_{CH-CH}	Channel-to-Channel Gain Matching		0.03		dB
V_{OS}	Output Offset Voltage	AUX Gain = 0dB From mono Input	1.4	6	mV (max)
		DAC Gain = 0dB From DAC Input, f_{MCLK} = 12.288MHz	1.6	6	mV (max)

Copyright © 2009–2013, Texas Instruments Incorporated

Electrical Characteristics
A_V_{DD} = LS_V_{DD} = 3.3V; HP_V_{DD} = D_V_{DD} = I/O_V_{DD} = 1.8V[1][2] (continued)

The following specifications apply for $R_{L(LS)}$ = 8Ω, $R_{L(HP)}$ = 32Ω, f = 1kHz, unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM49352		Units (Limit)
			Typical (3)	Limit (4)	
AUXILIARY OUTPUT/EARPIECE AMPLIFIER					
THD+N	Total Harmonic Distortion	AUX_LINE_OUT, f = 1kHz From Mono In R_L = 5kΩ, V_{OUT} = 1V_{RMS}	0.002		%
		Earpiece mode, f = 1kHz From Mono In R_L = 32Ω BTL, P_{OUT} = 20mW	0.02		%
P_{OUT}	Output Power	Earpiece mode, f = 1kHz R_L = 32Ω BTL, THD+N = 1%	58	50	mW (min)
PSRR	Power Supply Rejection Ratio	V_{RIPPLE} = 200mV_{P-P}, f_{RIPPLE} = 217Hz Mono Input terminated, C_{REF} = 1.0µF AUX_LINE_OUT	100		dB
		V_{RIPPLE} = 200mV_{P-P}, f_{RIPPLE} = 217Hz Mono Input terminated, C_{REF} = 1.0µF Earpiece mode, –6dB cut enabled	100	90	dB
SNR	Signal to Noise Ratio	Gain = 0dB, V_{REF} = V_{OUT} (1% THD+N) A-weighted, Mono Input Terminated	105		dB
$\in_{OUT}$	Output Noise	Gain = 0dB, V_{REF} = V_{OUT} (1% THD+N) A-weighted, Mono Input Terminated	7		µV
V_{OS}	Output Offset Voltage	MONO gain = 0dB, From Mono Input AUX_LINE_OUT	4		mV
		Gain = 0dB, From Mono Input Earpiece mode	4	12	mV (max)
T_{WU}	Turn-On time	PMC Clock = 300kHz	28		ms
STEREO ADC					
$THD+N_{ADC}$	ADC Total Harmonic Distortion + Noise	Mono Differential Input V_{IN} = 1V_{RMS}, f = 1kHz Gain = 0dB, f_S = 48kHz	0.007		%
PB_{ADC}	ADC Passband	HPF On, f_S = 48kHz Lower -3dB Point	220		Hz
		HPF On, Upper -3dB Point	0.41*f_S		kHz
R_{ADC}	ADC Ripple	OSR_{DAC} = 128	0.1		dB
SNR_{ADC}	ADC Signal to Noise Ratio	Reference = V_{OUT} (0dBFS) Gain = 6dB, A-weighted From MIC, f_S = 8kHz	98		dB
		Reference = V_{OUT} (0dBFS) Gain = 0dB, A-weighted From Stereo Input, f_S = 48kHz	97		dB
ADC_{LEVEL}	ADC Full Scale Input Level		1.6		V_{RMS}
STEREO DAC					
$THD+N_{DAC}$	DAC Total Harmonic Distortion + Noise	I^2S Input, AUXOUT, OSR_{DAC} = 64 V_{IN} = 500mFFS_{RMS}, f = 1kHz Gain = 0dB	0.01		%
DAC_{LEVEL}	DAC Full Scale Output Level		1.08		V_{RMS}
R_{DAC}	DAC Ripple		0.1		dB
PB_{DAC}	DAC Passband	Upper –3dB Point	0.45*f_S		kHz
SNR_{DAC}	DAC Signal to Noise Ratio	f_S = 48kHz, A-weighted, AUXOUT	103		dB

Copyright © 2009–2013, Texas Instruments Incorporated

Electrical Characteristics
A_V_{DD} = LS_V_{DD} = 3.3V; HP_V_{DD} = D_V_{DD} = I/O_V_{DD} = 1.8V[1][2] (continued)

The following specifications apply for $R_{L(LS)}$ = 8Ω, $R_{L(HP)}$ = 32Ω, f = 1kHz, unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM49352		Units (Limit)
			Typical (3)	Limit (4)	
VOLUME CONTROL					
VCR_{AUX}	Stereo Input Volume Control Range	Minimum Gain	–46.5		dB
		Maximum Gain	18		dB
VCR_{MONO}	MONO Input Volume Control Range	Minimum Gain	–46.5		dB
		Maximum Gain	18		dB
VCR_{DAC}	DAC Volume Control Range	Minimum Gain	–76.5		dB
		Maximum Gain	18		dB
VCR_{ADC}	ADC Volume Control Range	Minimum Gain	–76.5		dB
		Maximum Gain	18		dB
VCR_{MIC}	MIC Volume Control Range	Minimum Gain	6		dB
		Maximum Gain	36		dB
VCR_{LS}	Loudspeaker Amplifier Volume Control Range	Minimum Gain	0		dB
		Maximum Gain	12		dB
VCR_{HP}	Headphone Amplifier Volume Control Range	Minimum Gain	–18		dB
		Maximum Gain	0		dB
SS_{LS}	Loudspeaker Amplifier Volume Control Stepsize		4		dB
SS_{HP}	Headphone Amplifier Volume Control Stepsize		Refer to Table 19		dB
SS_{AUX}	AUX Input Volume Control Stepsize		1.5		dB
SS_{MONO}	MONO Input Volume Control Stepsize		1.5		dB
SS_{DAC}	DAC Volume Control Stepsize		1.5		dB
SS_{ADC}	ADC Volume Control Stepsize		1.5		dB
SS_{MIC}	MIC Volume Control Stepsize		2		dB
SV_{AUX}	AUX Volume Setting Variation			±1	dB (max)
SV_{MONO}	MONO Volume Setting Variation			±1	dB (min)
SV_{MIC}	MIC Volume Setting Variation			±1	dB (max)
ANALOG INPUTS					
AUX_R_{IN}	Auxiliary Input Impedance	AUX Gain = 18dB	10		kΩ
		AUX Gain = 0dB	38		kΩ
		AUX Gain = –46.5dB	64		kΩ
$MONO_R_{IN}$	Mono Input Impedance	MONO Gain = 18dB	10		kΩ
		MONO Gain = 0dB	38		kΩ
		MONO Gain = –46.5dB	64		kΩ
MIC_R_{IN}	Microphone Input Impedance	All MIC gain settings	50		kΩ

Copyright © 2009–2013, Texas Instruments Incorporated

Typical Performance Characteristics

Class D Loudspeaker Amplifier Efficiency vs Output Power
THD+N < 10%, R_L = 8Ω
Green >> LSVDD = 3.3V
Gray >> LSVDD = 4.2V
Blue >> LSVDD = 5V

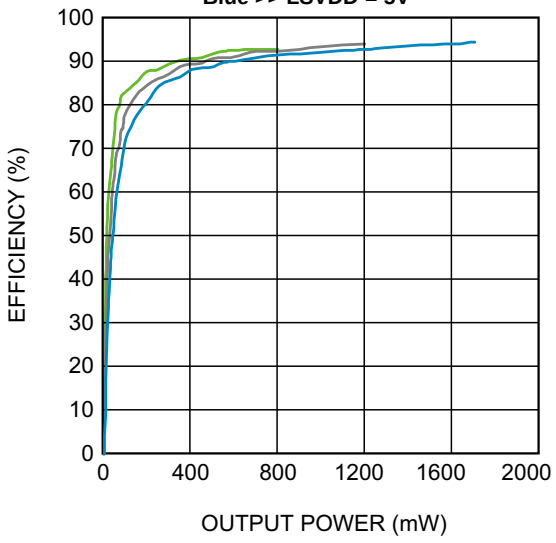


Figure 8.

DAC Frequency Response
f_S = 48kHz
Blue >> OSR = 64
Light Blue >> OSR = 128

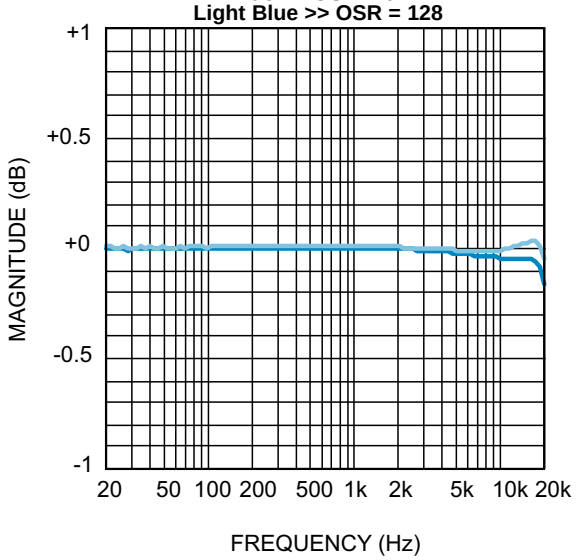


Figure 9.

DAC Frequency Response
f_S = 8kHz
Blue >> OSR = 64
Light Blue >> OSR = 128

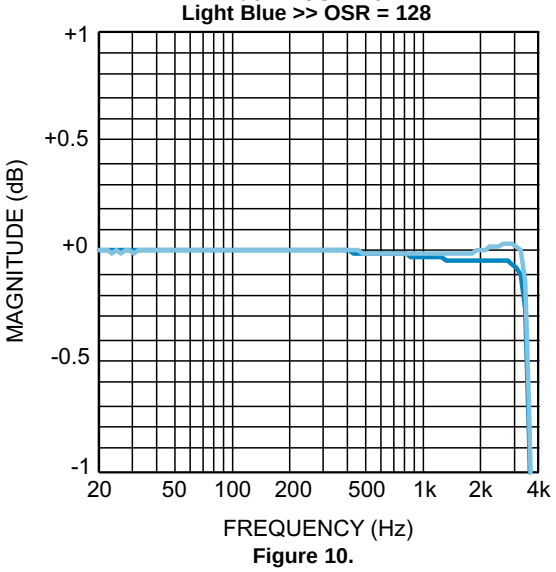


Figure 10.

DAC THD+N vs Frequency
f_S = 8kHz, OSR = 128
I^2S Input = 500mFFS

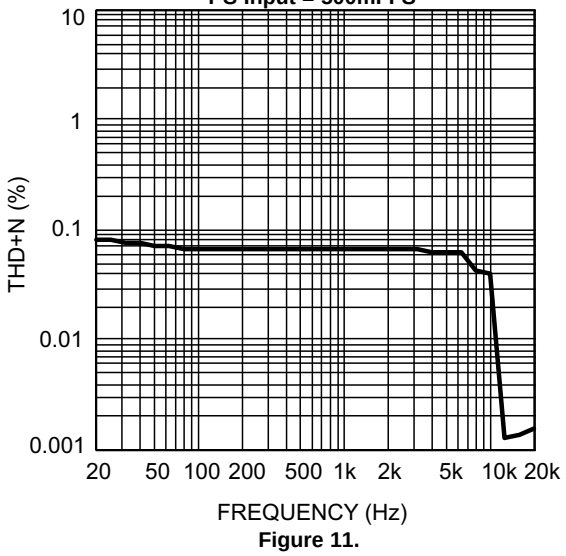


Figure 11.

Copyright © 2009–2013, Texas Instruments Incorporated

Typical Performance Characteristics (continued)

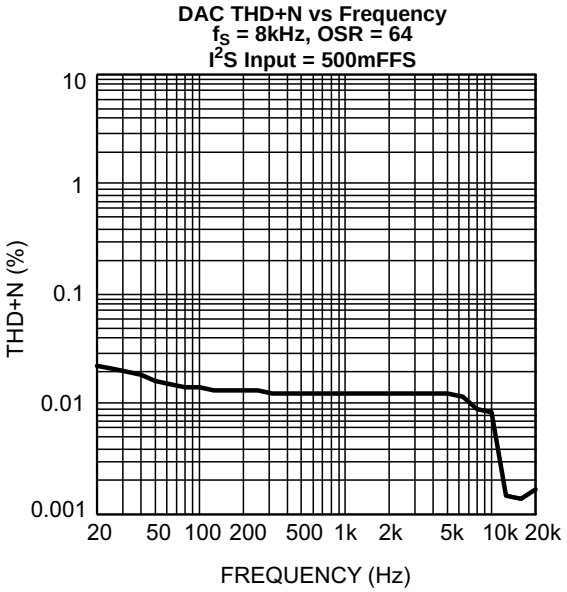


Figure 12.

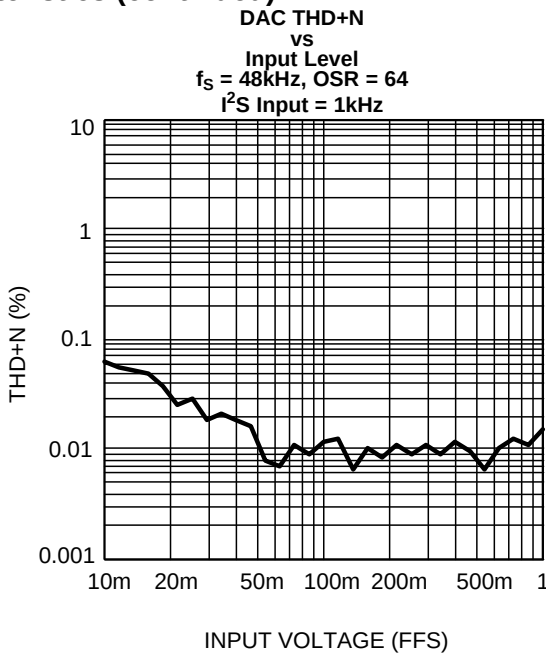


Figure 13.

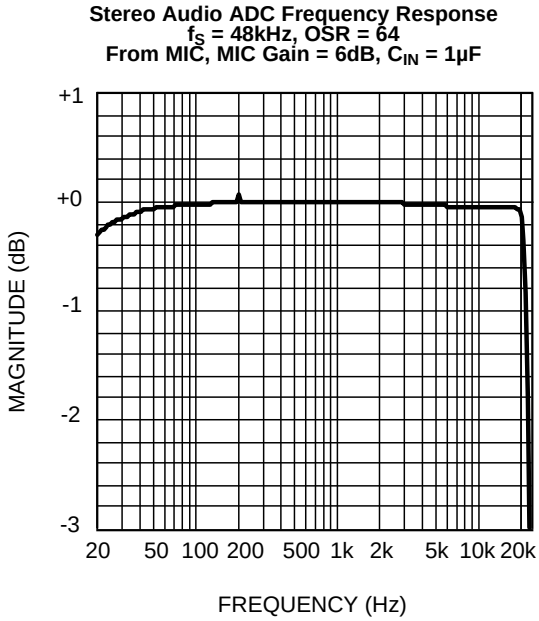


Figure 14.

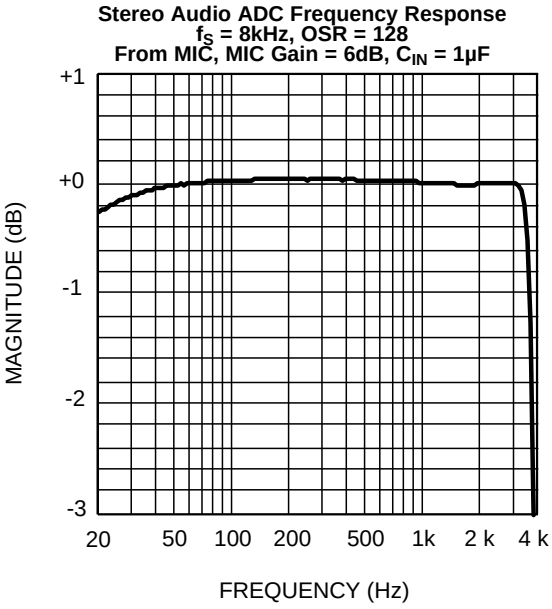


Figure 15.

Copyright © 2009–2013, Texas Instruments Incorporated

Typical Performance Characteristics (continued)

Mono Voice ADC Frequency Response
f_S = 48kHz, OSR = 128
From MIC, MIC Gain = 6dB, C_{IN} = 1µF

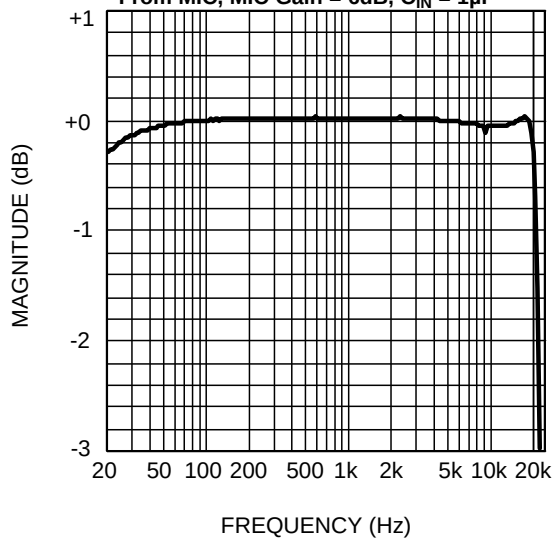


Figure 16.

Mono Voice ADC Frequency Response
f_S = 8kHz, OSR = 128
From MIC, MIC Gain = 6dB, C_{IN} = 1µF

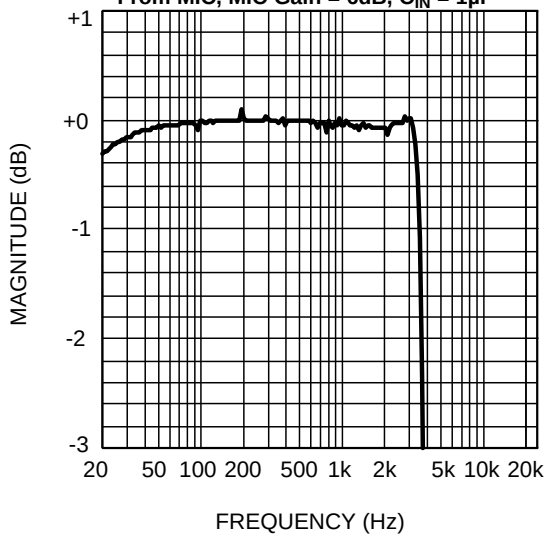


Figure 17.

Stereo Audio HPF ADC Frequency Response
f_S = 48kHz, OSR = 128
From MONO/AUX, MONO>AUX Gain = 0dB, C_{IN} = 1µF
Blue >> No HPF
Light Blue >> HPF Mode = '101'
Green >> HPF Mode = '110'
Light Green >> HPF Mode = '111'

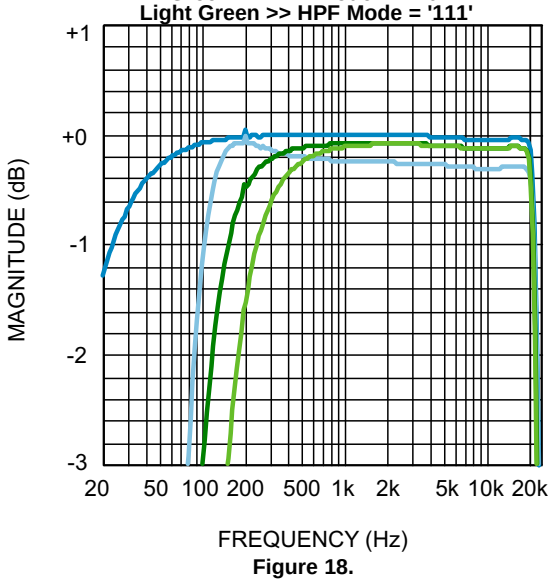


Figure 18.

Mono Voice HPF ADC Frequency Response
f_S = 48kHz, OSR = 128
From MIC, MIC Gain = 6dB, C_{IN} = 1µF
Gray >> No HPF
Blue >> HPF Mode = '000'
Light Blue >> HPF Mode = '001'
Green >> HPF Mode = '010'
Light Green >> HPF Mode = '011'
Yellow >> HPF Mode = '100'

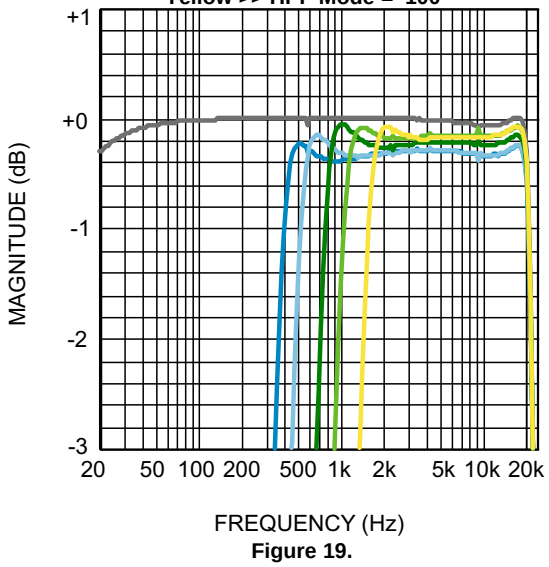


Figure 19.

Copyright © 2009–2013, Texas Instruments Incorporated

Typical Performance Characteristics (continued)

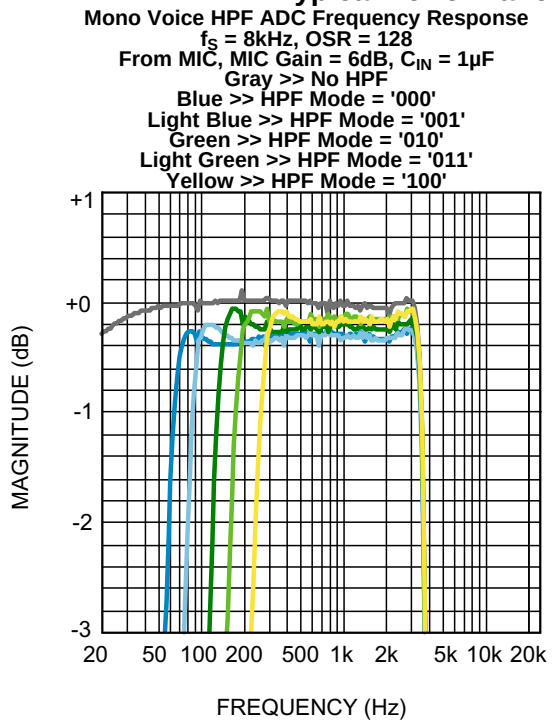


Figure 20.

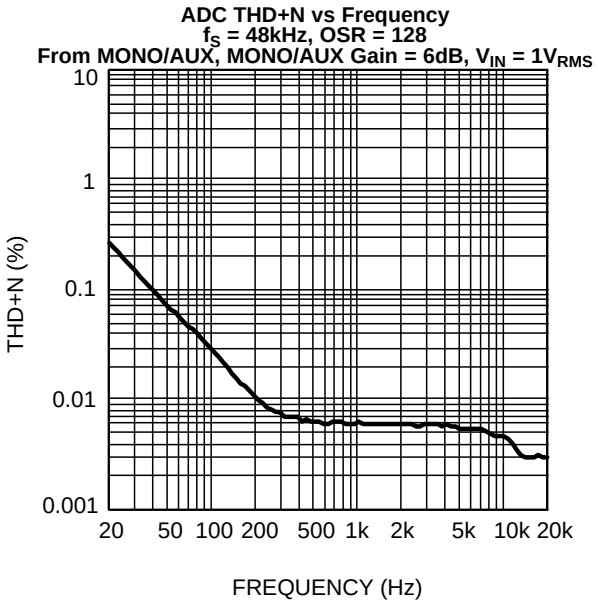


Figure 21.

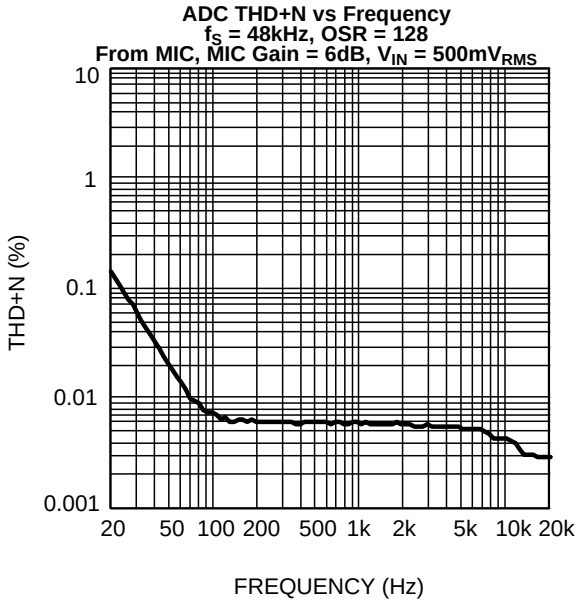


Figure 22.

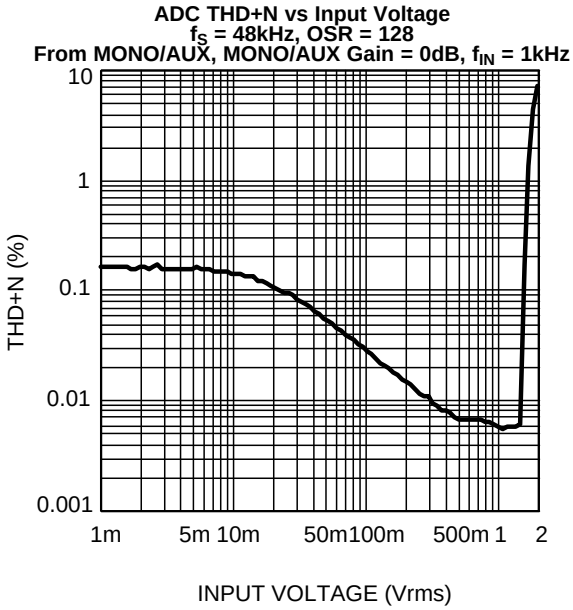


Figure 23.

Copyright © 2009–2013, Texas Instruments Incorporated

Typical Performance Characteristics (continued)

ADC THD+N vs Input Voltage
f_S = 48kHz, OSR = 128
From MIC, MIC Gain = 6dB, V_{IN} = 1kHz

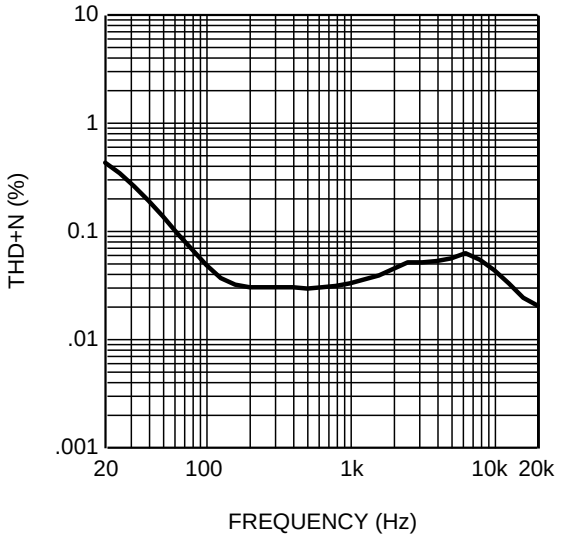


Figure 24.

Loudspeaker THD+N vs Input Voltage
From MONO/AUX Input, MONO/AUX Gain = 0dB
LS Gain = 8dB, LSVDD = 3.3V, P_{OUT} = 300V_{RMS}, R_L = 8Ω

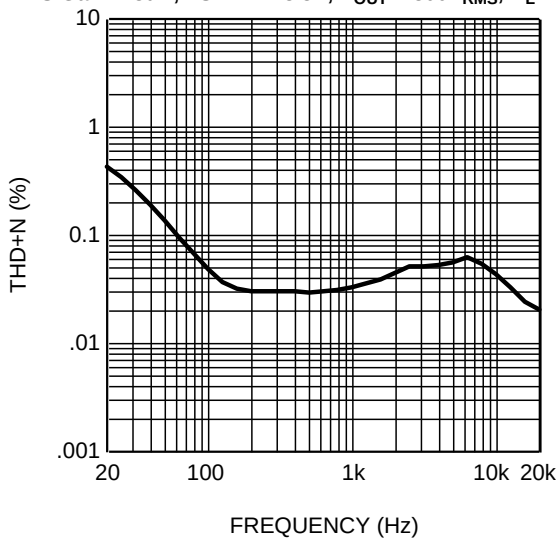


Figure 25.

Loudspeaker THD+N vs Input Voltage
From MONO/AUX Input, MONO/AUX Gain = 0dB
LS Gain = 8dB, LSVDD = 4.2V, P_{OUT} = 300V_{RMS}, R_L = 8Ω

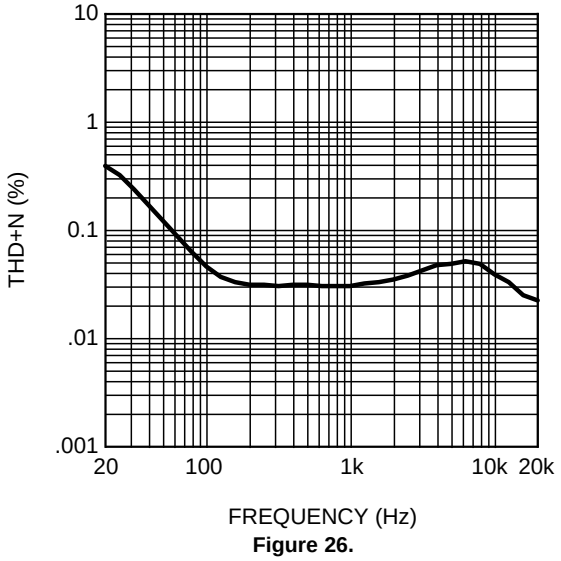


Figure 26.

Loudspeaker THD+N vs Input Voltage
From MONO/AUX Input, MONO/AUX Gain = 0dB
LS Gain = 8dB, LSVDD = 5V, P_{OUT} = 300V_{RMS}, R_L = 8Ω

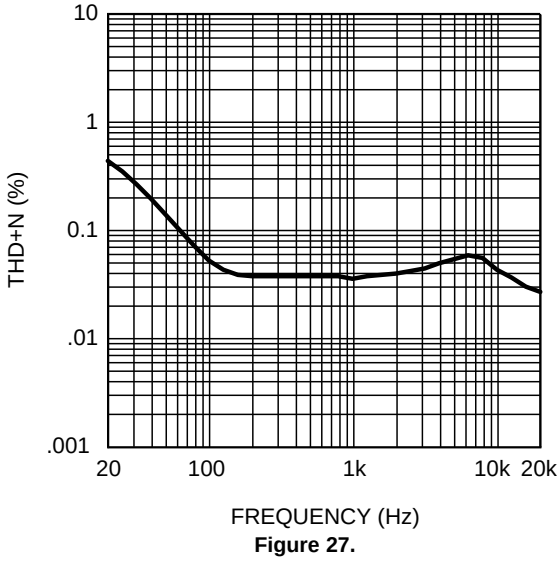


Figure 27.

Copyright © 2009–2013, Texas Instruments Incorporated

Typical Performance Characteristics (continued)

Loudspeaker THD+N vs Input Voltage
From MONO/AUX Input, MONO/AUX Gain = 0dB
LS Gain = 8dB, LSVDD = 3.3V, P_{OUT} = 300V_{RMS}, R_L = 4Ω

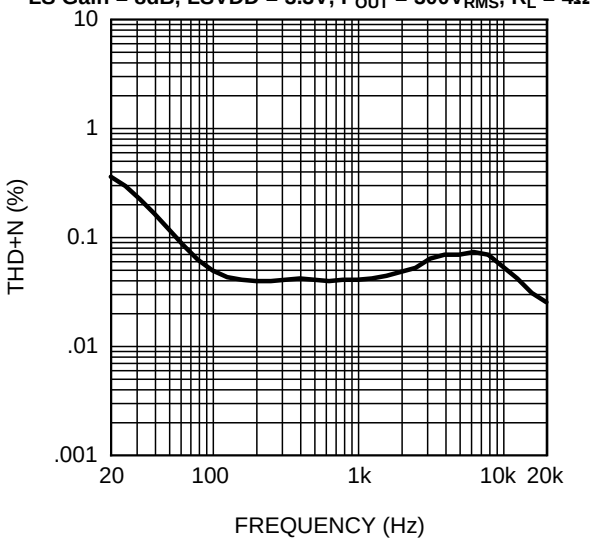


Figure 28.

Loudspeaker THD+N vs Output Power
From MONO/AUX Input, MONO/AUX Gain = 0dB
LS Gain = 8dB, f_{IN} = 1kHz, R_L = 8Ω
Blue >> LSVDD = 3.3V
Light Blue >> LSVDD = 4.2V
Green >> LSVDD = 5V

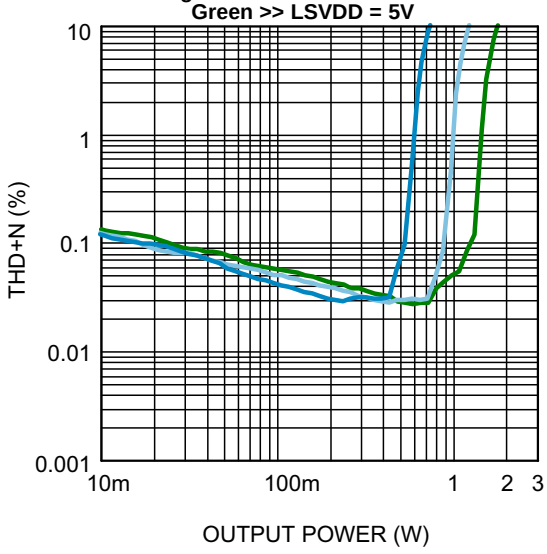


Figure 29.

Loudspeaker THD+N vs Output Power
f_S = 48kHz, OSR = 128
From MONO/AUX Input, MONO/AUX Gain = 0dB
LS Gain = 8dB, f_{IN} = 1kHz, R_L = 4Ω
Blue >> LSVDD = 3.3V
Light Blue >> LSVDD = 4.2V
Green >> LSVDD = 5V

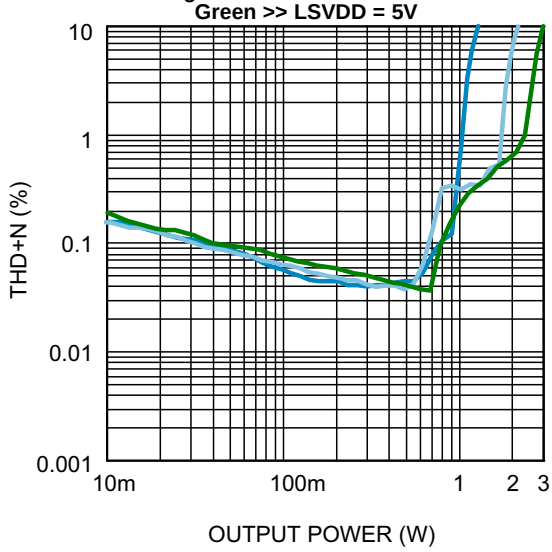


Figure 30.

Loudspeaker PSRR vs Frequency
MONO/AUX Input, MONO/AUX Gain = 0dB, LS Gain = 12dB
LSVDD = 3.3V, V_{RIPPLE} = 200mV_{PP}, Input Referred

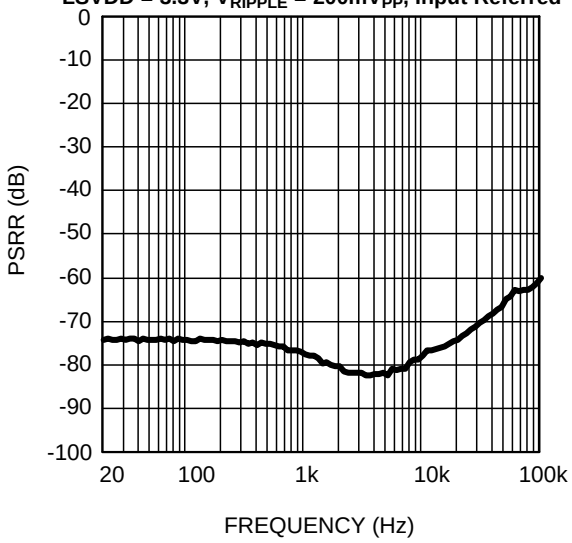


Figure 31.

Copyright © 2009–2013, Texas Instruments Incorporated

Typical Performance Characteristics (continued)

Loudspeaker PSRR vs Frequency
f_S = 48kHz, OSR = 128
MONO/AUX Input, MONO/AUX Gain = 0dB, LS Gain = 12dB
LSVDD = 4.2V, V_{RIPPLE} = 200mV_{PP}, Input Referred

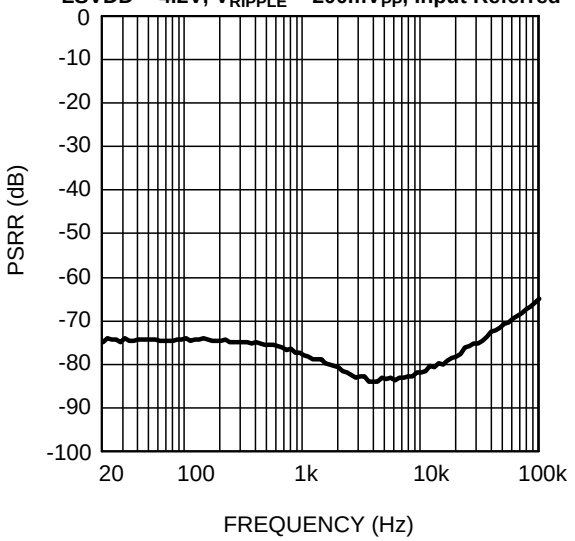


Figure 32.

Loudspeaker PSRR vs Frequency
MONO/AUX Input, MONO/AUX Gain = 0dB, LS Gain = 12dB
LSVDD = 5V, V_{RIPPLE} = 200mV_{PP}, Input Referred

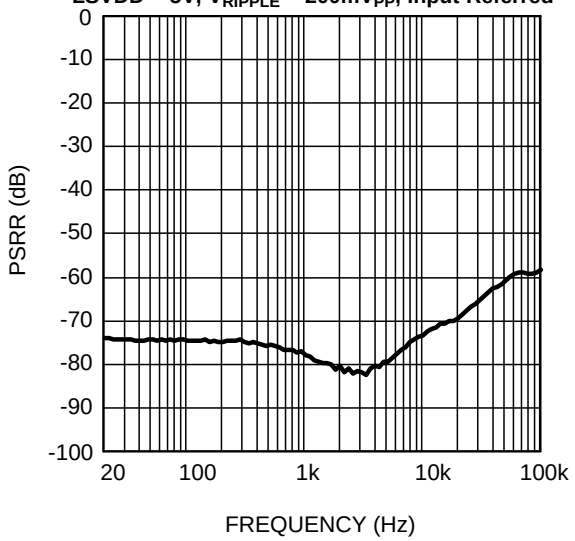


Figure 33.

Headphone PSRR vs Frequency
DAC Input, DAC Gain = 0dB, LS Gain = 12dB
LSVDD = 3,3V, AVDD = 3.3V, DVDD = 1.8V, V_{RIPPLE} = 200mV_{PP}
Ripple on LSVDD, AVDD, DVDD, Input Referred

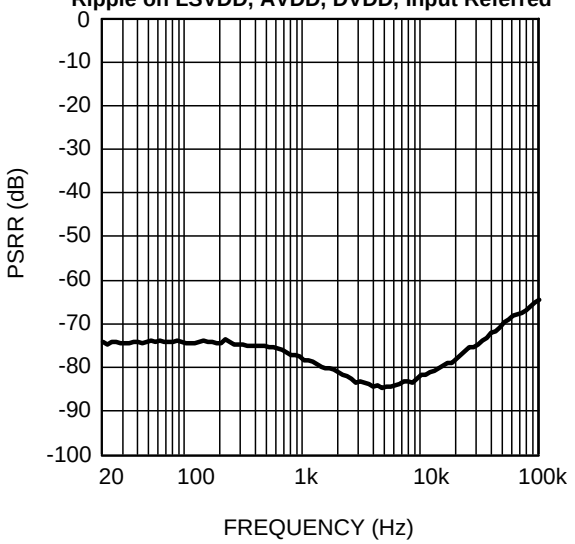


Figure 34.

HeadphoneTHD+N vs Frequency
MONO/AUX, MONO/AUX Gain = 0dB, HP Gain = 0dB
HPVDD = 3.3V, P_{OUT} = 15mW, R_L = 32Ω
Stereo In Phase

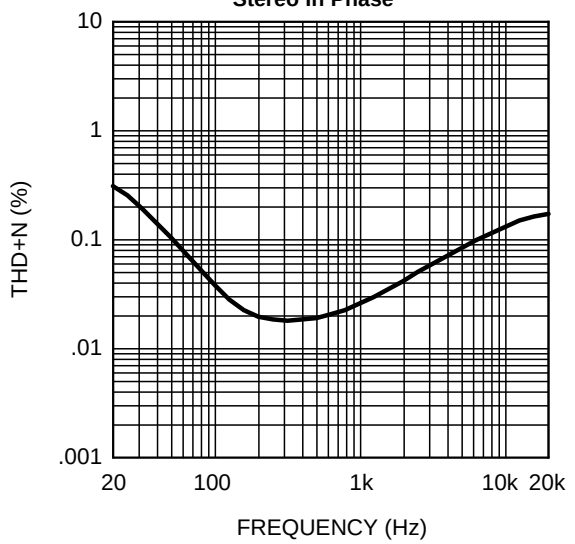


Figure 35.

Typical Performance Characteristics (continued)

Headphone THD+N vs Frequency
MONO/AUX, MONO/AUX Gain = 0dB, HP Gain = 0dB
HPVDD = 2.8V, P_{OUT} = 15mW, R_L = 32Ω
Stereo In Phase

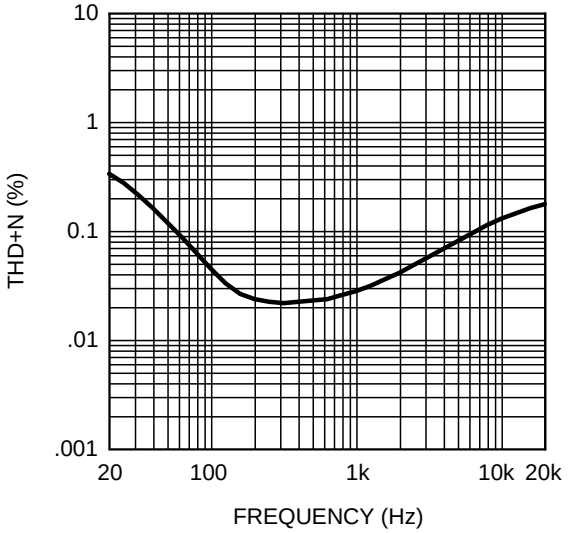


Figure 36.

Headphone THD+N vs Frequency
MONO/AUX, MONO/AUX Gain = 0dB, HP Gain = 0dB
HPVDD = 1.8V, P_{OUT} = 15mW, R_L = 16Ω
Stereo In Phase

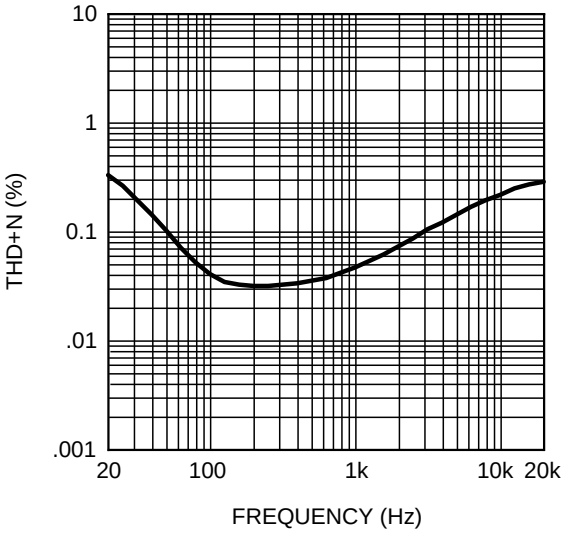


Figure 37.

Headphone THD+N vs Frequency
MONO/AUX, MONO/AUX Gain = 0dB, HP Gain = 0dB
HPVDD = 2.8V, P_{OUT} = 15mW, R_L = 16Ω
Stereo In Phase

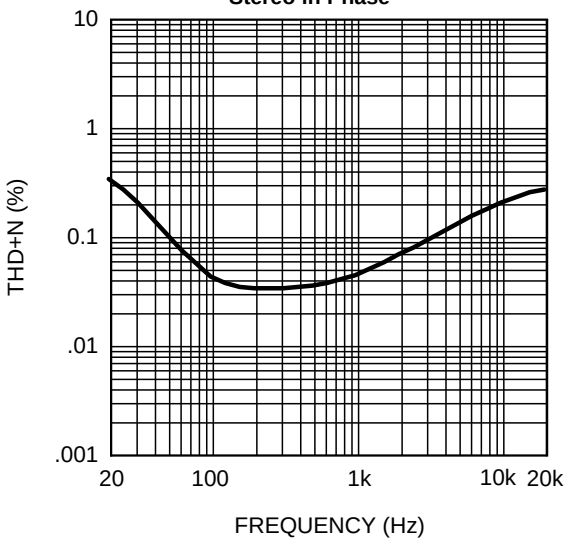


Figure 38.

Headphone THD+N vs Output Power
MONO/AUX Input, MONO/AUX Gain = 0dB, HP Gain = 0dB
Stereo In Phase, f_{IN} = 1kHz, R_L = 32Ω
Blue >> HPVDD = 1.8V
Light Blue >> HPVDD = 2.8V

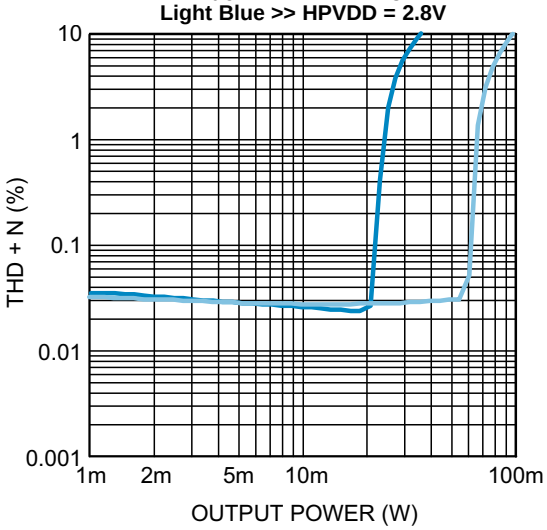


Figure 39.

Copyright © 2009–2013, Texas Instruments Incorporated

Typical Performance Characteristics (continued)

Headphone THD+N vs Output Power
MONO/AUX Input, MONO/AUX Gain = 0dB, HP Gain = 0dB
Stereo In Phase, f_{IN} = 1kHz, R_L = 16Ω
Blue >> HPVDD = 1.8V
Light Blue >> HPVDD = 2.8V

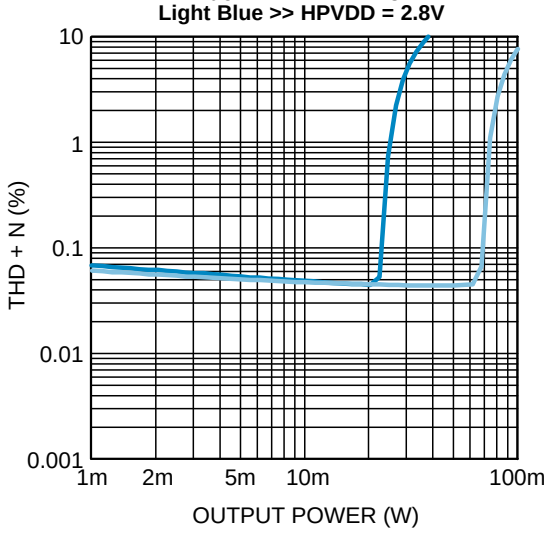


Figure 40.

Headphone PSRR vs Frequency
MONO/AUX Input, MONO/AUX Gain = 0dB, HP Gain = 0dB
HPVDD = 1.8V, AVDD = 3.3V, V_{RIPPLE} = 200mV_{PP}
Ripple on HPVDD, AVDD

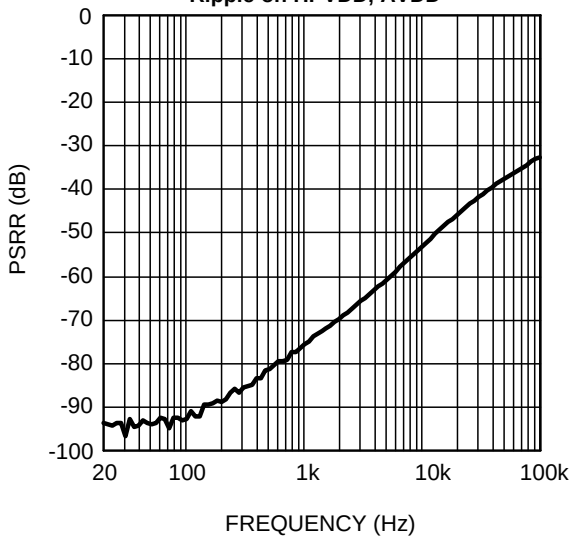


Figure 41.

Headphone PSRR vs Frequency
MONO/AUX Input, MONO/AUX Gain = 0dB, HP Gain = 0dB
HPVDD = 1.8V, AVDD = 3.3V, V_{RIPPLE} = 200mV_{PP}
Ripple on AVDD only

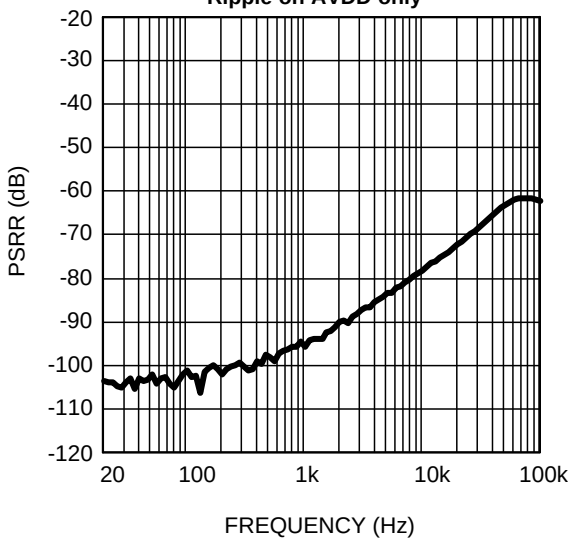


Figure 42.

Headphone PSRR vs Frequency
DAC Input, DAC Gain = 0dB, HP Gain = 0dB
HPVDD = 1.8V, AVDD = 3.3V, DVDD = 1.8V, V_{RIPPLE} = 200mV_{PP}
Ripple on HPVDD, AVDD, DVDD

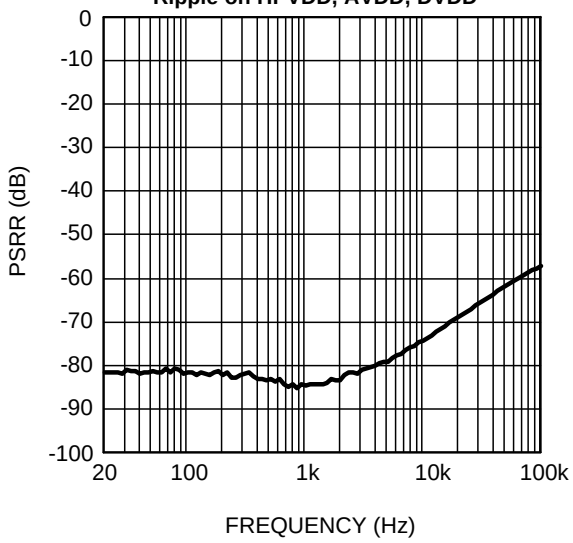


Figure 43.

Typical Performance Characteristics (continued)

Headphone Crosstalk vs Frequency
MONO/AUX Input, MONO/AUX Gain = 0dB, HP Gain = 0dB
HPVDD = 1.8V, AVDD = 3.3V, P_{OUT} = 15mW, R_L = 32Ω

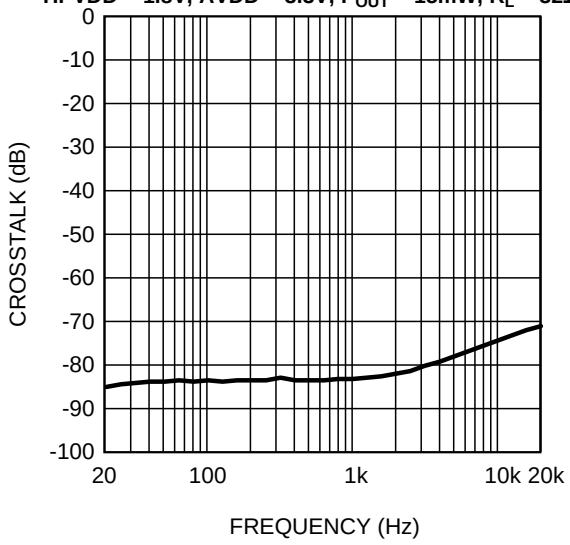


Figure 44.

Earpiece THD+N vs Frequency
MONO/AUX Input, MONO/AUX Gain = 0dB, EP Gain = 0dB
AVDD = 3.3V, P_{OUT} = 20mW, R_L = 32Ω
Earpiece Mode

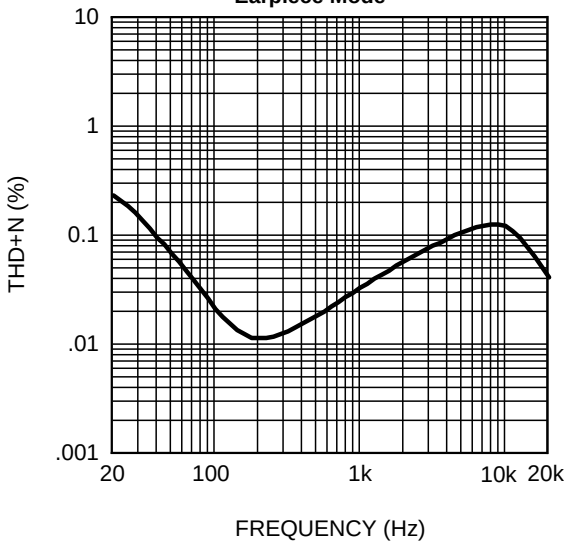


Figure 45.

Earpiece THD+N vs Output Power
MONO/AUX Input, MONO/AUX Gain = 0dB, EP Gain = 0dB
AVDD = 3.3V, f_{IN} = 1kHz, R_L = 32Ω
Earpiece Mode

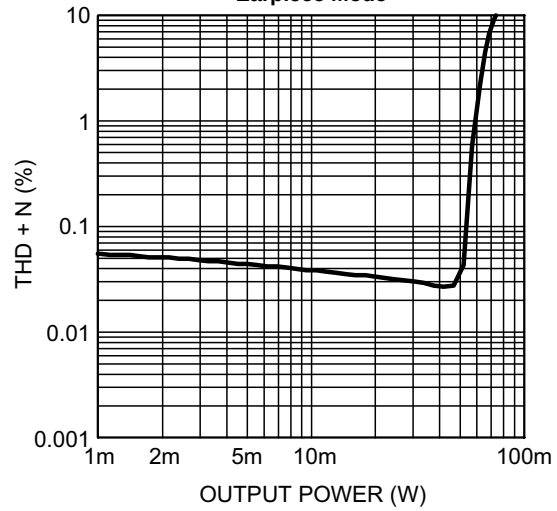


Figure 46.

Earpiece PSRR vs Frequency
MONO/AUX Input, MONO/AUX Gain = 0dB, EP Gain = –6dB
AVDD = 3.3V, V_{RIPPLE} = 200mV_{PP}, Earpiece Mode

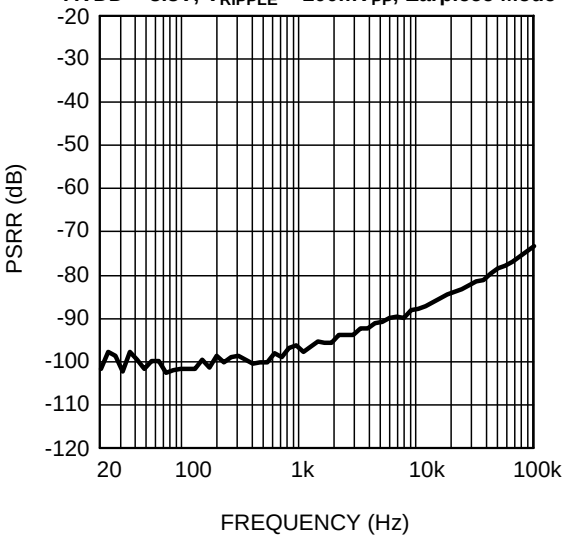


Figure 47.

Copyright © 2009–2013, Texas Instruments Incorporated

Typical Performance Characteristics (continued)

Auxiliary Output THD+N vs Frequency
MONO/AUX Input, MONO/AUX Gain = 0dB, EP Gain = 0dB
AVDD = 3.3V, V_{OUT} = 1V_{RMS}, R_L = 5kΩ
AUXOUT Mode

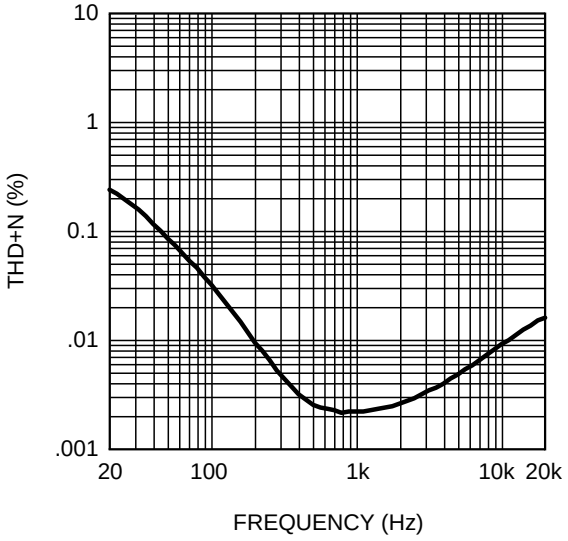


Figure 48.

Auxiliary Output THD+N vs Output Voltage
MONO/AUX Input, MONO/AUX Gain = 0dB, EP Gain = 0dB
AVDD = 3.3V, f_{IN} = 1kHz, R_L = 5kΩ
AUXOUT Mode

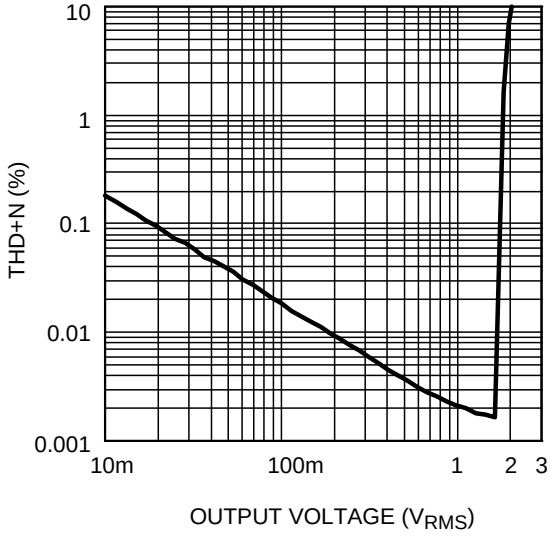


Figure 49.

Auxiliary Output PSRR vs FRequency
MONO/AUX Input, MONO/AUX Gain = 0dB, EP Gain = 0dB
AVDD = 3.3V, V_{RIPPLE} = 200mV_{PP}, AUXOUT Mode

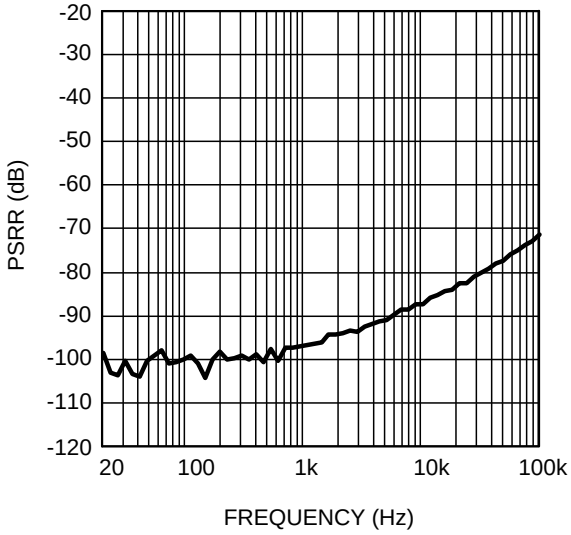


Figure 50.

Copyright © 2009–2013, Texas Instruments Incorporated

SYSTEM CONTROL

Method 1. I²C Compatible Interface

I²C SIGNALS

In I²C mode the LM49352 pin SCL is used for the I²C clock SCL and the pin SDA is used for the I²C data signal SDA. Both these signals need a pull-up resistor according to I²C specification. The I²C slave address for LM49352 is **0011010_2**.

I²C DATA VALIDITY

The data on SDA line must be stable during the HIGH period of the clock signal (SCL). In other words, state of the data line can only be changed when SCL is LOW.

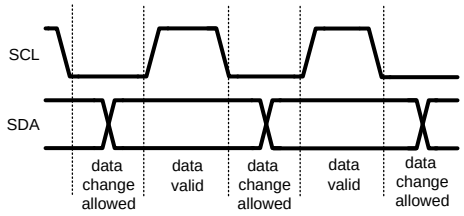


Figure 51. I²C Signals: Data Validity

I²C START AND STOP CONDITIONS

START and STOP bits classify the beginning and the end of the I²C session. START condition is defined as SDA signal transitioning from HIGH to LOW while SCL line is HIGH. STOP condition is defined as the SDA transitioning from LOW to HIGH while SCL is HIGH. The I²C master always generates START and STOP bits. The I²C bus is considered to be busy after START condition and free after STOP condition. During data transmission, I²C master can generate repeated START conditions. First START and repeated START conditions are equivalent, function-wise.

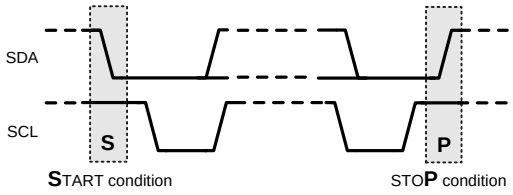


Figure 52. I²C Start and Stop Conditions

TRANSFERRING DATA

Every byte put on the SDA line must be eight bits long, with the most significant bit (MSB) being transferred first. Each byte of data has to be followed by an acknowledge bit. The acknowledge related clock pulse is generated by the master. The transmitter releases the SDA line (HIGH) during the acknowledge clock pulse. The receiver must pull down the SDA line during the 9th clock pulse, signifying an acknowledge. A receiver which has been addressed must generate an acknowledge after each byte has been received.

After the START condition, the I²C master sends a chip address. This address is seven bits long followed by an eight bit which is a data direction bit (R/W). The LM49352 address is **0011010_2**. For the eighth bit, a “0” indicates a WRITE and a “1” indicates a READ. The second byte selects the register to which the data will be written. The third byte contains data to write to the selected register.

Copyright © 2009–2013, Texas Instruments Incorporated

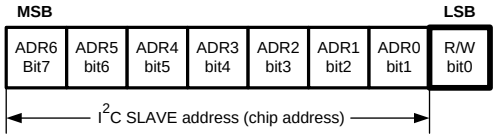
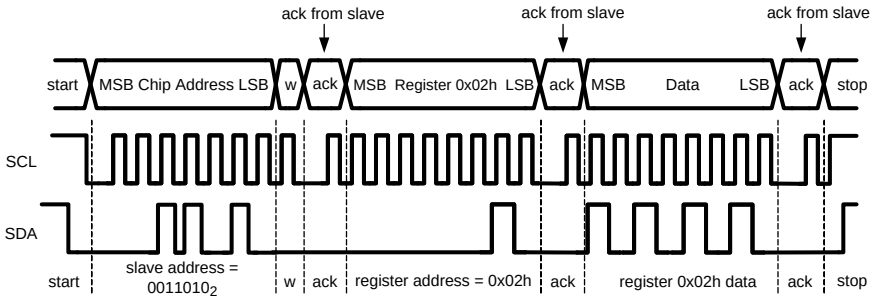


Figure 53. I²C Chip Address

Register changes take effect at the SCL rising edge during the last ACK from slave.



w = write (SDA = “0”)
r = read (SDA = “1”)
ack = acknowledge (SDA pulled down by slave)
rs = repeated start

Figure 54. Example I²C Write Cycle

When a READ function is to be accomplished, a WRITE function must precede the READ function, as shown in the Read Cycle waveform.

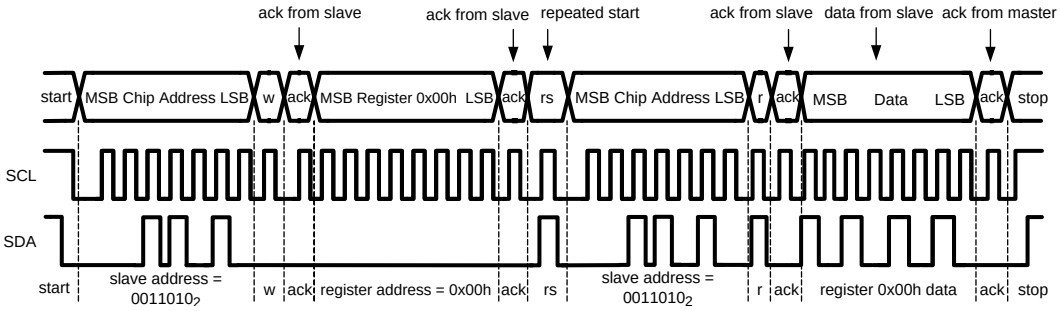


Figure 55. Example I²C Read Cycle

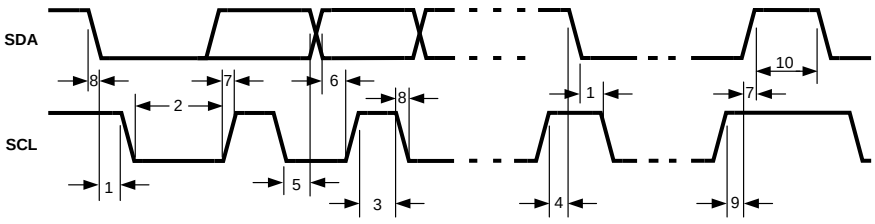


Figure 56. I²C Timing Diagram

I²C TIMING PARAMETERS

Symbol	Parameter	Limit			Units
		Min	Typ	Max	

1	Hold Time (repeated) START Condition	0.6			µs
2	Clock Low Time	1.3			µs
3	Clock High Time	600			ns
4	Setup Time for a Repeated START Condition	600			ns
5	Data Hold Time (Output direction, delay generated by LM49352)		50	See (1)	ns
	Data Hold Time (Input direction, delay generated by the Master)	50			ns
6	Data Setup Time	100			ns
7	Rise Time of SDA			300	ns
8	Fall Time of SDA			300	ns
9	Set-up Time for STOP condition	600			ns
10	Bus Free Time between a STOP and a START Condition	1.3			µs

(1) Data ensured by fall time.

Device Register Map

Table 1. Device Register Map

Address	Register	7	6	5	4	3	2	1	0
BASIC SETUP									
0x00h	PMC	CHIP	PORT2	PORT1	MCLK	OSC	PLL_P2 ENB	PLL	CHIP
	SETUP	ACTIVE	CLK OVR	CLK OVR	OVR	ENB		ENB	ENABLE
0x01h	PMC CLOCKS							PMC_CLK_SEL	
0x02h	PMC CLK_DIV	PMC_CLK_DIV(R)							
PLL									
0x03h								PLL_CLK_SEL	
0x04h	PLL M		PLL M						
0x05h	PLL N	PLL N							
0x06h	PLL N_MOD		PLL P2[8]	PLL P1[8]	PLL N_MOD				
0x07h	PLL P	PLL P1 [7:0]							
0x08h	PLL P2	PLL P2[7:0]							
ANALOG MIXER									
0x10h	CLASSD			AUX_LS	MONO_LS			DACL_LS	DACR_LS
0x11h	HEAD PHONESL			AUX_HPL	MONO _HPL			DACL_HPL	DACR_HPL
0x12h	HEAD PHONESR			AUX_HPR	MONO _HPR			DACL _HPR	DACR _HPR
0x13h	AUX_OUT			AUX_AUX	MONO _AUX		MIC_AUX	DACL_AUX	DACR _AUX
0x14h	OUTPUT OPTIONS	LS_LEVEL		AUX_LINE_ OUT	AUX_NEG_ 6dB	LR_HP_LEVEL			RSVD
0x15h	ADC			MONO _ADCL	AUX _ADCR	MIC_ADCL	MIC_ADCR	DACL _ADCL	DACR _ADCR
0x16h	MIC_LVL			MUTE	SE/DIFF	MIC_LEVEL			
0x18h	AUXL_LVL		SE/DIFF	AUX_LEVEL					
0x19h	MONO_LV	AUXL_MON O_IN	SE/DIFF	MONO_LEVEL					
0x1Bh	HP _SENSE					HP SENSE _AUX_D	HP SENSE _AUX	HP SENSE_D	HP SENSE
ADC									
0x20h	ADC BASIC	DSPONLY	ADC_CLK_SEL			MUTE_R	MUTE_L	ADC_OSR	MONO

Copyright © 2009–2013, Texas Instruments Incorporated

Table 1. Device Register Map (continued)

Address	Register	7	6	5	4	3	2	1	0
0x21h	ADC CLOCK	ADC_CLK_DIV (T)							
0x23h	ADC _MIXER				STEREO _LINK	ADC_MIX_LEVEL_R		ADC_MIX_LEVEL_L	
DAC									
0x30h	DAC _BASIC	DSPONLY	DAC_CLK_SEL			MUTE_R	MUTE_L	DAC_OSR	
0x31h	DAC _CLOCK	DAC_CLK_DIV (S)							
DIGITAL MIXER									
0x40h	IPLVL1	PORT2_RX_R_LVL		PORT2_RX_L_LVL		PORT1_RX_R_LVL		PORT1_RX_L_LVL	
0x41h	IPLVL2	INTERP_L_LVL		INTERP_R_LVL		ADC_R_LVL		ADC_L_LVL	
0x42h	OPPORT1			MONO	SWAP	R_SEL		L_SEL	
0x43h	OPPORT2			MONO	SWAP	R_SEL		L_SEL	
0x44h	OPDAC		SWAP	ADCR	PORT2R	PORT1R	ADCL	PORT2L	PORT1L
0x45h	OPDECI			MXRCLK_SEL		R_SEL		L_SEL	
AUDIO PORT 1									
0x50h	BASIC	STEREO _SYNC _MODE	STEREO _SYNC _PHASE	CLK_PH	SYNC_MS	CLK_MS	TX_ENB	RX_ENB	STEREO
0x51h	CLK_GEN1		CLK_SEL	HALF_CYCLE_DIVDER					
0x52h	CLK_GEN2					SYNTH _DENOM	SYNTH_NUM		
0x53h	SYNC _GEN			SYNC_WIDTH(MONO MODE)			SYNC_RATE		
0x54h	DATA _WIDTH	TX_EXTRA_BITS		TX_WIDTH			RX_WIDTH		
0x55h	RX_MODE	A/ULAW	COMPAND	MSB_POSITION					RX_MODE
0x56h	TX_MODE	A/ULAW	COMPAND	MSB_POSITION					TX_MODE
AUDIO PORT 2									
0x60h	BASIC	STEREO _SYNC _MODE	STEREO _SYNC _PHASE	CLK_PH	SYNC_MS	CLK_MS	TX_ENB	RX_ENB	STEREO
0x61h	CLK_GEN1		CLK_SEL	HALF_CYCLE_DIVDER					
0x62h	CLK_GEN2					SYNTH_DE NOM	SYNTH_NUM		
0x63h	SYNC _GEN			SYNC_WIDTH (MONO MODE)			SYNC_RATE		
0x64h	DATA _WIDTH	TX_EXTRA_BITS		TX_WIDTH			RX_WIDTH		
0x65h	RX_MODE	A/ULAW	COMPAND	MSB_POSITION					RX_MODE
0x66h	TX_MODE	A/ULAW	COMPAND	MSB_POSITION					TX_MODE
EFFECTS ENGINE									
0x70h	ADC FX				ADC SCLP ENB	ADC EQ ENB	ADC PK ENB	ADC ALC ENB	ADC HPF_ENB
0x71h	DAC FX				DAC SCLP ENB	RSVD	DAC EQ ENB	DAC PK ENB	DAC ALC ENB
ADC EFFECTS									
0x80h	HPF						HPF MODE		
0x81h	ADC ALC 1	SOURCE OVR	SOURCE RSEL	SOURCE LSEL	STEREO LINK	LIMITER	ADC_SAMPLE		
0x82h	ADC ALC 2				NG_ENB	NOISE_FLOOR			

Copyright © 2009–2013, Texas Instruments Incorporated

Table 1. Device Register Map (continued)

Address	Register	7	6	5	4	3	2	1	0
0x83h	ADC ALC 3	ALC_TARGET_LEVEL							
0x84h	ADC ALC 4	ATTACK_RATE							
0x85h	ADC ALC 5	PK_DECAY_RATE			DECAY_RATE/RELEASE_RATE				
0x86h	ADC ALC 6	HOLDTIME							
0x87h	ADC ALC 7	MAX_LEVEL							
0x88h	ADC ALC 8	MIN_LEVEL							
0x89h	ADC L LEVEL	STEREO LINK	ADC_L_LEVEL						
0x8Ah	ADC R LEVEL	ADC_R_LEVEL							
0x8Bh	EQ BAND 1	LEVEL						FREQ	
0x8Ch	EQ BAND 2	Q	LEVEL					FREQ	
0x8Dh	EQ BAND 3	Q	LEVEL					FREQ	
0x8Eh	EQ BAND 4	Q	LEVEL					FREQ	
0x8Fh	EQ BAND 5	LEVEL						FREQ	
0x90h	SOFTCLIP 1				SOFT KNEE	THRESHOLD			
0x91h	SOFTCLIP 2	RATIO							
0x92h	SOFTCLIP 3	LEVEL							
ADC EFFECT MONITORS									
0x98h	LVLMONL	ADC LEFT LEVEL MONITOR							
0x99h	LVLMONR	ADC RIGHT LEVEL MONITOR							
0x9Ah	FXCLIP	SCLP _R CLIP	SCLP _L CLIP	EQ _R CLIP	EQ _L CLIP	GAIN _R CLIP	GAIN _L CLIP	ADC _R CLIP	ADC _L CLIP
0x9Bh	ALCMONL	SCLP_R DISTORT	SCLP_L DISTORT	ADC LEFT ALC MONITOR					
0x9Ch	ALCMONR	SCLP_L DISTORT	SCLP_R DISTORT	ADC RIGHT ALC MONITOR					
DAC EFFECTS									
0xA0h	DAC ALC 1				STEREO LINK	LIMITER	DAC_SAMPLE		
0xA1h	DAC ALC 2				NG_ENB	NOISE_FLOOR			
0xA2h	DAC ALC 3	AGC_TARGET_LEVEL							
0xA3h	DAC ALC 4	ATTACK_RATE							
0xA4h	DAC ALC 5	PK_DECAY_RATE			DECAY_RATE/RELEASE_RATE				
0xA5h	DAC ALC 6	HOLDTIME							
0xA6h	DAC ALC 7	MAX_LEVEL							
0xA7h	DAC ALC 8	MIN_LEVEL							
0xA8h	DAC L LEVEL	STEREO LINK	DAC_L_LEVEL						

Copyright © 2009–2013, Texas Instruments Incorporated

Table 1. Device Register Map (continued)

Address	Register	7	6	5	4	3	2	1	0
0xA9h	DAC R LEVEL			DAC_R_LEVEL					
0xABh	EQ BAND 1		LEVEL					FREQ	
0xACh	EQ BAND 2	Q	LEVEL					FREQ	
0xADh	EQ BAND 3	Q	LEVEL					FREQ	
0xAEh	EQ BAND 4	Q	LEVEL					FREQ	
0xAFh	EQ BAND 5		LEVEL					FREQ	
0xB0h	SOFTCLIP 1				SOFT KNEE	THRESHOLD			
0xB1h	SOFTCLIP 2				RATIO				
0xB2h	SOFTCLIP 3				LEVEL				
DAC EFFECT MONITORS									
0xB8h	LVLMONL	DAC LEFT LEVEL MONITOR							
0xB9h	LVLMONR	DAC RIGHT LEVEL MONITOR							
0xBAh	FXCLIP	SCLP _R CLIP	SCLP _L CLIP	EQ _R CLIP	EQ _L CLIP	RSVD	RSVD	GAIN _R CLIP	GAIN _L CLIP
0xBBh	ALCMONL	SCLP_R DISTORT	SCLP_L DISTORT	DAC LEFT ALC MONITOR					
0xBCh	ALCMONR	SCLP_L DISTORT	SCLP_R DISTORT	DAC RIGHT ALC MONITOR					
GPIO									
0xE0h	GPIO1	GPIO_RX	GPIO_TX	GPIO_MODE					
0xE1h	GPIO2							TEMP	SHORT
SPREAD SPECTRUM									
0xF0h	RESET			SOFT _RESET	RSVD	RSVD	RSVD	RSVD	RSVD
0xF1h	SS						SS _DISABLE	RSVD	RSVD
0xFEh	FORCE						CPFORCE	DACREF	RSVD

Unless otherwise specified, the default values of the I^2C registers is 0x00h.

Table 2. Nonzero I^2C Default Registers

Address	Register	Default Data Value
0x02h	PMC_CLK_DIV	0x50h
0x30h	DAC_BASIC	0x02h
0x31h	DAC_CLOCK	0x03h
0x84h	ADC_ALC_4	0x0Ah
0x85h	ADC_ALC_5	0x0Ah
0x86h	ADC_ALC_6	0x0Ah
0x87h	ADC_ALC_7	0x1Fh
0x89h	ADC_L_LEVEL	0x33h
0x8Ah	ADC_R_LEVEL	0x33h
0xA3h	DAC_ALC_4	0x0Ah
0xA4h	DAC_ALC_5	0x0Ah
0xA5h	DAC_ALC_6	0x0Ah
0xA6h	DAC_ALC_7	0x33h

Copyright © 2009–2013, Texas Instruments Incorporated

Table 2. Nonzero I²C Default Registers (continued)

Address	Register	Default Data Value
0xA8h	DAC_L_LEVEL	0x33h
0xA9h	DAC_R_LEVEL	0x33h
0xF0h	RESET	0x02h

Basic PMC Setup Register

This register is used to control the LM49352's Basic Power Management Setup:

Table 3. PMC_SETUP (0x00h)

Bits	Field	Description	
0	CHIP_ENABLE	When this bit is set the power management will enable the MCLK I/O or internal oscillator(1). It will then use this clock to sequence the enabling of the analog references and bias points. When this bit is cleared the PMC will bring the analog down gently and disable the MCLK or oscillator.	
		CHIP _ENABLE	Chip Status
		0	Turn Chip Off
		1	Turn Chip On
1	PLL_ENB	This enables the PLL.	
		PLL_ENABLE	PLL Status
		0	PLL Off
		1	PLL On
2	PLL_P2ENB	This enables the P2 output of the PLL.	
		PLL_P2ENB	PLL P2 Status
		0	PLL P2 Off
		1	PLL P2 On
3	OSC_ENB	This enables the internal 300kHz Oscillator. For analog only chip modes, the oscillator can be used instead of an external system clock to drive the chip's power management (PMC).	
		OSC_ENABLE	Oscillator Status
		0	Oscillator Off
		1	Oscillator On
4	MCLK_OVR	This forces the MCLK input to enable, regardless of requirement. If set, the audio ports and digital mixer can be activated even if the chip is in shutdown mode. This assumes that MCLK is selected as the PMC clock source (reg 0x01h) and that there is an active clock signal driving the MCLK pin. Setting this bit reduces power consumption, by allowing audio ports and digital mixer to operate while the analog sections of the chip are powered down.	
		MCLK_OVR	Comment
		0	I/O control is automatic
		1	MCLK input forced on.
5	PORT1_CLK_OVR	This forces the clock input of Audio Port 1 input to enable, regardless of other port settings.	
		PORT1_CLK_OVR	Comment
		0	I/O control is automatic
		1	PORT_CLK input forced on
6	PORT2_CLK_OVR	This forces the clock input of Audio Port 2 input to enable, regardless of other port settings.	
		PORT2_CLK_OVR	Comment
		0	I/O control is automatic
		1	PORT_CLK input forced on
7	CHIP_ACTIVE	This bit is used to readback the enable status of the chip.	

(1) If the PMC is set to operate from one of the audio ports then it will wait for the port to be enabled or the relevant override bit to be set, forcing the port clock input to enable.

Copyright © 2009–2013, Texas Instruments Incorporated

PMC Clocks Register

This register is used to control the LM49352's Basic Power Management Clock:

Table 4. PMC_SETUP (0x01h)

Bits	Field	Description	
1:0	PMC_CLK_SEL	This selects the source of the PMC input clock.	
		PMC_CLK_SEL	PMC Input Clock Source
		00	MCLK (Default divide is 40.5)
		01	Internal 300kHz Oscillator
		10	DAC SOURCE CLOCK
		11	ADC SOURCE CLOCK

PMC Clock Divide Register

This register is used to control the LM49352's Power Management Circuit Clock Divider:

Table 5. PMC_SETUP (0x02h)

Bits	Field	Description	
7:0	PMC_CLK_DIV	This programs the half cycle divider that precedes the PMC. The PMC should run from a 300kHz clock. The default of this divider is 0x50h (divide by 40.5) to get a ≈300kHz PMC clock from a 12MHz or 12.288MHz MCLK. Program this divider with the required division, multiplied by 2, and subtract 1.	
		PMC_CLK_DIV	Divide by
		00000000	1
		00000001	1
		00000010	1.5
		00000011	2
		00000100	2.5
		00000101	3
		—	—
		11111101	126
		11111110	127.5
		11111111	128

LM49352 Clock Network

(Refer to Figure 57)

The audio DAC and ADC operate at a clock frequency of 2*OSR*f_S where OSR is the oversampling ratio and f_S is the sampling frequency of the DAC or ADC. The DAC can operate at three different OSR settings (128, 125, 64). The ADC can operate at two different OSR settings (128, 125). For example, if the stereo DAC or ADC is set at OSR = 128, a 12.288MHz clock is required for 48kHz data. If a 12.288MHz clock is not available, then the internal PLL can be used to generate the desired clock frequency. Otherwise, if a 12.288MHz is available, the PLL can be bypassed to reduce power consumption. The DAC clock divider or ADC clock divider can also be used to generate the correct clock. If an 18.432 MHz clock is available, the DAC or ADC clock divider could be set to 1.5 in order to generate a 12.288MHz clock from 18.432MHz without using a PLL.

The DAC path clock (DAC_SOURCE_CLK) and ADC path clock (ADC_SOURCE_CLK) can be driven directly by the MCLK input, the PORT1_CLK input, the PORT2_CLK input, or PLL output.

For instances where a PLL must be used, the PLL input clock can come from three sources. The clock input to the PLL can come from the MCLK input, the PORT1_CLK input, or the PORT2_CLK input.

The LM49352's Power Management Circuit (PMC) requires a clock that is independent from the DAC or ADC. It is recommended to provide a ≈300kHz clock at Point C. The PMC clock divider is available to generate the correct clock to the PMC block. The PMC clock path can be driven directly by the MCLK input, the internal 300kHz oscillator, the DAC_SOURCE_CLK, or the ADC_SOURCE_CLK.

Copyright © 2009–2013, Texas Instruments Incorporated

Table 6. DAC Clock Requirements

DAC Sample Rate (kHz)	Clock Required at A (OSR = 128)	Clock Required at A (OSR = 125)	Clock Required at A (OSR = 64)	Clock Required at A (OSR = 32)
8	2.048 MHz	2 MHz	1.024 MHz	0.512 MHz
11.025	2.8224 MHz	2.75625 MHz	1.4112 MHz	0.7056 MHz
12	3.072 MHz	3 MHz	1.536 MHz	0.768 MHz
16	4.096 MHz	4 MHz	2.048 MHz	1.024 MHz
22.05	5.6448 MHz	5.5125 MHz	2.8224 MHz	1.4112 MHz
24	6.144 MHz	6 MHz	3.072 MHz	1.536 MHz
32	8.192 MHz	8 MHz	4.096 MHz	2.048MHz
44.1	11.2896 MHz	11.025 MHz	5.6448 MHz	2.8224 MHz
48	12.288 MHz	12 MHz	6.144 MHz	3.072 MHz
96	24.576 MHz	24 MHz	12.288 MHz	6.144 MHz

Table 7. ADC Clock Requirements

ADC Sample Rate (kHz)	Clock Required at B (OSR = 128)	Clock Required at B (OSR = 125)
8	2.048 MHz	2 MHz
11.025	2.8224 MHz	2.75625 MHz
12	3.072 MHz	3 MHz
16	4.096 MHz	4 MHz
22.05	5.6448 MHz	5.5125 MHz
24	6.144 MHz	6 MHz
32	8.192 MHz	8 MHz
44.1	11.2896 MHz	11.025 MHz
48	12.288 MHz	12 MHz

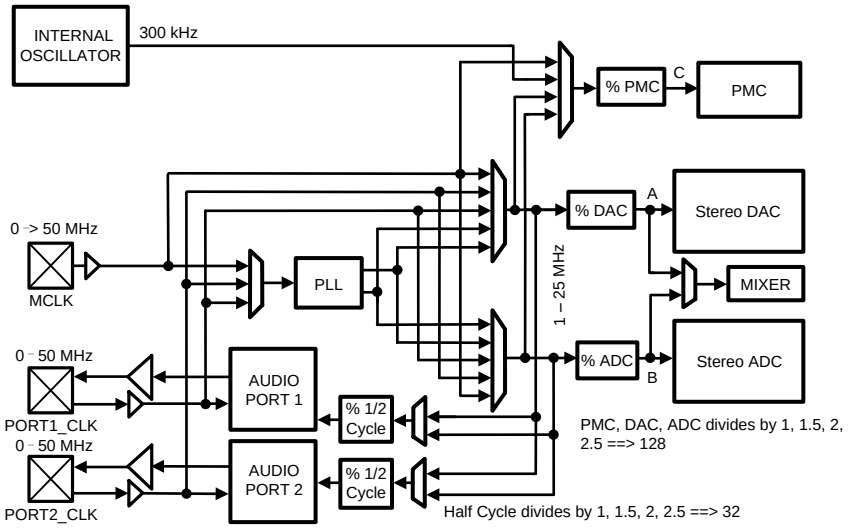


Figure 57. Internal Clock Network

Copyright © 2009–2013, Texas Instruments Incorporated

PLL Setup Registers

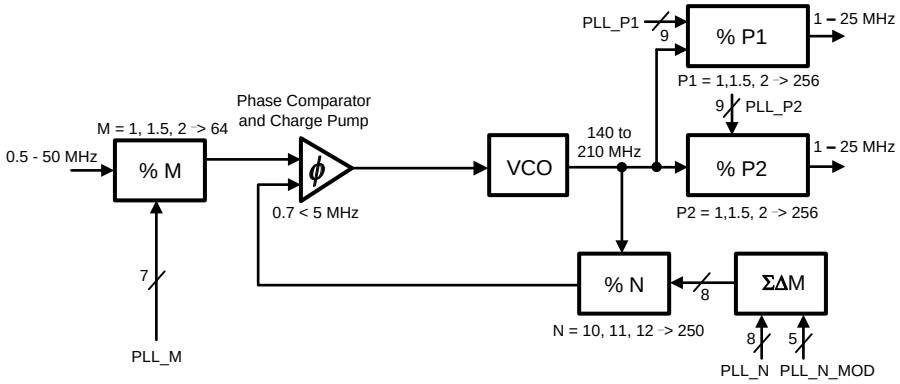


Figure 58. PLL Loop

The LM49352 contains a PLL for flexible operation of its dual audio ports. The PLL has a P1 and P2 output divider thereby allowing the PLL to generate two distinct clock outputs. The equations for the PLL's generated output clocks are as follows:

$f_{OUT1} = (f_{IN} . N / M . P_1)$

$f_{OUT2} = (f_{IN} . N / M . P_2)$

where:

N = PLL_N + PLL_N_MOD

M = (PLL_M + 1) / 2

P_1 = (PLL_P1 + 1) / 2

P_2 = (PLL_P2 + 1) / 2

The VCO frequency and comparison frequencies are as follows:

$f_{VCO} = f_{OUT}.P$

$f_{COMP} = f_{IN}/M$

Keep f_{VCO} between 140MHz to 240MHz and keep f_{COMP} between 700KHz to 5MHz.

Table 8. PLL Settings for Common System Clock Frequencies

f_{IN} (MHz)	M	N	N_MOD	P	f_{OUT} (Hz)	Error (Hz)
12	2.5	32	0	12.5	12288000	0
13	15.5	175	26	12	12287970	–30
14.4	12.5	128	0	12	12288000	0
16.2	13.5	128	0	12.5	12288000	0
16.8	3.5	32	0	12.5	12288000	0
19.2	12.5	96	0	12	12288000	0
19.68	20.5	160	0	12.5	12288000	0
19.8	16.5	128	0	12.5	12288000	0
26	32.5	192	0	12.5	12288000	0
27	22.5	128	0	12.5	12288000	0
12	12.5	147	0	12.5	11289600	0
12.288	10	147	0	16	11289600	0
13	9	144	19	18.5	11289603	+3
14.4	12.5	147	0	15	11289600	0
16.2	22.5	196	0	12.5	11289600	0
16.8	12.5	126	0	15	11289600	0
19.2	20	147	0	12.5	11289600	0

Copyright © 2009–2013, Texas Instruments Incorporated

Table 8. PLL Settings for Common System Clock Frequencies (continued)

f_{IN} (MHz)	M	N	N_MOD	P	f_{OUT} (Hz)	Error (Hz)
19.68	20.5	147	0	12.5	11289600	0
19.8	27.5	196	0	12.5	11289600	0
26	18.5	144	19	18	11289602.1	2.1
27	37.5	196	0	12.5	12289600	0
11.2896	10.5	195	0	17.5	12000000	0
12.288	8	125	0	16	12000000	0
13	6.5	102	0	17	12000000	0
13.5	4.5	68	0	17	12000000	0
14.4	6	85	0	17	12000000	0
16.2	13.5	170	0	17	12000000	0
16.8	7	85	0	17	12000000	0
19.2	8	85	0	17	12000000	0
19.68	20.5	200	0	16	12000000	0
19.8	16.5	170	0	17	12000000	0
26	6.5	36	0	12	12000000	0
11.2896	8	125	0	16	11025000	0
12	10	147	0	16	11025000	0
12.288	8	114	27	16	11025000	0
13	6.5	96	15	17.5	11025000	0
13.5	10	147	0	18	11025000	0
14.4	4	49	0	16	11025000	0
16.2	4	49	0	18	11025000	0
16.8	16	189	0	18	11025000	0
19.2	16	147	0	16	11025000	0
19.68	16	189	0	18	11025000	0
19.8	16	147	0	16.5	11025000	0
26	5	27	18	13	1102500	0

Table 9. PLL_CLOCK_SOURCE (0x03h)

Bits	Field	Description	
1:0	PLL_CLK_SEL	This selects the source of the input clock to the PLL.	
		PLL_CLK_SEL	PLL Input Clock Source
		00	MCLK
		01	PORT1_CLK
		10	PORT2_CLK
		11	RESERVED

Copyright © 2009–2013, Texas Instruments Incorporated

Table 10. PLL_M (0x04h)

Bits	Field	Description	
6:0	PLL_M	This programs the PLL's M divider to divide from 1 to 64.	
		PLL_M	PLL Input Divider Value
		000000	1
		000001	1
		000010	1.5
		000011	2
		000100	2.5
		000101	3
		—	—
		1111101	63
		1111110	63.5
		1111111	64

Table 11. PLL_N (0x05h)

Bits	Field	Description	
7:0	PLL_N	This programs the PLL N divider to divide from 1 to 250.	
		PLL_N	Feedback Divider Value
		00000000 to 00001010	10
		00001011	11
		00001100	12
		00001101	13
		00001110	14
		00001111	15
		—	—
		11111000	248
		11111001	249
		11111010 to 11111111	250

Table 12. PLL_N_MOD (0x06h)

Bits	Field	Description	
4:0	PLL_N_MOD	This programs the sigma-delta modulator in the PLL.	
		PLL_N_MOD	Fractional Part of N
		00000	0
		00001	1/32
		00010	2/32
		00011	3/32
		00100	4/32
		00101	5/32
		—	—
		11101	20/32
		11110	30/32
		11111	31/32
5	PLL_P1[8]	This sets the MSB of the 1st P Divider on the PLL which is part of a standard half-cycle divider control.	
6	PLL_P2[8]	This sets the MSB of the 2nd P Divider on PLL which is part of a standard half-cycle divider control.	

Copyright © 2009–2013, Texas Instruments Incorporated

Table 13. PLL_P1 (0x07h)

Bits	Field	Description	
7:0	PLL_P1[7:0]	This programs the 8 LSBs of the PLL's P1 Divider. These LSBs combine with PL1_P1[8] which allows the P1 divider to divide by up to 256.	
		PLL_P1 [8:0]	P1 Divider Value
		000000000	1
		000000001	1
		000000010	1.5
		000000011	2
		000000100	2.5
		000000101	3
		—	—
		111111101	255
		111111110	255.5
		111111111	256

Table 14. PLL_P2 (0x08h)

Bits	Field	Description	
7:0	PLL_P2[7:0]	This programs 8 LSBs of the PLL's P2 Divider. These LSBs combine with PLL_P2[8] which allows the P2 divider to divide by up to 256.	
		PLL_P2 [8:0]	P2 Divider Value
		000000000	1
		000000001	1
		000000010	1.5
		000000011	2
		000000100	2.5
		000000101	3
		—	—
		111111101	255
		111111110	255.5
		111111111	256

Analog Mixer Control Registers

This register is used to control the LM49352's Analog Mixer:

Table 15. CLASS_D_OUTPUT (0x10h)

Bits	Field	Description
0	DACR_LS	The right DAC output is added to the loudspeaker output.
1	DACL_LS	The left DAC output is added to the loudspeaker output.
2	RSVD	Reserved
3	RSVD	Reserved
4	MONO_LS	The MONO input is added to the loudspeaker output.
5	AUX_LS	The AUX input is added to the loudspeaker output.

Copyright © 2009–2013, Texas Instruments Incorporated

Class D Loudspeaker Amplifier

The LM49352 features a filterless modulation scheme. The differential outputs of the device switch at 300kHz from V_{DD} to GND. When there is no input signal applied, the two outputs (LS+ and LS-) switch with a 50% duty cycle, with both outputs in phase. Because the outputs of the LM49352 are differential, the two signals cancel each other. This results in no net voltage across the speaker, thus there is no load current during an idle state, conserving power.

With an input signal applied, the duty cycle (pulse width) of the LM49352 outputs changes. For increasing output voltages, the duty cycle of LS+ increases, while the duty cycle of LS- decreases. For decreasing output voltages, the converse occurs, the duty cycle of LS- increases while the duty cycle of LS+ decreases. The difference between the two pulse widths yields the differential output voltage.

Spread Spectrum Modulation

The LM49352 features a fitlerless spread spectrum modulation scheme that eliminates the need for output filters, ferrite beads or chokes. The switching frequency varies by ±30% about a 300kHz center frequency, reducing the wideband spectral content, improving EMI emissions radiated by the speaker and associated cables and traces. Where a fixed frequency class D exhibits large amounts of spectral energy at multiples of the switching frequency, the spread spectrum architecture of the LM49352 spreads that energy over a larger bandwidth. The cycle-to-cycle variation of the switching period does not affect the audio reproduction or efficiency.

Class D Power Dissipation and Efficiency

In general terms, efficiency is considered to be the ratio of useful work output divided by the total energy required to produce it with the difference being the power dissipated, typically, in the IC. The key here is “useful” work. For audio systems, the energy delivered in the audible bands is considered useful including the distortion products of the input signal. Sub-sonic (DC) and super-sonic components (>22kHz) are not useful. The difference between the power flowing from the power supply and the audio band power being transduced is dissipated in the LM49352 and in the transducer load. The amount of power dissipation in the LM49352's class D amplifier is very low. This is because the ON resistance of the switches used to form the output waveforms is typically less than 0.25Ω. This leaves only the transducer load as a potential "sink" for the small excess of input power over audio band output power. The LM49352 dissipates only a fraction of the excess power requiring no additional PCB area or copper plane to act as a heat sink.

EMI/RFI Filtering

If system level PCB layout constraints require the LM49352’s Class D output bumps to be placed far away from the speaker or the Class D output traces to be routed near EMI/RFI sensitive components, an external EMI/RFI filter should be used. A series ferrite bead placed close to the Class D output bumps along with a shunt capacitor to ground placed close to the ferrite bead will reduce the EMI/RFI emissions of the Class D amplifier’s switching outputs. The ferrite bead must be rated with a current rating high enough to properly drive the loudspeaker. The ferrite bead that is rated for 1A or greater is recommended. The DC resistance of the ferrite bead is another important specification that must be taken into consideration. A low DC resistance will minimize any power losses dissipated by the EMI/RFI filter thereby preserving the power efficiency advantages of the Class D amplifier. Selecting a ferrite bead with high DC resistance will decrease output power delivered to speaker and reduce the Class D amplifier’s efficiency. The shunt capacitor needs to have low ESR. A 10pF ceramic capacitor with a X7R dielectric is recommended as a starting point. Care needs to be taken to ensure that the value of the shunt capacitor does not exceed 47pF when using a low resistance ferrite bead in order to prevent permanent damage to the low side FETs of the Class D output stage.

Copyright © 2009–2013, Texas Instruments Incorporated

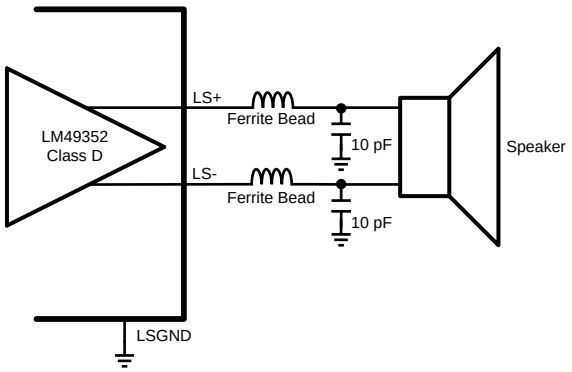


Figure 59. EMI/RFI Filter for the Class D Amplifier

Table 16. LEFT HEADPHONE_OUTPUT (0x11h)

Bits	Field	Description
0	DACR_HPL	The right DAC output is added to the left headphone output.
1	DACL_HPL	The left DAC output is added to the left headphone output.
2	RSVD	Reserved
3	RSVD	Reserved
4	MONO_HPL	The MONO input is added to the left headphone output.
5	AUX_HPL	The AUX input is added to the left headphone output.

Table 17. RIGHT HEADPHONE_OUTPUT (0x12h)

Bits	Field	Description
0	DACR_HPR	The right DAC output is added to the right headphone output.
1	DACL_HPR	The left DAC output is added to the right headphone output.
2	RSVD	Reserved
3	RSVD	Reserved
4	MONO_HPR	The MONO input is added to the right headphone output.
5	AUX _HPR	The AUX input is added to the right headphone output.

Headphone Amplifier Function

The LM49352 headphone amplifier features TI's ground referenced architecture that eliminates the large DC-blocking capacitors required at the outputs of traditional headphone amplifiers. A low-noise inverting charge pump creates a negative supply (HP_V_{SS}) from the positive supply voltage (LS_V_{DD}). The headphone amplifiers operate from these bipolar supplies, with the amplifier outputs biased about GND, instead of a nominal DC voltage (typically $V_{DD}/2$), like traditional amplifiers. Because there is no DC component to the headphone output signals, the large DC-blocking capacitors (typically 220µF) are not necessary, conserving board space and system cost, while improving frequency response.

Charge Pump Capacitor Selection

Use low ESR ceramic capacitors (less than 100mΩ) for optimum performance.

Charge Pump Flying Capacitor (C6)

The flying capacitor (C6) affects the load regulation and output impedance of the charge pump. A C6 value that is too low results in a loss of current drive, leading to a loss of amplifier headroom. A higher valued C6 improves load regulation and lowers charge pump output impedance to an extent. Above 2.2µF, the $R_{DS(ON)}$ of the charge pump switches and the ESR of C6 and C5 dominate the output impedance. A lower value capacitor can be used in systems with low maximum output power requirements. Please refer to the demonstration board schematic shown in Figure 72.

Copyright © 2009–2013, Texas Instruments Incorporated

Charge Pump Flying Capacitor (C5)

The value and ESR of the hold capacitor (C5) directly affects the ripple on CPV_{SS}. Increasing the value of C5 reduces output ripple. Decreasing the ESR of C5 reduces both output ripple and charge pump output impedance. A lower value capacitor can be used in systems with low maximum output power requirements. Please refer to the demonstration board schematic shown in Figure 72.

Table 18. AUX_OUTPUT (0x13h)

Bits	Field	Description
0	DACR_AUX	The right DAC output is added to the AUX output.
1	DACL_AUX	The left DAC output is added to the AUX output.
2	MIC_AUX	The MIC input is added to the AUX output.
3	RSVD	Reserved
4	MONO_AUX	The MONO input is added to the AUX output.
5	AUX_AUX	The AUX input is added to the AUX output.

Auxiliary Output Amplifier

The LM49352's auxiliary output (AUXOUT) amplifier provides differential drive capability to loads that are connected across its outputs. This results in output signals at the AUX_OUT+ and AUX_OUT- pins that are 180 degrees out of phase with respect to each other. This effectively doubles the maximum possible output swing for a specific supply voltage when compared to single-ended output configurations. The differential output configuration also allows the load to be isolated from ground since both the AUX_OUT+ and AUX_OUT- pins are biased at the same DC potential. This eliminates the need for any large and expensive DC blocking capacitors at the AUXOUT amplifier outputs. The load can then be directly connected to the positive and negative outputs of the AUXOUT amplifier which then isolates it from any ground noise, thereby improving signal to noise ratio (SNR) and power supply rejection ratio (PSRR).

The AUXOUT amplifier has two modes of operation. The primary mode of operation is high current drive mode (Earpiece Mode) where the AUXOUT amplifier can be used to differentially drive a mono earpiece speaker. The secondary mode of operation is low current drive mode where the AUXOUT amplifier operates in a power saving mode (AUX_LINE_OUT Mode) to provide a differential output that is used as a mono differential line level input to a standalone mono differential input class D amplifier (LM4675) for stereo loudspeaker applications.

Table 19. OUTPUT_OPTIONS (0x14h)

Bits	Field	Description	
0	RSVD	Reserved	
3:1	LR_HP_LEVEL	This sets the gain of the left and right headphone amplifiers. The gain of the left and right headphone amplifiers are always set to the same level.	
		LR_HP_LEVEL	Gain (dB)
		000	0
		001	–1.5
		010	–3
		011	–6
		100	–9
		101	–12
		110	–15
		111	–18
4	AUX_NEG_6dB	This sets the gain of the Auxiliary output amplifier.	
		AUX_NEG_6dB	Gain (dB)
		0	0
		1	–6

Copyright © 2009–2013, Texas Instruments Incorporated

Table 19. OUTPUT_OPTIONS (0x14h) (continued)

Bits	Field	Description	
5	AUX_LINE_OUT	This sets the Auxiliary output amplifier mode of operation.	
		AUX_LINE_OUT	Auxiliary Output Mode
		0	Earpiece Amplifier
		1	AUX_LINE_OUT
7:6	LS_LEVEL	This sets the gain of the Class D loudspeaker amplifier.	
		LS_LEVEL	Gain (dB)
		00	0
		01	4
		10	8
		11	12

Table 20. ADC_INPUT (0x15h)

Bits	Field	Description
0	DACR_ADCR	The right DAC output is added to the ADC right input.
1	DACL_ADCL	The left DAC output is added to the ADC left input.
2	MIC_ADCR	The MIC input is added to the ADC right input.
3	MIC_ADCL	The MIC input is added to the ADC left input.
4	AUX_ADCR	The AUX input is added to the ADC right input.
5	MONO_ADCL	The MONO input is added to the ADC left input.

Table 21. MIC_INPUT (0x16h)

Bits	Field	Description	
3:0	MIC_LEVEL	This sets the gain of the microphone preamp.	
		MIC_LEVEL	Gain
		0000	6dB
		0001	8dB
		0010	10dB
		0011	12dB
		0100	14dB
		0101	16dB
		0110	18dB
		0111	20dB
		1000	22dB
		1001	24dB
		1010	26dB
		1011	28dB
		1100	30dB
		1101	32dB
		1110	34dB
		1111	36dB
4	SE_DIFF	If set, the MIC negative input is ignored. In single-ended mode, the MIC negative input pin should left floating.	
5	MUTE	If set, the microphone preamp is muted.	

Copyright © 2009–2013, Texas Instruments Incorporated

Table 22. AUX_LEVEL (0x18h)

Bits	Field	Description			
5:0	AUX_LEVEL	This programs the AUX input level. All gain changes are performed at zero crossings.			
		AUX_LEVEL	Level	AUX_LEVEL	Level
		000000	–46.5dB	100000	1.5dB
		000001	–45dB	100001	3dB
		000010	–43.5dB	100010	4.5dB
		000011	–42dB	100011	6dB
		000100	–40.5dB	100100	7.5dB
		000101	–39dB	100101	9dB
		000110	–37.5dB	100110	10.5dB
		000111	–36dB	100111	12dB
		001000	–34.5dB	101000	13.5dB
		001001	–33dB	101001	15dB
		001010	–31.5dB	101010	16.5dB
		001011	–30dB	101011	18dB
		001100	–28.5dB		
		001101	–27dB		
		001110	–25.5dB		
		001111	–24dB		
		010000	–22.5dB		
		010001	–21dB		
		010010	–19.5dB		
		010011	–18dB		
		010100	–16.5dB		
		010101	–15dB		
		010110	–13.5dB		
		010111	–12dB		
		011000	–10.5dB		
		011000	–9dB		
		011001	–7.5dB		
		011010	–6dB		
		011100	–4.5dB		
		011101	–3dB		
		011110	–1.5dB		
		011111	0dB		
6	SE/DIFF	If set, the AUXL input is ignored. In single-ended mode, the AUXL input pin should be left floating.			

Copyright © 2009–2013, Texas Instruments Incorporated

Table 23. MONO_LEVEL (0x19h)

Bits	Field	Description			
5:0	MONO_LEVEL	This programs the MONO input level. All gain changes are performed at zero crossings.			
		MONO_LEVEL	Level	MONO_LEVEL	Level
		000000	–46.5dB	100000	1.5dB
		000001	–45dB	100001	3dB
		000010	–43.5dB	100010	4.5dB
		000011	–42dB	100011	6dB
		000100	–40.5dB	100100	7.5dB
		000101	–39dB	100101	9dB
		000110	–37.5dB	100110	10.5dB
		000111	–36dB	100111	12dB
		001000	–34.5dB	101000	13.5dB
		001001	–33dB	101001	15dB
		001010	–31.5dB	101010	16.5dB
		001011	–30dB	101011	18dB
		001100	–28.5dB		
		001101	–27dB		
		001110	–25.5dB		
		001111	–24dB		
		010000	–22.5dB		
		010001	–21dB		
		010010	–19.5dB		
		010011	–18dB		
		010100	–16.5dB		
		010101	–15dB		
		010110	–13.5dB		
		010111	–12dB		
		011000	–10.5dB		
		011000	–9dB		
		011001	–7.5dB		
		011010	–6dB		
		011100	–4.5dB		
		011101	–3dB		
		011110	–1.5dB		
		011111	0dB		
6	SE/DIFF	If set, the MONO– input is ignored. In single-ended mode, the MONO- input pin should be left floating.			
7	AUXL_MONO	If set, AUXL is routed to the MONO Input Amplifier.			

Headphone Detection Circuit

The LM49352 features a headphone detection circuit (HDC) that automatically enables the headphone amplifier whenever the insertion of a headphone plug is detected and disables the headphone amplifier during the removal of a headphone plug. The HDC optimizes power management by automatically disabling any output amplifier that is not in use. The HDC eliminates the necessity of polling the I^2C bus for status changes. However, since the HDC requires the use of the GPIO pin, the PORT2_SDO functionality sensing is required.

The HDC requires a headphone jack with a normally closed mechanical switch and a pullup resistor, R_{PU}, tied between the mechanical switch and I/O_V_{DD} (Refer to Figure 60). Choosing a R_{PU} value of at least 500kΩ ensures minimal current draw through the pullup resistor. When the headphone amplifier is disabled, an internal 50kΩ pulldown, R_{PD}, is connected to each headphone amplifier output. Without the presence of a headphone plug, the headphone jack's mechanical switch is closed thereby connecting the right headphone amplifier output

Copyright © 2009–2013, Texas Instruments Incorporated

to R_{PU}. The GPIO pin detects a logic low level due to the voltage division between R_{PU} and R_{PD}. When the GPIO pin is set to HPSENSE mode, a logic low voltage reading causes the HDC to disable the headphone amplifier. When a headphone plug is inserted, the mechanical connection between R_{PU} and R_{PD} is broken, resulting in a logic high level detected by the GPIO pin. A logic high voltage reading causes the HDC to enable the headphone amplifier.

The HDC has four modes of operation that automatically enable/disable different combinations of the audio output amplifiers contained within the LM49352. Having the choice of four different HDC settings maximizes power management flexibility to suit a particular application. Please refer to the HP_SENSE (reg 0x1Bh) register table for a detailed discussion on the different HDC modes of operation.

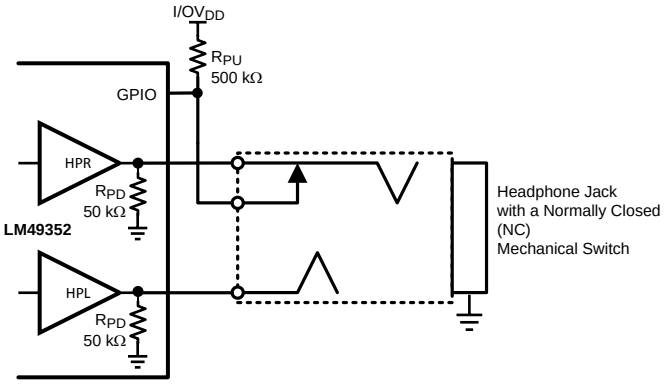


Figure 60. Application Circuit for Headphone Detection

Table 24. HP_SENSE (0x1Bh)

Bits	Field	Description	
0	HP SENSE	This bit enables the headphone sense circuit. If enabled, the headphone amplifier will automatically turn on/off based on the logic level of the GPIO pin whenever GPIO is selected as a headphone sense input. If the presence of a headphone insertion is detected, the headphone amplifier will automatically turn on. If a headphone removal is detected the headphone amplifier will automatically turn off.	
		HPSENSE	Headphone Sense Status
		0	Off
		1	On
1	HPSENSE_D	This bit enables the headphone sense circuit. If enabled, the headphone amplifier will automatically turn on/off based on the logic level of the GPIO pin whenever GPIO is selected as a headphone sense input. If the presence of a headphone insertion is detected, the headphone amplifier will automatically turn on and the Class D loudspeaker amplifier will turn off. If a headphone removal is detected the headphone amplifier will automatically turn off and the Class D loudspeaker amplifier will turn on. This bit overrides bit 0 of this register.	
		HPSENSE_D	Headphone Sense Status
		0	Off
		1	On
2	HPSENSE_AUX	This bit enables the headphone sense circuit. If enabled, the headphone amplifier will automatically turn on/off based on the logic level of the GPIO pin whenever GPIO is selected as a headphone sense input. If the presence of a headphone insertion is detected, the headphone amplifier will automatically turn on and the Earpiece / Auxout amplifier will turn off. If a headphone removal is detected the headphone amplifier will automatically turn off and the Earpiece / Auxout amplifier will turn on. This bit overrides bit 0 and bit 1 of this register.	
		HPSENSE_AUX	Headphone Sense Status
		0	Off
		1	On

Copyright © 2009–2013, Texas Instruments Incorporated

Table 24. HP_SENSE (0x1Bh) (continued)

Bits	Field	Description	
3	HPSENSE_AUX_D	This bit enables the headphone sense circuit. If enabled, the headphone amplifier will automatically turn on/off based on the logic level of the GPIO pin whenever GPIO is selected as a headphone sense input. If the presence of a headphone insertion is detected, the headphone amplifier will automatically turn on and the Class D loudspeaker amplifier along with the Earpiece / Auxout amplifier will turn off. If a headphone removal is detected the headphone amplifier will automatically turn off and the Class D loudspeaker amplifier along with the Earpiece / Auxout amplifier will turn on. This bit overrides bit 0, bit 1, and bit 2 of this register.	
		HPSENSE_AUX_D	Headphone Sense Status
		0	Off
		1	On

ADC Control Registers

This register is used to control the LM49352's ADC:

Table 25. ADC Basic (0x20h)

Bits	Field	Description		
0	MONO	This sets mono or stereo operation of the ADC.		
		MONO	ADC Operation	
		0	Stereo Audio	
		1	Mono Voice (Right ADC channel disabled, Left ADC channel active)	
1	OSR	This sets the oversampling ratio of the ADC.		
		OSR	Stereo Audio ADC Oversampling Ratio	Mono Voice ADC Oversampling Ratio
		0	128	125
		1	128	128
2	MUTE_L	If set, a digital mute is applied to the Left (or mono) ADC output.		
3	MUTE_R	If set, a digital mute is applied to the Right ADC output.		
6:4	ADC_CLK_SEL	This selects the source of the ADC clock domain, ADC_SOURCE_CLK.		
		ADC_CLK_SEL	Source	
		000	MCLK	
		001	PORT1_RX_CLK	
		010	PORT2_RX_CLK	
		011	PLL_OUTPUT1	
		100	PLL_OUTPUT2	
7	ADC_DSP_ONLY	If set, the ADC's analog circuitry is disabled to reduce power consumption, however, ADC DSP functionality is maintained. This can be used to perform asynchronous resampling between audio rates of a common family. Setting this bit is also useful whenever applying Automatic Level Control (ALC) to an analog only audio path.		

Copyright © 2009–2013, Texas Instruments Incorporated

Table 26. ADC_CLK_DIV (0x21h)

Bits	Field	Description	
7:0	ADC_CLK_DIV	This programs the half cycle divider that preceeds the ADC. The input of this divider should be around 12MHz. The default of this divider is 0x00. Program this divider with the division you want, multiplied by 2, and subtract 1.	
		ADC_CLK_DIV	Divides by
		00000000	1
		00000001	1
		00000010	1.5
		00000011	2
		—	—
		11111101	127
		11111110	127.5
		11111111	128

Table 27. ADC_MIXER (0x23h)

Bits	Field	Description	
1:0	ADC_MIX_LEVEL_L	This sets the input level to the left ADC channel.	
		ADC_MIX_LEVEL_L	Level
		00	0dB
		01	1.35dB
		10	3.5dB
		11	6dB
3.2	ADC_MIX_LEVEL_R	This sets the input level to the right ADC channel.	
		ADC_MIX_LEVEL_R	Level
		00	0dB
		01	1.35dB
		10	3.5dB
		11	6dB
4	STEREO_LINK	If set, this links ADC_MIX_LEVEL_R with ADC_MIX_LEVEL_L.	
		STEREO_LINK	Status
		0	Off
		1	On

DAC Control Registers

This register is used to control the LM49352's DAC:

Table 28. DAC Basic (0x30h)

Bits	Field	Description	
1:0	MODE	This programs the over sampling ratio of the stereo DAC.	
		MODE	DAC Oversampling Ratio
		00	125
		01	128
		10	64 (Default)
		11	RSVD
2	MUTE_L	This digitally mutes the Left DAC output.	
3	MUTE_R	This digitally mutes the Right DAC output.	

Copyright © 2009–2013, Texas Instruments Incorporated

Table 28. DAC Basic (0x30h) (continued)

Bits	Field	Description	
6:4	DAC_CLK_SEL	This selects the source of the DAC clock domain, DAC_SOURCE_CLK.	
		DAC_CLK_SEL	Source
		000	MCLK
		001	PORT1_RX_CLK
		010	PORT2_RX_CLK
		011	PLL_OUTPUT1
		100	PLL_OUTPUT2
7	DSP_ONLY	If set, the DAC's analog circuitry is disabled to reduce power consumption, however DAC DSP functionality is maintained. This can be used to perform asyncronous resampling between audio rates of a common family.	

Table 29. DAC_CLK_DIV (0x31h)

Bits	Field	Description	
7:0	DAC_CLK_DIV	This programs the half cycle divider that precedes the DAC. The input of this divider should be around 12MHz. The default of this divider is 0x03 which gives a division by 2. Program this divider with the division you want, multiplied by 2, and subtract 1.	
		DAC_CLK_DIV	Divides by
		00000000	1
		00000001	1
		00000010	1.5
		00000011	2 (Default)
		—	—
		11111101	127
		11111110	127.5
		11111111	128

Digital Mixer Control Registers

Digital Mixer

The LM49352's digital mixer allows for flexible routing of digital audio signals between both audio ports, DAC, and ADC. This mixer handles which digital data path (Port1 RX data, Port2 RX data, or ADC output) is routed to the DAC input. The digital mixer also selects the appropriate digital data path (Port1 RX data, Port2 RX data, ADC output, or DAC DSP (Interpolator) output) that is used for data transmission on Audio Port 1 and 2. Audio inputs to the digital mixer can be attenuated down to -18dB to avoid clipping conditions. The digital mixer also allows direct routing from the DAC interpolator output to the ADC decimator input which allows the DAC and ADC DSP blocks to be cascaded witjhout having to enable the analog of the DAC and ADC in order to save power.

Another key feature of the digital mixer is sample rate conversion (SRC) between audio ports. This allows simultaneous operation of the dual audio ports even if each port is operating at a different sample rate. The LM49352 can be used as an audio port bridge with SRC capability. The digital mixer allows either straight pass through between audio ports or, if desired, DSP effects can be added to the digital audio signal during audio port bridge operation. The digital mixer automatically handles stereo I^2S to mono PCM conversion between audio ports and vice versa.

Copyright © 2009–2013, Texas Instruments Incorporated

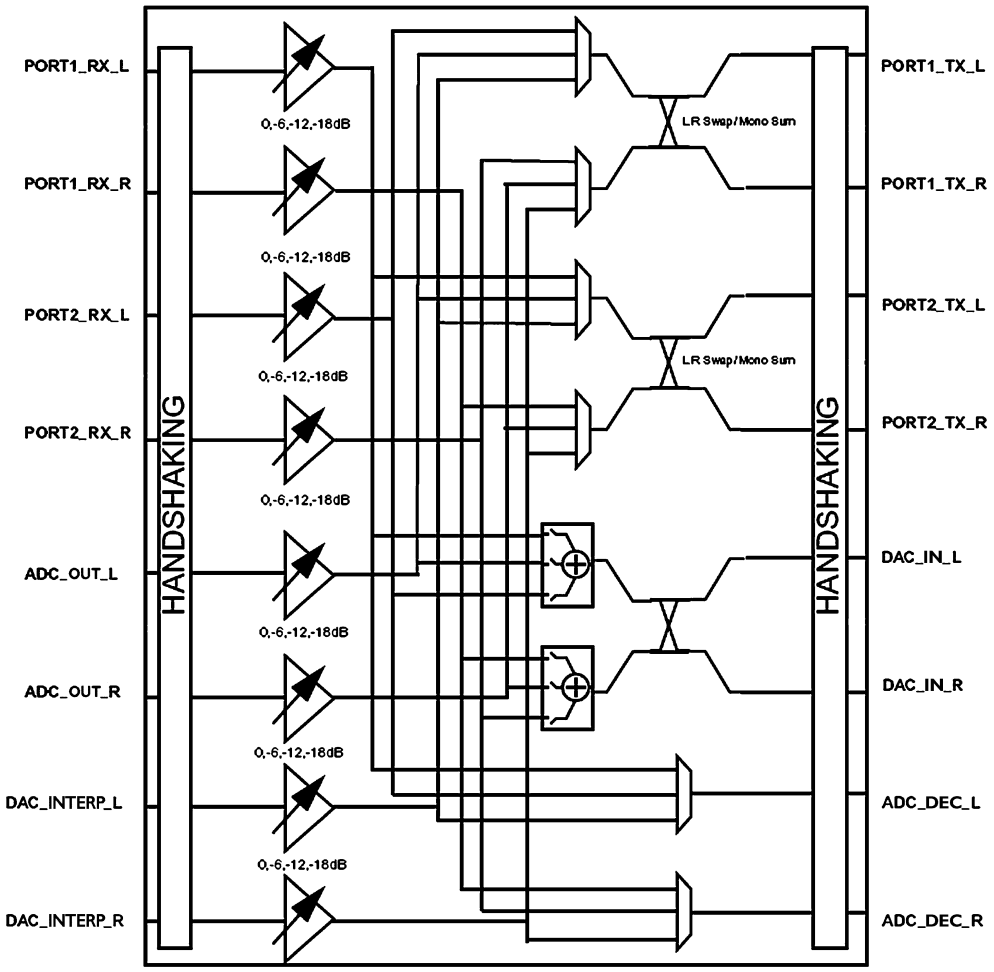


Figure 61. Digital Mixer

The LM49352 includes two separate and independent DSP blocks, one for the DAC and the other for the ADC. The digital mixer also allows both DSP blocks to be cascaded together in either order so that the DSP effects from both blocks can be combined into the same signal path. For example, the 5 band parametric EQ of each DSP block can be combined together to form a 10 band parametric EQ for added flexibility.

This register is used to control the LM49352's digital mixer:

Table 30. Input Levels 1 (0x40h)

Bits	Field	Description	
1:0	PORT1_RX_L _LVL	This programs the input level of the data arriving from the left receive channel of Audio Port 1.	
		PORT1_RX_L_LVL	Level
		00	0dB
		01	–6dB
		10	–12dB
		11	–18dB

Table 30. Input Levels 1 (0x40h) (continued)

Bits	Field	Description	
3:2	PORT1_RX_R_LVL	This programs the input level of the data arriving from the right receive channel of Audio Port 1.	
		PORT1_RX_R_LVL	Level
		00	0dB
		01	–6dB
		10	–12dB
		11	–18dB
5:4	PORT2_RX_L_LVL	This programs the input level of the data arriving from the left receive channel of Audio Port 2.	
		PORT2_RX_L_LVL	Level
		00	0dB
		01	–6dB
		10	–12dB
		11	–18dB
7:6	PORT2_RX_R_LVL	This programs the input level of the data arriving from the right receive channel of Audio Port 2.	
		PORT2_RX_R_LVL	Level
		00	0dB
		01	–6dB
		10	–12dB
		11	–18dB

Table 31. Input Levels 2 (0x41h)

Bits	Field	Description	
1:0	ADC_L_LVL	This programs the input level of the data arriving from the left ADC channel.	
		ADC_L_LVL	Level
		00	0dB
		01	–6dB
		10	–12dB
		11	–18dB
3:2	ADC_R_LVL	This programs the input level of the data arriving from the right ADC channel.	
		ADC_R_LVL	Level
		00	0dB
		01	–6dB
		10	–12dB
		11	–18dB
5:4	INTERP_L_LVL	This programs the input level of the data arriving from the left DAC's interpolator output.	
		INTERP_L_LVL	Level
		00	0dB
		01	–6dB
		10	–12dB
		11	–18dB
7:6	INTERP_R_LVL	This programs the input level of the data arriving from the right DAC's interpolator output.	
		INTERP_R_LVL	Level
		00	0dB
		01	–6dB
		10	–12dB
		11	–18dB

Copyright © 2009–2013, Texas Instruments Incorporated

Table 32. Audio Port 1 Input (0x42h)

Bits	Field	Description	
1:0	L_SEL	This selects which input is fed to the Left TX Channel of Audio Port 1.	
		L_SEL	Selected Input
		00	None
		01	ADC_L
		10	PORT2_RX_L
		11	DAC_INTERP_L
3:2	R_SEL	This selects which input is fed to the Right TX Channel of Audio Port 1.	
		R_SEL	Selected Input
		00	None
		01	ADC_R
		10	PORT2_RX_R
		11	DAC_INTERP_R
4	SWAP	If set, this swaps the Left and Right outputs to Audio Port 1.	
5	MONO	If set, the right channel is ignored and the left channel becomes (left+right)/2.	

Table 33. Audio Port 2 Input (0x43h)

Bits	Field	Description	
1:0	L_SEL	This selects which input is fed to Audio Port 2's Left TX Channel.	
		L_SEL	Selected Input
		00	None
		01	ADC_L
		10	PORT1_RX_L
		11	DAC_INTERP_L
3:2	R_SEL	This selects which input is fed to Audio Port 2's Right TX Channel.	
		R_SEL	Selected Input
		00	None
		01	ADC_R
		10	PORT1_RX_R
		11	DAC_INTERP_R
4	SWAP	If set, this swaps the Left and Right outputs to Audio Port 2.	
5	MONO	If set, the right channel is ignored and the left channel becomes (left+right)/2.	

Table 34. DAC Input Select (0x44h)

Bits	Field	Description
0	PORT1_L	This adds Audio Port 1's left RX channel to the DAC's left input.
1	PORT2_L	This adds Audio Port 2's left RX channel to the DAC's left input.
2	ADC_L	This adds the ADC's left output to the DAC's left input.
3	PORT1_R	This adds Audio Port 1's right RX channel to the DAC's right input.
4	PORT2_R	This adds Audio Port 2's right RX channel to the DAC's right input.
5	ADC_R	This adds the ADC's right output to the DAC's right input.
6	SWAP	If set, this swaps the Left and Right inputs to the DAC.

Copyright © 2009–2013, Texas Instruments Incorporated

Table 35. Decimator Input Select (0x45h)

Bits	Field	Description	
1:0	L_SEL	This selects which input is fed to the left ADC's decimator input.	
		L_SEL	Selected Input
		00	None
		01	PORT1_RX_L
		10	PORT2_RX_L
		11	DAC_INTERP_L
3:2	R_SEL	This selects which input is fed to the right ADC's decimator input.	
		R_SEL	Selected Input
		00	None
		01	PORT1_RX_R
		10	PORT2_RX_R
		11	DAC_INTERP_R
5:4	MXR_CLK_SEL	This selects sets the source of the Digital Mixer Clock. The 'Auto' setting will automatically select the source with the highest clock frequency. If the DAC interpolator output (DAC_OSR_L or DAC_OSR_R) is selected, then MXR_CLK_SEL should be set to '10'.	
		MXR_CLK_SEL	Selected Input
		00	Auto
		01	MCLK
		10	DAC
		11	ADC

Audio Port Control Registers

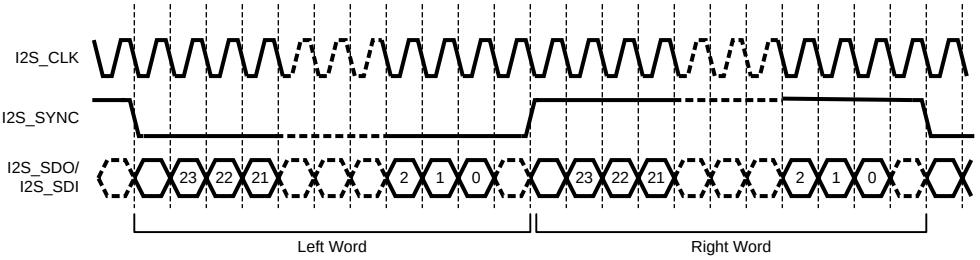


Figure 62. I²S Serial Data Format (24 bit example)

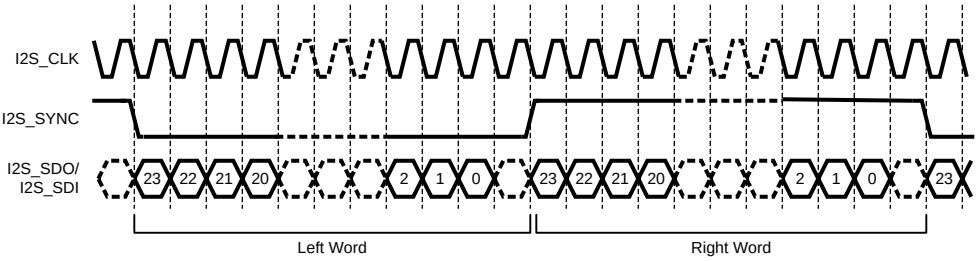


Figure 63. Left Justified Data Format (24 bit example)

Copyright © 2009–2013, Texas Instruments Incorporated

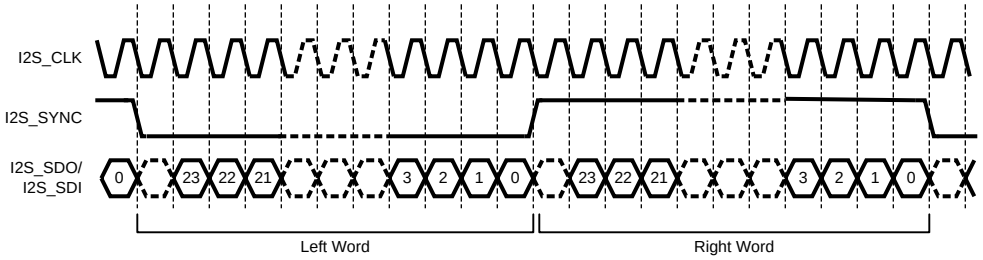


Figure 64. Right Justified Data Format (24 bit example)

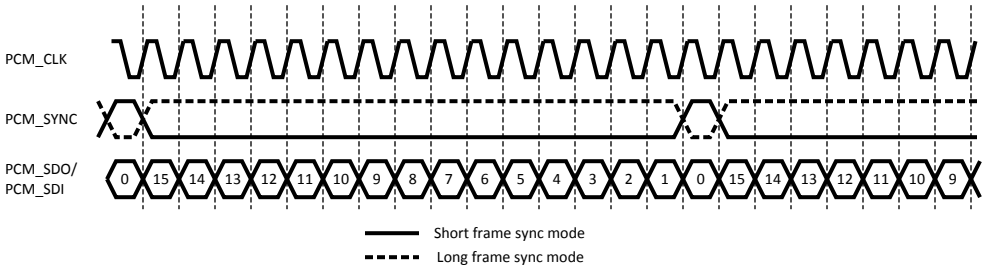


Figure 65. PCM Serial Data Format (16 bit example)

The following registers are used to control the LM49352's audio ports. Audio Port 1 and Audio Port 2 are identical. Port 1 is programmed through the (0x5Xh) registers. Port 2 is programmed through the (0x6Xh) registers.

Table 36. BASIC_SETUP (0x50h/0x60h)

Bits	Field	Description	
0	STEREO	If set, the audio port will receive and transmit stereo data.	
1	RX_ENABLE	If set, the input is enabled (enables the SDI port and input shift register and any clock generation required).	
2	TX_ENABLE	If set, the output is enabled (enables the SDO port and output shift register and any clock generation required).	
3	CLOCK_MS	If set, the audio port will transmit the clock when either the RX or TX is enabled.	
4	SYNC_MS	If set, the audio port will transmit the sync signal when either the RX or TX is enabled.	
5	CLOCK_PHASE	This sets how data is clocked by the Audio Port.	
		CLOCK_PHASE	Audio Data Mode
		0	I^2S (TX on falling edge, RX on rising edge)
		1	PCM (TX on rising edge, RX on falling edge)
6	STEREO_SYNC_PHASE	If set, this reverses the left and right channel data of the Audio Port.	
		STEREO_SYNC_PHASE	Audio Port Data Orientation
		0	Left channel data goes to left channel output. Right channel data goes to right channel output.
		1	Right channel data goes to left channel output. Left channel data goes to right channel output.

Table 36. BASIC_SETUP (0x50h/0x60h) (continued)

Bits	Field	Description	
7	SYNC_INVERT	If this bit is set the SYNC is inverted before the receiver and transmitter.	
		SYNC_INVERT	SYNC ORIENTATION
		0	SYNC Low = Left, SYNC High = Right
		1	SYNC Low = Right, SYNC High = Left

Table 37. CLK_GEN_1 (0x51h/0x61h)

Bits	Field	Description	
5:0	HALF_CYCLE_CLK_DIV	This programs the half-cycle divider that generates the master clocks in the audio port. The default of this divider is 0x00, i.e. bypassed. Program this divider with the required division multiplied by 2, and subtract 1.	
		HALF_CYCLE_CLK_DIV	Divides By
		000000	BYPASS
		000001	1
		000010	1.5
		000011	2
		—	—
		111101	31
		111110	31.5
		11111	32
6	CLOCK_SEL	This selects the clock source of the master mode Audio Port Clock generator's half-cycle divider. 0 = DAC_SOURCE_CLK 1 = ADC_SOURCE_CLK	

Table 38. CLK_GEN_1 (0x52h/62h)

Bits	Field	Description	
2:0	SYNTH_NUM	Along with SYNTH_DENOM, this sets the clock divider that generates the Port 1 or Port 2 clock in master mode.	
		SYNTH_NUM	Numerator
		000	SYNTH_DENOM (1/1)
		001	100/SYNTH_DENOM
		010	96/SYNTH_DENOM
		011	80/SYNTH_DENOM
		100	72/SYNTH_DENOM
		101	64/SYNTH_DENOM
		110	48/SYNTH_DENOM
		111	0/SYNTH_DENOM
3	SYNTH_DENOM	Along with SYNTH_NUM, this sets the clock divider that generates the Port 1 or Port 2 clock in master mode.	
		SYNTH_DENOM	Denominator
		0	128
		1	125

Copyright © 2009–2013, Texas Instruments Incorporated

Table 39. CLK_GEN_1 (0x53h/63h)

Bits	Field	Description	
2:0	SYNC_RATE	This sets the number of clock cycles before the sync pattern repeats. This depends if the audio port data is mono or stereo.	
		In MONO mode:	
		SYNC_RATE	Number of Clock Cycles
		000	8
		001	12
		010	16
		011	18
		100	20
		101	24
		110	25
		111	32
		In STEREO mode:	
		SYNC_RATE	Number of Clock Cycles
		000	16
		001	24
		010	32
		011	36
		100	40
		101	48
		110	50
		111	64
5:3	SYNC_WIDTH	In MONO mode, this programs the width (in number of bits) of the SYNC signal.	
		SYNC_WIDTH	Width of SYNC (in bits)
		000	1
		001	2
		010	4
		011	7
		100	8
		101	11
		110	15
		111	16

Table 40. DATA_WIDTHS (0x54h/64h)

Bits	Field	Description	
2:0	RX_WIDTH	This programs the expected bits per word of the serial data input SDI.	
		RX_WIDTH	Bits
		000	24
		001	20
		010	18
		011	16
		100	14
		101	13
		110	12
		111	8

Copyright © 2009–2013, Texas Instruments Incorporated

Table 40. DATA_WIDTHS (0x54h/64h) (continued)

Bits	Field	Description	
5:3	TX_WIDTH	This programs the bits per word of the serial data output SDO.	
		TX_WIDTH	Description
		000	24
		001	20
		010	18
		011	16
		100	14
		101	13
		110	12
		111	8
7:6	TX_EXTRA_BITS	This programs the TX data output padding.	
		TX_EXTRA_BITS	Description
		00	0
		01	1
		10	High-Z
		11	High-Z

Table 41. RX_MODE (0x55h/x65h)

Bits	Field	Description	
0	RX_MODE	This sets the RX data input justification with respect to the SYNC signal.	
		RX_MODE	Description
		0	MSB Justified
		1	LSB Justified

Copyright © 2009–2013, Texas Instruments Incorporated

Table 41. RX_MODE (0x55h/x65h) (continued)

Bits	Field	Description	
5:1	MSB_POSITION	This specifies the bit location of the MSB from the start of the frame (MSB Justified) or from the end of the frame (LSB Justified).	
		MSB_POSITION	Description
		00000	0(Left Justified/PCM Long)
		00001	1(I^2S/PCM Short)
		00010	2
		00011	3
		00100	4
		00101	5
		00110	6
		00111	7
		01000	8
		01001	9
		01010	10
		01011	11
		01100	12
		01101	13
		01110	14
		01111	15
		10000	16
		10001	17
		10010	18
		10011	19
		10100	20
		10101	21
		10110	22
		10111	23
		11000	24
		11001	25
		11010	26
		11011	27
		11100	28
		11101	29
		11110	30
		11111	31
6	COMPAND	If set, audio data will be companded.	
7	µLaw/A-Law	This sets the audio companding mode.	
		µLaw/A-Law	Compand Mode
		0	µLaw
		1	A-Law

Table 42. TX_MODE (0x56h/x66h)

Bits	Field	Description	
0	TX_MODE	This sets the TX data output justification with respect to the SYNC signal.	
		TX_MODE	Description
		0	MSB Justified
		1	LSB Justified

Copyright © 2009–2013, Texas Instruments Incorporated

Table 42. TX_MODE (0x56h/x66h) (continued)

Bits	Field	Description	
5:1	MSB_POSITION	This specifies the bit location of the MSB from the start of the frame (MSB Justified) or from the end of the frame (LSB Justified).	
		MSB_POSITION	Description
		00000	0(Left Justified/PCM Long)
		00001	1(I^2S/PCM Short)
		00010	2
		00011	3
		00100	4
		00101	5
		00110	6
		00111	7
		01000	8
		01001	9
		01010	10
		01011	11
		01100	12
		01101	13
		01110	14
		01111	15
		10000	16
		10001	17
		10010	18
		10011	19
		10100	20
		10101	21
		10110	22
		10111	23
		11000	24
		11001	25
		11010	26
		11011	27
		11100	28
		11101	29
		11110	30
		11111	31
6	COMPAND	If set, audio data will be companded.	
7	µLaw/A-Law	This sets the audio companding mode.	
		µLaw/A-Law	Compand Mode
		0	µLaw
		1	A-Law

Copyright © 2009–2013, Texas Instruments Incorporated

Digital Effects Engine

Digital Signal Processor (DSP)

The LM49352 is designed to handle the entire audio signal conditioning and processing within the audio system, thereby freeing up the workload of any other applications processor contained within the system. The LM49352 features two independent DSPs, one for the DAC and the other for the ADC. Each DSP is fully featured and performs as a professional quality digital audio effects engine. Both DSP engines feature digital volume control, automatic level control (ALC), digital soft clip compression, and a 5-band parametric EQ. The effects chain of each DSP engine is shown by the diagrams below.

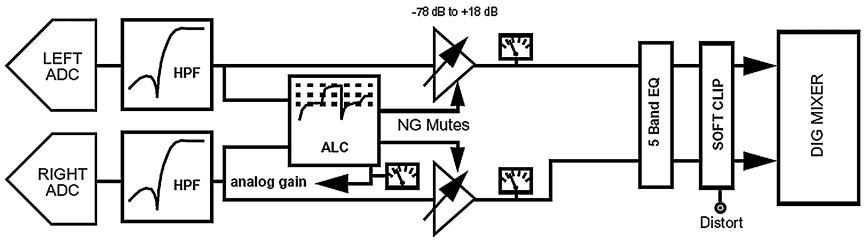


Figure 66. ADC DSP Effects Chain

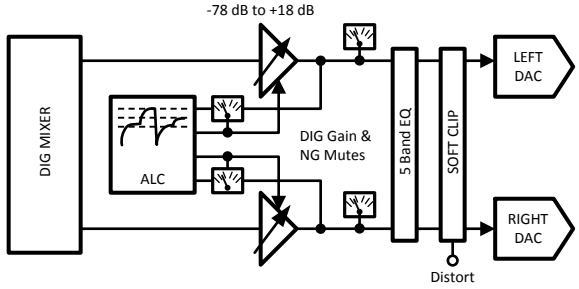


Figure 67. DAC DSP Effects Chain

The ADC and DAC DSP engines can be cascaded together in any order via the digital mixer to combine different audio effects to the same signal path. For example, a signal can be processed with high-pass filtering from the ADC effects engine with ALC from the DAC effects engine. The 5-band parametric EQs from each DSP engine can be combined to form a single 10-band parametric EQ or a single 5-band parametric EQ with ±30dB (instead of ±15dB) gain control for each band.

Table 43. ADC EFFECTS (0x70h)

Bits	Field	Description
0	ADC_HPF_ENB	This enables the ADC's High Pass Filter.
1	ADC_ALC_ENB	This enables the ADC's Automatic Level Control.
2	ADC_PK_ENB	This enables the ADC's Peak Detector.
3	ADC_EQ_ENB	This enables the ADC's 5-band Parametric EQ.
4	ADC_SCLP_ENB	This enables the ADC's Soft Clip Feature.

Table 44. DAC EFFECTS (0x71h)

Bits	Field	Description
0	DAC_ALC_ENB	This enables the DAC's Automatic Level Control.
1	DAC_PK_ENB	This enables the DAC's Peak Detector.

Copyright © 2009–2013, Texas Instruments Incorporated

Table 44. DAC EFFECTS (0x71h) (continued)

Bits	Field	Description
2	DAC_EQ_ENB	This enables the DAC's 5-band Parametric EQ.
3	RSVD	Reserved
4	ADC_SCLP_ENB	This enables the DAC's Soft Clip Feature.

Table 45. HPF MODE (0x80h)

Bits	Field	Description		
2:0	HPF_MODE	This configures the ADC's High Pass Filter (HPF). To calculate the –3dB cutoff frequency, multiply the coefficient by the sample rate (Hz): $f_C = X_n.f_{S(Hz)}$		
		HPF_MODE	Coefficient	Filter Characteristics
				f_C = 220Hz for:
		000	X_0 = 0.0275	8kHz Voice
		001	X_1 = 0.01833	12kHz Voice
		010	X_2 = 0.01375	16kHz Voice
		011	X_3 = 0.009166	24kHz Voice
		100	X_4 = 0.006875	32kHz Voice
				f_C = 100Hz for:
		101	X_5 = 0.003125	32kHz Audio
		110	X_6 = 0.0020833	48kHz Audio
				f_C = 150Hz for:
		111	X_7 = 0.0015625	96kHz Audio

ALC Overview

The Automatic Level Control (ALC) system can be used to regulate the audio output level to a user defined target level. The ALC feature is especially useful whenever the level of the audio input is unknown, unpredictable, or has a large dynamic range. The main purpose of the ALC is to optimize the dynamic range of the audio input to audio output path.

There are two separate and independent ALC circuits in the LM49352. One of the ALC circuits is located within the DAC DSP effects block. The other ALC circuit is integrated into the ADC DSP effects block. The DAC ALC controls the DAC digital gain. The ADC ALC controls the mono/auxiliary input amplifier gain or microphone preamplifier gain. The dual ALCs can be used to regulate the level of the analog (AUX, MONO, MIC) and digital (Port1 Data In, Port2 Data In) audio inputs. The ALC regulated output can be routed to any of the LM49352's amplifier outputs for playback. The ALC regulated output can also be routed to Audio Port1 or Audio Port2 for digital data transmission via I^2S or PCM.

Only audio inputs that are considered signals (rather than noise) are sent to the ALC's peak detector block. The peak detector compares the level of the audio input versus the ALC target level (TARGET_LEVEL). Signals lower than the target level will be amplified and signals higher than the target level will be attenuated. Any audio input that is lower than the level specified by the noise floor level (NOISE_FLOOR) will be considered as noise and will be gated from the ALC's peak detector in order to avoid noise pumping. So it is important to set NOISE_FLOOR to correlate with the signal to noise ratio of the corresponding audio path. In some instances (ie. Conference calls), it may be desirable to mute audio input signals that consist solely of background noise from the audio output. This is accomplished by enabling the ALC's noise gate (NG_ENB). When the noise gate is enabled, signals lower than the noise floor level will be muted from the audio output.

If the audio input signal is below the target level, the ALC will increase the gain of the corresponding volume control until the signal reaches the target level. The rate at which the ALC performs gain increases is known as decay rate (DECAY RATE). But before each ALC gain increase the ALC must wait a predetermined amount of time (HOLD TIME). If the audio input signal is above the target level, the ALC will decrease the gain of the corresponding volume control until the signal reaches the target level. The rate at which the ALC performs attenuation is known as attack rate (ATTACK RATE). The ALC's peak detector tracks increases in audio input

Copyright © 2009–2013, Texas Instruments Incorporated

signal amplitude instantaneously, but tracks decreases in audio input signal amplitude at programmable rate (PEAK DECAY TIME). ATTACK RATE, DECAY RATE, HOLD TIME, and PEAK DECAY TIME are fully adjustable which allows flexible operation of the ALC circuit. The ALC's timers are based on the sample rate of the DAC or ADC, so the closest corresponding sample rate must be programmed into the DAC SAMPLE setting (for DAC ALC) or the ADC SAMPLE (for ADC ALC).

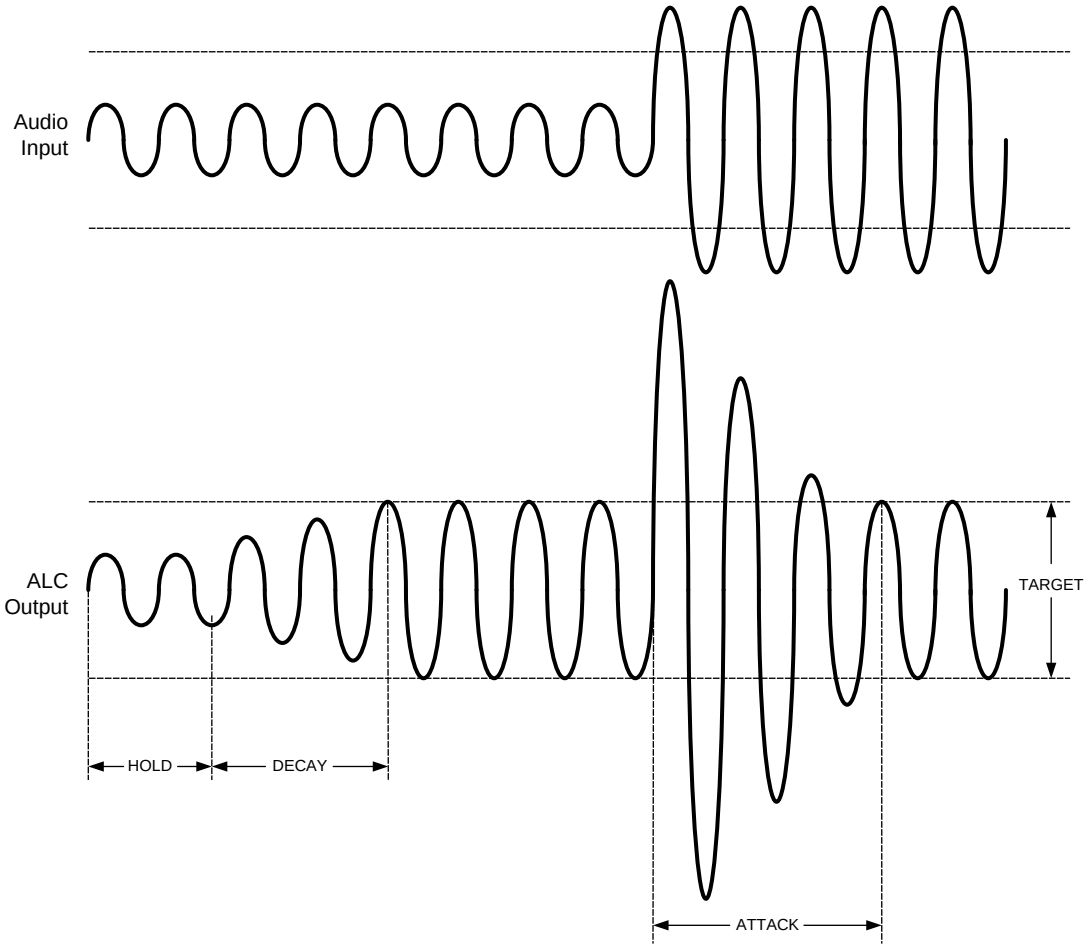


Figure 68. ALC Example

Limiter

The LM49352's ALC features a limiter function. The purpose of the limiter is to limit the maximum level of the audio signal to the specified ALC target level. When the limiter is enabled, the ALC will decrease the gain of the volume control whenever the audio signal is higher than the specified target level. The programmed I^2C gain setting when the limiter is first enabled is the maximum gain setting that the ALC limiter will apply to the audio signal. Gain increases beyond the original I^2C gain setting are disabled. This is in contrast to ALC operation with the limiter disabled, where the ALC may increase gain of audio signals below target level using gain settings beyond the original I^2C gain setting. Therefore, it is important to set the gain of the audio path to the desired setting before enabling the ALC limiter function.

The limiter's target level can be set just below the clipping level of the output amplifier or ADC in order to prevent harsh distortions delivered to the loudspeaker or headphone on the receiving end. This method of ALC limiter operation is also known as "no clip" mode. Operating the ALC limiter in "no clip" mode maximizes the dynamic range of the audio amplifier or ADC while ensuring that the audio signal will never clip. Utilizing the ALC limiter in "no clip" mode also protects the loudspeaker from damage due to harmful overdriven conditions.

Copyright © 2009–2013, Texas Instruments Incorporated

The ALC limiter's target level can also be set for a predetermined maximum output power or voltage level. This method of ALC limiter operation is known as "power limit" mode. Operating the ALC limiter in "power limit" mode prevents the speaker or headphone from playing at unsafe hearing levels that can permanently damage the end user's ears. "Power limit" operation is especially useful for applications such as listening to music through a set of headphones. Another benefit of using the ALC limit in "power limit" mode is to extend battery life by reducing power consumption of the output amplifiers during audio playback.

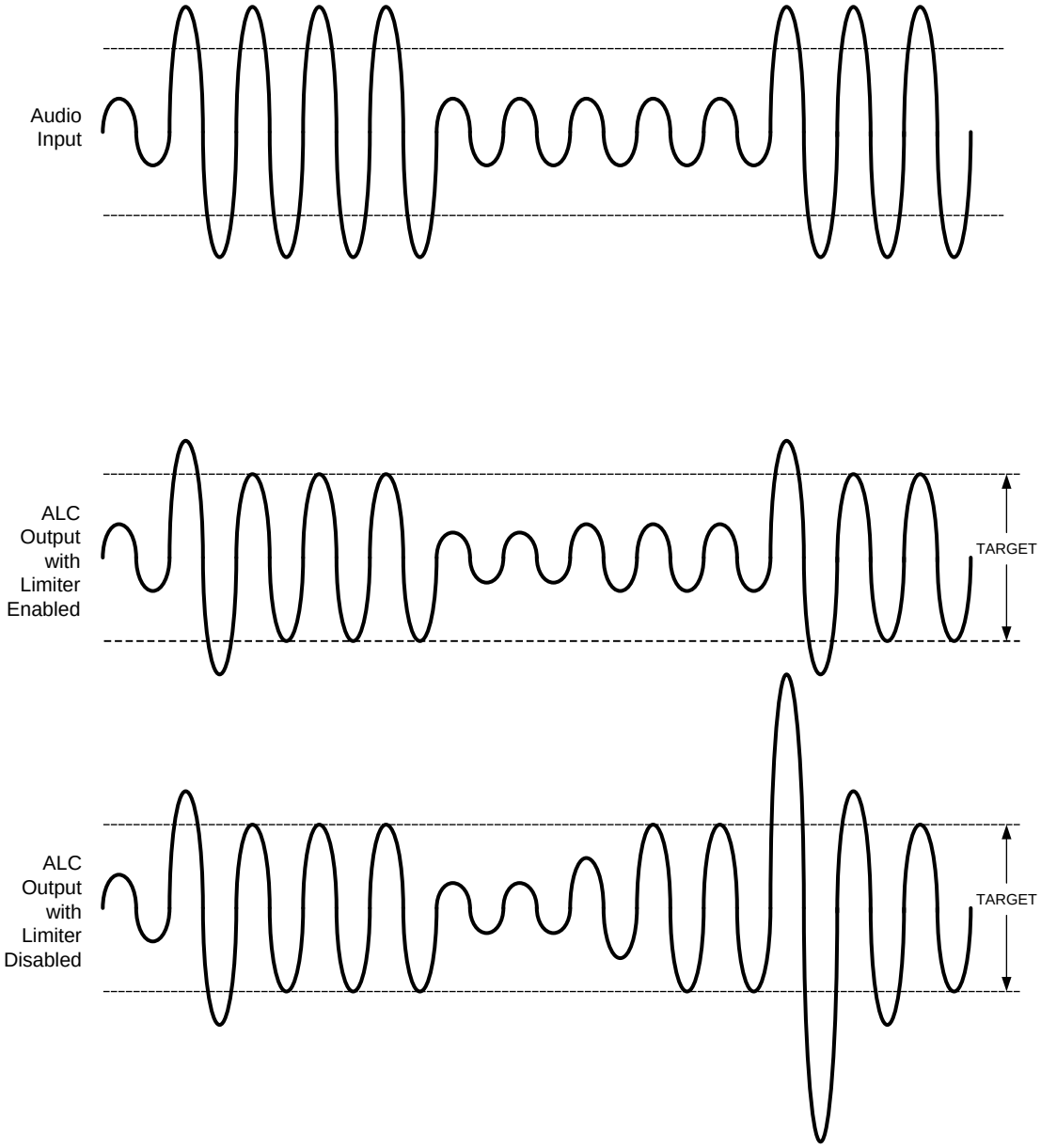


Figure 69. ALC Limiter

Copyright © 2009–2013, Texas Instruments Incorporated

Table 46. ADC_ALC_1 (0x81h)

Bits	Field	Description	
2:0	ADC_SAMPLE	This programs the timers on the ALC with the closest sample rate of the ADC.	
		ADC_SAMPLE	Expected ADC f_S
		000	8kHz
		001	12kHz
		010	16kHz
		011	24kHz
		100	32kHz
		101	48kHz
		110	96kHz
		111	192kHz
3	LIMITER	If set, the circuit will never apply gain to the signal, no matter how small, but it will attenuate the signal as soon as it reaches target and release it at the decay rate, once signal level reduces below target. The I^2C gain setting (at the time the LIMITER is enabled) is the maximum gain that the ALC will apply. Care should be taken when choosing the optimum I^2C gain setting whenever enabling the Limiter.	
4	STEREO LINK	If set, the ALC circuit uses the stereo average of the input signals to control the gain of the stereo output. This maintains stereo imaging. If this bit is cleared, then both channels operate as dual mono.	
5	SOURCE_RSEL	If both SOURCE_OVR and this bit is set, the right ADC ALC channel will be active.	
6	SOURCE_LSEL	If both SOURCE_OVR and this bit is set, the left ADC ALC channel will be active.	
7	SOURCE_OVR	If set, the active channel of the ADC ALC is determined by SOURCE_RSEL and SOURCE_LSEL. If cleared, the active channel of the ADC ALC is determined by the selected input to the ADC. MONO enables left ALC, AUX enables right ALC, MIC enables left and / or right ALC depending on which ADC channel MIC is selected to.	

Table 47. ADC_ALC_2 (0x82h)

Bits	Field	Description	
3:0	NOISE_FLOOR	This sets the anticipated noise floor. Signals lower than the noise floor specified will be gated from the ALC to avoid noise pumping.	
		NOISE_FLOOR	Noise Floor (dB)
		0000	–39
		0001	–42
		0010	–45
		0011	–48
		0100	–51
		0101	–54
		0110	–57
		0111	–60
		1000	–63
		1001	–66
		1010	–69
		1011	–72
		1100	–75
		1101	–78
		1110	–81
		1111	–84
4	NG_ENB	This enables the Noise Gate.	

Copyright © 2009–2013, Texas Instruments Incorporated

Table 48. ADC_ALC_3 (0x83h)

Bits	Field	Description	
4:0	TARGET_LEVEL	This sets the desired target output level. Signals lower than this will be amplified and signals larger than this will be attenuated.	
		TARGET_LEVEL	Target Level (dB)
		00000	–1.5
		00001	–3
		00010	–4.5
		00011	–6
		00100	–7.5
		00101	–9
		00110	–10.5
		00111	–12
		01000	–13.5
		01001	–15
		01010	–16.5
		01011	–18
		01100	–19.5
		01101	–21
		01110	–22.5
		01111	–24
		10000	–25.5
		10001	–27
		10010	–28.5
		10011	–30
		10100	–31.5
		10101	–33
		10110	–34.5
		10111	–36
		11000	–37.5
		11001	–39
		11010	–40.5
		11011	–42
		11100	–43.5
		11101	–45
		11110	–46.5
		11111	–48

Copyright © 2009–2013, Texas Instruments Incorporated

Table 49. ADC_ALC_4 (0x84h)

Bits	Field	Description	
4:0	ATTACK_RATE	This sets the rate at which the ALC will reduce gain if it detects the input signal is large.	
		ATTACK_RATE	Time between gain steps (µs)
		00000	21
		00001	42
		00010	83
		00011	167
		00100	250
		00101	333
		00110	417
		00111	542
		01000	729
		01001	958
		01010	1250 (Default)
		01011	1604
		01100	1896
		01101	2208
		01110	2792
		01111	3708
		10000	4792
		10001	5688
		10010	6563
		10011	8396
		10100	11000
		10101	14167
		10110	17083
		10111	20000
		11000	25000
		11001	32000
		11010	45000
		11011	60000
		11100	75000
		11101	87500
		11110	100000
		11111	114583

Copyright © 2009–2013, Texas Instruments Incorporated

Table 50. ADC_ALC_5 (0x85h)

Bits	Field	Description	
4:0	DECAY_RATE	This sets the rate at which the ALC will increase gain if it detects the input signal is too small.	
		DECAY_RATE	Time between gain steps (µs)
		00000	104
		00001	125
		00010	167
		00011	250
		00100	292
		00101	396
		00110	500
		00111	708
		01000	896
		01001	1250
		01010	1396 (Default)
		01011	2000
		01100	2708
		01101	3500
		01110	4750
		01111	6250
		10000	8000
		10001	11000
		10010	14000
		10011	18500
		10100	25000
		10101	32000
		10110	42000
		10111	55000
		11000	72500
		11001	100000
		11010	125000
		11011	160000
		11100	225000
		11101	300000
		11110	375000
		11111	500000 (0.5s)
7:5	PK_DECAY_RATE	PK_DECAY_RATE	Max Time to track decay
		000	1.3ms (Default)
		001	2.6ms
		010	5.3ms
		011	10.6ms
		100	21.3ms
		101	42.6.3ms
		110	85.5ms
		111	2.73 secs

Copyright © 2009–2013, Texas Instruments Incorporated

Table 51. ADC_ALC_6 (0x86h)

Bits	Field	Description	
4:0	HOLD_TIME	This sets how long the ALC circuit waits before increasing the gain.	
		HOLD_TIME	Time (ms)
		00000	1
		00001	1.25
		00010	1.6
		00011	2
		00100	2.5
		00101	3.2
		00110	4
		00111	5
		01000	6.25
		01001	8
		01010	10 (Default)
		01011	12.5
		01100	16
		01101	20
		01110	25
		01111	32
		10000	40
		10001	50
		10010	64
		10011	80
		10100	100
		10101	125
		10110	160
		10111	200
		11000	250
		11001	320
		11010	400
		11011	500
		11100	640
		11101	800
		11110	1000
		11111	1250

Table 52. ADC_ALC_7 (0x87h)

Bits	Field	Description
5:0	MAX_LEVEL	This sets the maximum allowed gain of the volume control to the output amplifier whenever the ALC is use. If the volume control is less than 6 bits the relevant LSBs are used as the limit and the MSBs are ignored.

Table 53. ADC_ALC_8 (0x88h)

Bits	Field	Description
5:0	MIN_LEVEL	This sets the minimum allowed gain of the volume control to the output amplifier whenever the ALC is use. If the volume control is less than 6 bits the relevant LSBs are used as the limit and the MSBs are ignored.

Copyright © 2009–2013, Texas Instruments Incorporated

Table 54. ADC_L_LEVEL (0x89h)

Bits	Field	Description			
5:0	ADC_L_LEVEL	This sets the post ADC digital gain of the left channel.			
		ADC_L_LEVEL	Level	ADC_L_LEVEL	Level
		000000	-76.5dB	100000	-28.5dB
		000001	-75dB	100001	-27dB
		000010	-73.5dB	100010	-25.5dB
		000011	-72dB	100011	-24dB
		000100	-70.5dB	100100	-22.5dB
		000101	-69dB	100101	-21dB
		000110	-67.5dB	100110	-20.5dB
		000111	-66dB	100111	-18dB
		001000	-64.5dB	101000	-16.5dB
		001001	-63dB	101001	-15dB
		001010	-61.5dB	101010	-13.5dB
		001011	-60dB	101011	-12dB
		001100	-58.5dB	101100	-10.5dB
		001101	-57dB	101101	-9dB
		001110	-55.5dB	101110	-7.5dB
		001111	-54dB	101111	-6dB
		010000	-52.5dB	110000	-4.5dB
		010001	-51dB	110001	-3dB
		010010	-49.5dB	110010	-1.5dB
		010011	-48dB	110011	0dB
		010100	-46.5dB	110100	1.5dB
		010101	-45dB	110101	3dB
		010110	-43.5dB	110110	4.5dB
		010111	-42dB	110111	6dB
		011000	-40.5dB	111000	7.5dB
		011001	-39dB	111001	9dB
		011010	-37.5dB	111010	10.5dB
		011011	-36dB	111011	12dB
		011100	-34.5dB	111100	13.5dB
		011101	-33dB	111101	15dB
		011110	-31.5dB	111110	16.5dB
		011111	-30dB	111111	18dB
6	STEREO_LINK	If set, this links the ADC_R_LEVEL with ADC_L_LEVEL.			

Copyright © 2009–2013, Texas Instruments Incorporated

Table 55. ADC_R_LEVEL (0x8Ah)

Bits	Field	Description			
5:0	ADC_R_LEVEL	This sets the post ADC digital gain of the right channel.			
		ADC_R_LEVEL	Level	ADC_R_LEVEL	Level
		000000	-76.5dB	100000	-28.5dB
		000001	-75dB	100001	-27dB
		000010	-73.5dB	100010	-25.5dB
		000011	-72dB	100011	-24dB
		000100	-70.5dB	100100	-22.5dB
		000101	-69dB	100101	-21dB
		000110	-67.5dB	100110	-20.5dB
		000111	-66dB	100111	-18dB
		001000	-64.5dB	101000	-16.5dB
		001001	-63dB	101001	-15dB
		001010	-61.5dB	101010	-13.5dB
		001011	-60dB	101011	-12dB
		001100	-58.5dB	101100	-10.5dB
		001101	-57dB	101101	-9dB
		001110	-55.5dB	101110	-7.5dB
		001111	-54dB	101111	-6dB
		010000	-52.5dB	110000	-4.5dB
		010001	-51dB	110001	-3dB
		010010	-49.5dB	110010	-1.5dB
		010011	-48dB	110011	0dB
		010100	-46.5dB	110100	1.5dB
		010101	-45dB	110101	3dB
		010110	-43.5dB	110110	4.5dB
		010111	-42dB	110111	6dB
		011000	-40.5dB	111000	7.5dB
		011001	-39dB	111001	9dB
		011010	-37.5dB	111010	10.5dB
		011011	-36dB	111011	12dB
		011100	-34.5dB	111100	13.5dB
		011101	-33dB	111101	15dB
		011110	-31.5dB	111110	16.5dB
		011111	-30dB	111111	18dB

Table 56. EQ_BAND_1 (0x8Bh)

Bits	Field	Description	
1:0	FREQ	This sets the Sub-bass shelving filter's cut-off frequency. The cut-off frequencies shown are based on a 48kHz sample rate. Using lower sample rates will scale down the cut-off frequencies proportionately.	
		FREQ	Frequency (Hz)
		00	60
		01	80
		10	100
		11	120

Copyright © 2009–2013, Texas Instruments Incorporated

Table 56. EQ_BAND_1 (0x8Bh) (continued)

Bits	Field	Description	
6:2	LEVEL	This sets the gain at f_C.	
		LEVEL	Effect
		00000	Off (0dB)
		00001	-15dB
		00010	-14dB
		00011	-13dB
		00100	-12dB
		00101	-11dB
		00110	-10dB
		00111	-9dB
		01000	-8dB
		01001	-7dB
		01010	-6dB
		01011	-5dB
		01100	-4dB
		01101	-3dB
		01110	-2dB
		01111	-1dB
		10000	0dB
		10001	1dB
		10010	2dB
		10011	3dB
		10100	4dB
		10101	5dB
		10110	6dB
		10111	7dB
		11000	8dB
		11001	9dB
		11010	10dB
		11011	11dB
		11100	12dB
		11101	13dB
		11110	14dB
		11111	15dB

Table 57. EQ_BAND_2 (0x8Ch)

Bits	Field	Description	
1:0	FREQ	This sets the Bass peak filter's center frequency. The cut-off frequencies shown are based on a 48kHz sample rate. Using lower sample rates will scale down the cut-off frequencies proportionately.	
		FREQ	Frequency (Hz)
		00	150
		01	200
		10	250
		11	300

Copyright © 2009–2013, Texas Instruments Incorporated

Table 57. EQ_BAND_2 (0x8Ch) (continued)

Bits	Field	Description	
6:2	LEVEL	This sets the gain at f_C.	
		LEVEL	Effect
		00000	Off (0dB)
		00001	-15dB
		00010	-14dB
		00011	-13dB
		00100	-12dB
		00101	-11dB
		00110	-10dB
		00111	-9dB
		01000	-8dB
		01001	-7dB
		01010	-6dB
		01011	-5dB
		01100	-4dB
		01101	-3dB
		01110	-2dB
		01111	-1dB
		10000	0dB
		10001	1dB
		10010	2dB
		10011	3dB
		10100	4dB
		10101	5dB
		10110	6dB
		10111	7dB
		11000	8dB
		11001	9dB
		11010	10dB
		11011	11dB
		11100	12dB
		11101	13dB
		11110	14dB
		11111	15dB
7	Q	Programs the width of the peak filter.	
		Q	Bandwidth
		0	2/3 Octave
		1	4/3 Octave

Copyright © 2009–2013, Texas Instruments Incorporated

Table 58. EQ_BAND_3 (0x8Dh)

Bits	Field	Description	
1:0	FREQ	This sets the Mid peak filter's center frequency. The cut-off frequencies shown are based on a 48kHz sample rate. Using lower sample rates will scale down the cut-off frequencies proportionately.	
		FREQ	Frequency (Hz)
		00	600
		01	800
		10	1k
		11	1.2k
6:2	LEVEL	This sets the gain at f_C.	
		LEVEL	Effect
		00000	Off (0dB)
		00001	-15dB
		00010	-14dB
		00011	-13dB
		00100	-12dB
		00101	-11dB
		00110	-10dB
		00111	-9dB
		01000	-8dB
		01001	-7dB
		01010	-6dB
		01011	-5dB
		01100	-4dB
		01101	-3dB
		01110	-2dB
		01111	-1dB
		10000	0dB
		10001	1dB
		10010	2dB
		10011	3dB
		10100	4dB
		10101	5dB
		10110	6dB
		10111	7dB
		11000	8dB
		11001	9dB
		11010	10dB
		11011	11dB
		11100	12dB
		11101	13dB
		11110	14dB
		11111	15dB
7	Q	This programs the width of the peak filter.	
		Q	Bandwidth
		0	2/3 Octave
		1	4/3 Octave

Copyright © 2009–2013, Texas Instruments Incorporated

Table 59. EQ_BAND_4 (0x8Eh)

Bits	Field	Description	
1:0	FREQ	This sets the Treble peak filter's center frequency. The cut-off frequencies shown are based on a 48kHz sample rate. Using lower sample rates will scale down the cut-off frequencies proportionately.	
		FREQ	Frequency (Hz)
		00	2k
		01	2.7k
		10	3.4k
		11	4.1k
6:2	LEVEL	This sets the gain at f_C.	
		LEVEL	Effect
		00000	Off (0dB)
		00001	-15dB
		00010	-14dB
		00011	-13dB
		00100	-12dB
		00101	-11dB
		00110	-10dB
		00111	-9dB
		01000	-8dB
		01001	-7dB
		01010	-6dB
		01011	-5dB
		01100	-4dB
		01101	-3dB
		01110	-2dB
		01111	-1dB
		10000	0dB
		10001	1dB
		10010	2dB
		10011	3dB
		10100	4dB
		10101	5dB
		10110	6dB
		10111	7dB
		11000	8dB
		11001	9dB
		11010	10dB
		11011	11dB
		11100	12dB
		11101	13dB
		11110	14dB
		11111	15dB
7	Q	This programs the width of the peak filter.	
		Q	Bandwidth
		0	2/3 Octave
		1	4/3 Octave

Copyright © 2009–2013, Texas Instruments Incorporated

Table 60. EQ_BAND_5 (0x8Fh)

Bits	Field	Description	
1:0	FREQ	This sets the presence shelving filter's cut-off frequency. The cut-off frequencies shown are based on a 48kHz sample rate. Using lower sample rates will scale down the cut-off frequencies proportionately.	
		FREQ	Frequency (Hz)
		00	7k
		01	9k
		10	11k
		11	13k
6:2	LEVEL	This sets the gain at f_C.	
		LEVEL	Effect
		00000	Off (0dB)
		00001	-15dB
		00010	-14dB
		00011	-13dB
		00100	-12dB
		00101	-11dB
		00110	-10dB
		00111	-9dB
		01000	-8dB
		01001	-7dB
		01010	-6dB
		01011	-5dB
		01100	-4dB
		01101	-3dB
		01110	-2dB
		01111	-1dB
		10000	0dB
		10001	1dB
		10010	2dB
		10011	3dB
		10100	4dB
		10101	5dB
		10110	6dB
		10111	7dB
		11000	8dB
		11001	9dB
		11010	10dB
		11011	11dB
		11100	12dB
		11101	13dB
		11110	14dB
		11111	15dB

Copyright © 2009–2013, Texas Instruments Incorporated

Digital Audio Compressor

The LM49352 features a digital audio compressor on both the DAC and ADC paths. The compressor works by reducing the level of the audio signal that is higher than the level set by the audio compressor threshold level (THRESHOLD) by a fixed ratio (compressor output / compressor input) that is set by a predetermined audio compression ratio (RATIO). Higher compression ratios result in more compression as shown in Figure 70. The audio compressor can be used in conjunction with the ALC to limit audio peaks that the ALC may not be fast enough to react to.

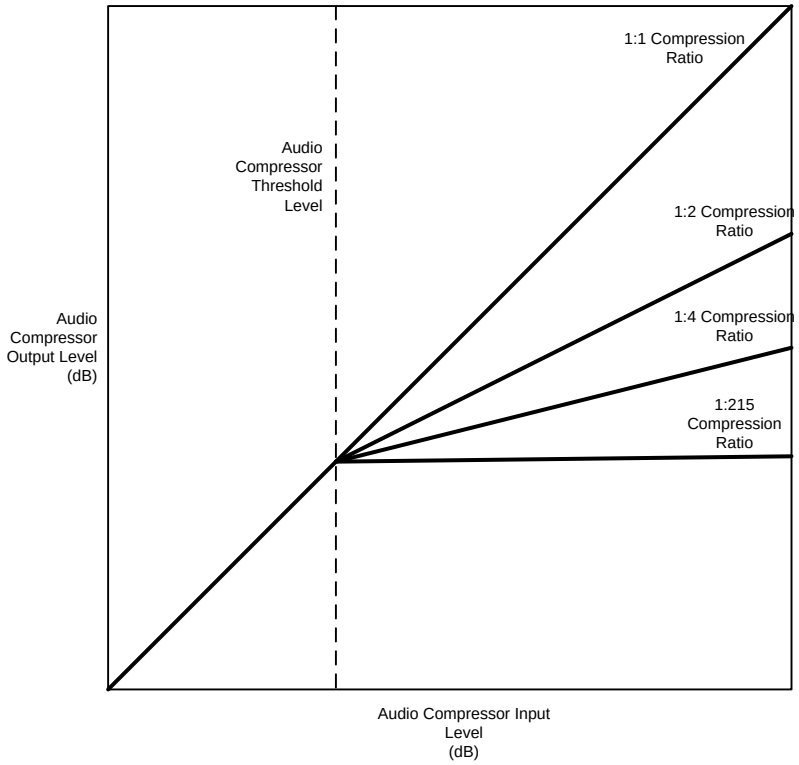


Figure 70. Audio Compressor Effect

Soft Knee Function

The LM49352's audio compressor also features a soft knee function that smooths the harsh edges found during clipping of an audio signal. For audio signals higher than the compressor threshold level, the soft knee function gradually increases the compression ratio for increasing levels of audio signal beyond the compressor threshold. To achieve the smoothing effect to prevent hard clipping, the soft knee function initially compresses the audio signal at the smallest ratio and then incrementally increases the compression ratio if required. The highest level of compression applied by the soft knee function is set by the compressor ratio. The effect of the soft knee function is shown in Figure 71.

Copyright © 2009–2013, Texas Instruments Incorporated

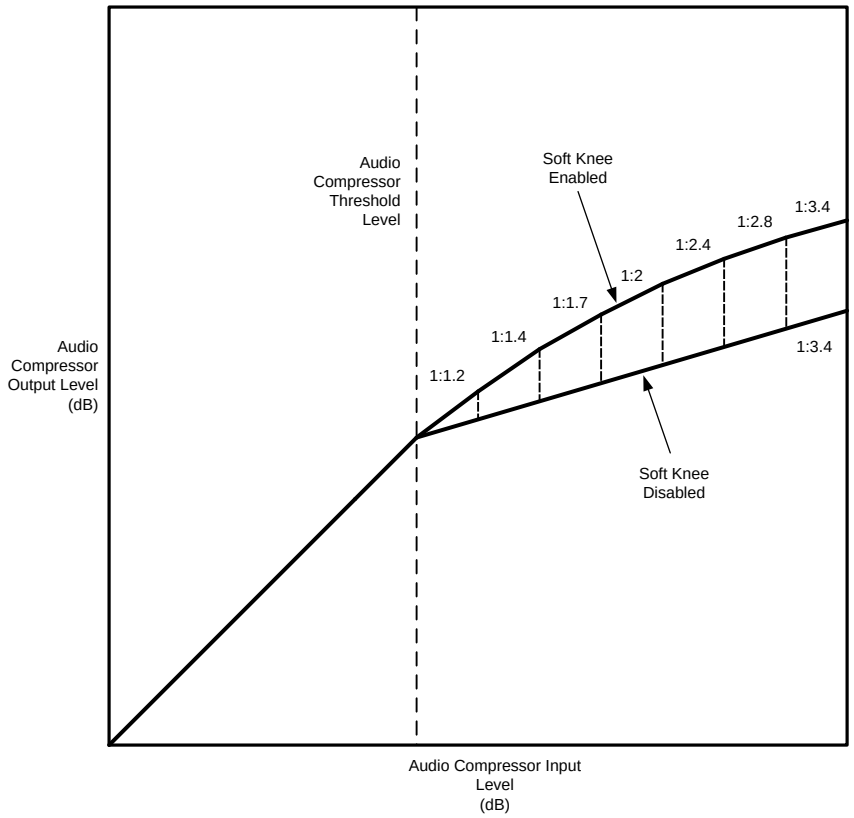


Figure 71. Soft Knee Example with Compression Ratio Setting of 1:3.4

Table 61. SOFTCLIP1 (0x90h)

Bits	Field	Description	
3:0	THRESHOLD	This sets the threshold level of the audio compressor. Audio signals above the threshold will be compressed.	
		THRESHOLD	Threshold Level (dB)
		0000	-36dB
		0001	-30dB
		0010	-24dB
		0011	-20dB
		0100	-18dB
		0101	-17dB
		0110	-16dB
		0111	-15dB
		1000	-14dB
		1001	-12dB
		1010	-10dB
		1011	-8dB
		1100	-6dB
		1101	-4dB
		1110	-2.5dB
		1111	-1dB

Copyright © 2009–2013, Texas Instruments Incorporated

Table 61. SOFTCLIP1 (0x90h) (continued)

Bits	Field	Description
4	SOFT_KNEE	If set, the audio compressor will automatically apply higher compression ratios to audio signals higher than the threshold level. As the audio signal approaches levels higher than the threshold, SOFT_KNEE will increase the compression RATIO. The highest compression that the SOFT_KNEE algorithm will apply is the compression that is set by RATIO.

Table 62. SOFTCLIP2 (0x91h)

Bits	Field	Description	
4:0	RATIO	This sets the ratio at which the audio is compressed to when it passes beyond the threshold. In SOFT_KNEE mode this is the final level of compression.	
		RATIO	Ratio
		00000	1:1 (Bypass)
		00001	1:1.2
		00010	1:1.4
		00011	1:1.7
		00100	1:2.0
		00101	1:2.4
		00110	1:2.8
		00111	1:3.4
		01000	1:4.0
		01001	1:4.7
		01010	1:5.7
		01011	1:6.7
		01100	1:8.0
		01101	1:9.5
		01110	1:11.3
		01111	1:13.5
		10000	1:16.0
		10001	1:19.0
		10010	1:22.8
		10011	1:27.0
		10100	1:32.0
		10101	1:37.9
		10110	1:45.5
		10111	1:53.9
		11000	1:64.0
		11001	1:75.0
		11010	1:91.0
		11011	1:108
		11100	1:128
		11101	1:152
		11110	1:182
		11111	1:215

Copyright © 2009–2013, Texas Instruments Incorporated

Table 63. SOFTCLIP3 (0x92h)

Bits	Field	Description	
3:0	LEVEL	This sets the post compressor gain level.	
		LEVEL	Level (dB)
		00000	-22.5dB
		00001	-21dB
		00010	-19.5dB
		00011	-18dB
		00100	-16.5dB
		00101	-15dB
		00110	-13.5dB
		00111	-12dB
		01000	-10.5dB
		01001	-9dB
		01010	-7.5dB
		01011	-6dB
		01100	-4.5dB
		01101	-3dB
		01110	-1.5dB
		01111	0dB
		10000	1.5dB
		10001	3dB
		10010	4.5dB
		10011	6dB
		10100	7.5dB
		10101	9dB
		10110	10.5dB
		10111	12dB
		11000	13.5dB
		11001	15dB
		11010	16.5dB
		11011	18dB
		11100	19.5dB
		11101	21dB
		11110	22.5dB
		11111	24dB

Copyright © 2009–2013, Texas Instruments Incorporated

DAC Effects Registers

Table 64. DAC_ALC_1 (0xA0h)

Bits	Field	Description	
2:0	DAC_SAMPLE	This programs the timers on the ALC with the closest DAC sample rate.	
		DAC_SAMPLE	Expected DAC f_S
		000	8kHz
		001	12kHz
		010	16kHz
		011	24kHz
		100	32kHz
		101	48kHz
		110	96kHz
		111	192kHz
3	LIMITER	If set, the circuit will never apply gain to the signal, no matter how small, but it will attenuate the signal as soon as it reaches target and release it at the decay rate, once signal level reduces below target. The I^2C gain setting (at the time the LIMITER is enabled) is the maximum gain that the ALC will apply. Care should be taken when choosing the optimum I^2C gain setting whenever enabling the Limiter.	
4	STEREO LINK	If set, the ALC circuit uses the stereo average of the input signals to control the gain of the stereo output. This maintains stereo imaging. If this bit is cleared, then both channels operate as dual mono.	

Table 65. DAC_ALC_2 (0xA1h)

Bits	Field	Description	
3:0	NOISE_FLOOR	This sets the anticipated noise floor. Signals lower than the specified noise floor will be gated from the ALC to avoid noise pumping.	
		NOISE_FLOOR	Noise Floor (dB)
		0000	-39
		0001	-42
		0010	-45
		0011	-48
		0100	-51
		0101	-54
		0110	-57
		0111	-60
		1000	-63
		1001	-66
		1010	-69
		1011	-72
		1100	-75
		1101	-78
		1110	-81
		1111	-84
4	NG_ENB	This enables the Noise Gate	

Copyright © 2009–2013, Texas Instruments Incorporated

Table 66. DAC_ALC_3 (0xA2h)

Bits	Field	Description	
4:0	TARGET_LEVEL	This sets the desired output level. Signals lower than this will be amplified and signals larger than this will be attenuated.	
		TARGET_LEVEL	Target Level (dB)
		00000	-1.5
		00001	-3
		00010	-4.5
		00011	-6
		00100	-7.5
		00101	-9
		00110	-10.5
		00111	-12
		01000	-13.5
		01001	-15
		01010	-16.5
		01011	-18
		01100	-19.5
		01101	-21
		01110	-22.5
		01111	-24
		10000	-25.5
		10001	-27
		10010	-28.5
		10011	-30
		10100	-31.5
		10101	-33
		10110	-34.5
		10111	-36
		11000	-37.5
		11001	-39
		11010	-40.5
		11011	-42
		11100	-43.5
		11101	-45
		11110	-46.5
		11111	-48

Copyright © 2009–2013, Texas Instruments Incorporated

Table 67. DAC_ALC_4 (0xA3h)

Bits	Field	Description	
4:0	ATTACK_RATE	This sets the rate at which the ALC will reduce gain if it detects the input signal is too large.	
		ATTACK_RATE	Time between gain steps (µs)
		00000	21
		00001	42
		00010	83
		00011	167
		00100	250
		00101	333
		00110	417
		00111	542
		01000	729
		01001	958
		01010	1250 (Default)
		01011	1604
		01100	1896
		01101	2208
		01110	2792
		01111	3708
		10000	4792
		10001	5688
		10010	6563
		10011	8396
		10100	11000
		10101	14167
		10110	17083
		10111	20000
		11000	25000
		11001	32000
		11010	45000
		11011	60000
		11100	75000
		11101	87500
		11110	100000
		11111	114583

Copyright © 2009–2013, Texas Instruments Incorporated

Table 68. DAC_ALC_5 (0xA4h)

Bits	Field	Description	
4:0	DECAY_RATE	This sets the rate at which the ALC will increase gain if it detects the input signal is too small.	
		DECAY_RATE	Time between gain steps(us)
		00000	104
		00001	125
		00010	167
		00011	250
		00100	292
		00101	396
		00110	500
		00111	708
		01000	896
		01001	1250
		01010	1396 (Default)
		01011	2000
		01100	2708
		01101	3500
		01110	4750
		01111	6250
		10000	8000
		10001	11000
		10010	14000
		10011	18500
		10100	25000
		10101	32000
		10110	42000
		10111	55000
		11000	72500
		11001	100000
		11010	125000
		11011	160000
		11100	225000
		11101	300000
		11110	375000
		11111	500000 (0.5s)
7:5	PK_DECAY_RATE	This sets how precise the ALC will track amplitude reductions of the audio input. The shorter the length of time for PK_DECAY_RATE, the more responsive the ALC will be when applying gain increases whenever the audio falls below target level.	
		PK_DECAY_RATE	Time
		000	1.3ms (Default)
		001	2.6ms
		010	5.3ms
		011	10.6ms
		100	21.3ms
		101	42.6ms
		110	85.5ms
		111	2.73secs

Copyright © 2009–2013, Texas Instruments Incorporated

Table 69. DAC_ALC_6 (0xA5h)

Bits	Field	Description	
4:0	HOLD_TIME	This sets how long the ALC circuit waits before increasing the gain.	
		HOLDTIME	Time (ms)
		00000	1
		00001	1.25
		00010	1.6
		00011	2
		00100	2.5
		00101	3.2
		00110	4
		00111	5
		01000	6.25
		01001	8
		01010	10 (Default)
		01011	12.5
		01100	16
		01101	20
		01110	25
		01111	32
		10000	40
		10001	50
		10010	64
		10011	80
		10100	100
		10101	125
		10110	160
		10111	200
		11000	250
		11001	320
		11010	400
		11011	500
		11100	640
		11101	800
		11110	1000
		11111	1250

Table 70. DAC_ALC_7 (0xA6h)

Bits	Field	Description
5:0	MAX_LEVEL	This sets the maximum allowed gain to the digital level control when the ALC is used.

Table 71. DAC_ALC_8 (0xA7h)

Bits	Field	Description
5:0	MIN_LEVEL	This sets the minimum allowed gain to the digital level control when the ALC is used.

Copyright © 2009–2013, Texas Instruments Incorporated

Table 72. DAC_L_LEVEL (0xA8h)

Bits	Field	Description			
5:0	DAC_L_LEVEL	This sets the pre DAC digital gain.			
		DAC_L_LEVEL	Level	DAC_L_LEVEL	Level
		000000	-76.5dB	100000	-28.5dB
		000001	-75dB	100001	-27dB
		000010	-73.5dB	100010	-25.5dB
		000011	-72dB	100011	-24dB
		000100	-70.5dB	100100	-22.5dB
		000101	-69dB	100101	-21dB
		000110	-67.5dB	100110	-20.5dB
		000111	-66dB	100111	-18dB
		001000	-64.5dB	101000	-16.5dB
		001001	-63dB	101001	-15dB
		001010	-61.5dB	101010	-13.5dB
		001011	-60dB	101011	-12dB
		001100	-58.5dB	101100	-10.5dB
		001101	-57dB	101101	-9dB
		001110	-55.5dB	101110	-7.5dB
		001111	-54dB	101111	-6dB
		010000	-52.5dB	110000	-4.5dB
		010001	-51dB	110001	-3dB
		010010	-49.5dB	110010	-1.5dB
		010011	-48dB	110011	0dB
		010100	-46.5dB	110100	1.5dB
		010101	-45dB	110101	3dB
		010110	-43.5dB	110110	4.5dB
		010111	-42dB	110111	6dB
		011000	-40.5dB	111000	7.5dB
		011001	-39dB	111001	9dB
		011010	-37.5dB	111010	10.5dB
		011011	-36dB	111011	12dB
		011100	-34.5dB	111100	13.5dB
		011101	-33dB	111101	15dB
		011110	-31.5dB	111110	16.5dB
		011111	-30dB	111111	18dB
6	STEREO_LINK	If set, this links DAC_R_LEVEL with DAC_L_LEVEL.			

Copyright © 2009–2013, Texas Instruments Incorporated

Table 73. DAC_R_LEVEL (0xA9h)

Bits	Field	Description			
5:0	DAC_R_LEVEL	This sets the pre DAC digital gain.			
		DAC_R_LEVEL	Level	DAC_R_LEVEL	Level
		000000	-76.5dB	100000	-28.5dB
		000001	-75dB	100001	-27dB
		000010	-73.5dB	100010	-25.5dB
		000011	-72dB	100011	-24dB
		000100	-70.5dB	100100	-22.5dB
		000101	-69dB	100101	-21dB
		000110	-67.5dB	100110	-20.5dB
		000111	-66dB	100111	-18dB
		001000	-64.5dB	101000	-16.5dB
		001001	-63dB	101001	-15dB
		001010	-61.5dB	101010	-13.5dB
		001011	-60dB	101011	-12dB
		001100	-58.5dB	101100	-10.5dB
		001101	-57dB	101101	-9dB
		001110	-55.5dB	101110	-7.5dB
		001111	-54dB	101111	-6dB
		010000	-52.5dB	110000	-4.5dB
		010001	-51dB	110001	-3dB
		010010	-49.5dB	110010	-1.5dB
		010011	-48dB	110011	0dB
		010100	-46.5dB	110100	1.5dB
		010101	-45dB	110101	3dB
		010110	-43.5dB	110110	4.5dB
		010111	-42dB	110111	6dB
		011000	-40.5dB	111000	7.5dB
		011001	-39dB	111001	9dB
		011010	-37.5dB	111010	10.5dB
		011011	-36dB	111011	12dB
		011100	-34.5dB	111100	13.5dB
		011101	-33dB	111101	15dB
		011110	-31.5dB	111110	16.5dB
		011111	-30dB	111111	18dB

Table 74. EQ_BAND_1 (0xABh)

Bits	Field	Description	
1:0	FREQ	This sets the Sub-bass shelving filter's cut-off frequency. The cut-off frequencies shown are based on a 48kHz sample rate. Using lower sample rates will scale down the cut-off frequencies proportionately.	
		FREQ	Frequency (Hz)
		00	60
		01	80
		10	100
		11	120

Copyright © 2009–2013, Texas Instruments Incorporated

Table 74. EQ_BAND_1 (0xABh) (continued)

Bits	Field	Description	
6:2	LEVEL	This sets the gain at f_C.	
		LEVEL	Effect
		00000	Off (0dB)
		00001	-15dB
		00010	-14dB
		00011	-13dB
		00100	-12dB
		00101	-11dB
		00110	-10dB
		00111	-9dB
		01000	-8dB
		01001	-7dB
		01010	-6dB
		01011	-5dB
		01100	-4dB
		01101	-3dB
		01110	-2dB
		01111	-1dB
		10000	0dB
		10001	1dB
		10010	2dB
		10011	3dB
		10100	4dB
		10101	5dB
		10110	6dB
		10111	7dB
		11000	8dB
		11001	9dB
		11010	10dB
		11011	11dB
		11100	12dB
		11101	13dB
		11110	14dB
		11111	15dB

Table 75. EQ_BAND_2 (0xACh)

Bits	Field	Description	
1:0	FREQ	This sets the Bass peak filter's center frequency. The cut-off frequencies shown are based on a 48kHz sample rate. Using lower sample rates will scale down the cut-off frequencies proportionately.	
		FREQ	Frequency (Hz)
		00	150
		01	200
		10	250
		11	300

Copyright © 2009–2013, Texas Instruments Incorporated

Table 75. EQ_BAND_2 (0xACh) (continued)

Bits	Field	Description	
6:2	LEVEL	This sets the gain at f_C.	
		LEVEL	Effect
		00000	Off (0dB)
		00001	-15dB
		00010	-14dB
		00011	-13dB
		00100	-12dB
		00101	-11dB
		00110	-10dB
		00111	-9dB
		01000	-8dB
		01001	-7dB
		01010	-6dB
		01011	-5dB
		01100	-4dB
		01101	-3dB
		01110	-2dB
		01111	-1dB
		10000	0dB
		10001	1dB
		10010	2dB
		10011	3dB
		10100	4dB
		10101	5dB
		10110	6dB
		10111	7dB
		11000	8dB
		11001	9dB
		11010	10dB
		11011	11dB
		11100	12dB
		11101	13dB
		11110	14dB
		11111	15dB
7	Q	This programs the width of the peak filter.	
		Q	Bandwidth
		0	2/3 Octave
		1	4/3 Octave

Copyright © 2009–2013, Texas Instruments Incorporated

Table 76. EQ_BAND_3 (0xADh)

Bits	Field	Description	
1:0	FREQ	This sets the Mid peak filter's center frequency. The cut-off frequencies shown are based on a 48kHz sample rate. Using lower sample rates will scale down the cut-off frequencies proportionately.	
		FREQ	Frequency (Hz)
		00	600
		01	800
		10	1k
		11	1.2k
6:2	LEVEL	This sets the gain at f_C.	
		LEVEL	Effect
		00000	Off (0dB)
		00001	-15dB
		00010	-14dB
		00011	-13dB
		00100	-12dB
		00101	-11dB
		00110	-10dB
		00111	-9dB
		01000	-8dB
		01001	-7dB
		01010	-6dB
		01011	-5dB
		01100	-4dB
		01101	-3dB
		01110	-2dB
		01111	-1dB
		10000	0dB
		10001	1dB
		10010	2dB
		10011	3dB
		10100	4dB
		10101	5dB
		10110	6dB
		10111	7dB
		11000	8dB
		11001	9dB
		11010	10dB
		11011	11dB
		11100	12dB
		11101	13dB
		11110	14dB
		11111	15dB
7	Q	This programs the width of the peak filter.	
		Q	Bandwidth
		0	2/3 Octave
		1	4/3 Octave

Copyright © 2009–2013, Texas Instruments Incorporated

Table 77. EQ_BAND_4 (0xAEh)

Bits	Field	Description	
1:0	FREQ	This sets the Treble peak filter's center frequency. The cut-off frequencies shown are based on a 48kHz sample rate. Using lower sample rates will scale down the cut-off frequencies proportionately.	
		FREQ	Frequency (Hz)
		00	2k
		01	2.7k
		10	3.4k
		11	4.1k
6:2	LEVEL	This sets the gain at f_C.	
		LEVEL	Effect
		00000	Off (0dB)
		00001	-15dB
		00010	-14dB
		00011	-13dB
		00100	-12dB
		00101	-11dB
		00110	-10dB
		00111	-9dB
		01000	-8dB
		01001	-7dB
		01010	-6dB
		01011	-5dB
		01100	-4dB
		01101	-3dB
		01110	-2dB
		01111	-1dB
		10000	0dB
		10001	1dB
		10010	2dB
		10011	3dB
		10100	4dB
		10101	5dB
		10110	6dB
		10111	7dB
		11000	8dB
		11001	9dB
		11010	10dB
		11011	11dB
		11100	12dB
		11101	13dB
		11110	14dB
		11111	15dB
7	Q	This programs the width of the peak filter.	
		Q	Bandwidth
		0	2/3 Octave
		1	4/3 Octave

Copyright © 2009–2013, Texas Instruments Incorporated

Table 78. EQ_BAND_5 (0xAFh)

Bits	Field	Description	
1:0	FREQ	This sets the presence shelving filter's cut-off frequency. The cut-off frequencies shown are based on a 48kHz sample rate. Using lower sample rates will scale down the cut-off frequencies proportionately.	
		FREQ	Frequency (Hz)
		00	7k
		01	9k
		10	11k
		11	13k
6:2	LEVEL	This sets the gain at f_C.	
		LEVEL	Effect
		00000	Off (0dB)
		00001	-15dB
		00010	-14dB
		00011	-13dB
		00100	-12dB
		00101	-11dB
		00110	-10dB
		00111	-9dB
		01000	-8dB
		01001	-7dB
		01010	-6dB
		01011	-5dB
		01100	-4dB
		01101	-3dB
		01110	-2dB
		01111	-1dB
		10000	0dB
		10001	1dB
		10010	2dB
		10011	3dB
		10100	4dB
		10101	5dB
		10110	6dB
		10111	7dB
		11000	8dB
		11001	9dB
		11010	10dB
		11011	11dB
		11100	12dB
		11101	13dB
		11110	14dB
		11111	15dB

Copyright © 2009–2013, Texas Instruments Incorporated

Table 79. SOFTCLIP1 (0xB0h)

Bits	Field	Description	
3:0	TRESHOLD	This sets the threshold level of the audio compressor. Audio signals above the threshold will be compressed.	
		THRESHOLD	Threshold Level (dB)
		0000	-36dB
		0001	-30dB
		0010	-24dB
		0011	-20dB
		0100	-18dB
		0101	-17dB
		0110	-16dB
		0111	-15dB
		1000	-14dB
		1001	-12dB
		1010	-10dB
		1011	-8dB
		1100	-6dB
		1101	-4dB
		1110	-2.5dB
		1111	-1dB
4	SOFT_KNEE	If set, the audio compressor will automatically apply higher compression ratios to audio signals higher than the threshold level. As the audio signal approaches levels higher than the threshold, SOFT_KNEE will increase the compression RATIO. The highest compression that the SOFT_KNEE algorithm will apply is the compression that is set by RATIO.	

Copyright © 2009–2013, Texas Instruments Incorporated

Table 80. SOFTCLIP2 (0xB1h)

Bits	Field	Description	
4:0	RATIO	This sets the ratio at which the audio is compressed to when it passes beyond the threshold. In soft clip mode this is the final level of compression.	
		RATIO	Ratio
		00000	1:1 (Bypass)
		00001	1:1.2
		00010	1:1.4
		00011	1:1.7
		00100	1:2.0
		00101	1:2.4
		00110	1:2.8
		00111	1:3.4
		01000	1:4.0
		01001	1:4.7
		01010	1:5.7
		01011	1:6.7
		01100	1:8.0
		01101	1:9.5
		01110	1:11.3
		01111	1:13.5
		10000	1:16.0
		10001	1:19.0
		10010	1:22.8
		10011	1:27.0
		10100	1:32.0
		10101	1:37.9
		10110	1:45.5
		10111	1:53.9
		11000	1:64
		11001	1:75.9
		11010	1:91.0
		11011	1:108
		11100	1:128
		11101	1:152
		11110	1:182
		11111	1:215

Copyright © 2009–2013, Texas Instruments Incorporated

Table 81. SOFTCLIP3 (0xB2h)

Bits	Field	Description	
4:0	LEVEL	This sets the post compressor gain level.	
		LEVEL	Level (dB)
		00000	-22.5dB
		00001	-21dB
		00010	-19.5dB
		00011	-18dB
		00100	-16.5dB
		00101	-15dB
		00110	-13.5dB
		00111	-12dB
		01000	-10.5dB
		01001	-9dB
		01010	-7.5dB
		01011	-6dB
		01100	-4.5dB
		01101	-3dB
		01110	-1.5dB
		01111	0dB
		10000	1.5dB
		10001	3dB
		10010	4.5dB
		10011	6dB
		10100	7.5dB
		10101	9dB
		10110	10.5dB
		10111	12dB
		11000	13.5dB
		11001	15dB
		11010	16.5dB
		11011	18dB
		11100	19.5dB
		11101	21dB
		11110	22.5dB
		11111	24dB

Copyright © 2009–2013, Texas Instruments Incorporated

GPIO Registers

Table 82. GPIO1 (0xE0h)

Bits	Field	Description	
5:0	GPIO_MODE	This sets the mode of the GPIO Pin.	
		GPIO_MODE	GPIO STATUS
		000000	GPIO Mode is disabled .PORT2_SDO is controlled by the Port2 serial interface configuration. In all the other modes PORT2_SDO is configured as the GPIO pin.
		000001	GPIO_RX (in)
		000010	CHIP ENABLE (in)
		000011	$\overline{\text{CHIP ENABLE}}$ (in)
		000100	ADC MUTE (in)
		000101	$\overline{\text{ADC MUTE}}$ (in)
		000110	HP SENSE (in)
		000111	$\overline{\text{HP SENSE}}$ (in)
		001000	SPARE (in)
		001001	$\overline{\text{SPARE}}$ (in)
		001010	GPIO TX (out)
		001011	CHIP ACTIVE (out)
		001100	$\overline{\text{CHIP ACTIVE}}$ (out)
		001101	HP ENABLE (out)
		001110	$\overline{\text{HP ENABLE}}$ (out)
		001111	LS ENABLE (out)
		010000	$\overline{\text{LS ENABLE}}$ (out)
		010001	EP ENABLE (out)
		010010	$\overline{\text{EP ENABLE}}$ (out)
		010011	ADC CLIPPED (out)
		010100	$\overline{\text{ADC CLIPPED}}$ (out)
		010101	DAC CLIPPED (out)
		010110	$\overline{\text{DAC CLIPPED}}$ (out)
		010111	SOMETHING CLIPPED (out)
		011000	$\overline{\text{SOMETHING CLIPPED}}$ (out)
		011001	ADC NG ACTIVE (out)
		011010	$\overline{\text{ADC NG ACTIVE}}$ (out)
		011011	DAC NG ACTIVE (out)
		011100	$\overline{\text{DAC NG ACTIVE}}$ (out)
		011101	THERMAL (out)
		011110	$\overline{\text{THERMAL}}$ (out)
		011111	LS SHORT CCT (out)
5:0	GPIO_MODE	100000	$\overline{\text{LS SHORT CCT}}$ (out)
		100001	ANALOG ERROR Thermal or LS CCT condition (out)
		100010	$\overline{\text{ANALOG ERROR}}$ (out)
		100011	ERROR (out) Thermal or LS CCT or Clipping
		100100	$\overline{\text{ERROR}}$ (out)
		100101 – 111111	RESERVED
6	GPIO_TX	Whenever GPIO_MODE is set to '001010', the GPIO pin will output a logic level based on this bit setting. Setting this bit high will result in a logic high GPIO output.	

Copyright © 2009–2013, Texas Instruments Incorporated

Table 82. GPIO1 (0xE0h) (continued)

Bits	Field	Description
7	GPIO_RX	This bit reports the logic level is present on the GPIO pin.

Table 83. GPIO2 (0xE1h)

Bits	Field	Description
0	SHORT	This bit will go high whenever a short circuit condition occurs on the Class D loudspeaker amplifier outputs. Once triggered by a short circuit event, an I^2C write of 1 to this bit clear this bit.
1	TEMP	This bit will go high whenever the temperature of the LM49352 reaches a critical temperature. Once triggered by a thermal event, an I^2C write of 1 to this bit clear this bit.

Table 84. RESET (0xF0h)

Bits	Field	Description
4:0	RSVD	Reserved.
5	SOFT_RESET	Setting this bit resets the digital core of LM49352. SOFT_RESET does not affect the current I^2C register settings.

Table 85. Spread Spectrum (0xF1h)

Bits	Field	Description
1:0	RSVD	Reserved
2	SS_DISABLE	If this bit is set, Spread Spectrum mode will be disabled from the Class D amplifier.

Table 86. FORCE (0xFE)

Bits	Field	Description	
0	RSVD	Reserved	
1	DACREF	This bit determines whether the DAC reference voltage is internally generated or externally driven.	
		DACREF	STATUS
		0	DACREF uses an internal bandgap reference.
		1	DACREF is driven by an external voltage reference.
2	CP_FORCE	If set, a -LS_VDD rail will be generated on HP_VSS, even if the headphone output stage is not required.	

Copyright © 2009–2013, Texas Instruments Incorporated

Schematic Diagram

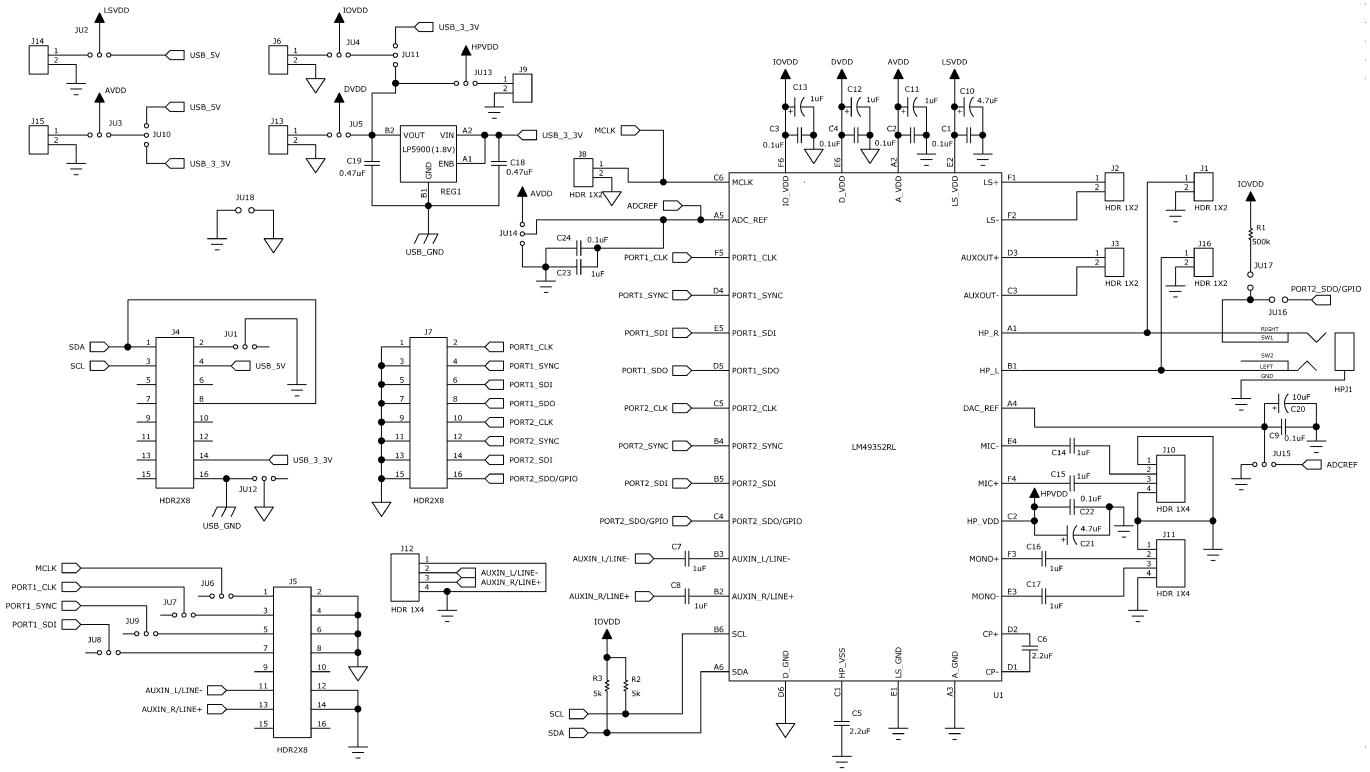


Figure 72. Demo Board Schematic

Copyright © 2009–2013, Texas Instruments Incorporated

Demonstration Board Layout

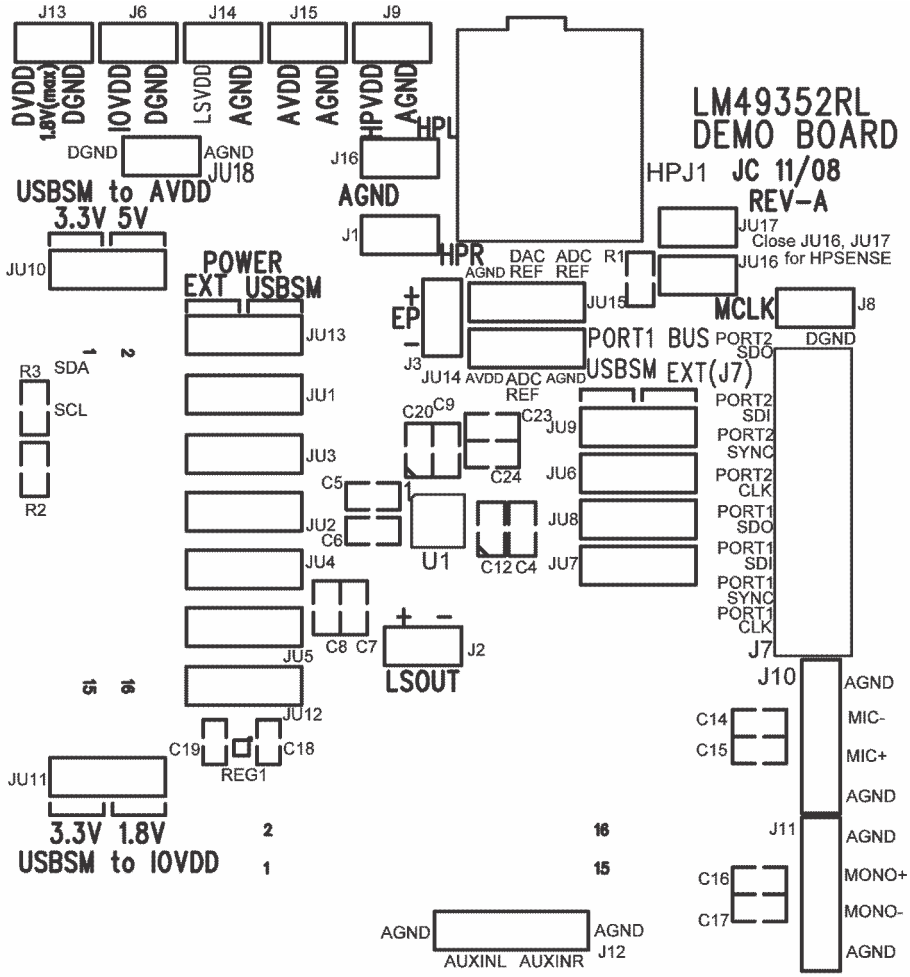


Figure 73. Top Silkscreen

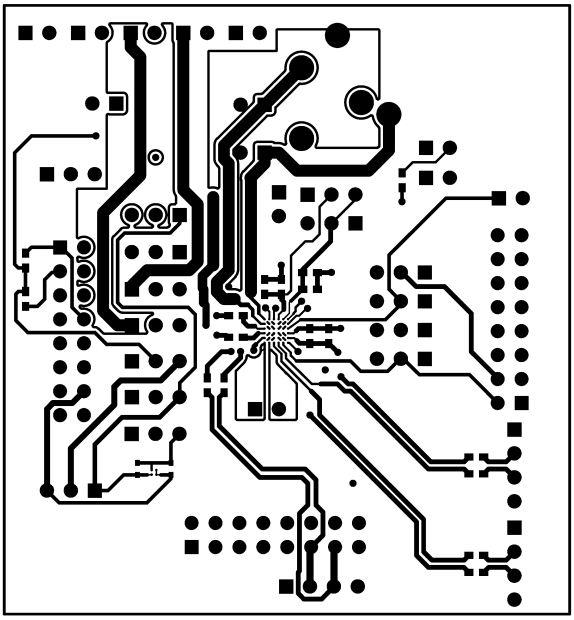


Figure 74. Top Layer

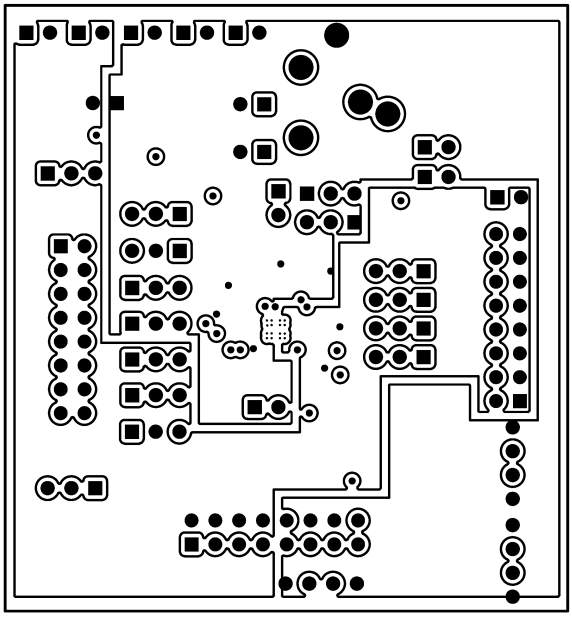


Figure 75. Inner Layer 2

Copyright © 2009–2013, Texas Instruments Incorporated

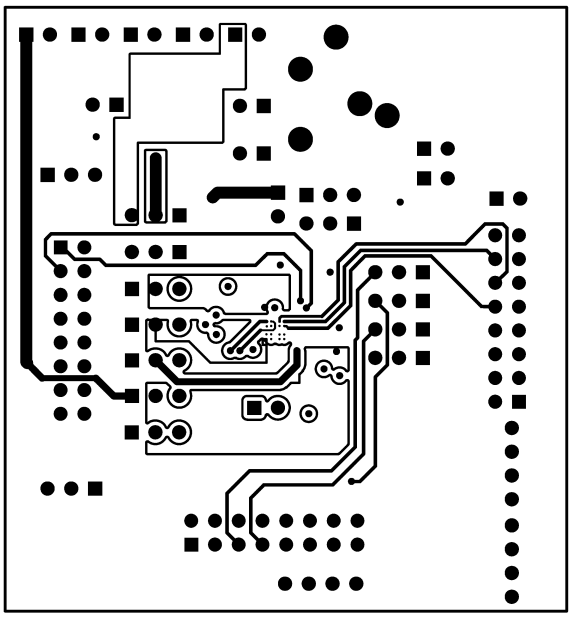


Figure 76. Inner Layer 3

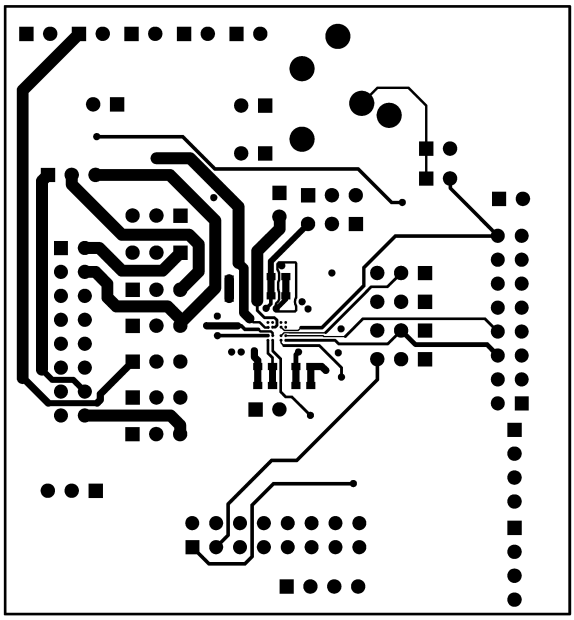


Figure 77. Bottom Layer

Copyright © 2009–2013, Texas Instruments Incorporated

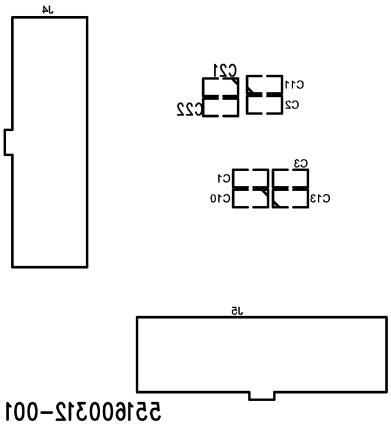


Figure 78. Bottom Silkscreen

Revision History

Rev	Date	Description
1.0	05/03/10	Initial released.
1.01	06/30/10	Fixed a typo in the I^2C Timing Parameters table.

Copyright © 2009–2013, Texas Instruments Incorporated

REVISION HISTORY

Changes from Revision D (March 2013) to Revision E	Page
• Changed layout of National Data Sheet to TI format	100

Copyright © 2009–2013, Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LM49352RL/NOPB	ACTIVE	DSBGA	YPG	36	250	Green (RoHS & no Sb/Br)	SNAG	Level-1-260C-UNLIM	-40 to 85	GL5	Samples
LM49352RLX/NOPB	ACTIVE	DSBGA	YPG	36	1000	Green (RoHS & no Sb/Br)	SNAG	Level-1-260C-UNLIM	-40 to 85	GL5	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

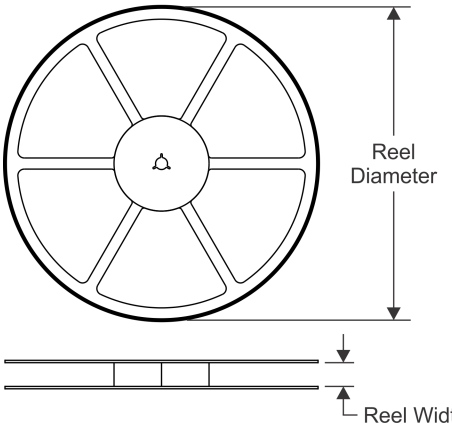
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

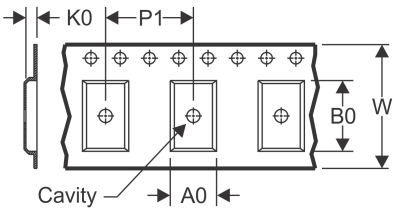
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

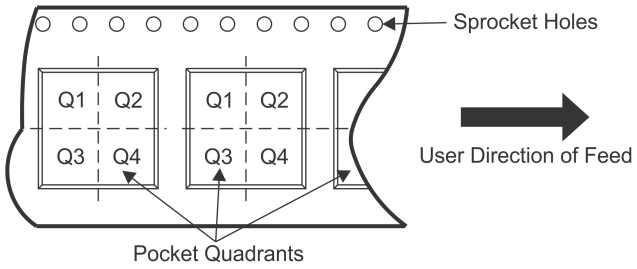


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

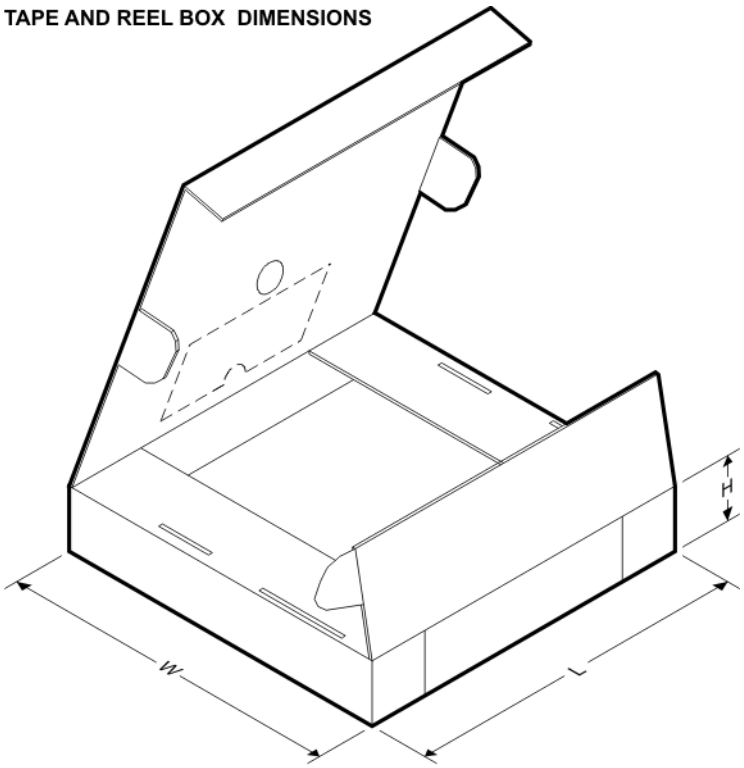
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM49352RL/NOPB	DSBGA	YPG	36	250	178.0	12.4	3.43	3.59	0.76	8.0	12.0	Q1
LM49352RLX/NOPB	DSBGA	YPG	36	1000	178.0	12.4	3.43	3.59	0.76	8.0	12.0	Q1

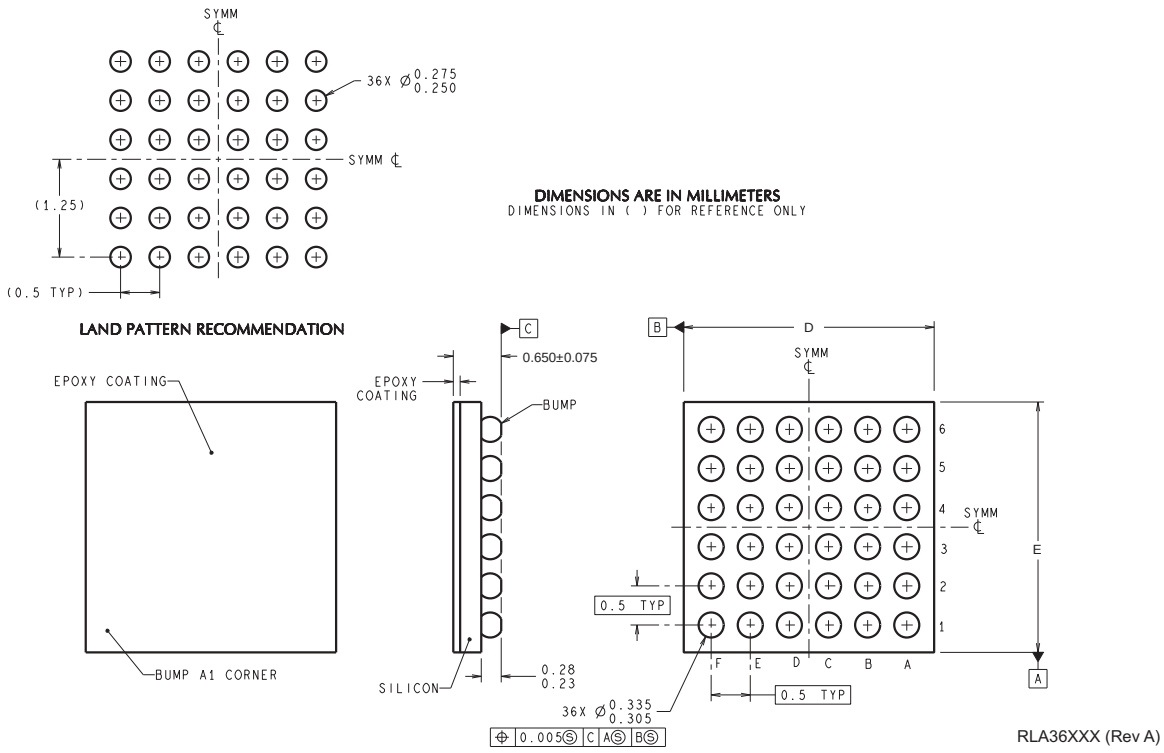
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM49352RL/NOPB	DSBGA	YPG	36	250	210.0	185.0	35.0
LM49352RLX/NOPB	DSBGA	YPG	36	1000	210.0	185.0	35.0

YPG0036



D: Max = 3.305 mm, Min =3.245 mm

E: Max = 3.305 mm, Min =3.245 mm

4214895/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2015, Texas Instruments Incorporated