LMP8601, LMP8601-Q1 60-V Common-Mode Bidirectional Precision Current-Sensing Amplifier

1 Features

- Unless Otherwise Noted, Typical Values at T_A = 25°C, V_S = 5.0 V, Gain = 20x
  - TCV_{OS} 10 µV/°C Maximum
  - CMRR 90 dB Minimum
  - Input offset voltage 1 mV Maximum
  - CMVR at V_S = 3.3 V, –4 V, to 27 V
  - CMVR at V_S = 5 V, –22 V to 60 V
  - Operating Ambient Temperature Range –40°C to 125°C
  - Single-Supply Bidirectional Operation
  - All Minimum and Maximum Limits 100% Tested
  - LMP8601-Q1 is Qualified for Automotive Applications:
    - Device Temperature AEC-Q100 Grade 1: –40°C to 125°C Operating Range
    - Device HBM ESD Classification: Level 2 (3A on inputs)
    - Device CDM ESD Classification: Level C6
    - Device MM ESD Classification: Level M2

2 Applications

- High-Side and Low-Side Driver Configuration Current Sensing
- Bidirectional Current Measurement
- Current Loop to Voltage Conversion
- Automotive Fuel Injection Control
- Transmission Control
- Power Steering
- Battery Management Systems

3 Description

The LMP8601 and LMP8601-Q1 devices are fixed 20x gain precision amplifiers that will amplify and filter small differential signals in the presence of high common-mode voltages. The input common-mode voltage range is –22 V to +60 V when operating from a single 5-V supply, or –4 V to +27 V with a 3.3-V supply. The LMP8601 and LMP8601-Q1 are ideal parts for unidirectional and bidirectional current sensing applications.

The fixed gain is achieved in two separate stages, a preamplifier with a gain of 10x and an output stage buffer amplifier with a gain of 2x. The path between the two stages is brought out on two pins to enable the option of an additional filter network or modifying the gain.

The offset input pin enables the user to use these devices for unidirectional or bidirectional single supply voltage current sensing.

The LMP8601-Q1 incorporates enhanced manufacturing and support processes for the automotive market and is compliant with the AEC Q100 standard.

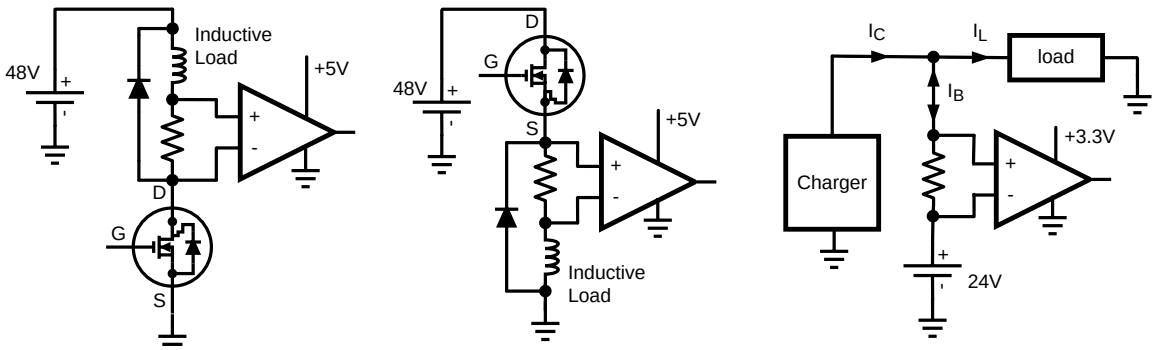
If higher gain is required, the LMP8602 is available with a gain of 50, or the LMP8603 with a gain of 100.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMP8601	SOIC (8)	4.90 mm x 3.91 mm
LMP8601-Q1		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Applications



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (January 2014) to Revision G — **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Revision E (March 2013) to Revision F — **Page**

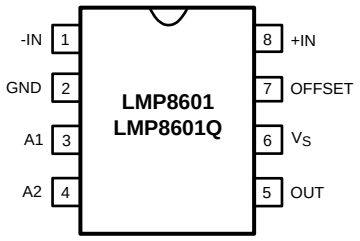
- Added four typical curves ... 13

Changes from Revision D (October 2009) to Revision E — **Page**

- Changed layout of National Data Sheet to TI format ... 24

5 Pin Configuration and Functions

D Package
8-Pin SOIC
Top View



Pin Descriptions

PIN		TYPE	DESCRIPTION
NAME	NO.		
A1	3	O	Preamplifier output
A2	4	I	Input from the external filter network and / or A1
GND	2	P	Power Ground
+IN	8	I	Positive Input
-IN	1	I	Negative Input
OFFSET	7	I	DC Offset for bidirectional signals
OUT	5	O	Single-ended output
V_S	6	P	Positive Supply Voltage

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply Voltage (V_S – GND)		–0.3	6	V
Continuous Input Voltage (-IN and +IN)		–22	60	V
Transient (400 ms)		–25	65	V
Maximum Voltage at A1, A2, OFFSET and OUT Pins		V_S + 0.3	GND – 0.3	V
Junction Temperature(2)		–40	150	°C
Mounting Temperature	Infrared or Convection (20 sec)		235	°C
	Wave Soldering Lead (10 sec)		260	
Storage Temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The maximum power dissipation must be derated at elevated temperatures and is dictated by $T_{J(MAX)}$, $R_{\theta JA}$, and the ambient temperature, T_A. The maximum allowable power dissipation $P_{DMAX} = (T_{J(MAX)} - T_A)/ R_{\theta JA}$ or the number given in Absolute Maximum Ratings, whichever is lower.

6.2 ESD Ratings: LMP8601

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	All pins except 1 and 8	±2000	V
			Pins 1 and 8	±4000	
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)		±1000	
		Machine Model		±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 ESD Ratings: LMP8601-Q1

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	All pins except 1 and 8	±2000	V
			Pins 1 and 8	±4000	
		Charged-device model (CDM), per AEC Q100-011		±1000	
		Machine Model		±200	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Supply Voltage (V_S – GND)	3	5.5	V
Offset Voltage (Pin 7)	0	V_S	
Temperature Range (1), Packaged devices	–40	125	°C

(1) The maximum power dissipation must be derated at elevated temperatures and is dictated by $T_{J(MAX)}$, $R_{\theta JA}$, and the ambient temperature, T_A. The maximum allowable power dissipation $P_{DMAX} = (T_{J(MAX)} - T_A)/ R_{\theta JA}$ or the number given in Absolute Maximum Ratings, whichever is lower.

6.5 Thermal Information

THERMAL METRIC[1]		LMP8601, LMP8601-Q1	UNIT
		D (SOIC)	
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance[2]	190	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) The maximum power dissipation must be derated at elevated temperatures and is dictated by $T_{J(MAX)}$, $R_{\theta JA}$, and the ambient temperature, T_A. The maximum allowable power dissipation $P_{DMAX} = (T_{J(MAX)} - T_A)/ R_{\theta JA}$ or the number given in Absolute Maximum Ratings, whichever is lower.

6.6 3.3-V Electrical Characteristics

Unless otherwise specified, all limits ensured at T_A = 25°C, V_S = 3.3 V, GND = 0 V, –4 V ≤ V_{CM} ≤ 27 V, and R_L = ∞, Offset (Pin 7) is grounded, 10 nF between V_S and GND.[1]

PARAMETER		TEST CONDITIONS		MIN[2]	TYP[3]	MAX[2]	UNIT
OVERALL PERFORMANCE (FROM -IN (PIN 1) AND +IN (PIN 8) TO OUT (PIN 5) WITH PINS A1 (PIN 3) AND A2 (PIN 4) CONNECTED)							
I_S	Supply Current				1		mA
		At the temperature extremes		0.6		1.3	
A_V	Total Gain			19.9	20	20.1	V/V
	Gain Drift [4]	–40°C ≤ T_A ≤ 125°C			–2.7	±20	ppm/°C
SR	Slew Rate [5]	V_{IN} = ±0.165 V		0.4	0.7		V/µs
BW	Bandwidth			50	60		kHz
V_{OS}	Input Offset Voltage	$V_{CM} = V_S / 2$			0.15	±1	mV
TCV_{OS}	Input Offset Voltage Drift [6]	–40°C ≤ T_A ≤ 125°C			2	±10	µV/°C
e_n	Input Referred Voltage Noise	0.1 Hz - 10 Hz, 6 Sigma			16.4		μV_{P-P}
		Spectral Density, 1 kHz			830		nV/√Hz
PSRR	Power Supply Rejection Ratio	DC, 3.0 V ≤ V_S ≤ 3.6 V, $V_{CM} = V_S/2$			86		dB
			At the temperature extremes	70			
	Mid-scale Offset Scaling Accuracy				±0.15	±0.5%	
		Input Referred				±0.413	mV
PREAMPLIFIER (FROM INPUT PINS -IN (PIN 1) AND +IN (PIN 8) TO A1 (PIN 3))							
R_{CM}	Input Impedance Common Mode	–4 V ≤ V_{CM} ≤ 27 V			295		kΩ
			At the temperature extremes	250		350	
R_{DM}	Input Impedance Differential Mode	–4 V ≤ V_{CM} ≤ 27 V			590		kΩ
			At the temperature extremes	500		700	
V_{OS}	Input Offset Voltage	$V_{CM} = V_S / 2$			±0.15	±1	mV
DC CMRR	DC Common-Mode Rejection Ratio	–2 V ≤ V_{CM} ≤ 24 V			96		dB
			At the temperature extremes	86			
AC CMRR	AC Common-Mode Rejection Ratio [7]	f = 1 kHz		80	94		dB
		f = 10 kHz			85		
CMVR	Input Common-Mode Voltage Range	for 80 dB CMRR	At the temperature extremes	–4		27	V
$A1_V$	Gain [4]			9.95	10.0	10.05	V/V
R_{F-INT}	Output Impedance Filter Resistor				100		kΩ
		At the temperature extremes		99		101	
TCR_{F-INT}	Output Impedance Filter Resistor Drift	At the temperature extremes			±5	±50	ppm/°C

(1) The *Electrical Characteristics* tables list ensured specifications under the listed *Recommended Operating Conditions* except as otherwise modified or specified by the *Electrical Characteristics* conditions and/or notes. Typical specifications are estimations only and are not ensured.
(2) Datasheet min/max specification limits are ensured by test.
(3) Typical values represent the most likely parameter norms at T_A = +25°C, and at the *Recommended Operation Conditions* at the time of product characterization and are not ensured.
(4) Both the gain of the preamplifier $A1_V$ and the gain of the buffer amplifier $A2_V$ are measured individually. The over all gain of both amplifiers A_V is also measured to assure the gain of all parts is always within the A_V limits
(5) Slew rate is the average of the rising and falling slew rates.
(6) Offset voltage drift determined by dividing the change in V_{OS} at temperature extremes into the total temperature change.
(7) AC Common-Mode Signal is a 5 V_{PP} sine-wave (0 V to 5 V) at the given frequency.

3.3-V Electrical Characteristics (continued)

Unless otherwise specified, all limits ensured at T_A = 25°C, V_S = 3.3 V, GND = 0 V, –4 V ≤ V_{CM} ≤ 27 V, and R_L = ∞, Offset (Pin 7) is grounded, 10 nF between V_S and GND.(1)

PARAMETER		TEST CONDITIONS		MIN(2)	TYP(3)	MAX(2)	UNIT
A1 V_{OUT}	A1 Output Voltage Swing	V_{OL}, R_L = ∞			2		mV
			At the temperature extremes			10	
		V_{OH}, R_L = ∞			3.25		V
			At the temperature extremes	3.2			
OUTPUT BUFFER (FROM A2 (PIN 4) TO OUT (PIN 5))							
V_{OS}	Input Offset Voltage	0V ≤ V_{CM} ≤ V_S		–2	±0.5	2	mV
			At the temperature extremes	–2.5		2.5	
$A2_V$	Gain (4)			1.99	2	2.01	V/V
I_B	Input Bias Current of A2 (8),				–40		fA
		At the temperature extremes				±20	nA
A2 V_{OUT}	A2 Output Voltage Swing (9) (10)	V_{OL}, R_L = 100 kΩ			4		mV
			At the temperature extremes			20	
		V_{OH}, R_L = 100 kΩ			3.29		V
			At the temperature extremes	3.28			
I_{SC}	Output Short-Circuit Current (11)	Sourcing, V_{IN} = V_S, V_{OUT} = GND		–25	–38	–60	mA
		Sinking, V_{IN} = GND, V_{OUT} = V_S		30	46	65	

(8) Positive current corresponds to current flowing into the device
(9) For this test input is driven from A1 stage.
(10) For V_{OL}, R_L is connected to V_S and for V_{OH}, R_L is connected to GND.
(11) Short-Circuit test is a momentary test. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C

6.7 5-V Electrical Characteristics

Unless otherwise specified, all limits ensured for at T_A = 25°C, V_S = 5 V, GND = 0 V, –22 V ≤ V_{CM} ≤ 60 V, and R_L = ∞, Offset (Pin 7) is grounded, 10 nF between V_S and GND.(1)

PARAMETER		TEST CONDITIONS		MIN(2)	TYP(3)	MAX(2)	UNIT
OVERALL PERFORMANCE (FROM -IN (PIN 1) AND +IN (PIN 8) TO OUT (PIN 5) WITH PINS A1 (PIN 3) AND A2 (PIN 4) CONNECTED)							
I_S	Supply Current				1.1		mA
		At the temperature extremes		0.7		1.5	
A_V	Total Gain (4)			19.9	20	20.1	V/V
	Gain Drift	–40°C ≤ T_A ≤ 125°C			–2.8	±20	ppm/°C
SR	Slew Rate (5)	V_{IN} = ±0.25 V		0.6	0.83		V/µs
BW	Bandwidth			50	60		kHz
V_{OS}	Input Offset Voltage				0.15	±1	mV
TCV_{OS}	Input Offset Voltage Drift (6)	–40°C ≤ T_A ≤ 125°C			2	±10	µV/°C
e_N	Input Referred Voltage Noise	0.1 Hz - 10 Hz, 6 Sigma			17.5		μV_{P-P}
		Spectral Density, 1 kHz			890		$nV/\sqrt{Hz}$
PSRR	Power Supply Rejection Ratio	DC 4.5 V ≤ V_S ≤ 5.5 V			90		dB
			At the temperature extremes	70			
	Mid-scale Offset Scaling Accuracy				±0.15%	±0.5%	
		Input Referred				±0.625	mV

(1) The *Electrical Characteristics* tables list ensured specifications under the listed *Recommended Operating Conditions* except as otherwise modified or specified by the *Electrical Characteristics* conditions and/or notes. Typical specifications are estimations only and are not ensured.
(2) Datasheet min/max specification limits are ensured by test.
(3) Typical values represent the most likely parameter norms at T_A = +25°C, and at the *Recommended Operation Conditions* at the time of product characterization and are not ensured.
(4) Both the gain of the preamplifier $A1_V$ and the gain of the buffer amplifier $A2_V$ are measured individually. The over all gain of both amplifiers A_V is also measured to assure the gain of all parts is always within the A_V limits
(5) Slew rate is the average of the rising and falling slew rates.
(6) Offset voltage drift determined by dividing the change in V_{OS} at temperature extremes into the total temperature change.

5-V Electrical Characteristics (continued)

Unless otherwise specified, all limits ensured for at T_A = 25°C, V_S = 5 V, GND = 0 V, –22 V ≤ V_{CM} ≤ 60 V, and R_L = ∞, Offset (Pin 7) is grounded, 10 nF between V_S and GND.(1)

PARAMETER		TEST CONDITIONS		MIN(2)	TYP(3)	MAX(2)	UNIT
PREAMPLIFIER (FROM INPUT PINS -IN (PIN 1) AND +IN (PIN 8) TO A1 (PIN 3))							
R_{CM}	Input Impedance Common Mode	0 V ≤ V_{CM} ≤ 60 V			295		kΩ
			At the temperature extremes	250		350	
		–20 V ≤ V_{CM} ≤ 0 V			193		kΩ
			At the temperature extremes	165		250	
R_{DM}	Input Impedance Differential Mode	0 V ≤ V_{CM} ≤ 60 V			590		kΩ
			At the temperature extremes	500		700	
		–20 V ≤ V_{CM} ≤ 0 V			386		kΩ
			At the temperature extremes	300		500	
V_{OS}	Input Offset Voltage	V_{CM} = V_S / 2			±0.15	±1	mV
DC CMRR	DC Common-Mode Rejection Ratio	–20 V ≤ V_{CM} ≤ 60 V			105		dB
			At the temperature extremes	90			
AC CMRR	AC Common-Mode Rejection Ratio (7)	f = 1 kHz		80	96		dB
		f = 10 kHz			83		
CMVR	Input Common-Mode Voltage Range	for 80 dB CMRR	At the temperature extremes	–22		60	V
$A1_V$	Gain (4)			9.95	10	10.05	V/V
R_{F-INT}	Output Impedance Filter Resistor				100		kΩ
		At the temperature extremes		99		101	
TCR_{F-INT}	Output Impedance Filter Resistor Drift				±5	±50	ppm/°C
A1 V_{OUT}	A1 Ouput Voltage Swing	V_{OL}, R_L = ∞			2		mV
			At the temperature extremes			10	
		V_{OH}, R_L = ∞			4.985		V
			At the temperature extremes	4.95			
OUTPUT BUFFER (FROM A2 (PIN 4) TO OUT (PIN 5))							
V_{OS}	Input Offset Voltage	0V ≤ V_{CM} ≤ V_S		–2	±0.5	2	mV
			At the temperature extremes	–2.5		2.5	
$A2_V$	Gain (4)			1.99	2	2.01	V/V
I_B	Input Bias Current of A2 (8)				–40		fA
		At the temperature extremes				±20	nA
A2 V_{OUT}	A2 Ouput Voltage Swing (9) (10)	V_{OL}, R_L = ∞			4		mV
			At the temperature extremes			20	
		V_{OH}, R_L = ∞			4.99		V
			At the temperature extremes	4.98			
I_{SC}	Output Short-Circuit Current (11)	Sourcing, V_{IN} = V_S, V_{OUT} = GND		–25	–42	–60	mA
		Sinking, V_{IN} = GND, V_{OUT} = V_S		30	48	65	

(7) AC Common-Mode Signal is a 5 V_{PP} sine-wave (0 V to 5 V) at the given frequency.
(8) Positive current corresponds to current flowing into the device
(9) For this test input is driven from A1 stage.
(10) For V_{OL}, R_L is connected to V_S and for V_{OH}, R_L is connected to GND.
(11) Short-Circuit test is a momentary test. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C

6.8 Typical Characteristics

Unless otherwise specified, all limits ensured for at T_A = 25°C, V_S = 5 V, GND = 0 V, –22 ≤ V_{CM} ≤ 60 V, and R_L = ∞, Offset (Pin 7) connected to V_S, 10 nF between V_S and GND.

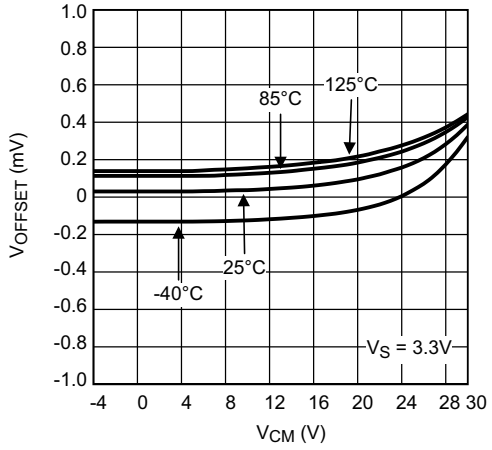


Figure 1. V_{OS} vs. V_{CM} at V_S = 3.3 V

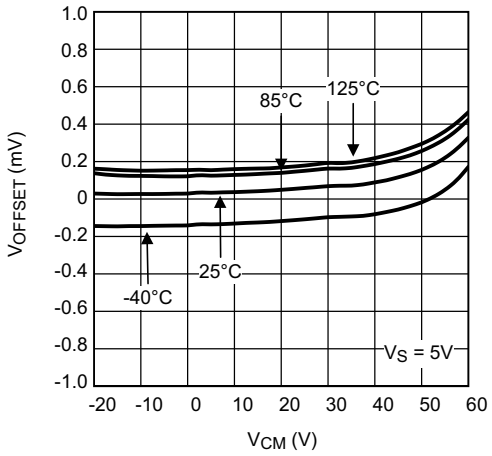


Figure 2. V_{OS} vs. V_{CM} at V_S = 5 V

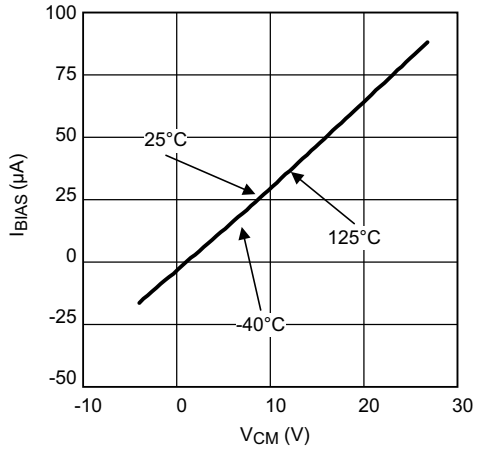


Figure 3. Input Bias Current Over Temperature (+IN and -IN pins) at V_S = 3.3 V

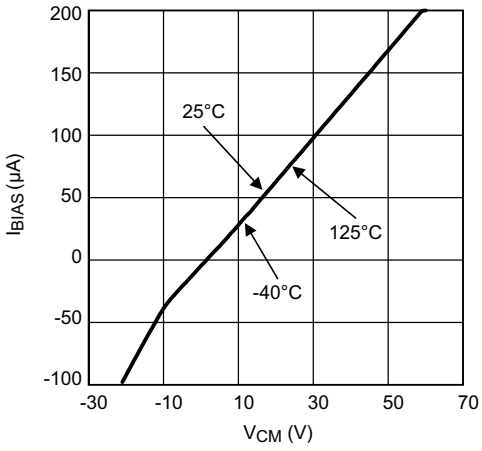


Figure 4. Input Bias Current Over Temperature (+IN and -IN pins) at V_S = 5 V

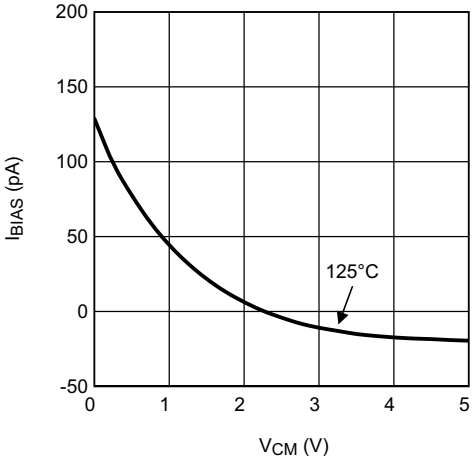


Figure 5. Input Bias Current Over Temperature (A2 pin) at V_S = 5 V

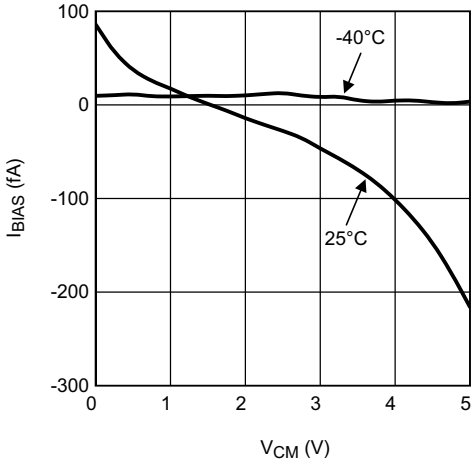


Figure 6. Input Bias Current Over Temperature (A2 pin) at V_S = 5 V

Typical Characteristics (continued)

Unless otherwise specified, all limits ensured for at T_A = 25°C, V_S = 5 V, GND = 0 V, –22 ≤ V_{CM} ≤ 60 V, and R_L = ∞, Offset (Pin 7) connected to V_S, 10 nF between V_S and GND.

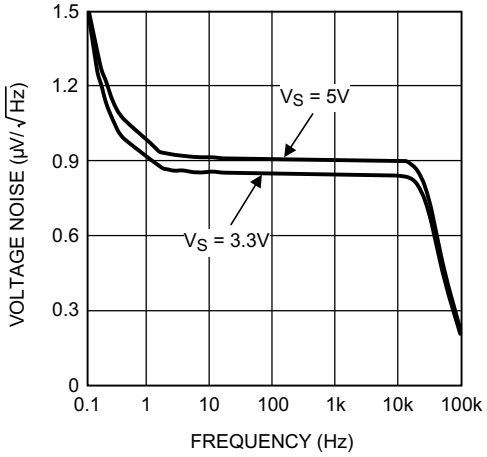


Figure 7. Input Referred Voltage Noise vs. Frequency

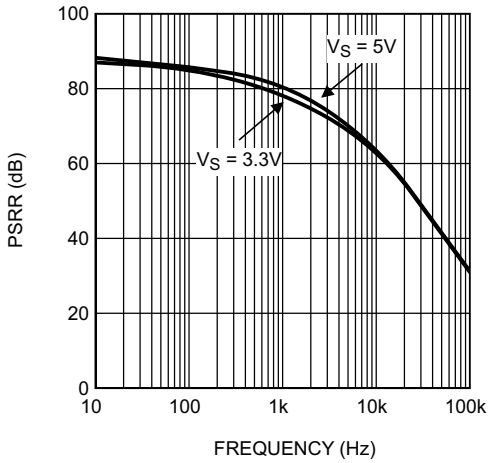


Figure 8. PSRR vs. Frequency

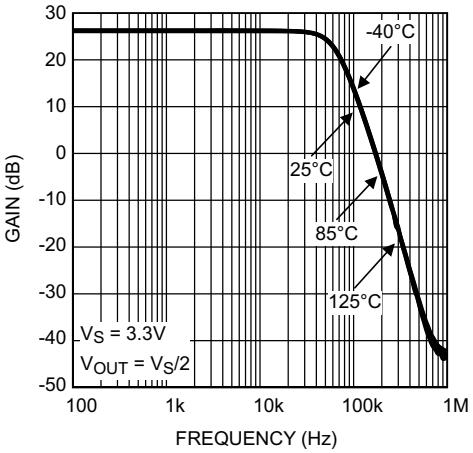


Figure 9. Gain vs. Frequency at V_S = 3.3 V

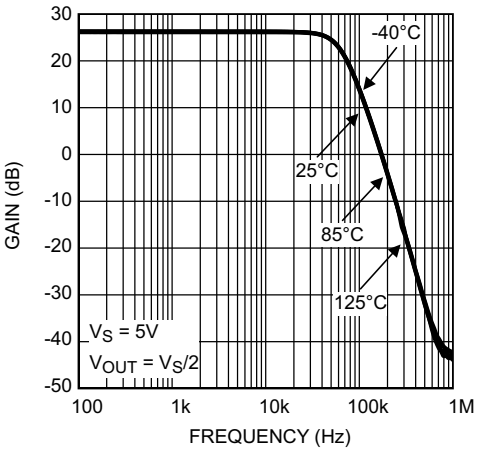


Figure 10. Gain vs. Frequency at V_S = 5 V

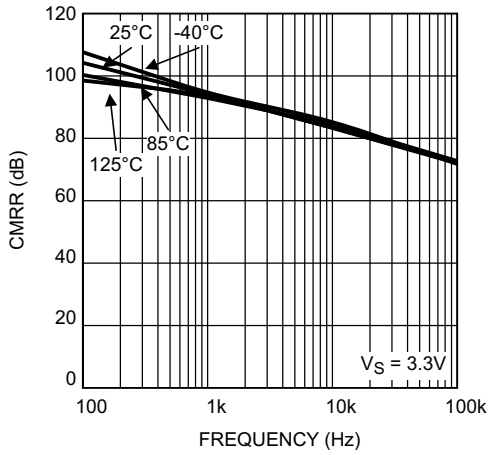


Figure 11. CMRR vs. Frequency at V_S = 3.3 V

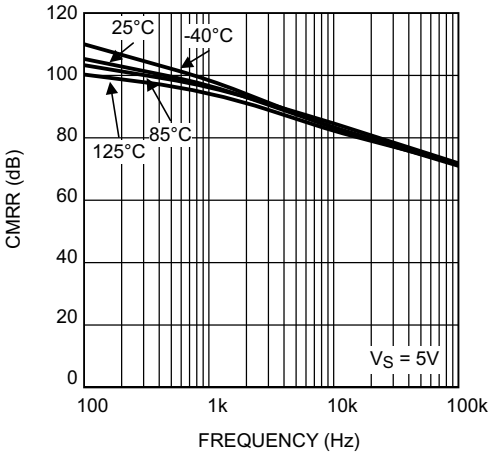


Figure 12. CMRR vs. Frequency at V_S = 5 V

Typical Characteristics (continued)

Unless otherwise specified, all limits ensured for at T_A = 25°C, V_S = 5 V, GND = 0 V, –22 ≤ V_{CM} ≤ 60 V, and R_L = ∞, Offset (Pin 7) connected to V_S, 10 nF between V_S and GND.

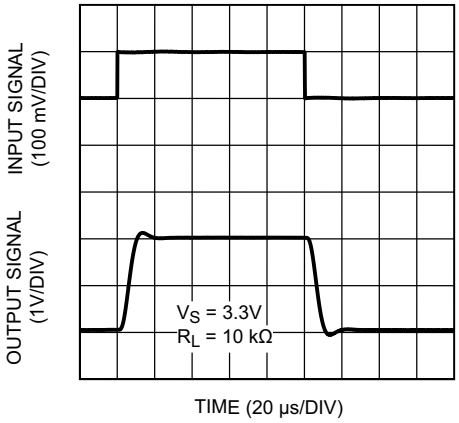


Figure 13. Step Response at V_S = 3.3 V

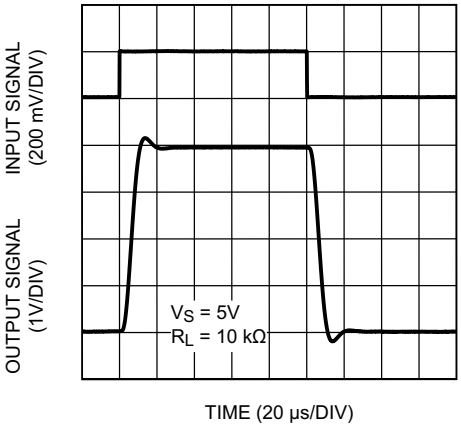


Figure 14. Step Response at V_S = 5 V

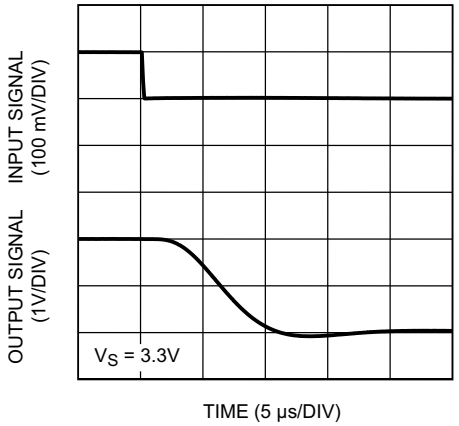


Figure 15. Settling Time (Falling Edge) at V_S = 3.3 V

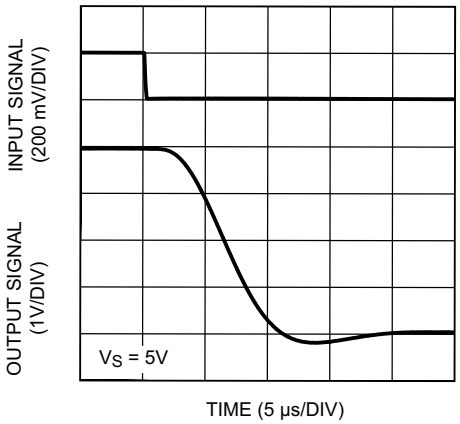


Figure 16. Settling Time (Falling Edge) at V_S = 5 V

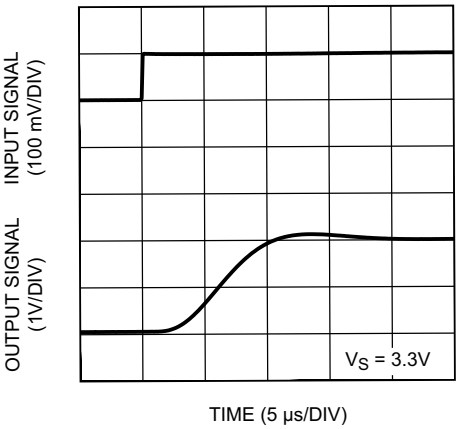


Figure 17. Settling Time (Rising Edge) at V_S = 3.3 V

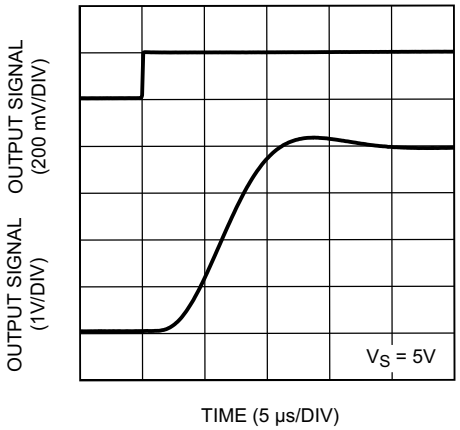


Figure 18. Settling Time (Rising Edge) at V_S = 5 V

Typical Characteristics (continued)

Unless otherwise specified, all limits ensured for at T_A = 25°C, V_S = 5 V, GND = 0 V, –22 ≤ V_{CM} ≤ 60 V, and R_L = ∞, Offset (Pin 7) connected to V_S, 10 nF between V_S and GND.

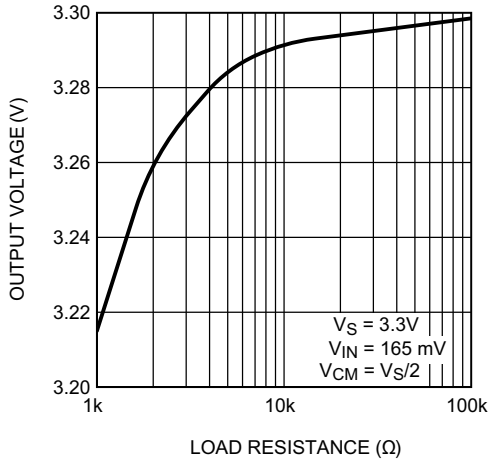


Figure 19. Positive Swing vs. R_{LOAD} at V_S = 3.3 V

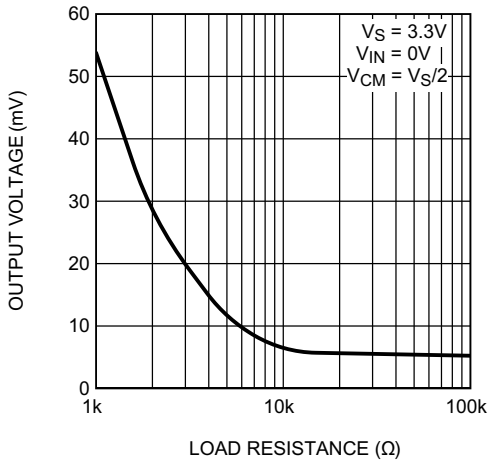


Figure 20. Negative Swing vs. R_{LOAD} at V_S = 3.3 V

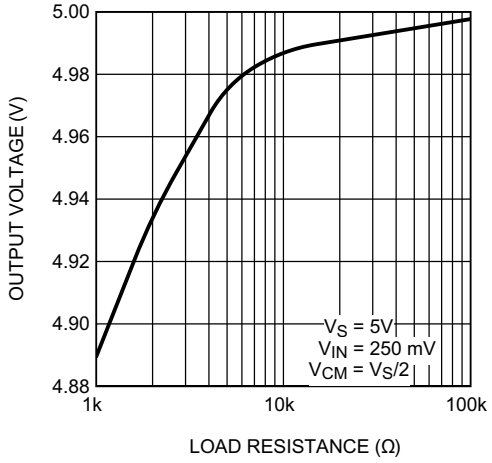


Figure 21. Positive Swing vs. R_{LOAD} V_S = 5 V

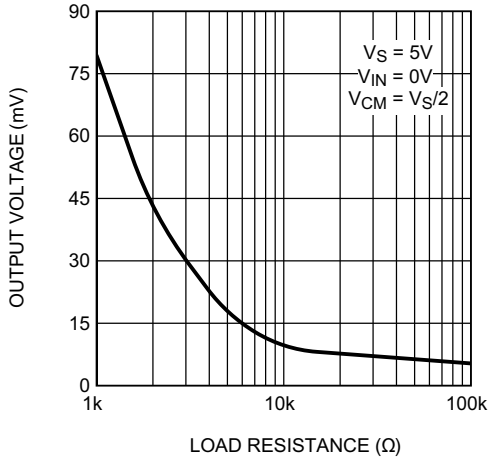


Figure 22. Negative Swing vs. R_{LOAD} at V_S = 5 V

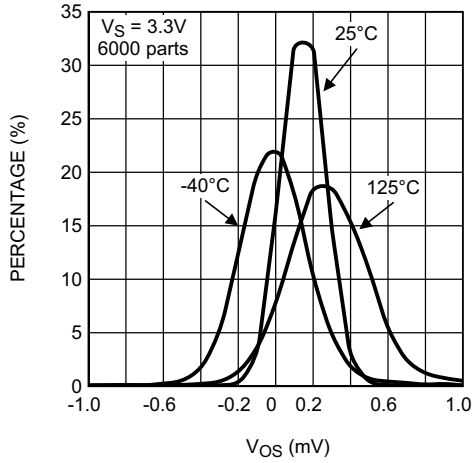


Figure 23. V_{OS} Distribution at V_S = 3.3 V

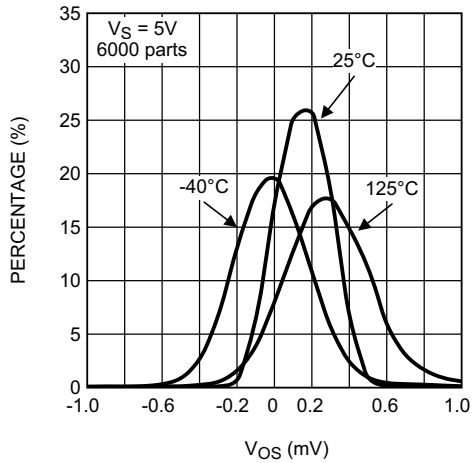


Figure 24. V_{OS} Distribution at V_S = 5 V

Typical Characteristics (continued)

Unless otherwise specified, all limits ensured for at T_A = 25°C, V_S = 5 V, GND = 0 V, –22 ≤ V_{CM} ≤ 60 V, and R_L = ∞, Offset (Pin 7) connected to V_S, 10 nF between V_S and GND.

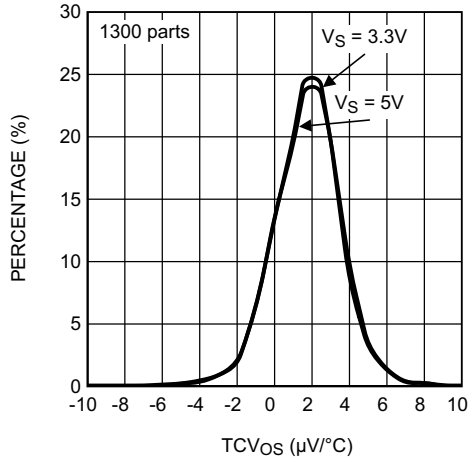


Figure 25. TCV_{OS} Distribution

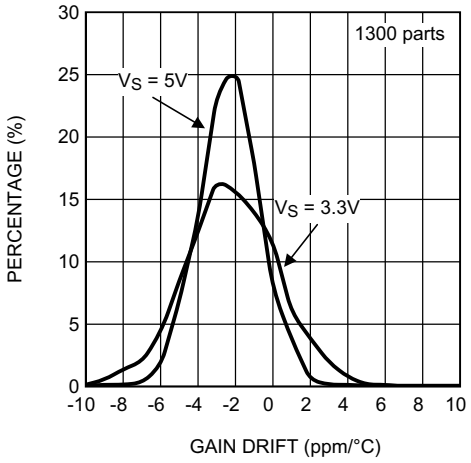


Figure 26. Gain Drift Distribution

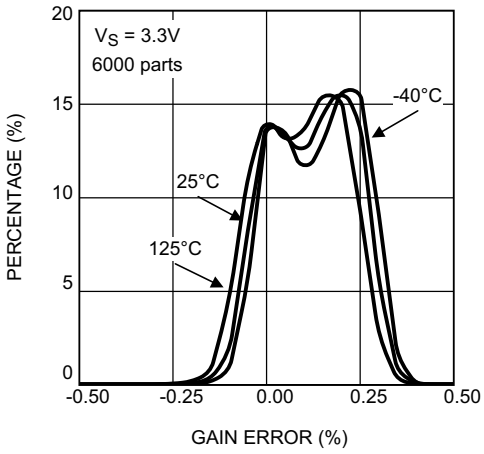


Figure 27. Gain Error Distribution at V_S = 3.3 V

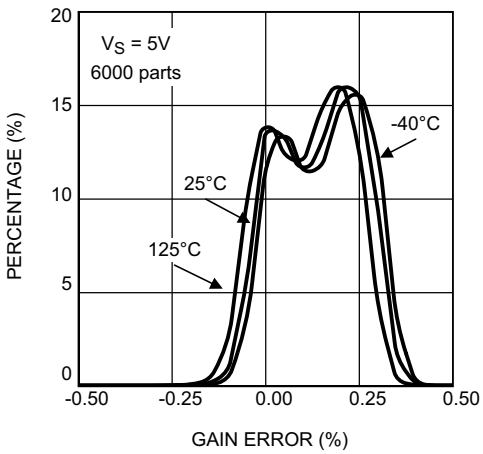


Figure 28. Gain Error Distribution at V_S = 5 V

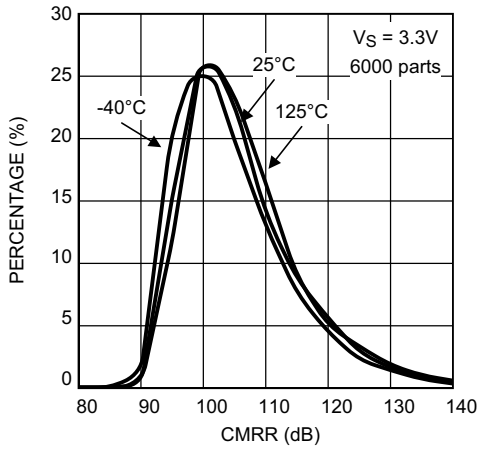


Figure 29. CMRR Distribution at V_S = 3.3 V

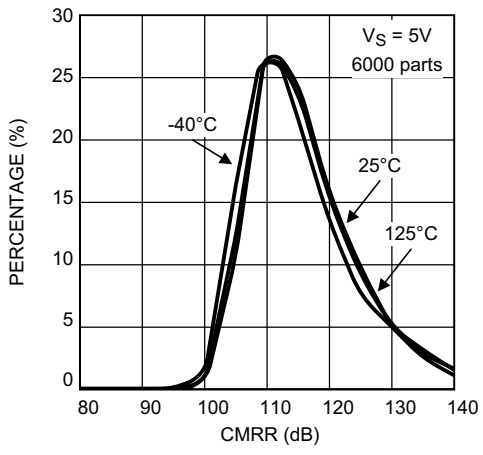


Figure 30. CMRR Distribution at V_S = 5 V

Typical Characteristics (continued)

Unless otherwise specified, all limits ensured for at T_A = 25°C, V_S = 5 V, GND = 0 V, –22 ≤ V_{CM} ≤ 60 V, and R_L = ∞, Offset (Pin 7) connected to V_S, 10 nF between V_S and GND.

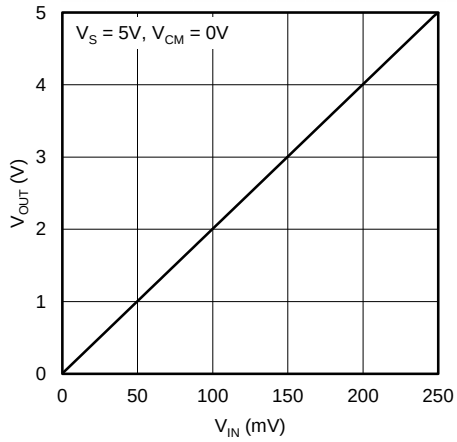


Figure 31. Output Voltage vs. VIN

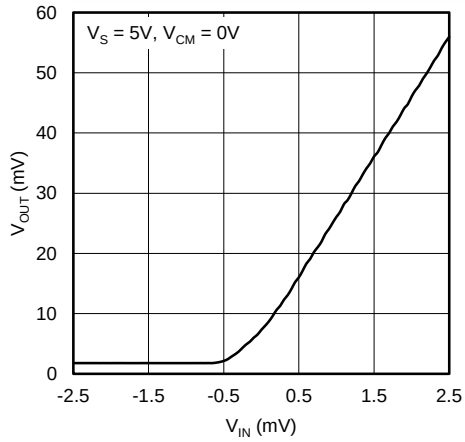


Figure 32. Output Voltage vs. VIN (Zoom Close to 0 V)

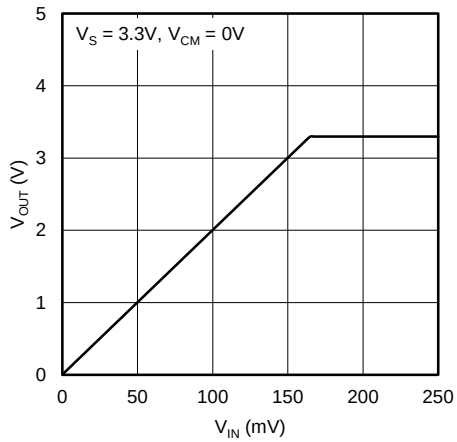


Figure 33. Output Voltage vs. VIN

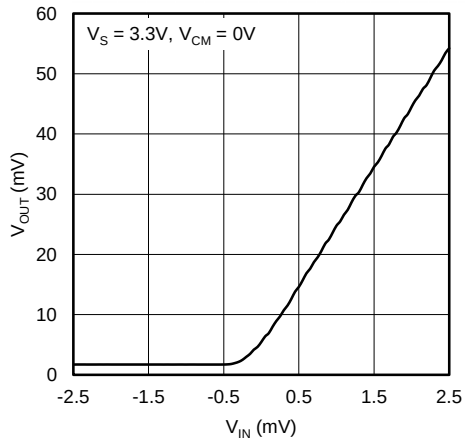


Figure 34. Output Voltage vs. VIN (Zoom Close to 0 V)

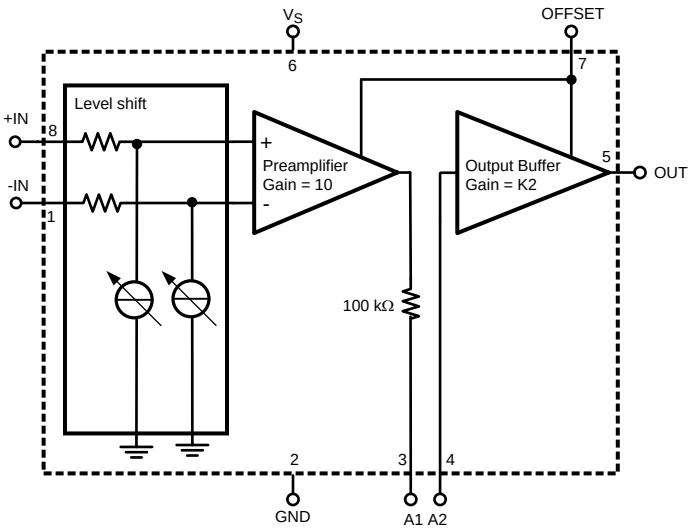
7 Detailed Description

7.1 Overview

The LMP8601 and LMP8601-Q1 are fixed gain differential voltage precision amplifiers with a gain of 20x and a –22-V to +60-V input common-mode voltage range when operating from a single 5-V supply, or a –4-V to +27-V input common-mode voltage range when operating from a single 3.3-V supply. The LMP8601 and LMP8601-Q1 are members of the LMP family and are ideal parts for unidirectional and bidirectional current sensing applications. Because of the proprietary chopping level-shift input stage, the LMP8601 and LMP8601-Q1 achieve very low offset, very low thermal offset drift, and very high CMRR. The LMP8601 and LMP8601-Q1 will amplify and filter small differential signals in the presence of high common-mode voltages.

The LMP8601/LMP8601-Q1 use level shift resistors at the inputs. Because of these resistors, the LMP8601 and LMP8601-Q1 can easily withstand very large differential input voltages that may exist in fault conditions where some other less protected high-performance current sense amplifiers might sustain permanent damage.

7.2 Functional Block Diagram



K2 = 2

7.2.1 Theory of Operation

The schematic shown in the *Functional Block Diagram* gives a basic representation of the internal operation of the LMP8601 and LMP8601-Q1.

The signal on the input pins is typically a small differential voltage developed across a current sensing shunt resistor. The input signal may also appear at a high common-mode voltage. The input signals are accessed through two input resistors that change the voltage into a current. The proprietary chopping level-shift current circuit pulls or pushes current through the input resistors to bring the common-mode voltage behind these resistors within the supply rails.

Subsequently, the signal is gained up by a factor of 10 and brought out on the A1 pin through a trimmed 100-kΩ resistor. In the application, additional gain adjustment or filtering components can be added between the A1 and A2 pins as will be explained in subsequent sections. The signal on the A2 pin is further amplified by a factor of 2 and brought out on the OUT pin.

7.3 Feature Description

7.3.1 Offset Input Pin

The OFFSET pin allows the output signal to be level-shifted to enable bidirectional current sensing. The output signal is bidirectional and mid-rail referenced when the offset pin is connected to the positive supply rail. With the offset pin connected to ground, the output signal is unidirectional and ground-referenced.

Feature Description (continued)

The signal on the A1 and OUT pins is ground-referenced when the offset pin is connected to ground. This means that the output signal can only represent positive values of the current through the shunt resistor, so only currents flowing in one direction can be measured.

When the offset pin is tied to the positive supply rail, the signal on the A1 and OUT pins is referenced to a mid-rail voltage which allows bidirectional current sensing. The operation of the amplifier will be fully bidirectional and symmetrical around 0 V differential at the input pins. The signal at the output will follow this voltage difference multiplied by the gain and at an offset voltage at the output of half V_S.

When the offset pin is connected to an external voltage source, the output signal will be level shifted to that voltage divided by two. In principle, the output signal can be shifted to any voltage between 0 and $V_S/2$ by applying twice that voltage to the OFFSET pin.

NOTE

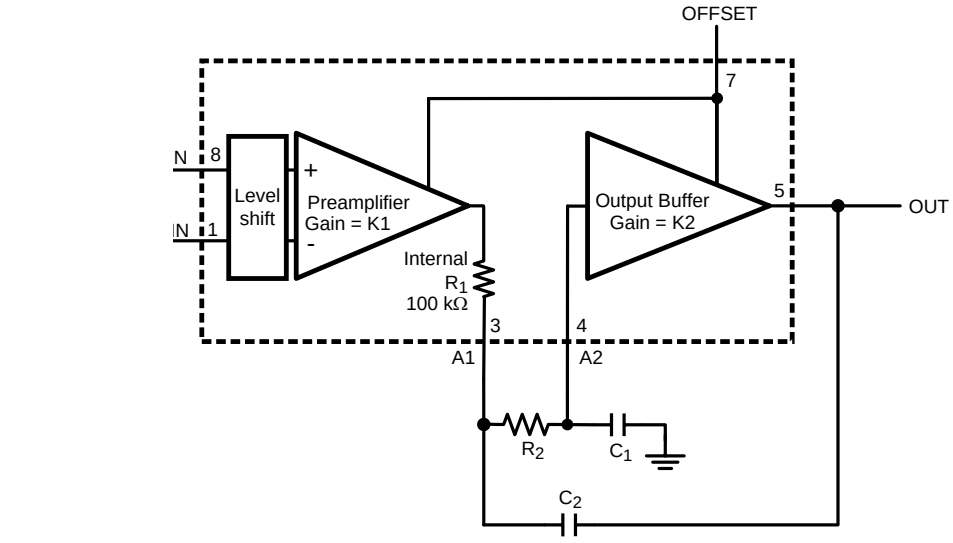
The OFFSET pin has to be driven from a very low-impedance source (<10Ω). This is because the OFFSET pin internally connects directly to the resistive feedback networks of the two gain stages. When the OFFSET pin is driven from a relatively large impedance (e.g. a resistive divider between the supply rails) accuracy will decrease.

Example:

With 5-V supply and a gain of 20x, Offset pin tied to V_S, and a differential input signal of +10 mV will result in 2.7 V at the output pin. Similarly –10 mV at the input will result in 2.3 V at the output pin.

7.3.2 Additional Second Order Lowpass Filter

The LMP8601 and LMP8601-Q1 have a third-order Butterworth lowpass characteristic with a typical bandwidth of 60 kHz integrated in the preamplifier stage. The bandwidth of the output buffer can be reduced by adding a capacitor on the A1 pin to create a first order low pass filter with a time constant determined by the 100-kΩ internal resistor and the external filter capacitor.



K1 = 10, K2 = 2

Figure 35. Second-Order Lowpass Filter

It is also possible to create an additional second-order Sallen-Key low pass filter by adding external components R_2, C_1 and C_2. Together with the internal 100-kΩ resistor R_1 as illustrated in Figure 35, this circuit creates a second-order lowpass filter characteristic.

Feature Description (continued)

When the corner frequency of the additional filter is much lower than 60 kHz, the transfer function of the described amplifier van be written as:

$$H(s) = \frac{K_1 * K_2 \frac{1}{R_1R_2C_1C_2}}{s^2 + s * \left[\frac{1}{R_1C_2} + \frac{1}{R_2C_2} + \frac{(1 - K_2)}{R_2C_1}\right] + \frac{1}{R_1R_2C_1C_2}}$$

where

- K_1 equals the gain of the preamplifier and K_2 that of the buffer amplifier. (1)

Equation 1 can be written in the normalized frequency response for a second-order lowpass filter:

$$G(j\omega) = K_1 * \frac{K_2}{\frac{(j\omega)^2}{\omega_o^2} + \frac{j\omega}{Q\omega_o} + 1} \quad (2)$$

The cutoff frequency ω_o in rad/sec (divide by 2π to get the cut-off frequency in Hz) is given by:

$$\omega_o = \frac{1}{\sqrt{R_1R_2C_1C_2}} \quad (3)$$

and the quality factor of the filter is given by:

$$Q = \frac{\sqrt{R_1R_2C_1C_2}}{R_1C_1 + R_2C_1 + (1 - K_2) * R_1C_2} \quad (4)$$

With K_2 = 2x, Equation 4 transforms results in:

$$Q = \frac{\sqrt{R_1R_2C_1C_2}}{R_1C_1 + R_2C_1 - R_1C_2} \quad (5)$$

With this filter gain K2= 2x, the design procedure can be very simple if the two capacitors are chosen to be equal, C_1=C_2=C. In this case, given the predetermined value of R1 = 100kΩ(the internal resistor), the quality factor is set solely by the value of the resistor R_2.

R_2 can be calculated based on the desired value of Q as the first step of the design procedure with Equation 6:

$$R_2 = \frac{R_1}{Q^2} \quad (6)$$

For instance, the value of Q can be set to 0.5√2 to create a Butterworth response, to 1/√3 to create a Bessel response, or a 0.5 to create a critically damped response. Once the value of R_2 has been found, the second and last step of the design procedure is to calculate the required value of C to give the desired lowpass cut-off frequency using:

$$C = \frac{Q}{R_1\omega_o} \quad (7)$$

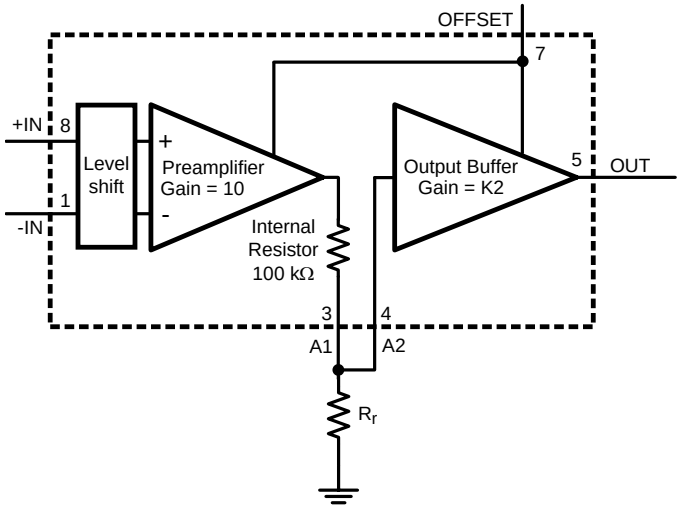
Note that the frequency response achieved using this procedure will only be accurate if the cut-off frequency of the second-order filter is much smaller than the intrinsic 60-kHz lowpass filter. In other words, to have the frequency response of the LMP8601 and LMP8601-Q1 circuit chosen such that the internal poles do not affect the external second order filter.

7.4 Device Functional Modes

7.4.1 Gain Adjustment

The gain of the LMP8601 and LMP8601-Q1 is internal set at 20; however, the overall gain may be adjusted as the signal path between the two internal amplifiers is available on the A1 and A2 pins.

7.4.1.1 Reducing Gain



K2 = 2

Figure 36. Reduce Gain

Figure 36 shows the configuration that can be used to reduce the gain of the LMP8601 and LMP8601-Q1.

R_r creates a resistive divider together with the internal 100-kΩ resistor such that the reduced gain G_r becomes:

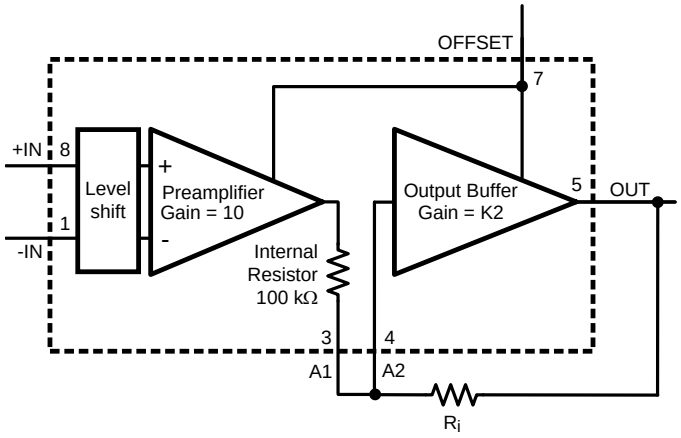
$$G_r = \frac{20\ R_r}{R_r + 100\ k\Omega} \tag{8}$$

Given a desired value of the reduced gain G_r, using this equation the required value for R_r can be calculated with:

$$R_r = 100\ k\Omega\ X\ \frac{G_r}{20 - G_r} \tag{9}$$

Device Functional Modes (continued)

7.4.1.2 Increasing Gain



K2 = 2

Figure 37. Increase Gain

Figure 37 shows the configuration that can be used to increase the gain of the LMP8601 and LMP8601-Q1.

R_i creates positive feedback from the output pin to the input of the buffer amplifier. The positive feedback increases the gain. The increased gain G_i becomes:

$$G_i = \frac{20\ R_i}{R_i - 100\ k\Omega} \tag{10}$$

From this equation, for a desired value of the gain, the required value of R_i can be calculated with:

$$R_i = 100\ k\Omega\ X\ \frac{G_i}{G_i - 20} \tag{11}$$

It should be noted from the equation for the gain G_i that for large gains R_i approaches 100 kΩ. In this case, the denominator in the equation becomes close to zero. In practice, for large gains the denominator will be determined by tolerances in the value of the external resistor R_i and the internal 100-kΩ resistor. In this case, the gain becomes very inaccurate. If the denominator becomes equal to zero, the system will even become instable. TI recommends to limit the application of this technique to gain values of 50 or smaller.

7.4.2 Driving Switched Capacitive Loads

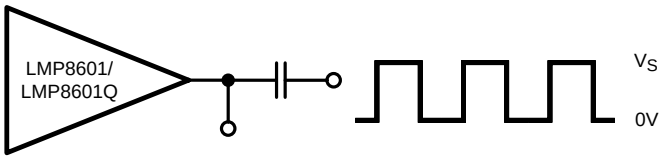


Figure 38. Driving Switched Capacitive Load

Some ADCs load their signal source with a sample and hold capacitor. The capacitor may be discharged prior to being connected to the signal source. If the LMP8601 and LMP8601-Q1 are driving such ADCs the sudden current that should be delivered when the sampling occurs may disturb the output signal. This effect was simulated with the circuit shown in Figure 38 where the output is to a capacitor that is driven by a rail to rail square wave.

This circuit simulates the switched connection of a discharged capacitor to the LMP8601 and LMP8601-Q1 output. The resulting V_{OUT} disturbance signals are shown in Figure 39 and Figure 40.

Device Functional Modes (continued)

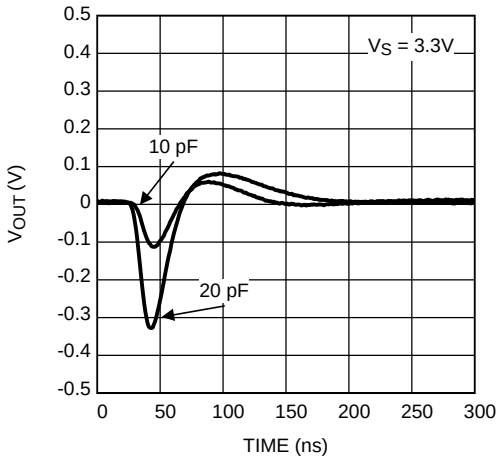


Figure 39. Capacitive Load Response at 3.3 V

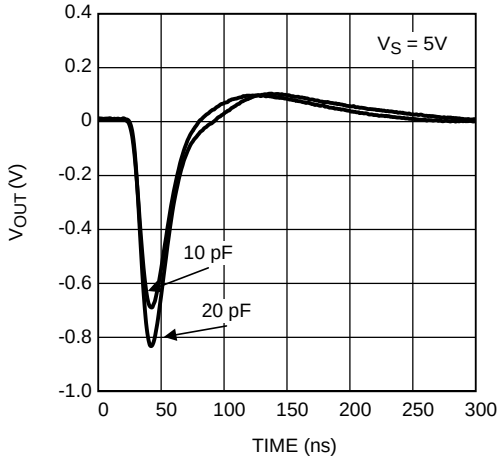


Figure 40. Capacitive Load Response at 5.0 V

These figures can be used to estimate the disturbance that will be caused when driving a switched capacitive load. To minimize the error signal introduced by the sampling that occurs on the ADC input, an additional RC filter can be placed in between the LMP8601 and LMP8601-Q1 and the ADC as illustrated in Figure 41.

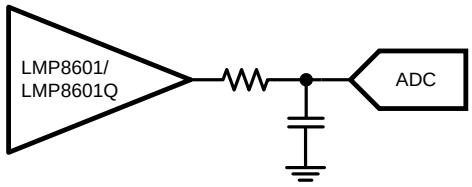


Figure 41. Reduce Error When Driving ADCs

The external capacitor absorbs the charge that flows when the ADC sampling capacitor is connected. The external capacitor should be much larger than the sample and hold capacitor at the input of the ADC and the RC time constant of the external filter should be such that the speed of the system is not affected.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Specifying Performance

To specify the high performance of the LMP8601 and LMP8601-Q1, all minimum and maximum values shown in the parameter tables of this data sheet are 100% tested, and all over temperature limits are also 100% tested over temperature.

8.2 Typical Applications

8.2.1 High-Side, Current-Sensing Application

Figure 42 illustrates the application of the LMP8601 and LMP8601-Q1 in a high-side sensing application. This application is similar to the low-side sensing discussed below, except in this application the common-mode voltage on the shunt drops below ground when the driver is switched off. Because the common-mode voltage range of the LMP8601 and LMP8601-Q1 extends below the negative rail, the LMP8601 and LMP8601-Q1 are also very well suited for this application.

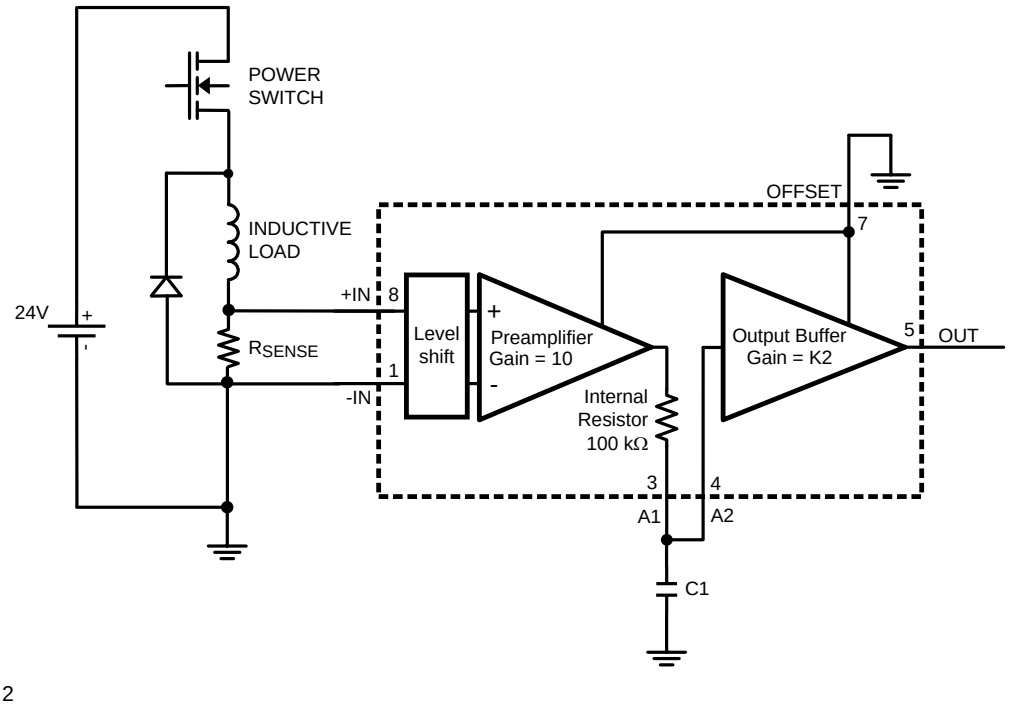


Figure 42. High-Side, Current-Sensing Application

8.2.1.1 Design Requirements

Using the circuit in Figure 42, the requirement is to measure coil current up to 10 A and drive the ADC input to a maximum of 3.3 V. The Offset pin is grounded, so zero current will result in a zero volt output.

Typical Applications (continued)

8.2.1.2 Detailed Design Procedure

First the value of R_{SENSE} needs to be determined. This can be found by dividing the maximum desired output swing by the gain to determine the maximum input voltage:

$$V_{INMAX} = \frac{V_{OUTMAX}}{Gain} = \frac{3.3\ V}{20\ V/V} = 165\ mV \quad (12)$$

Knowing 165 mV must be generated, the ideal value of the sense resistor can be determined through simple ohms law:

$$R_{SENSE} = \frac{V_{INMAX}}{I_{LOADMAX}} = \frac{165\ mV}{10A} = 16.5\ m\Omega \quad (13)$$

The ideal sense resistor value would be 16.5 mΩ. The closest standard value would be 15 mΩ, but this may cause the output to slightly overrange at 10 V. It is recommended to reduce the expected maximum output by a few percent to allow for overloads and component tolerances. The next most popular values would be 10 mΩ, 15 mΩ and 20 mΩ. 10 mΩ would allow for a maximum output of 2 V at 10 A, which may be too low and not utilize the full output range. 20 mΩ would provide more sensitivity, but would limit the maximum current to 8.25 A. 15 mΩ is a good compromise at 11 A maximum and allows for some component tolerance variation.

If a suitable sense resistor value is not available, it is possible to adjust the gain as detailed in the *Gain Adjustment* section.

The sense resistor does dissapate power, so the maximum wattage rating and appropriate power deratings must be observed. In the example above, the sense resistor dissapates 0.165 V × 10 A = 1.65 Watts, so a sense resistor of at least twice the maximum expected power should be used (greater than 4 W).

8.2.1.3 Application Curve

Below is the expected output value using a 15-mΩ sense resistor.

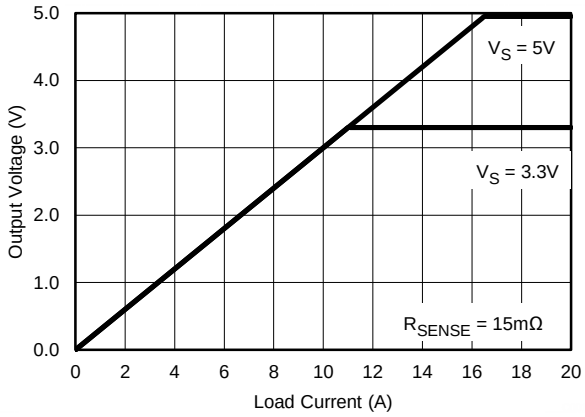


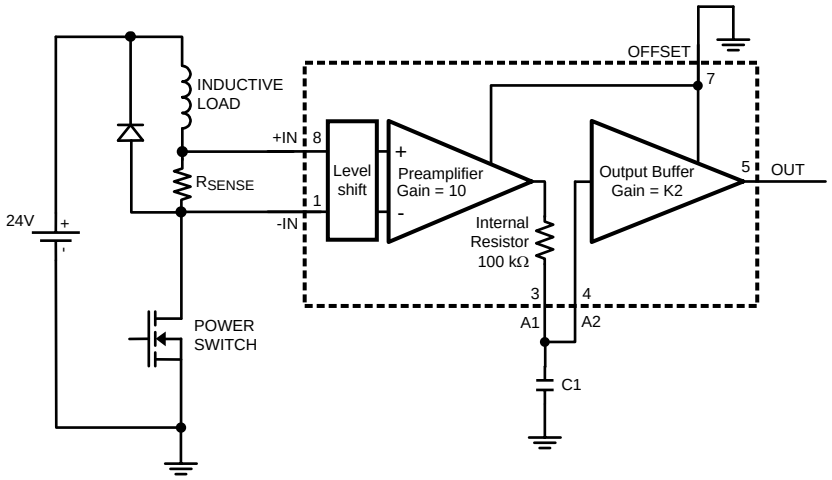
Figure 43. Expected Output Voltage vs. Load Current Using 15-mΩ Sense Resistor

Typical Applications (continued)

8.2.2 Other Applications

8.2.2.1 Low-Side, Current-Sensing Application

Figure 44 illustrates a low-side, current-sensing application with a low-side driver. The power transistor is pulse width modulated to control the average current flowing through the inductive load which is connected to a relatively high battery voltage. The current through the load is measured across a shunt resistor R_{SENSE} in series with the load. When the power transistor is on, current flows from the battery through the inductive load, the shunt resistor and the power transistor to ground. In this case, the common-mode voltage on the shunt is close to ground. When the power transistor is off, current flows through the inductive load, through the shunt resistor and through the freewheeling diode. In this case the common-mode voltage on the shunt is at least one diode voltage drop above the battery voltage. Therefore, in this application the common-mode voltage on the shunt is varying between a large positive voltage and a relatively low voltage. Because the large common-mode voltage range of the LMP8601 and LMP8601-Q1 and because of the high AC common-mode rejection ratio, the LMP8601 and LMP8601-Q1 are very well suited for this application.



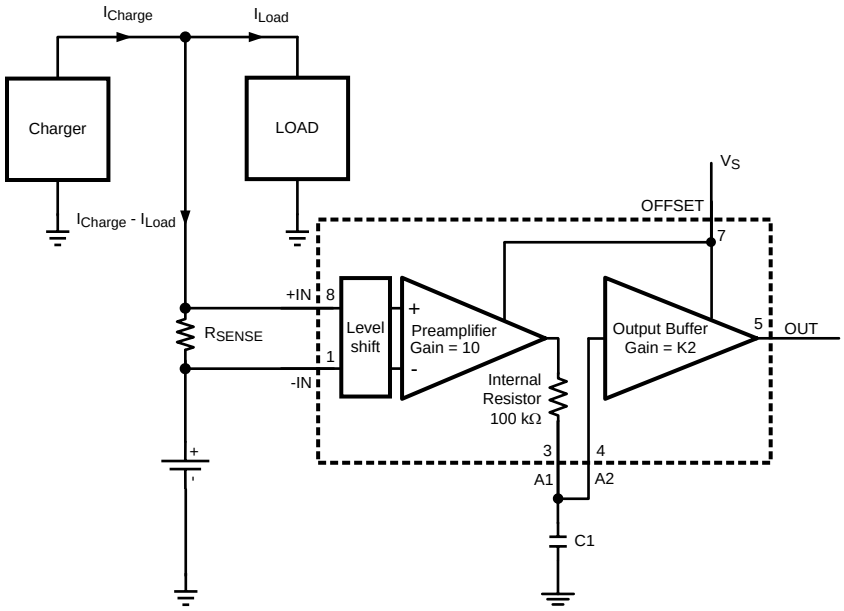
R_{SENSE} = 0.01 Ω, K2 = 2, V_{OUT} = 0.2 V/A

Figure 44. Low-Side Current-Sensing Application

Typical Applications (continued)

8.2.2.2 Battery Current Monitor Application

This application example shows how the LMP8601 and LMP8601-Q1 can be used to monitor the current flowing in and out of a battery pack. The fact that the LMP8601 and LMP8601-Q1 can measure small voltages at a high offset voltage outside the parts own supply range makes this part a very good choice for such applications. If the load current of the battery is higher then the charging current, the output voltage of the LMP8601 and LMP8601-Q1 will be above the *half offset voltage* for a net current flowing out of the battery. When the charging current is higher then the load current the output will be below this “half offset voltage”.



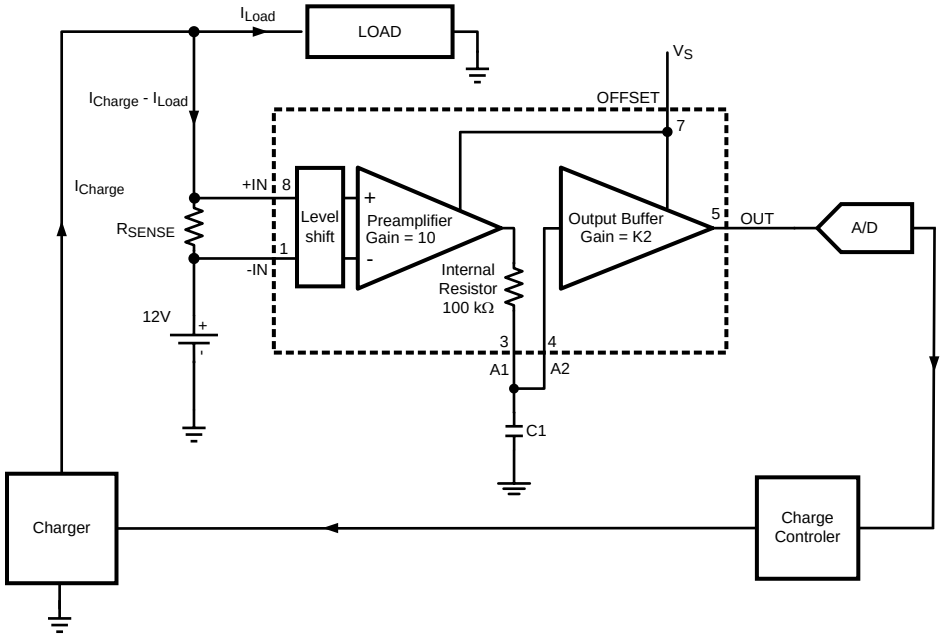
K2 = 2

Figure 45. Battery Current Monitor Application

Typical Applications (continued)

8.2.2.3 Advanced Battery Charger Application

Figure 45 can be used to realize an advanced battery charger that has the capability to monitor the exact net current that flows in and out the battery as show in Figure 46. The output signal of the LMP8601 and LMP8601-Q1 is digitized with the A/D converter and used as an input for the charge controller. The Charge controller can be used to regulate the charger circuit to deliver exactly the current that is required by the load, avoiding overcharging a fully loaded battery.

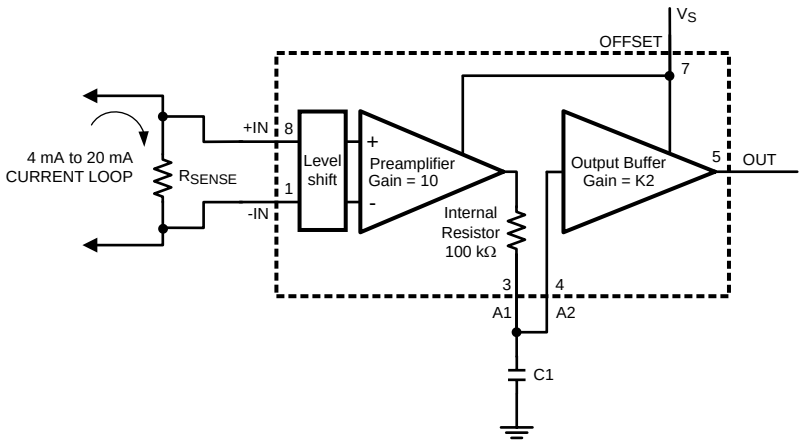


K2 = 2

Figure 46. Advanced Battery Charger Application

8.2.2.4 Current Loop Receiver Application

Many industrial applications use 4-mA to 20-mA transmitters to send an analog value of a sensor to a central control room. The LMP8601 and LMP8601-Q1 can be used as a current loop receiver as shown in Figure 47.



K2 = 2

Figure 47. Current Loop Receiver Application

9 Power Supply Recommendations

In order to decouple the LMP8601 and LMP8601-Q1 from AC noise on the power supply, TI recommends using a 0.1-µF bypass capacitor between the V_S and GND pins. This capacitor should be placed as close as possible to the supply pins. In some cases, an additional 10-µF bypass capacitor may further reduce the supply noise.

10 Layout

10.1 Layout Guidelines

The traces leading to and from the sense resistor can be significant error sources. With small value sense resistors (< 100 mΩ), any trace resistance shared with the load current can cause significant errors.

The amplifier inputs should be directly connected to the sense resistor pads using “Kelvin” or “4-wire” connection techniques. The traces should be one continuous piece of copper from the sense resistor pad to the amplifier input pin pad, and ideally on the same copper layer with minimal vias or connectors. This can be important around the sense resistor if it is generating any significant heat gradients.

To minimize noise pickup and thermal errors, the input traces should be treated as a differential signal pair and routed tightly together with a direct path to the input pins. The input traces should be run away from noise sources, such as digital lines, switching supplies or motor drive lines. Remember that these traces can contain high voltage, and should have the appropriate trace routing clearances.

Since the sense traces only carry the amplifier bias current, the connecting input traces can be thinner, signal level traces. Excessive Resistance in the trace should also be avoided.

The paths of the traces should be identical, including connectors and vias, so that any errors will be equal and cancel.

The sense resistor will heat up as the load increases. As the resistor heats up, the resistance generally goes up, which will cause a change in the readings. The sense resistor should have as much heatsinking as possible to remove this heat through the use of heatsinks or large copper areas coupled to the resistor pads. A reading drifting over time after turnon can usually be traced back to sense resistor heating.

10.2 Layout Example

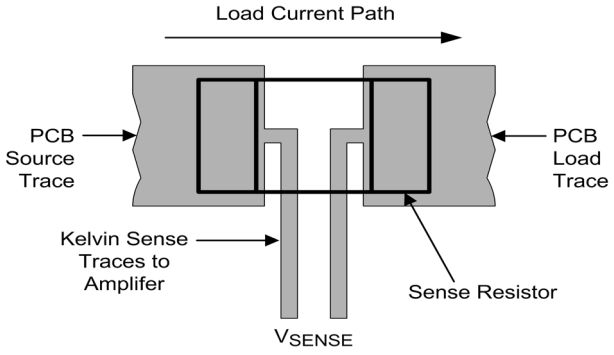


Figure 48. Kelvin or 4–wire Connection to the Sense Resistor

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

LMP8601 TINA SPICE Model, SNOM084

TINA-TI SPICE-Based Analog Simulation Program, http://www.ti.com/tool/tina-ti

Evaluation Board for the LMP8601, http://www.ti.com/tool/lmp8601maeval

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation, see the following:

60-V Common Mode, Fixed Gain, Bidirectional Precision Current-Sensing Amplifier, SNOSB36

11.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LMP8601	Click here	Click here	Click here	Click here	Click here
LMP8601-Q1	Click here	Click here	Click here	Click here	Click here

11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMP8601MA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LMP86 01MA	Samples
LMP8601MAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LMP86 01MA	Samples
LMP8601QMA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LMP86 01QMA	Samples
LMP8601QMAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LMP86 01QMA	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF LMP8601, LMP8601-Q1 :

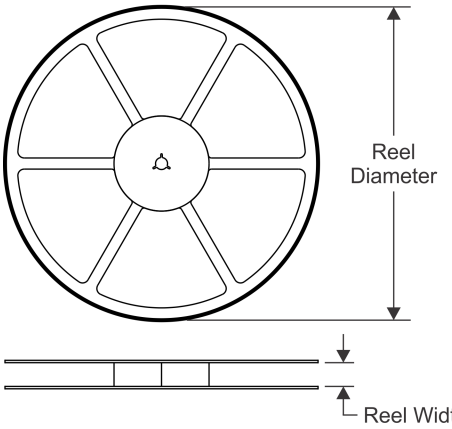
- Catalog: LMP8601
- Automotive: LMP8601-Q1

NOTE: Qualified Version Definitions:

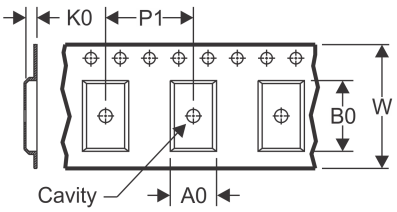
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

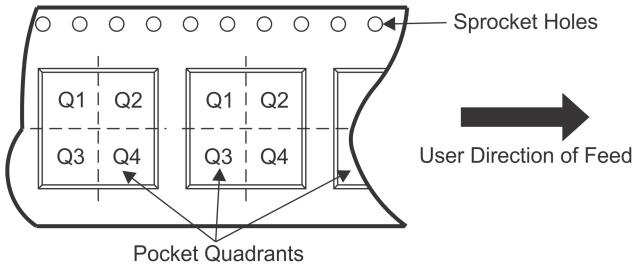


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

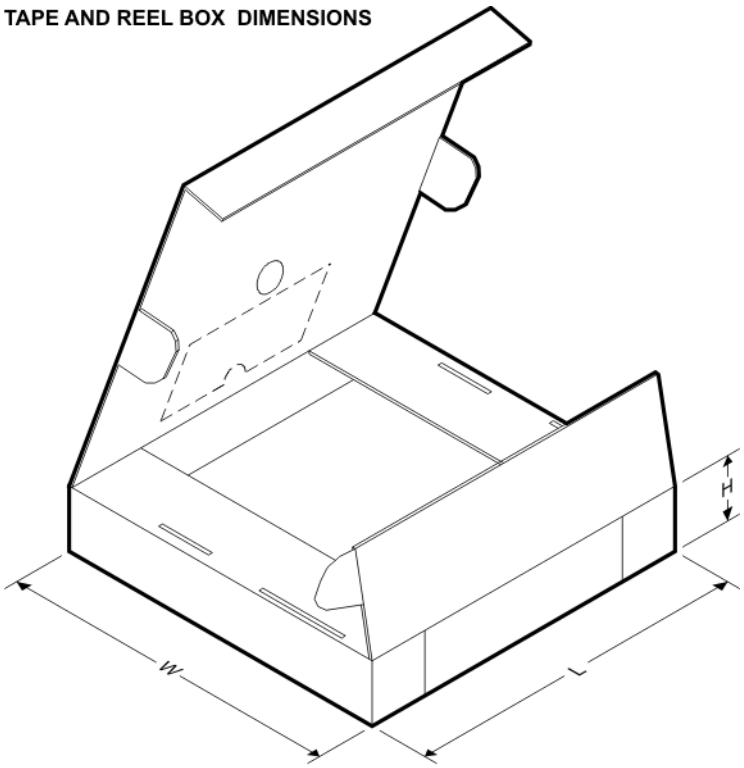
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMP8601MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMP8601QMAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

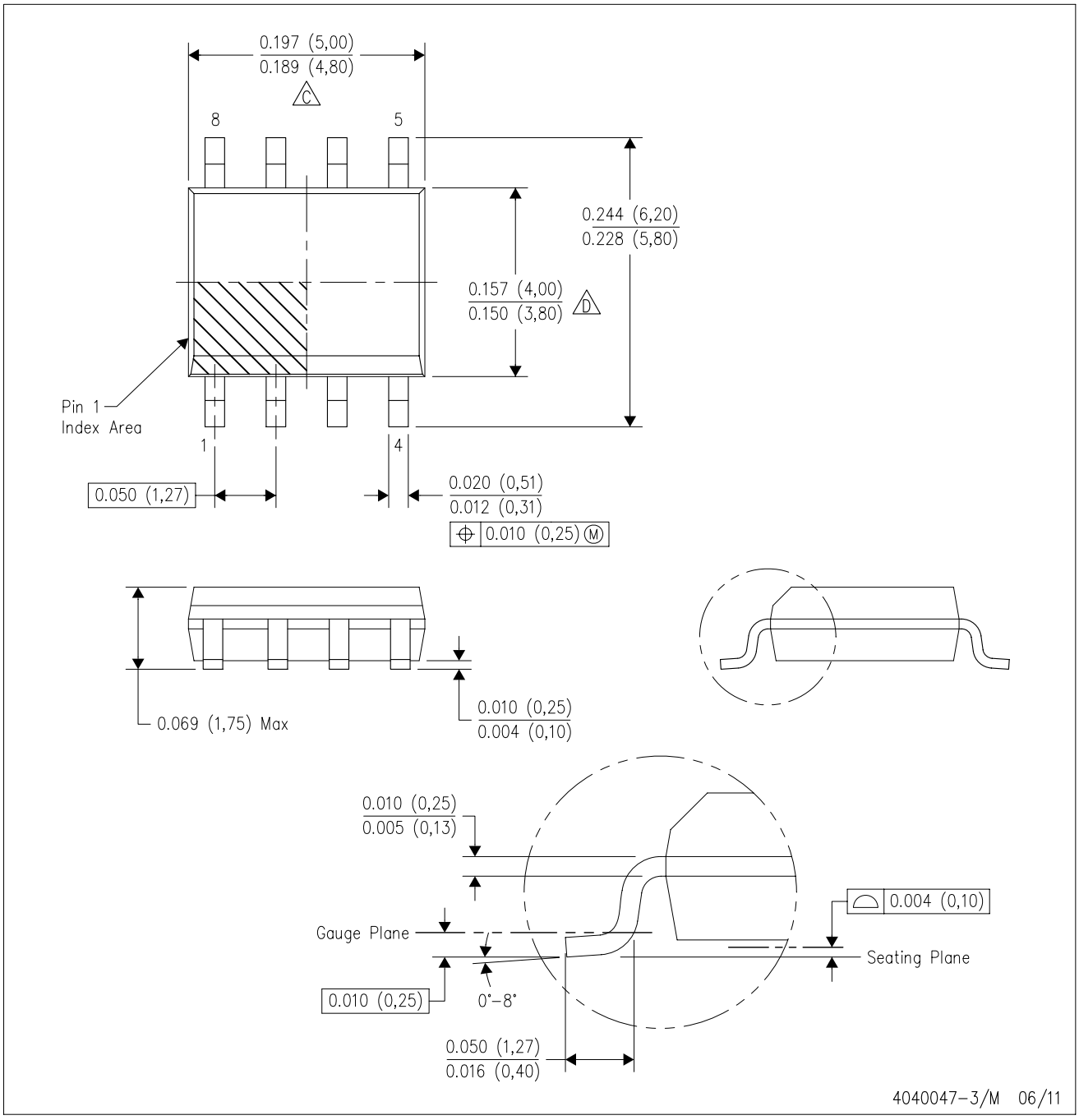
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMP8601MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMP8601QMAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

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