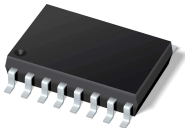


SLLS588C–NOVEMBER 2003–REVISED JANUARY 2008

QUAD DIFFERENTIAL PECL RECEIVERS

FEATURES

- **Functional Replacements for the Agere BRF1A, BRF2A, BRS2A, and BRS2B**
- **Pin Equivalent to General Trade 26LS32**
- **High Input Impedance Approximately 8 kΩ**
- **4-ns Maximum Propagation Delay**
- **TB5R1 Provides 50-mV Hysteresis**
- **TB5R2 With -125-mV Threshold Offset for Preferred State Output**
- **-1.1-V to 7.1-V Common Mode Range**
- **Single 5-V 10% Supply**
- **Slew Rate Limited (1 ns min 80% to 20%)**
- **TB5R2 Output Defaults to Logic 1 When Inputs Left Open or Shorted to V_{CC} or GND**
- **ESD Protection HBM > 3 kV, CDM > 2 kV**
- **Operating Temperature Range: -40C to 85C**
- **Available in Gull-Wing SOIC (JEDEC MS-013, DW) and SOIC (D) Package**

APPLICATIONS

- **Digital Data or Clock Transmission Over Balanced Lines**

DESCRIPTION

These quad differential receivers accept digital data over balanced transmission lines. They translate differential input logic levels to TTL output logic levels.

The TB5R1 is a pin- and function-compatible replacement for the Agere systems BRF1A and BRF2A; it includes 3-kV HBM and 2-kV CDM ESD protection.

The TB5R2 is a pin- and function-compatible replacement for the Agere systems BRS2A and BRS2B and incorporates a 125-mV receiver input offset, preferred state output, 3-kV HBM and 2-kV CDM ESD protection. The TB5R2 preferred state feature places the high state when the inputs are open, shorted to ground, or shorted to the power supply.

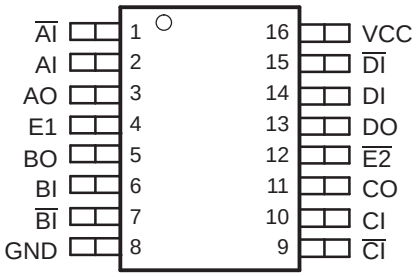
The power-down loading characteristics of the receiver input circuit are approximately 8 kΩ relative to the power supplies; hence they do not load the transmission line when the circuit is powered down.

The packaging for these differential line receivers include a 16-pin gull wing SOIC (DW) and SOIC (D).

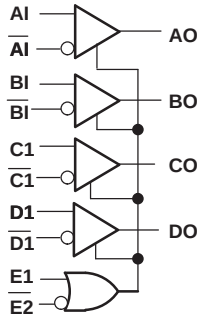
The enable inputs of this device include internal pullup resistors of approximately 40 kΩ that are connected to V_{CC} to ensure a logical high level input if the inputs are open circuited.

PIN ASSIGNMENTS

D PACKAGE
(TOP VIEW)



FUNCTIONAL BLOCK DIAGRAM



Enable Truth Table

E1	$\overline{E2}$	CONDITION
0	0	Active
1	0	Active
0	1	Disabled

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2003–2008, Texas Instruments Incorporated

Enable Truth Table (continued)

E1	$\overline{E2}$	CONDITION
1	1	Active

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

PART NUMBER	PART MARKING	Package	LEAD FINISH	STATUS
TB5R1DW	TB5R1	Gull-Wing SOIC	NiPdAu	Production
TB5R1D	TB5R1	SOIC	NiPdAu	Production
TB5R2DW	TB5R2	Gull-Wing SOIC	NiPdAu	Production
TB5R2D	TB5R2	SOIC	NiPdAu	Production

POWER DISSIPATION RATINGS

PACKAGE	CIRCUIT BOARD MODEL	POWER RATING $T_A \leq 25°C$	THERMAL RESISTANCE, JUNCTION-TO-AMBIENT WITH NO AIR FLOW	DERATING FACTOR(1) $T_A \geq 25°C$	POWER RATING $T_A = 85°C$
D	Low-K(2)	763 mW	131.1°C/W	7.6 mW/°C	305 mW
	High-K(3)	1190 mW	84.1°C/W	11.9 mW/°C	475 mW
DW	Low-K(2)	831 mW	120.3°C/W	8.3 mW/°C	332 mW
	High-K(3)	1240 mW	80.8°C/W	12.4 mW/°C	494 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted with no air flow.
(2) In accordance with the low-K thermal metric definitions of EIA/JESD51-3.
(3) In accordance with the high-K thermal metric definitions of EIA/JESD51-7.

THERMAL CHARACTERISTICs

PARAMETER		PACKAGE	VALUE	UNIT
θ_{JB}	Junction-to-Board Thermal Resistance	D	47.5	°C/W
		DW	53.7	°C/W
θ_{JC}	Junction-to-Case Thermal Resistance	D	44.2	°C/W
		DW	47.1	°C/W

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

			UNIT
Supply voltage, V_{CC}			0 V to 6 V
Magnitude of differential bus (input) voltage, $\lvert V_{AI} - V\rvert$, $\lvert V_{BI} - V\rvert$, $\lvert V_{CI} - V\rvert$, $\lvert V_{DI} - V\rvert$			8.4 V
ESD	Human Body Model(2)	All pins	3 kV
	Charged-Device Model(3)	All pins	2 kV
Continuous power dissipation			See Dissipation Rating Table
Storage temperature, T_{stg}			–65°C to 150°C

(1) Stresses beyond those listed under„ absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under„ recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Tested in accordance with JEDEC Standard 22, Test Method A114-A.
(3) Tested in accordance with JEDEC Standard 22, Test Method C101.

Copyright © 2003–2008, Texas Instruments Incorporated

RECOMMENDED OPERATING CONDITIONS

	MIN	Nom	MAX	UNIT
Supply voltage, V_{CC}	4.5	5	5.5	V
Bus pin input voltage, V_{AI}, V, V_{BI}, V, V_{CI}, V, V_{DI}, V	–1.2 (1)		7.2	V
Magnitude of differential input voltage, $\|V_{AI}$ - V$\|$, $\|V_{BI}$ - V$\|$, $\|V_{CI}$ - V$\|$, $\|V_{DI}$ - V$\|$	0.1		6	V
Operating free-air temperature, T_A	-40		85	°C

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet, unless otherwise noted.

DEVICE ELECTRICAL CHARACTERISTICS

over operating free-air temperature range unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	Supply current (1)	Outputs disabled			40	mA
		Outputs enabled			38	mA

(1) Current is dc power draw as measured through GND pin and does not include power delivered to load.

RECEIVER ELECTRICAL CHARACTERISTICS

over operating free-air temperature range unless otherwise noted

parameter		test conditions		min	typ	max	unit
V_{OL}	Output low voltage	V_{CC} = 4.5 V,	I_{OL} = 8 mA			0.4	V
V_{OH}	Output high voltage	V_{CC} = 4.5 V,	I_{OH} = -400 A	2.4			V
V_{IL}	Low level enable input voltage (1)	V_{CC} = 5.5 V				0.8	V
V_{IH}	High level enable input voltage (1)	V_{CC} = 5.5 V		2			V
V_{IK}	Enable input clamp voltage	V_{CC} = 4.5 V,	I_I = -5 mA			-1 (2)	V
V_{TH+}	Positive-going differential input threshold voltage (1), (V_{xI} - V)	x = A, B, C, or D	TB5R1			100	mV
			TB5R2 (3)			-50	mV
V_{TH-}	Negative-going differential input threshold voltage (1), (V_{xI} - V)	x = A, B, C, or D	TB5R1			-100 (2)	mV
			TB5R2 (3)			-200 (2)	mV
V_{HYST}	Differential input threshold voltage hysteresis, (V_{TH+} - $V_{TH_}$)	TB5R1			50		mV
I_{OZL}	Output off-state current, (High-Z)	V_{CC} = 5.5 V	V_O = 0.4 V			-20 (2)	A
I_{OZH}			V_O = 2.4 V			20	A
I_{OS}	Output short circuit current (4)	V_{CC} = 5.5 V				-100 (2)	mA
I_{IL}	Enable input low current	V_{CC} = 5.5 V,	V_{IN} = 0.4 V			-400 (2)	A
I_{IH}	Enable input high current	V_{CC} = 5.5 V	V_{IN} = 2.7 V			20	A
	Enable input reverse current		V_{IN} = 5.5 V			100	A
II_L	Differential input low current	V_{CC} = 5.5V,	V_{IN} = -1.2 V			-2 (2)	mA
I_{IH}	Differential input high current	V_{CC}= 5.5V,	V_{IN} = 7.2 V			1	mA
R_O	Output resistance				20		Ω

(1) The input levels and difference voltage provide no noise immunity and should be tested only in a static, noise-free environment.
(2) This parameter is listed using a magnitude and polarity/direction convention, rather than an algebraic convention, to match the original Agere data sheet.
(3) Outputs of unused receivers assume a logic 1 level when the inputs are left open. (It is recomended that all unused positive inputs be tied to the positive power supply. No external series resistor is required.)
(4) Test must be performed one lead at a time to prevent damage to the device.

Copyright © 2003–2008, Texas Instruments Incorporated

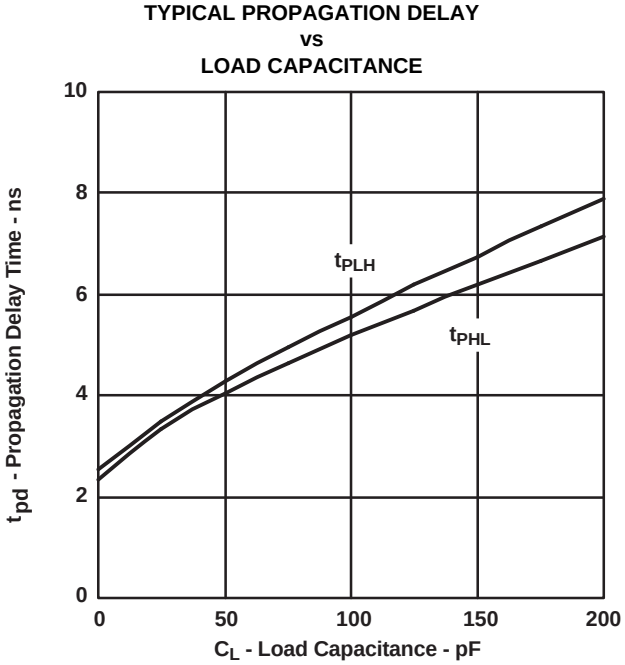
SWITCHING CHARACTERISTICS

over operating free-air temperature range unless otherwise noted

parameter		test conditions	min	typ	max	unit
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 0 pF(1), See Figure 2 and Figure 4		2.5	4	ns
t_{PHL}	Propagation delay time, high-to-low-level output			2.5	4	
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15 pF, See Figure 2 and Figure 4		3	5	ns
t_{PHL}	Propagation delay time, high-to-low-level output			3	5	
t_{PHZ}	Output disable time, high-level-to-high-impedance output(2)	C_L = 5 pF, See Figure 3 and Figure 5		4.1	12	ns
t_{PLZ}	Output disable time, low-level-to-high-impedance output(2)			2.8	12	ns
t_{skew1}	Pulse width distortion, $\|t_{PHL} - t_{PLH}\|$	C_L = 10 pF, See Figure 2 and Figure 4			0.7	ns
		C_L = 150 pF, See Figure 2 and Figure 4			4	ns
$\Delta t_{skew1p-p}$	Part-to-part output waveform skew(3)	C_L = 10 pF, T_A = 75C, See Figure 2 and Figure 4		0.8	1.4	ns
		C_L = 10 pF, T_A = -40C to 85C, See Figure 2 and Figure 4			1.5	ns
Δt_{skew}	Same part output waveform skew(3)	C_L = 10 pF, See Figure 2 and Figure 4			0.3	ns
t_{PZH}	Output enable time, high-impedance-to-high-level output(2)	C_L = 10 pF, See Figure 3 and Figure 4		5	12	ns
t_{PZL}	Output enable time, high-impedance-to-low-level output(2)			4	12	ns
t_{TLH}	Rise time (20%-80%)	C_L = 10 pF, See Figure 2 and Figure 4	1		3.5	ns
t_{THL}	Fall time (80%-20%)		1		3.5	ns

(1) The propagation delay values with a 0 pF load are based on design and simulation.
(2) See Table 1.
(3) Output waveform skews are when devices operate with the same supply voltage at the same temperature and have the same packages and the same test circuits.

TYPICAL CHARACTERISTICS



A. NOTE: This graph is included as an aid to the system designers. Total circuit delay varies with load capacitance. The total delay is the sum of the delay due to external capacitance and the intrinsic delay of the device. Intrinsic delay is listed in the table above as the 0 pF load condition. The incremental increase in delay between the 0 pF load condition and the actual total load capacitance represents the extrinsic, or external delay contributed by the load.

Figure 1. Typical Propagation Delay

Copyright © 2003–2008, Texas Instruments Incorporated

TYPICAL CHARACTERISTICS (continued)

vs
Load Capacitance at 25C

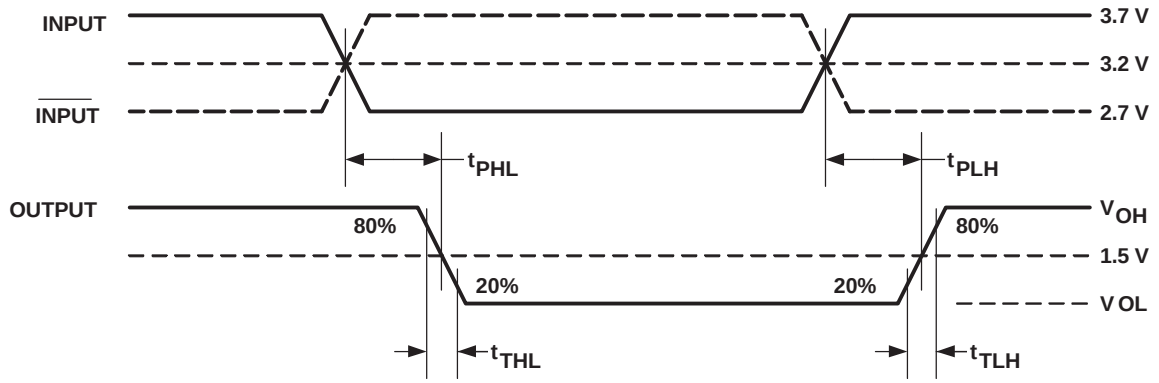
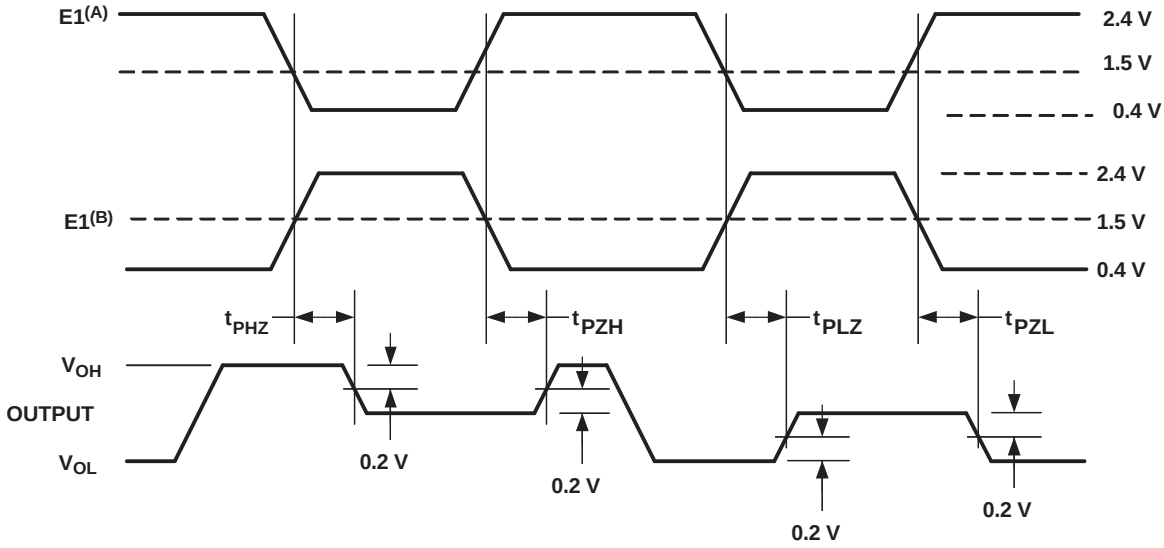


Figure 2. Receiver Propagation Delay Times

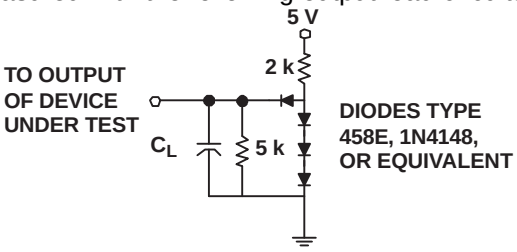


A. $\overline{E2}$ = 1 while E1 changes states.

B. E1 = 0 while $\overline{E2}$ changes states.

Figure 3. Receiver Enable and Disable Timing

Parametric values specified under the Electrical Characteristics and Timing Characteristics sections for the data transmission driver devices are measured with the following output load circuits.

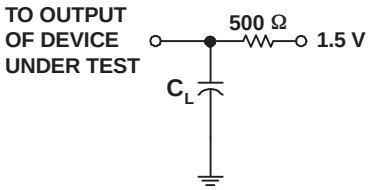


C_L includes test-fixture and probe capacitance.

Figure 4. Receiver Propagation Delay Time and Enable Time (t_{PZH}, t_{PZL}) Test Circuit

Copyright © 2003–2008, Texas Instruments Incorporated

TYPICAL CHARACTERISTICS (continued)



C_L includes test-fixture and probe capacitance.

Figure 5. Receiver Disable Time (t_{PHZ}, t_{PLZ}) Test Circuit

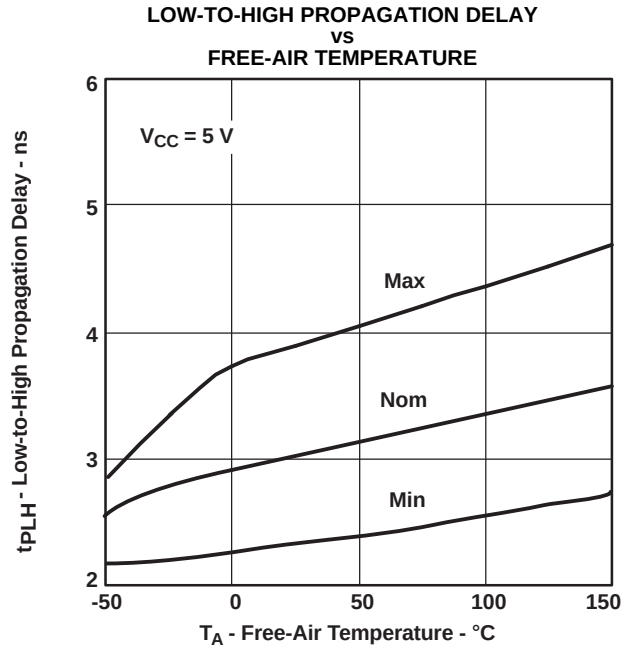


Figure 6.

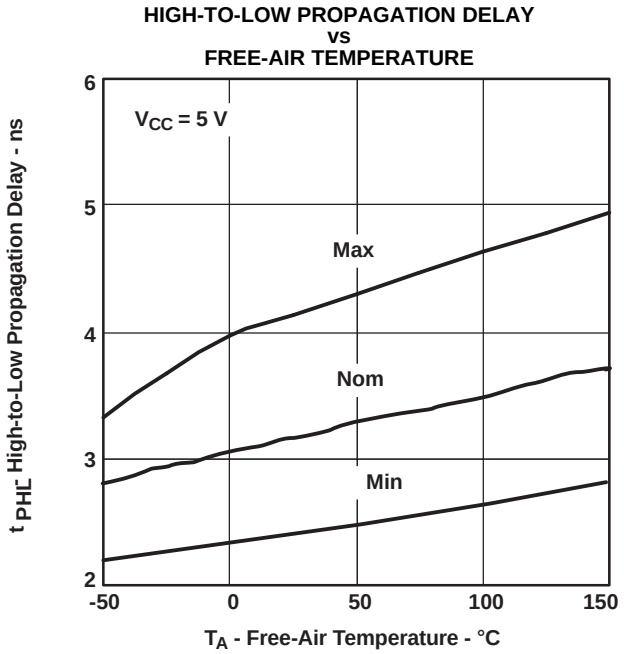


Figure 7.

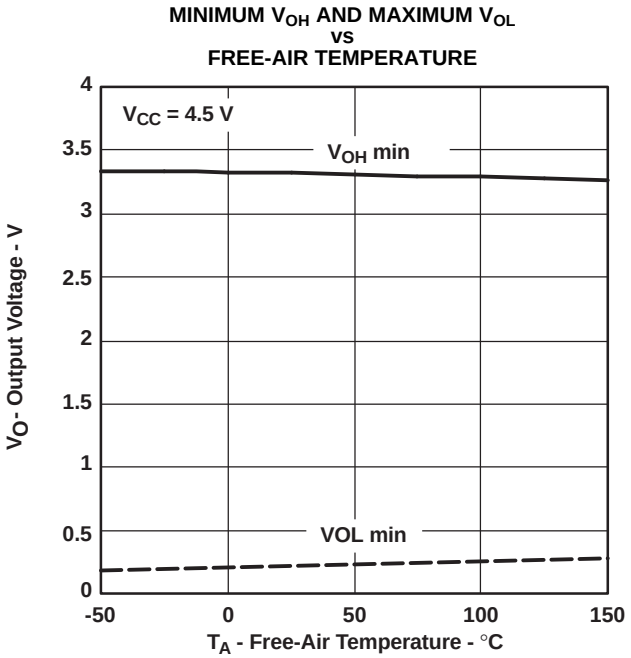


Figure 8.

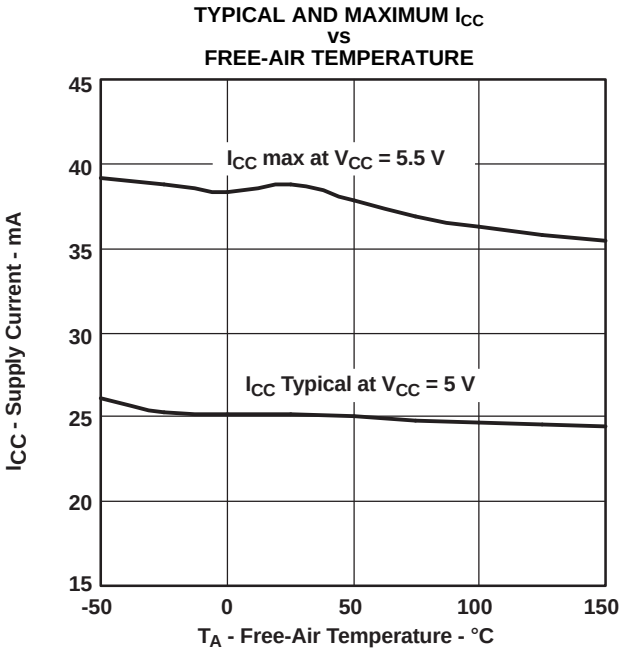


Figure 9.

Copyright © 2003–2008, Texas Instruments Incorporated

APPLICATION INFORMATION

Power Dissipation

The power dissipation rating, often listed as the package dissipation rating, is a function of the ambient temperature, T_A, and the airflow around the device. This rating correlates with the device's maximum junction temperature, sometimes listed in the absolute maximum ratings tables. The maximum junction temperature accounts for the processes and materials used to fabricate and package the device, in addition to the desired life expectancy.

There are two common approaches to estimating the internal die junction temperature, T_J. In both of these methods, the device internal power dissipation P_D needs to be calculated This is done by totaling the supply power(s) to arrive at the system power dissipation:

$$\sum(V_{Sn} \times I_{Sn}) \quad (1)$$

and then subtracting the total power dissipation of the external load(s):

$$\sum(V_{Ln} \times I_{Ln}) \quad (2)$$

The first T_J calculation uses the power dissipation and ambient temperature, along with one parameter: θ_{JA}, the junction-to-ambient thermal resistance, in degrees Celsius per watt.

The product of P_D and θ_{JA} is the junction temperature rise above the ambient temperature. Therefore:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad (3)$$

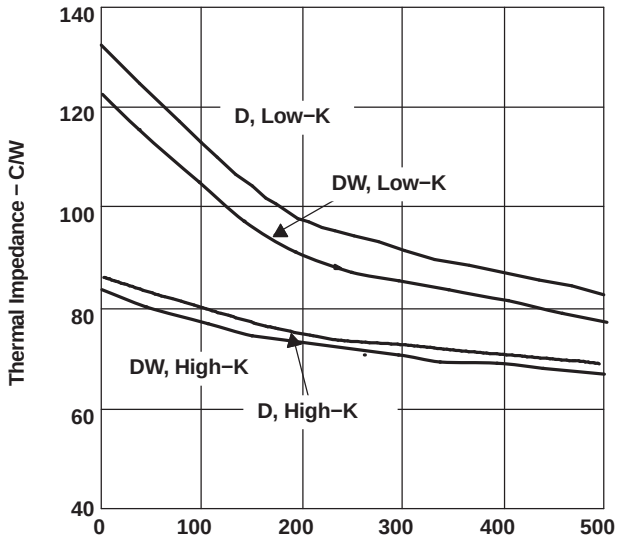


Figure 10. Thermal Impedance vs Air Flow

Note that θ_{JA} is highly dependent on the PCB on which the device is mounted and on the airflow over the device and PCB. JEDEC/EIA has defined standardized test conditions for measuring θ_{JA}. Two commonly used conditions are the low-K and the high-K boards, covered by EIA/JESD51-3 and EIA/JESD51-7 respectively. Figure 10 shows the low-K and high-K values of θ_{JA} versus air flow for this device and its package options.

The standardized θ_{JA} values may not accurately represent the conditions under which the device is used. This can be due to adjacent devices acting as heat sources or heat sinks, to nonuniform airflow, or to the system PCB having significantly different thermal characteristics than the standardized test PCBs. The second method of system thermal analysis is more accurate. This calculation uses the power dissipation and ambient temperature, along with two device and two system-level parameters:

- θ_{JC}, the junction-to-case thermal resistance, in degrees Celsius per watt
- θ_{JB}, the junction-to-board thermal resistance, in degrees Celsius per watt
- θ_{CA}, the case-to-ambient thermal resistance, in degrees Celsius per watt
- θ_{BA}, the board-to-ambient thermal resistance, in degrees Celsius per watt.

In this analysis, there are two parallel paths, one through the case (package) to the ambient, and another through the device to the PCB to the ambient. The system-level junction-to-ambient thermal impedance, $\theta_{JA(S)}$, is the equivalent parallel impedance of the two parallel paths:

$$T_J = T_A + \left(P_D \times \theta_{JA(S)}\right) \quad (4)$$

where

$$\theta_{JA(S)} = \frac{\left[\left(\theta_{JC} + \theta_{CA}\right) \times \left(\theta_{JB} + \theta_{BA}\right)\right]}{\left(\theta_{JC} + \theta_{CA} + \theta_{JB} + \theta_{BA}\right)} \quad (5)$$

The device parameters θ_{JC} and θ_{JB} account for the internal structure of the device. The system-level parameters θ_{CA} and θ_{BA} take into account details of the PCB construction, adjacent electrical and mechanical components, and the environmental conditions including airflow. Finite element (FE), finite difference (FD), or computational fluid dynamics (CFD) programs can determine θ_{CA} and θ_{BA}. Details on using these programs are beyond the scope of this data sheet, but are available from the software manufacturers.

Copyright © 2003–2008, Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TB5R1D	ACTIVE	SOIC	D	16	40	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1YEAR/ Level-1-220C-UNLIM	-40 to 85	TB5R1	Samples
TB5R1DE4	ACTIVE	SOIC	D	16	40	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1YEAR/ Level-1-220C-UNLIM	-40 to 85	TB5R1	Samples
TB5R1DW	ACTIVE	SOIC	DW	16	40	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1YEAR/ Level-1-220C-UNLIM	-40 to 85	TB5R1	Samples
TB5R1DWR	ACTIVE	SOIC	DW	16	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1YEAR/ Level-1-220C-UNLIM	-40 to 85	TB5R1	Samples
TB5R2D	ACTIVE	SOIC	D	16	40	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1YEAR/ Level-1-220C-UNLIM	-40 to 85	TB5R2	Samples
TB5R2DW	ACTIVE	SOIC	DW	16	40	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1YEAR/ Level-1-220C-UNLIM	-40 to 85	TB5R2	Samples
TB5R2DWR	ACTIVE	SOIC	DW	16	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1YEAR/ Level-1-220C-UNLIM	-40 to 85	TB5R2	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

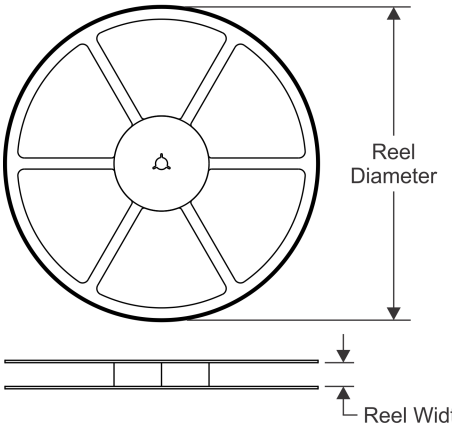
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

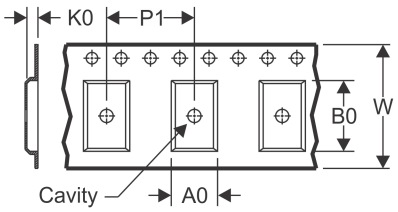
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

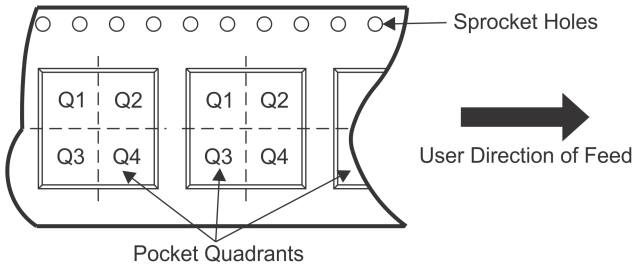


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

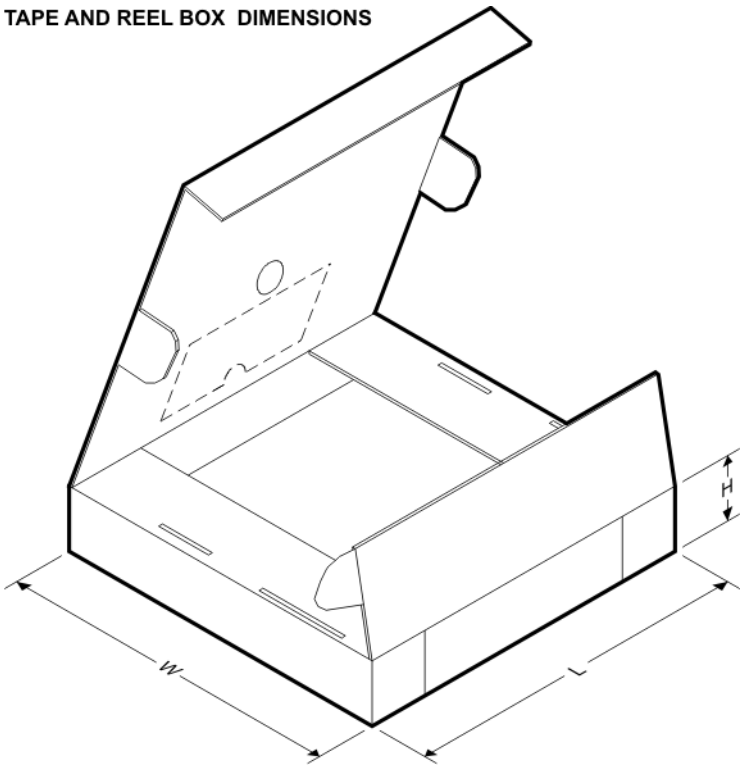
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TB5R1DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
TB5R2DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

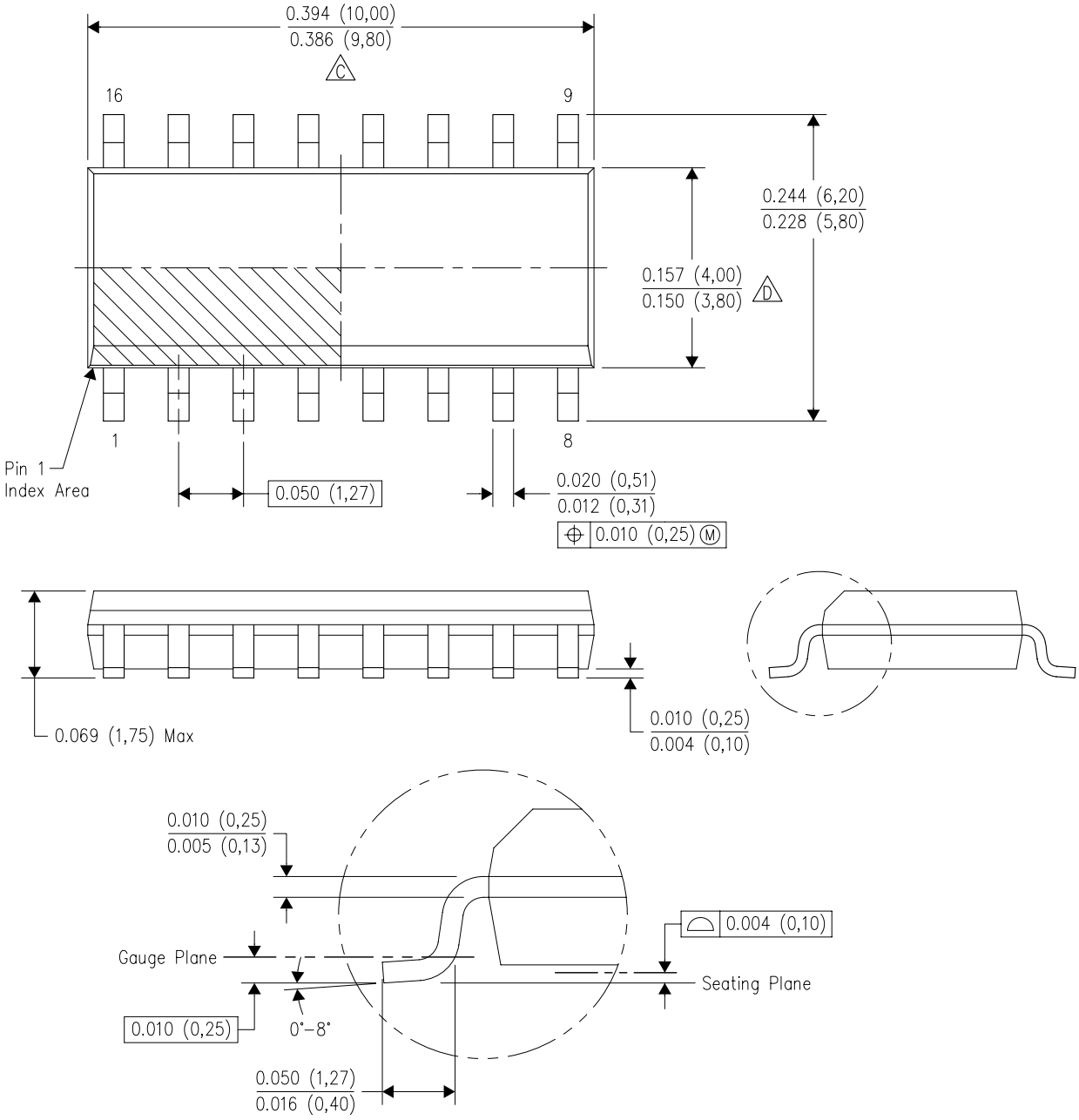
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

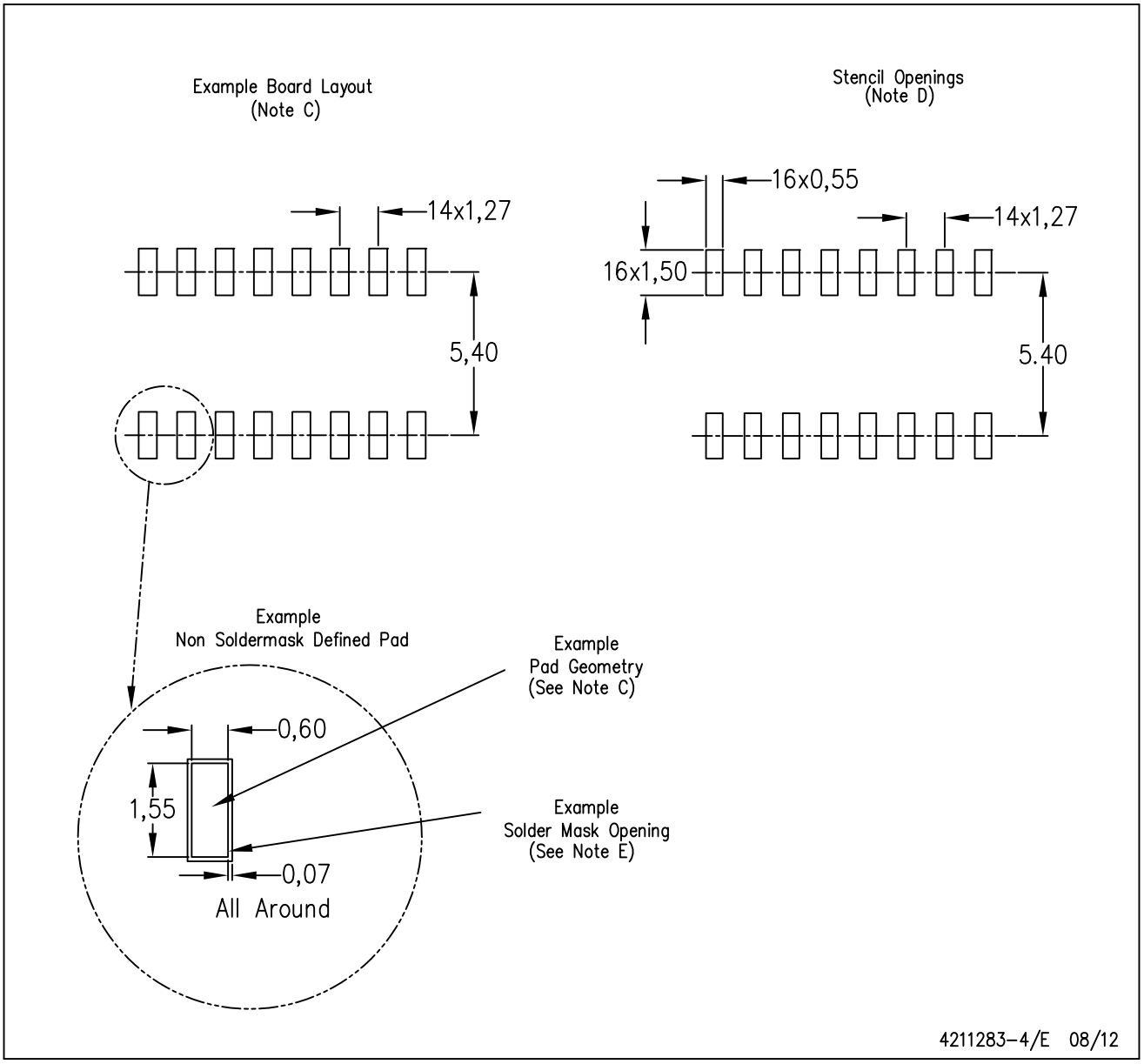
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TB5R1DWR	SOIC	DW	16	2000	367.0	367.0	38.0
TB5R2DWR	SOIC	DW	16	2000	367.0	367.0	38.0

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



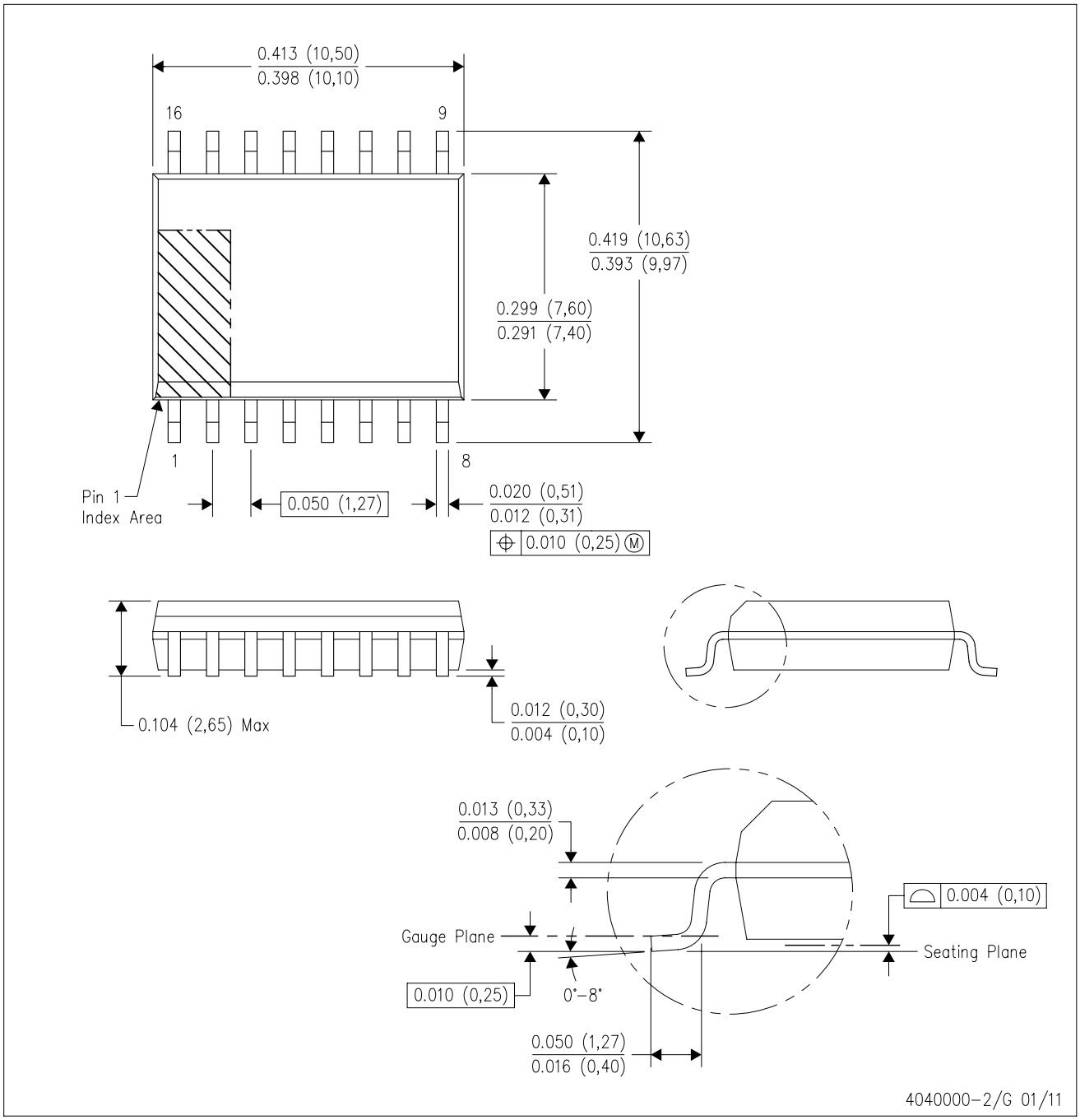
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



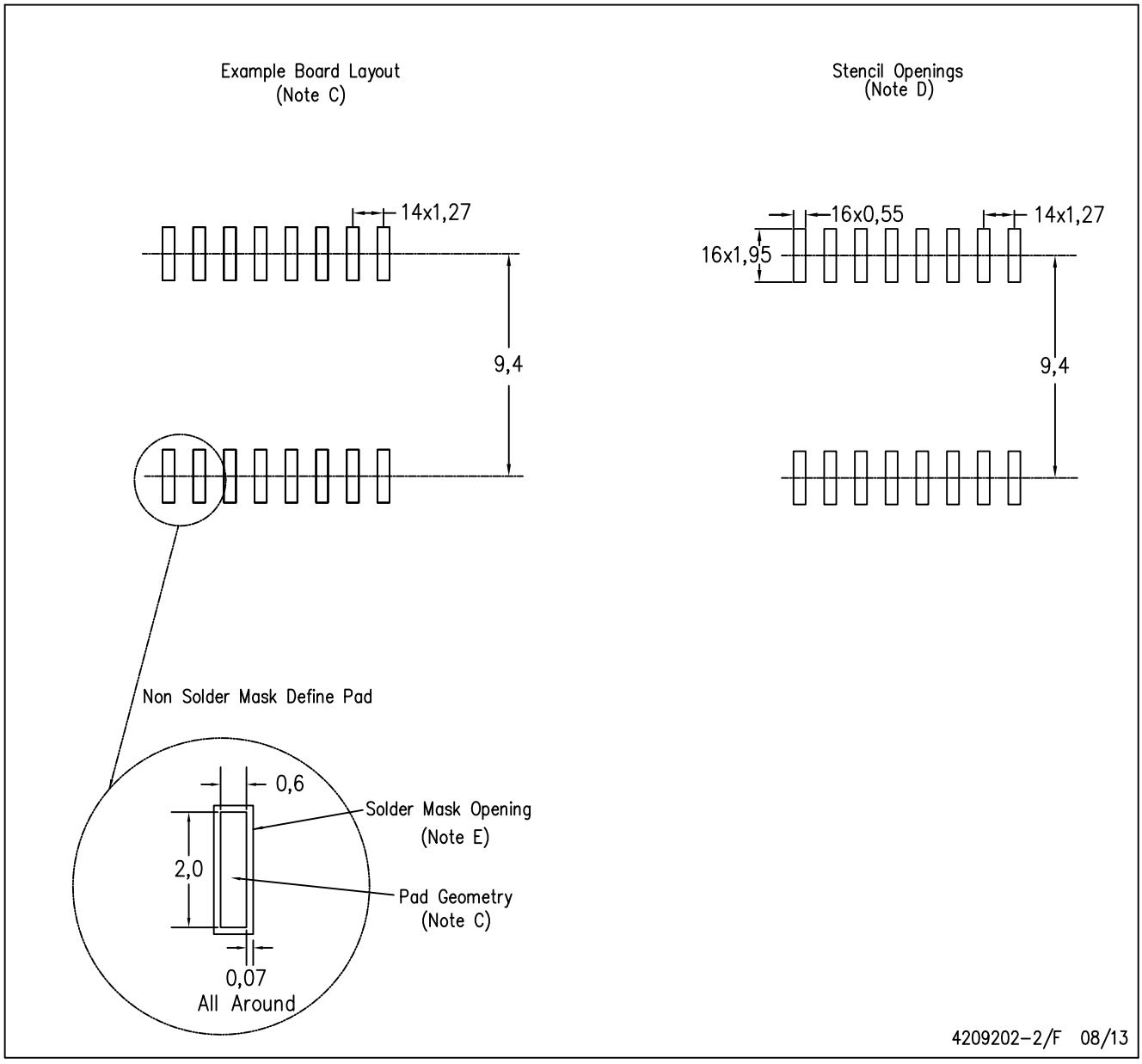
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DW (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AA.

DW (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Refer to IPC7351 for alternate board design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2015, Texas Instruments Incorporated