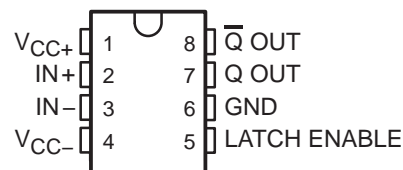
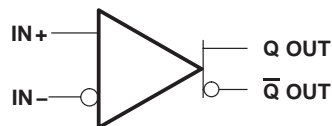


- Ultra-Fast Operation . . . 10 ns (typ)
- Low Positive Supply Current
12.7 mA (Typ)
- Operates From a Single 5-V Supply or From a Split ± 5 -V Supply
- Complementary Outputs
- Input Common-Mode Voltage Includes Negative Rail
- Low Offset Voltage
- No Minimum Slew Rate Requirement
- Output Latch Capability
- Functional Replacement to the LT1116

D AND PW PACKAGE
(TOP VIEW)



symbol (each comparator)



description

The TL3116 is an ultra-fast comparator designed to interface directly to TTL logic while operating from either a single 5-V power supply or dual ± 5 -V supplies. The input common-mode voltage extends to the negative rail for ground sensing applications. It features extremely tight offset voltage and high gain for precision applications. It has complementary outputs that can be latched using the LATCH ENABLE terminal. Figure 1 shows the positive supply current of the comparator. The TL3116 only requires 12.7 mA (typical) to achieve a propagation delay of 10 ns.

The TL3116 is a pin-for-pin functional replacement for the LT1116 comparator, offering high-speed operation but consuming much less power.

POSITIVE SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

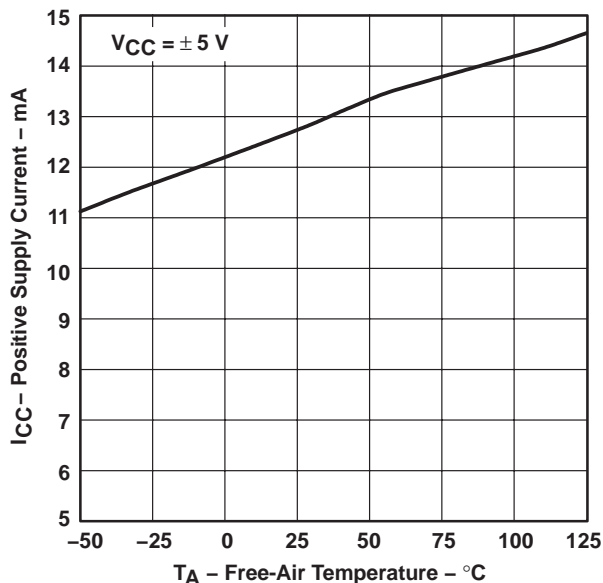


Figure 1

AVAILABLE OPTIONS

T _A	PACKAGED DEVICES		CHIP FORM [‡] (Y)
	SMALL OUTLINE [†] (D)	TSSOP (PW)	
0°C to 70°C	TL3116CD	TL3116CPWLE	TL3116Y
-40°C to 85°C	TL3116ID	TL3116IPWLE	—

[†] The PW packages are available left-ended taped and reeled only.

[‡] Chip forms are tested at T_A = 25°C only.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

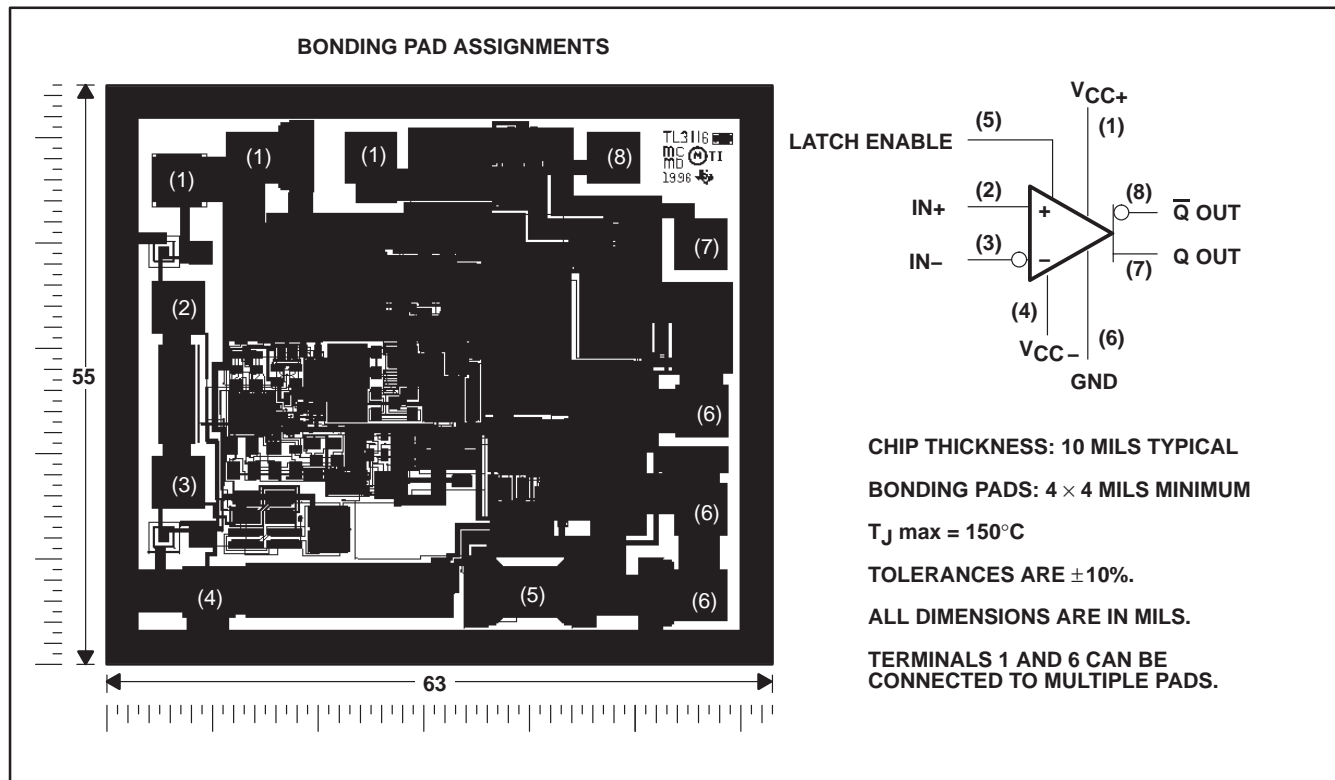


TL3116, TL3116Y ULTRA-FAST LOW-POWER PRECISION COMPARATORS

SLCS132C – MARCH 1997 – REVISED MAY 1997

TL3116Y chip information

This chip, when properly assembled, displays characteristics similar to the TL3116C. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.



COMPONENT COUNT	
Bipolars	53
MOSFETs	49
Resistors	46
Capacitors	14

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1)	– 7 V to 7 V
Differential input voltage, V_{ID} (see Note 2)	7 V
Input voltage range, V_I	7 V
Input voltage, V_I (LATCH ENABLE)	7 V
Output current, I_O	± 20 mA
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A	–40°C to 85°C
Storage temperature range, T_{stg}	– 65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
 2. Differential voltages are at IN+ with respect to IN–.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW
PW	525 mW	4.2 mW/°C	336 mW

TL3116, TL3116Y

ULTRA-FAST LOW-POWER PRECISION COMPARATORS

SLCS132C – MARCH 1997 – REVISED MAY 1997

electrical characteristics at specified operating free-air temperature, $V_{DD} = \pm 5\text{ V}$, $V_{LE} = 0$ (unless otherwise noted)

PARAMETER		TEST CONDITION†	TL3116C			TL3116I			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IO}	Input offset voltage	$T_A = 25^\circ\text{C}$		0.5	3		0.5	3	mV
		$T_A = \text{full range}$			3.5			3.5	
α_{VIO}	Temperature coefficient of input offset voltage			-2.5			-2.8	$\mu\text{V}/^\circ\text{C}$	
I_{IO}	Input offset current	$T_A = 25^\circ\text{C}$		0.1	0.2		0.1	0.2	μA
		$T_A = \text{full range}$			0.3			0.35	
I_{IB}	Input bias current	$T_A = 25^\circ\text{C}$		0.7	1.1		0.7	1.1	μA
		$T_A = \text{full range}$			1.2			1.5	
V_{ICR}	Common-mode input voltage range	$V_{DD} = \pm 5\text{ V}$	-5		2.5	-5		2.5	V
		$V_{DD} = 5\text{ V}$	0		2.5	0		2.5	
CMRR	Common-mode rejection ratio	$-5 \leq V_{IC} \leq 2.5\text{ V}$	75	100		75	100	dB	
k_{SVR}	Supply-voltage rejection ratio	Positive supply: $4.6\text{ V} \leq +V_{DD} \leq 5.4\text{ V}$, $T_A = 25^\circ\text{C}$	60	80		60	80	dB	
		Negative supply: $-7\text{ V} \leq -V_{DD} \leq -2\text{ V}$, $T_A = 25^\circ\text{C}$	80	100		80	100		
V_{OL}	Low-level output voltage	$I_{(\text{sink})} = 4\text{ mA}$, $T_A = 25^\circ\text{C}$, $V_+ \leq 4.6\text{ V}$		400	600		400	600	mV
		$I_{(\text{sink})} = 10\text{ mA}$, $T_A = 25^\circ\text{C}$, $V_+ \leq 4.6\text{ V}$		750			750		
V_{OH}	High-level output voltage	$V_+ \leq 4.6\text{ V}$, $T_A = 25^\circ\text{C}$, $I_O = 1\text{ mA}$	3.6	3.9		3.6	3.9	V	
		$V_+ \leq 4.6\text{ V}$, $T_A = 25^\circ\text{C}$, $I_O = 10\text{ mA}$	3.4	3.8		3.4	3.8		
I_{CC}	Positive supply current	$T_A = \text{full range}$		12.7	14.7		12.7	15	mA
	Negative supply current			-2.6			-3		
V_{IL}	Low-level input voltage (LATCH ENABLE)			0.8			0.8	V	
V_{IH}	High-level input voltage (LATCH ENABLE)		2			2		V	
I_{IL}	Low-level input current (LATCH ENABLE)	$V_{LE} = 0$		0	1		0	1	μA
		$V_{LE} = 2\text{ V}$		24	39		24	45	μA

† Full range for the TL3116C is $T_A = 0^\circ\text{C}$ to 70°C . Full range for the TL3116I is $T_A = -40^\circ\text{C}$ to 85°C .

‡ All typical values are measures with $T_A = 25^\circ\text{C}$.



switching characteristics, $V_{DD} = \pm 5\text{ V}$, $V_{LE} = 0$

PARAMETER	TEST CONDITION†		TL3116C			TL3116I			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{pd1} Propagation delay time‡	$\Delta V_I = 100\text{ mV}$, $V_{OD} = 5\text{ mV}$	$T_A = 25^\circ\text{C}$	9.9	12		9.9	12	ns	
		$T_A = \text{full range}$	9.9	14		9.9	15		
	$\Delta V_I = 100\text{ mV}$, $V_{OD} = 20\text{ mV}$	$T_A = 25^\circ\text{C}$	8.2	10.3		8.2	10.3		
		$T_A = \text{full range}$	8.2	12.7		8.2	13.7		
$t_{sk(p)}$ Pulse skew ($t_{pd+} - t_{pd-}$)	$\Delta V_I = 100\text{ mV}$, $T_A = 25^\circ\text{C}$	$V_{OD} = 5\text{ mV}$	0.5			0.5	ns		
t_{su} Setup time, LATCH ENABLE			3.4			3.4	ns		

† Full range for the TL3116C is 0°C to 70°C . Full range for the TL3116I is -40°C to 85°C .

‡ t_{pd1} cannot be measured in automatic handling equipment with low values of overdrive. The TL3116 is 100% tested with a 1-V step and 500-mV overdrive at $T_A = 25^\circ\text{C}$ only. Correlation tests have shown that t_{pd1} limits given can be ensured with this test, if additional dc tests are performed to ensure that all internal bias conditions are correct. For low overdrive conditions, V_{OS} is added to the overdrive.

TYPICAL CHARACTERISTICS

Table of Graphs

		FIGURE	
I_{CC}	Positive supply current	vs Input voltage	2
		vs Frequency	3
		vs Free-air temperature	4
I_{CC}	Negative supply current	vs Free-air temperature	5
t_{pd}	Propagation delay time	vs Overdrive voltage	6
		vs Supply voltage	7
		vs Input impedance	8
		vs Load capacitance	9
		vs Free-air temperature	10
V_{IC}	Common-mode input voltage	vs Free-air temperature	11
V_{IT}	Input threshold voltage (LATCH ENABLE)	vs Free-air temperature	12
V_O	Output voltage	vs Output source current	13
		vs Output sink current	14
I_I	Input current (LATCH ENABLE)	vs Input voltage	15

TYPICAL CHARACTERISTICS

**POSITIVE SUPPLY CURRENT
 vs
 INPUT VOLTAGE**

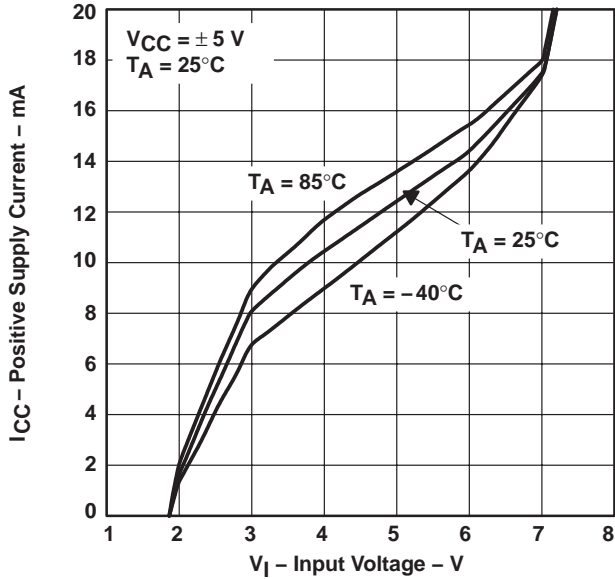


Figure 2

**POSITIVE SUPPLY CURRENT
 vs
 FREQUENCY**

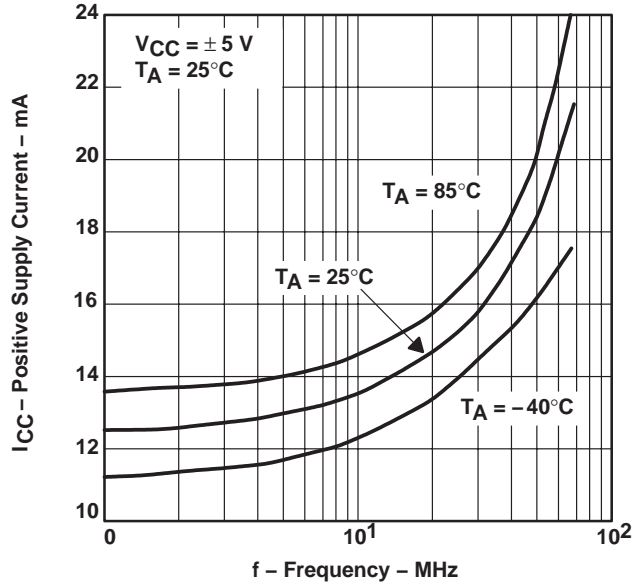


Figure 3

**POSITIVE SUPPLY CURRENT
 vs
 FREE-AIR TEMPERATURE**

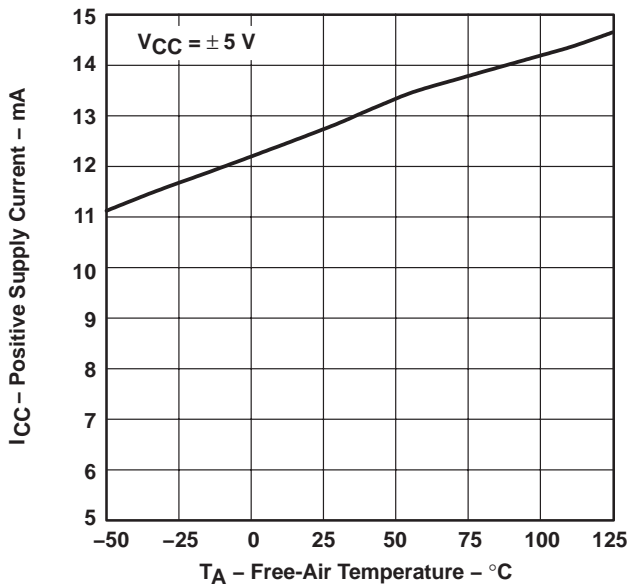


Figure 4

**NEGATIVE SUPPLY CURRENT
 vs
 FREE-AIR TEMPERATURE**

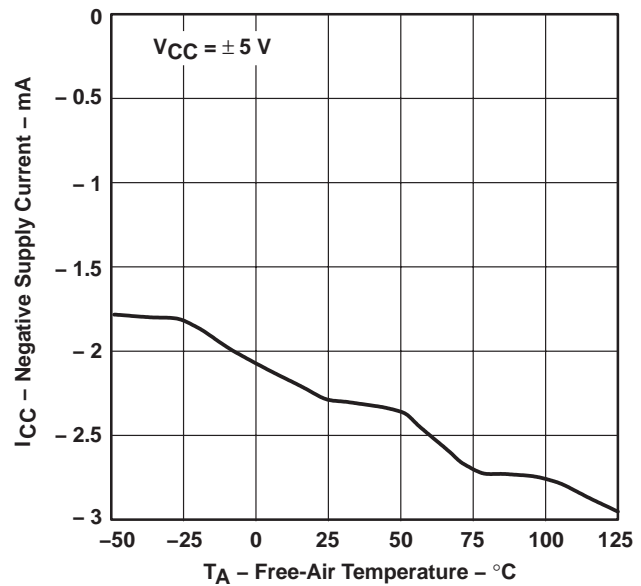


Figure 5

TYPICAL CHARACTERISTICS

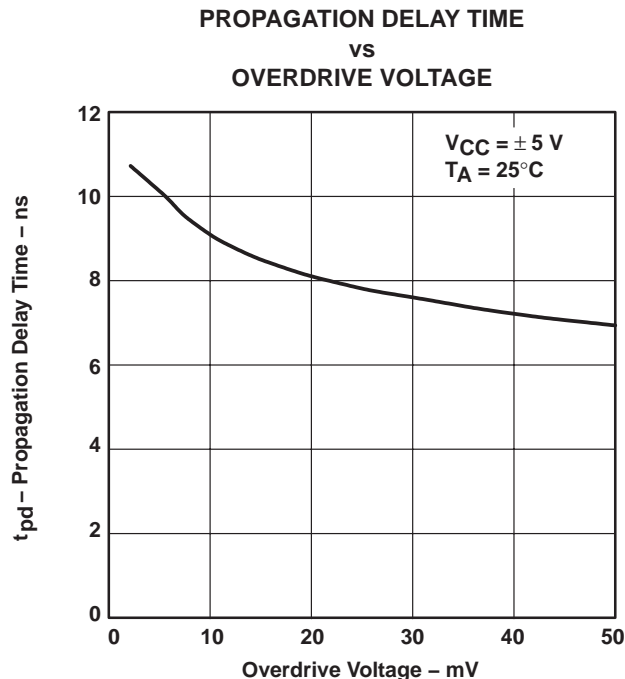


Figure 6

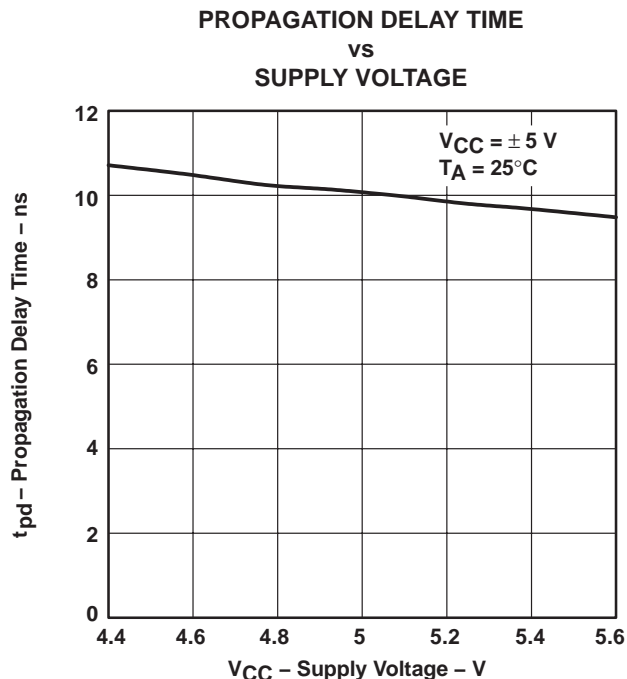


Figure 7

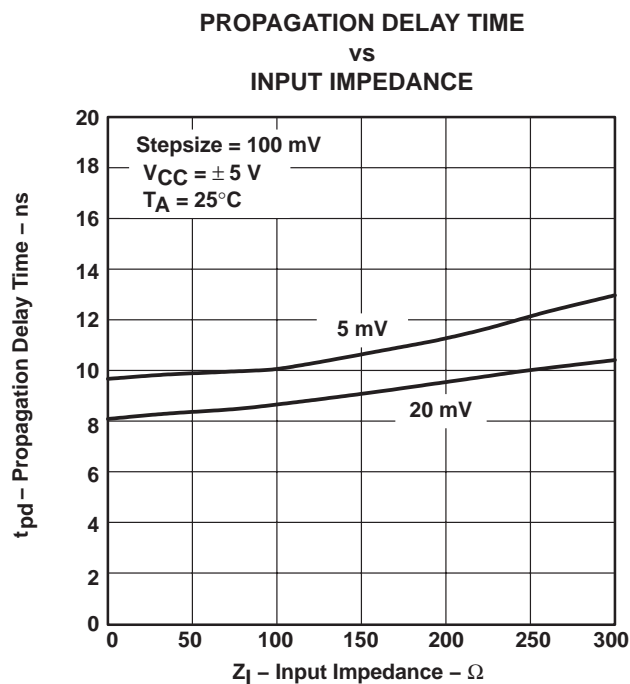


Figure 8

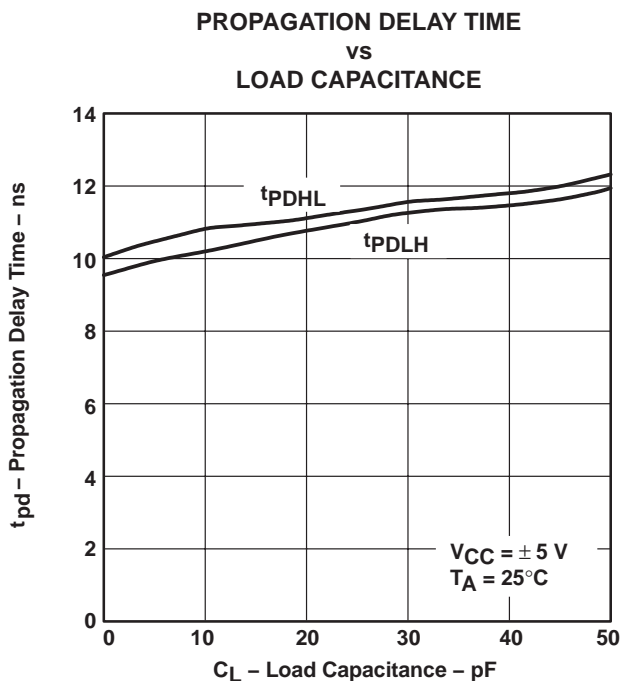


Figure 9

TYPICAL CHARACTERISTICS

PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

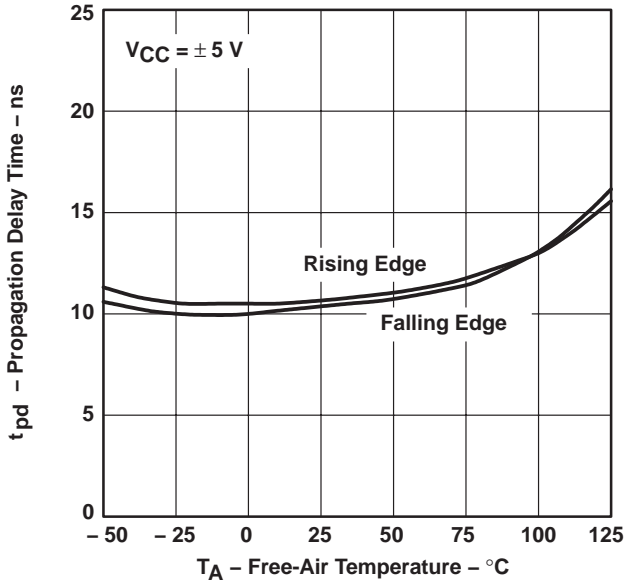


Figure 10

COMMON-MODE INPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

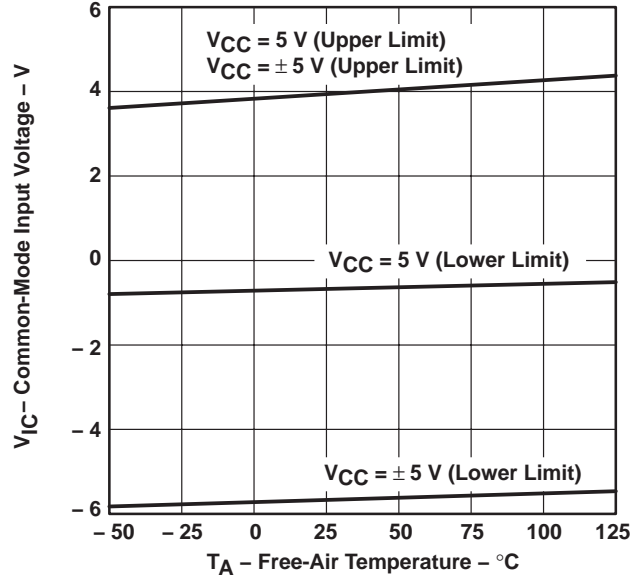


Figure 11

INPUT THRESHOLD VOLTAGE (LATCH ENABLE)
vs
FREE-AIR TEMPERATURE

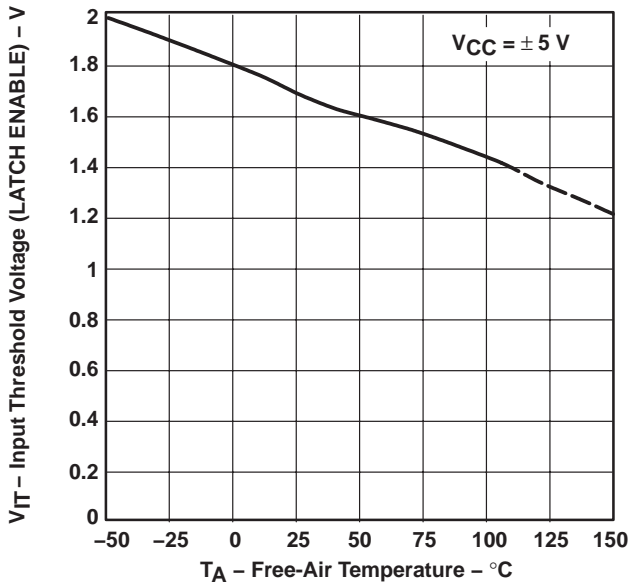


Figure 12

OUTPUT VOLTAGE
vs
OUTPUT SOURCE CURRENT

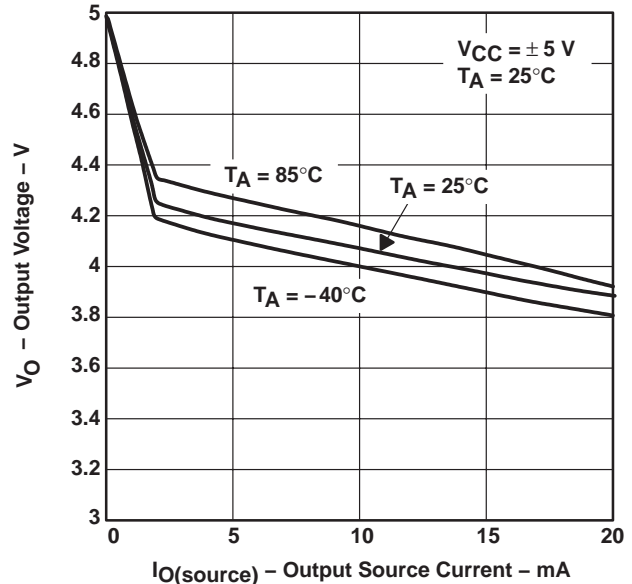


Figure 13

TYPICAL CHARACTERISTICS

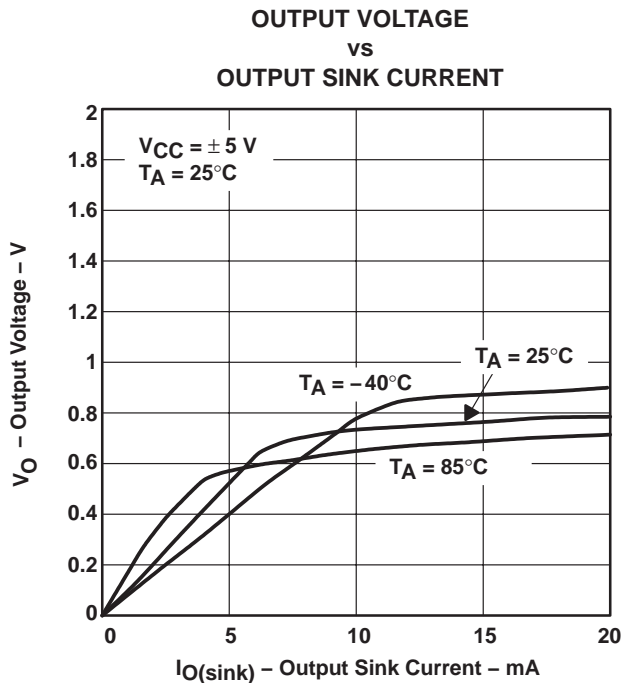


Figure 14

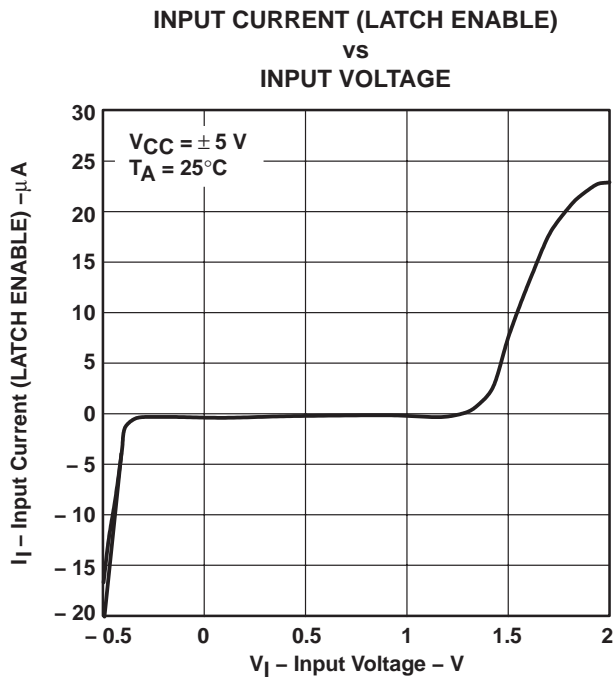


Figure 15

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL3116CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	3116C	Samples
TL3116CDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	3116C	Samples
TL3116CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	3116C	Samples
TL3116CPW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T3116	Samples
TL3116CPWLE	OBSOLETE	TSSOP	PW	8		TBD	Call TI	Call TI			
TL3116CPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	T3116	Samples
TL3116ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	3116I	Samples
TL3116IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	3116I	Samples
TL3116IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	3116I	Samples
TL3116IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	3116I	Samples
TL3116IPW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	Z3116	Samples
TL3116IPWLE	OBSOLETE	TSSOP	PW	8		TBD	Call TI	Call TI			
TL3116IPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	Z3116	Samples
TL3116IPWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	Z3116	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL3116CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL3116CPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TL3116IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL3116IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

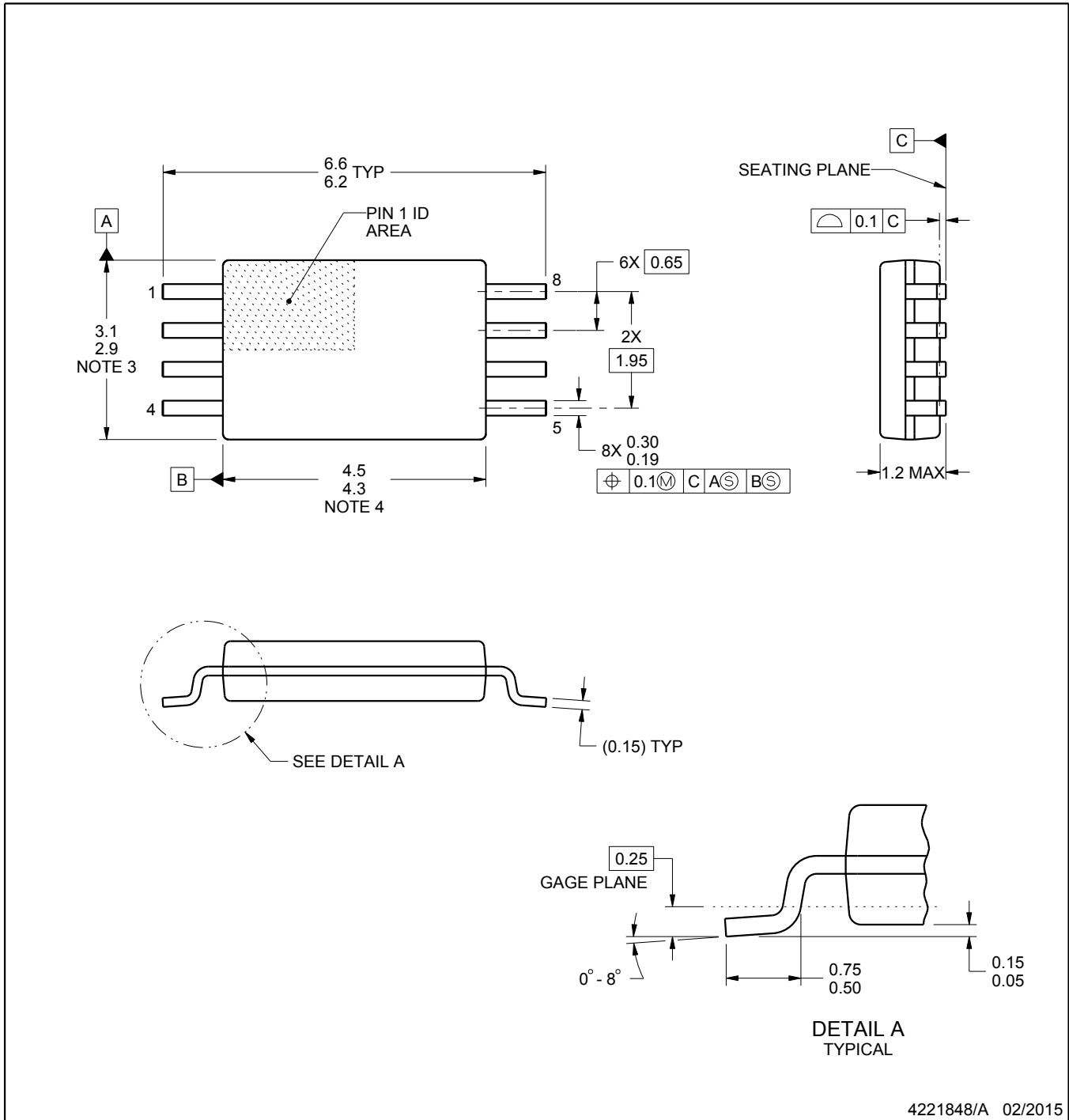
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL3116CDR	SOIC	D	8	2500	367.0	367.0	35.0
TL3116CPWR	TSSOP	PW	8	2000	367.0	367.0	35.0
TL3116IDR	SOIC	D	8	2500	367.0	367.0	35.0
TL3116IPWR	TSSOP	PW	8	2000	367.0	367.0	35.0

PW0008A



PACKAGE OUTLINE
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4221848/A 02/2015

NOTES:

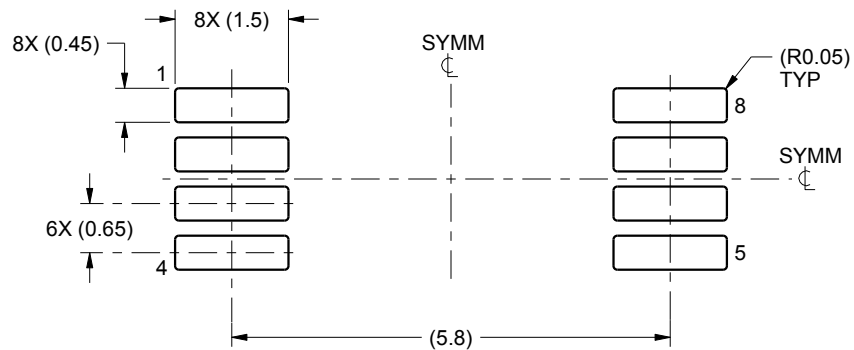
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.

EXAMPLE BOARD LAYOUT

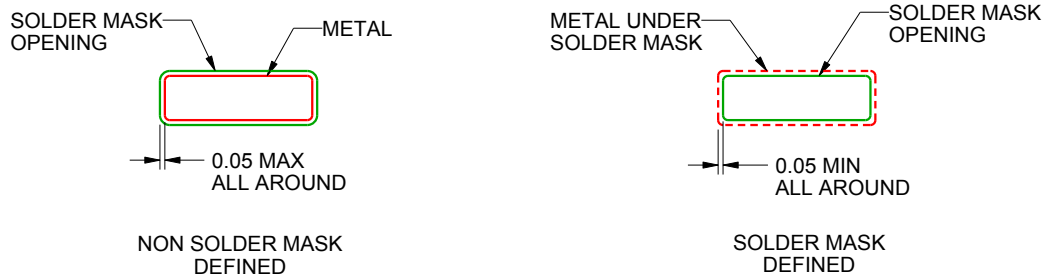
PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

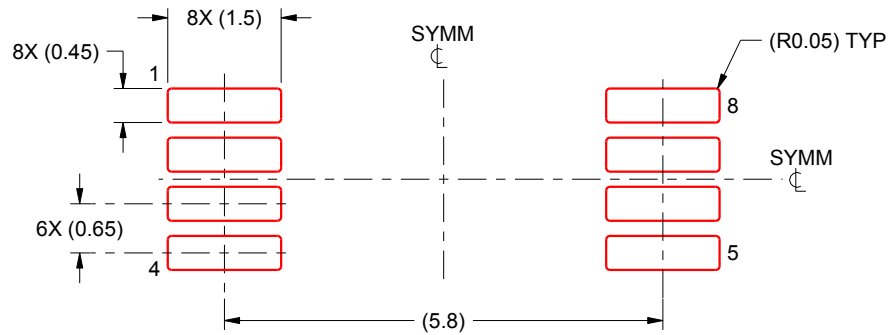
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

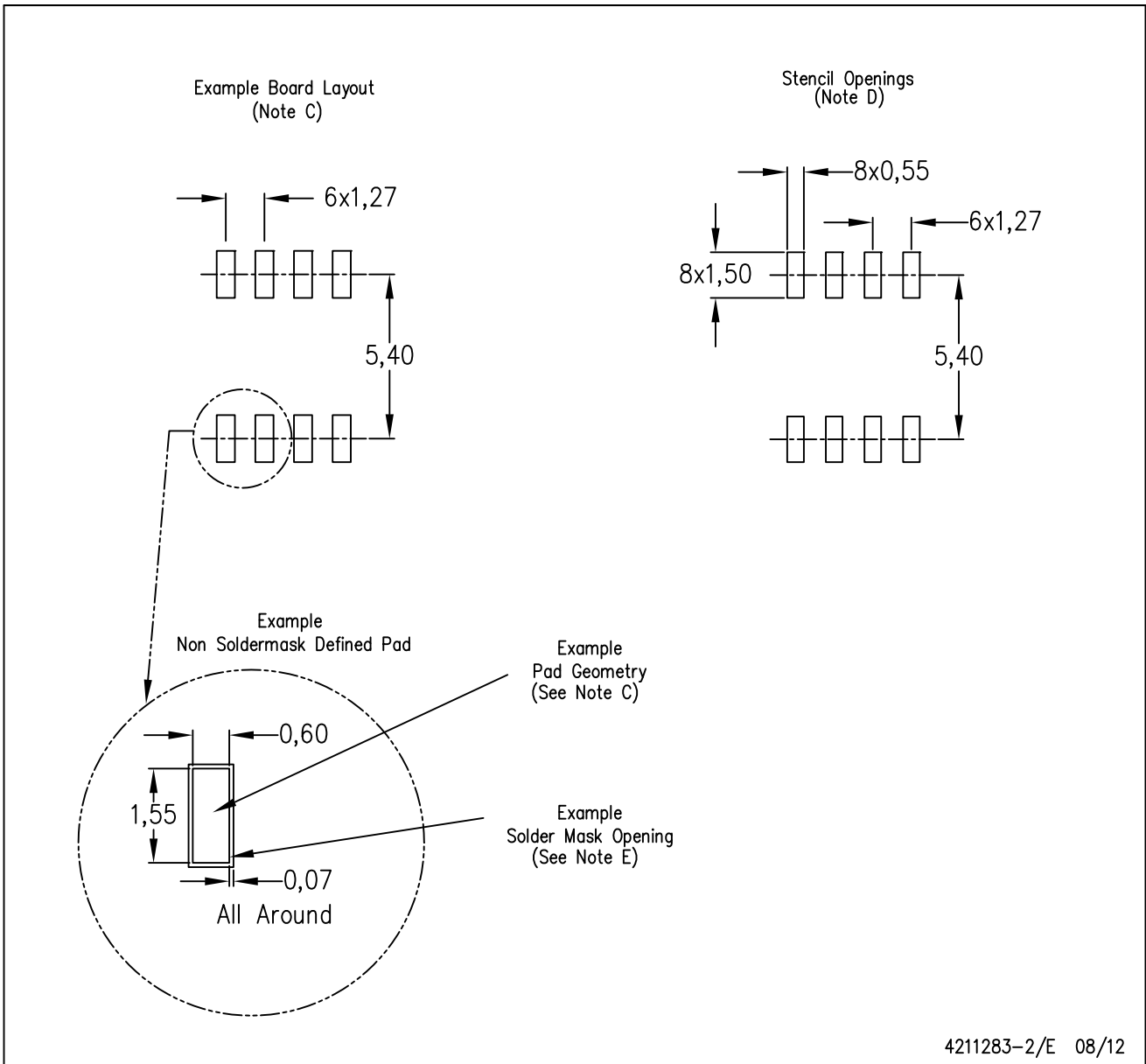
4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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