

ADVANCED LinCMOS™ RAIL-TO-RAIL OPERATIONAL AMPLIFIERS

 Check for Samples: [TLC2272-Q1](#) , [TLC2272A-Q1](#) , [TLC2274-Q1](#) , [TLC2274A-Q1](#)

FEATURES

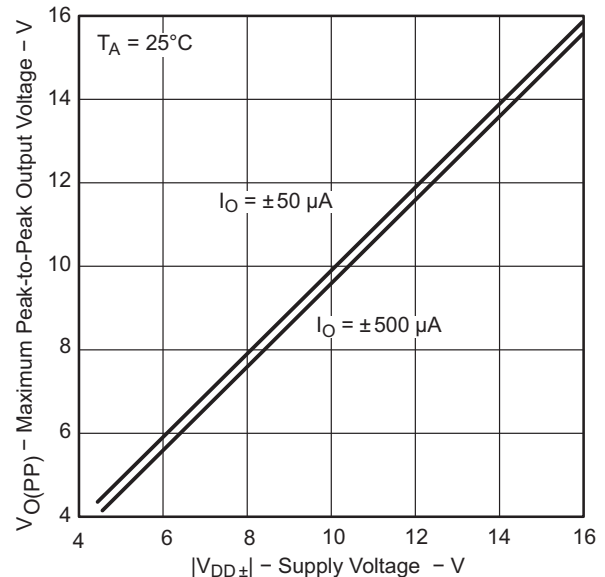
- Qualified for Automotive Applications
- Output Swing Includes Both Supply Rails
- Low Noise . . . 9 nV/√Hz Typ at f = 1 kHz
- Low Input Bias Current . . . 1 pA Typ
- Fully Specified for Both Single-Supply and Split-Supply Operation
- Common-Mode Input Voltage Range Includes Negative Rail
- High-Gain Bandwidth . . . 2.2 MHz Typ
- High Slew Rate . . . 3.6 V/μs Typ
- Low Input Offset Voltage
950 μV Max at T_A = 25°C
- Macromodel Included
- Performance Upgrades for the TS272, TS274, TLC272, and TLC274

DESCRIPTION

The TLC2272 and TLC2274 are dual and quadruple operational amplifiers from Texas Instruments. Both devices exhibit rail-to-rail output performance for increased dynamic range in single- or split-supply applications. The TLC227x family offers 2 MHz of bandwidth and 3 V/μs of slew rate for higher speed applications. These devices offer comparable ac performance while having better noise, input offset voltage, and power dissipation than existing CMOS operational amplifiers. The TLC227x has a noise voltage of 9 nV/√Hz, two times lower than competitive solutions.

The TLC227x, exhibiting high input impedance and low noise, is excellent for small-signal conditioning for high-impedance sources, such as piezoelectric transducers. Because of the micropower dissipation levels, these devices work well in hand-held monitoring and remote-sensing applications. In addition, the rail-to-rail output feature, with single- or split-supplies, makes this family a great choice when interfacing with analog-to-digital converters (ADCs). For precision applications, the TLC227xA family is available with a maximum input offset voltage of 950 μV. This family is fully characterized at 5 V and ±5 V.

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE



The TLC2272/4 also makes great upgrades to the TLC272/4 or TS272/4 in standard designs. They offer increased output dynamic range, lower noise voltage, and lower input offset voltage. This enhanced feature set allows them to be used in a wider range of applications. For applications that require higher output drive and wider input voltage range, see the TLV2432 and TLV2442 devices.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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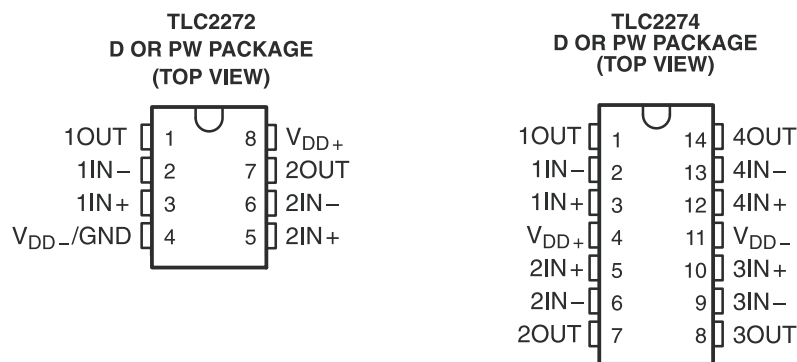
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

AVAILABLE OPTIONS

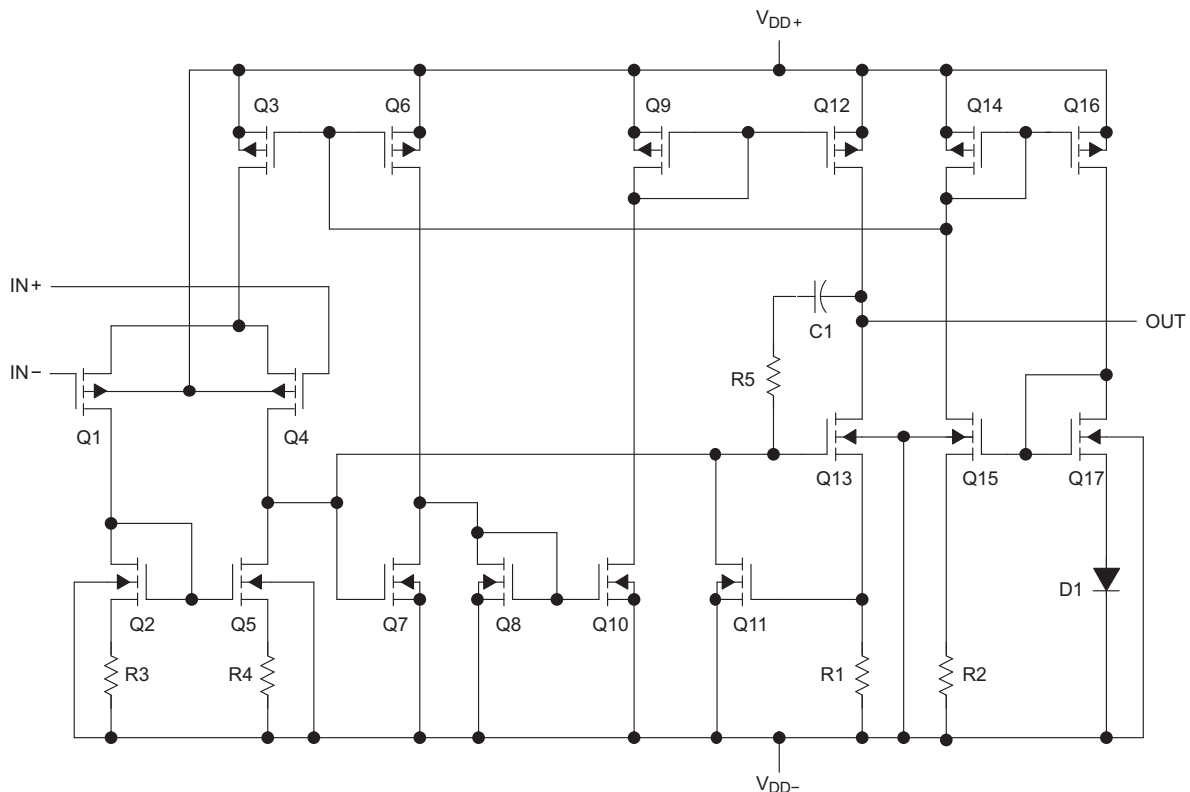
T _A	V _{IO} max At 25°C	PACKAGED DEVICES ⁽¹⁾⁽²⁾	
		SMALL OUTLINE (D)	TSSOP (PW)
-40°C to 125°C	950 μV	TLC2272AQDRQ1	TLC2272AQPWRQ1
	2.5 mV	TLC2272QDRQ1	TLC2272QPWRQ1
-40°C to 125°C	950 μV	TLC2274AQDRQ1	TLC2274AQPWRQ1
	2.5 mV	TLC2274QDRQ1	TLC2274QPWRQ1

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.



Equivalent Schematic (Each Amplifier)



Actual Device Component Count⁽¹⁾

COMPONENT	TLC2272	TLC2274
Transistors	38	76
Resistors	26	52
Diodes	9	18
Capacitors	3	6

(1) Includes both amplifiers and all ESD, bias, and trim circuitry

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT
V _{DD+}	Supply voltage ⁽²⁾	8	V
V _{DD-}	Supply voltage ⁽²⁾	-8	V
V _{ID}	Differential input voltage ⁽³⁾	±16	V
V _I	Input voltage range ⁽²⁾	Any input	V _{DD-} - 0.3 to V _{DD+}
I _I	Input current	Any input	±5
I _O	Output current		±50
	Total current into V _{DD+}		±50
	Total current out of V _{DD-}		±50
	Duration of short-circuit current at (or below) 25°C ⁽⁴⁾		unlimited
	Continuous total dissipation		See Dissipation Ratings
T _A	Operating free-air temperature range		-40°C to 125°C
T _{stg}	Storage temperature range		-65 to 150
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D or PW package	260

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential voltages, are with respect to the midpoint between V_{DD+} and V_{DD-}.
- (3) Differential voltages are at I_{N+} with respect to I_{N-}. Excessive current will flow if input is brought below V_{DD-} - 0.3 V.
- (4) The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATINGS

PACKAGE	T _A ≤ 25°C POWER RATING	DERATING FACTOR ABOVE T _A = 25°C	T _A = 70°C POWER RATING	T _A = 85°C POWER RATING	T _A = 125°C POWER RATING
D-8	725 mW	5.8 mW/°C	464 mW	337 mW	145 mW
D-14	950 mW	7.6 mW/°C	608 mW	494 mW	190 mW
D-14	525 mW	4.2 mW/°C	336 mW	273 mW	105 mW
D-14	700 mW	5.6 mW/°C	448 mW	364 mW	-

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _{DD±}	Supply voltage	±2.2	±8	V
V _I	Input voltage	V _{DD-}	V _{DD+} - 1.5	V
V _{IC}	Common-mode input voltage	V _{DD-}	V _{DD+} - 1.5	V
T _A	Operating free-air temperature	-40	125	°C

TLC2272Q ELECTRICAL CHARACTERISTICS

at specified free-air temperature, $V_{DD} = 5\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A ⁽¹⁾	TLC2272Q			TLC2272AQ			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO} Input offset voltage		25°C		300	2500		300	950	μV
		Full range			3000			1600	
αV_{IO} Temperature coefficient of input offset voltage		25°C to 125°C		2			2	$\mu\text{V}/^\circ\text{C}$	
Input offset voltage long-term drift ⁽²⁾	$V_{IC} = 0\text{ V}$, $V_O = 0\text{ V}$, $V_{DD\pm} = \pm 2.5\text{ V}$, $R_S = 50\ \Omega$	25°C		0.002			0.002	$\mu\text{V}/\text{m}_o$	
I_{IO} Input offset current		25°C		0.5	60		0.5	60	pA
		Full range			800			800	
I_{IB} Input bias current		25°C		1			1	60	pA
		Full range						800	
V_{ICR} Common-mode input voltage range	$R_S = 50\ \Omega$ $ V_{IO} \leq 5\text{ mV}$	25°C	0 to 4	-0.3 to 4.2		0 to 4	-0.3 to 4.2	V	
		Full range	0 to 3.5			0 to 3.5			
V_{OH} High-level output voltage	$I_{OH} = -20\ \mu\text{A}$	25°C		4.99			4.99	V	
		Full range		4.85	4.93		4.85		4.93
	$I_{OH} = -1\text{ mA}$	25°C		4.25	4.65		4.25		4.65
		Full range		4.25			4.25		
V_{OL} Low-level output voltage	$V_{IC} = 2.5\text{ V}$, $I_{OL} = 50\ \mu\text{A}$	25°C		0.01			0.01	V	
		Full range		0.09	0.15		0.09		0.15
	$V_{IC} = 2.5\text{ V}$, $I_{OL} = 500\ \mu\text{A}$	25°C			0.15				0.15
		Full range			0.9	1.5			0.9
	$V_{IC} = 2.5\text{ V}$, $I_{OL} = 5\text{ mA}$	25°C			1.5				1.5
		Full range			1.5				1.5
A_{VD} Large-signal differential voltage amplification	$V_{IC} = 2.5\text{ V}$, $V_O = 1\text{ V to }4\text{ V}$,	$R_L = 10\text{ k}\Omega$ ⁽³⁾	25°C	10	35		10	35	V/mV
			Full range		10			10	
		$R_L = 1\text{ M}\Omega$ ⁽³⁾	25°C		175			175	
r_{id} Differential input resistance		25°C		10^{12}			10^{12}	Ω	
r_i Common-mode input resistance		25°C		10^{12}			10^{12}	Ω	
c_i Common-mode input capacitance	$f = 10\text{ kHz}$, P package	25°C		8			8	pF	
z_o Closed-loop output impedance	$f = 1\text{ MHz}$, $A_v = 10$	25°C		140			140	Ω	
CMR R Common-mode rejection ratio	$V_{IC} = 0\text{ V to }2.7\text{ V}$, $V_O = 2.5\text{ V}$, $R_S = 50\ \Omega$	25°C	70	75		70	75	dB	
		Full range	70			70			
k_{SVR} Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 4.4\text{ V to }16\text{ V}$, $V_{IC} = V_{DD}/2$, No load	25°C	80	95		80	95	dB	
		Full range	80			80			
I_{DD} Supply current	$V_O = 2.5\text{ V}$, No load	25°C		2.2	3		2.2	3	mA
		Full range				3		3	

- (1) Full range is -40°C to 125°C for Q level part.
- (2) Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.
- (3) Referenced to 2.5 V

TLC2272Q OPERATING CHARACTERISTICS

 at specified free-air temperature, $V_{DD} = 5\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$T_A^{(1)}$	TLC2272Q			TLC2272AQ			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
SR Slew rate at unity gain	$V_O = 1.25\text{ V to } 2.75\text{ V},$ $R_L = 10\text{ k}\Omega^{(2)}$	$C_L = 100\text{ pF}^{(2)}$	25°C	2.3	3.6	2.3	3.6	V/ μs	
			Full range	1.7		1.7			
V_n Equivalent input noise voltage	$f = 10\text{ Hz}$	25°C		50		50	nV/ $\sqrt{\text{Hz}}$		
	$f = 1\text{ kHz}$	25°C		9		9			
$V_{N(pp)}$ Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ to } 1\text{ Hz}$	25°C		1		1	μV		
	$f = 0.1\text{ to } 10\text{ Hz}$	25°C		1.4		1.4			
I_n Equivalent input noise current		25°C		0.6		0.6	fA/ $\sqrt{\text{Hz}}$		
THD + N Total harmonic distortion plus noise	$V_O = 0.5\text{V to } 2.5\text{V},$ $R_L = 10\text{ k}\Omega,$ $f = 20\text{ kHz}^{(2)}$	$A_V = 1$	25°C		0.0013%		0.0013%		
				$A_V = 10$		0.004%			0.004%
					$A_V = 100$		0.03%		
Gain-bandwidth product	$f = 10\text{ kHz},$ $C_L = 100\text{ pF}^{(2)}$	$R_L = 10\text{ k}\Omega^{(2)}$	25°C		2.18		2.18	MHz	
B_{OM} Maximum output-swing bandwidth	$V_{O(pp)} = 2\text{V},$ $R_L = 10\text{ k}\Omega^{(2)}$	$A_V = 1,$ $C_L = 100\text{ pF}^{(2)}$	25°C		1		1	MHz	
t_s Settling time	$A_V = -1,$ Step = 0.5V to 2.5V, $R_L = 10\text{ k}\Omega^{(3)}$ $C_L = 100\text{ pF}^{(3)}$	To 0.1%	25°C		1.5		1.5	μs	
		To 0.01%			2.6		2.6		
ϕ_m Phase margin at unity gain	$R_L = 10\text{ k}\Omega^{(3)},$ $C_L = 100\text{ pF}^{(3)}$		25°C		50°		50°		
Gain margin			25°C		10		10	dB	

 (1) Full range is -40°C to 125°C for Q level part.

(2) Referenced to 2.5 V

(3) Referenced to 2.5 V

TLC2272Q ELECTRICAL CHARACTERISTICS

at specified free-air temperature, $V_{DD\pm} = \pm 5\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$T_A^{(1)}$	TLC2272Q			TLC2272AQ			UNIT	
			MIN	TYP	MAX	MIN	TYP	MAX		
V_{IO} Input offset voltage		25°C	300			300			μV	
		Full range				1500				
αV_{IO} Temperature coefficient of input offset voltage		25°C to 125°C	2			2			$\mu\text{V}/^\circ\text{C}$	
Input offset voltage long-term drift ⁽²⁾	$V_{IC} = 0\text{ V},$ $R_S = 50\ \Omega$	$V_O = 0\text{ V}$	25°C	0.002			0.002			$\mu\text{V}/\text{m}_o$
I_{IO} Input offset current		25°C	0.5			0.5			pA	
		Full range				800				
I_{IB} Input bias current		25°C	1			1			pA	
		Full range				800				
V_{ICR} Common-mode input voltage range	$R_S = 50\ \Omega$	$ V_{IO} \leq 5\text{ mV}$	25°C	-5 to 4	-5.3 to 4.2	-5 to 4	-5.3 to 4.2	V		
			Full range			-5 to 3.5				
V_{OM+} Maximum positive peak output voltage	$I_O = -20\ \mu\text{A}$	25°C	4.99			4.99			V	
		25°C	4.85	4.93	4.85	4.93				
	Full range	4.85			4.85					
	$I_O = -1\text{ mA}$	25°C	4.25	4.65	4.25	4.65				
Full range		4.25			4.25					
V_{OM-} Maximum negative peak output voltage	$V_{IC} = 0\text{ V},$ $I_O = 50\ \mu\text{A}$	25°C	-4.99			-4.99			V	
		25°C	-4.85	-4.91	-4.85	-4.91				
	Full range	-4.85			-4.85					
	$V_{IC} = 0\text{ V},$ $I_O = 5\text{ mA}$	25°C	-3.5	-4.1	-3.5	-4.1				
Full range		-3.5			-3.5					
A_{VD} Large-signal differential voltage amplification	$V_O = \pm 4\text{ V},$	$R_L = 10\text{ k}\Omega$	25°C	20	50	20	50	V/mV		
			Full range	20			20			
			$R_L = 1\text{ M}\Omega$	25°C	300				300	
r_{id} Differential input resistance		25°C	10^{12}			10^{12}			Ω	
r_i Common-mode input resistance		25°C	10^{12}			10^{12}			Ω	
c_i Common-mode input capacitance	$f = 10\text{ kHz},$	N package	25°C	8			8			pF
z_o Closed-loop output impedance	$f = 1\text{ MHz},$	$AV = 10$	25°C	130			130			Ω
CMR R Common-mode rejection ratio	$V_{IC} = -5\text{ V to } 2.7\text{ V},$ $V_O = 0\text{ V},$	$R_S = 50\ \Omega$	25°C	75	80	75	80	dB		
			Full range	75			75			
k_{SVR} Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = \pm 2.2\text{ V to } \pm 8\text{ V},$ $V_{IC} = 0\text{ V},$	No load	25°C	80	95	80	95	dB		
			Full range	80			80			
I_{DD} Supply current	$V_O = 0\text{ V},$	No load	25°C	2.4	3	2.4	3	mA		
			Full range	3			3			

- (1) Full range is -40°C to 125°C for Q level part.
(2) Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLC2272Q OPERATING CHARACTERISTICS

 at specified free-air temperature, $V_{DD\pm} = \pm 5\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$T_A^{(1)}$	TLC2272Q			TLC2272AQ			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain $V_O = \pm 2.3\text{ V}$, $R_L = 10\text{ k}\Omega$	$C_L = 100\text{ pF}$	25°C	2.3	3.6		2.3	3.6	V/ μs
			Full range	1.7			1.7		
V_n	Equivalent input noise voltage	$f = 10\text{ Hz}$	25°C		50			50	$\text{nV}/\sqrt{\text{Hz}}$
					9			9	
$V_{N(\text{pp})}$	Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ to }1\text{ Hz}$	25°C		1			1	μV
					1.4			1.4	
I_n	Equivalent input noise current		25°C		0.6			$\text{fA}/\sqrt{\text{Hz}}$	
THD + N	Total harmonic distortion plus noise $V_O = \pm 2.3\text{ V}$, $f = 20\text{ kHz}$, $R_L = 10\text{ k}\Omega$	$A_V = 1$	25°C		0.0011%			0.0011%	
				$A_V = 10$	0.004%			0.004%	
				$A_V = 100$	0.03%			0.03%	
	Gain-bandwidth product	$f = 10\text{ kHz}$, $C_L = 100\text{ pF}$	$R_L = 10\text{ k}\Omega$	25°C		2.25		2.25	MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(\text{pp})} = 4.6\text{ V}$, $R_L = 10\text{ k}\Omega$	$A_V = 1$, $C_L = 100\text{ pF}$	25°C		0.54		0.54	MHz
t_s	Settling time	$A_V = -1$, Step = -2.3 V to 2.3 V, $R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$	To 0.1%	25°C		1.5		1.5	μs
			To 0.01%			3.2		3.2	
Φ_m	Phase margin at unity gain	$R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$	25°C		52°			52°	
	Gain margin		25°C		10			10	dB

(1) Full range is -40°C to 125°C for Q level part.

TLC2274Q ELECTRICAL CHARACTERISTICS

at specified free-air temperature, $V_{DD} = 5\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A ⁽¹⁾	TLC2274Q			TLC2274AQ			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO} Input offset voltage		25°C		300	2500		300	950	μV
		Full range			3000		1600		
αV_{IO} Temperature coefficient of input offset voltage		25°C to 125°C		2			2	$\mu\text{V}/^\circ\text{C}$	
Input offset voltage long-term drift ⁽²⁾	$V_{IC} = 0\text{ V}$, $V_O = 0\text{ V}$, $V_{DD\pm} = \pm 2.5\text{ V}$, $R_S = 50\ \Omega$	25°C		0.002			0.002	$\mu\text{V}/\text{m o}$	
I_{IO} Input offset current		25°C		0.5	60		0.5	60	pA
		Full range			800		800		
I_{IB} Input bias current		25°C		1			1	60	pA
		Full range					800		
V_{ICR} Common-mode input voltage range	$R_S = 50\ \Omega$ $ V_{IO} \leq 5\text{ mV}$	25°C	0 to 4	-0.3 to 4.2		0 to 4	-0.3 to 4.2	V	
		Full range	0 to 3.5			0 to 3.5			
V_{OH} High-level output voltage	$I_{OH} = -20\ \mu\text{A}$	25°C		4.99			4.99	V	
		Full range		4.85	4.93		4.85		4.93
	$I_{OH} = -1\text{ mA}$	25°C		4.25	4.65		4.25		4.65
		Full range		4.25			4.25		
V_{OL} Low-level output voltage	$V_{IC} = 2.5\text{ V}$, $I_{OL} = 50\ \mu\text{A}$	25°C		0.01			0.01	V	
		Full range		0.09	0.15		0.09		0.15
	$V_{IC} = 2.5\text{ V}$, $I_{OL} = 500\ \mu\text{A}$	25°C			0.15				0.15
		Full range			1.5		1.5		
A_{VD} Large-signal differential voltage amplification	$V_{IC} = 2.5\text{ V}$, $V_O = 1\text{ V to }4\text{ V}$, $R_L = 10\text{ k}\Omega$ ⁽³⁾ $R_L = 1\text{ M}\Omega$ ⁽³⁾	25°C		10	35		10	35	V/mV
		Full range		10			10		
		25°C			175			175	
r_{id} Differential input resistance		25°C		10^{12}			10^{12}	Ω	
r_i Common-mode input resistance		25°C		10^{12}			10^{12}	Ω	
c_i Common-mode input capacitance	$f = 10\text{ kHz}$, N package	25°C		8			8	pF	
z_o Closed-loop output impedance	$f = 1\text{ MHz}$, $A_v = 10$	25°C		140			140	Ω	
CMR R Common-mode rejection ratio	$V_{IC} = 0\text{ V to }2.7\text{ V}$, $V_O = 2.5\text{ V}$, $R_S = 50\ \Omega$	25°C		70	75		70	75	dB
		Full range		70			70		
k_{SVR} Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 4.4\text{ V to }16\text{ V}$, $V_{IC} = V_{DD}/2$, No load	25°C		80	95		80	95	dB
		Full range		80			80		
I_{DD} Supply current	$V_O = 2.5\text{ V}$, No load	25°C		4.4	6		4.4	6	mA
		Full range			6		6		

- (1) Full range is -40°C to 125°C for Q level part.
- (2) Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.
- (3) Referenced to 2.5 V

TLC2274Q OPERATING CHARACTERISTICS

 at specified free-air temperature, $V_{DD} = 5\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A ⁽¹⁾	TLC2274Q			TLC2274AQ			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
SR Slew rate at unity gain	$V_O = 0.5\text{ V}$ to 2.5 V , $R_L = 10\text{ k}\Omega$ ⁽²⁾ $C_L = 100\text{ pF}$ ⁽²⁾	25°C	2.3	3.6		2.3	3.6	V/ μ s	
		Full range	1.7			1.7			
V_n Equivalent input noise voltage	$f = 10\text{ Hz}$	25°C		50		50	nV/ $\sqrt{\text{Hz}}$		
	$f = 1\text{ kHz}$	25°C		9		9			
$V_{N(pp)}$ Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ to }1\text{ Hz}$	25°C		1		1	μ V		
	$f = 0.1\text{ to }10\text{ Hz}$	25°C		1.4		1.4			
I_n Equivalent input noise current		25°C		0.6		0.6	fA/ $\sqrt{\text{Hz}}$		
THD + N Total harmonic distortion plus noise	$V_O = 0.5\text{ V}$ to 2.5 V , $R_L = 10\text{ k}\Omega$, $f = 20\text{ kHz}$ ⁽²⁾	$A_V = 1$	25°C	0.0013%		0.0013%			
		$A_V = 10$		0.004%		0.004%			
		$A_V = 100$		0.03%		0.03%			
Gain-bandwidth product	$f = 10\text{ kHz}$, $C_L = 100\text{ pF}$ ⁽²⁾	$R_L = 10\text{ k}\Omega$ ⁽²⁾	25°C	2.18		2.18	MHz		
B_{OM} Maximum output-swing bandwidth	$V_{O(pp)} = 2\text{ V}$, $R_L = 10\text{ k}\Omega$ ⁽²⁾	$A_V = 1$, $C_L = 100\text{ pF}$ ⁽²⁾	25°C	1		1	MHz		
t_s Settling time	$A_V = -1$, Step = 0.5 V to 2.5 V , $R_L = 10\text{ k}\Omega$ ⁽³⁾ , $C_L = 100\text{ pF}$ ⁽³⁾	To 0.1%	25°C	1.5		1.5	μ s		
		To 0.01%		2.6		2.6			
ϕ_m Phase margin at unity gain	$R_L = 10\text{ k}\Omega$ ⁽³⁾ , $C_L = 100\text{ pF}$ ⁽³⁾	25°C		50°		50°			
Gain margin		25°C		10		10	dB		

 (1) Full range is -40°C to 125°C for Q level part.

(2) Referenced to 2.5 V

(3) Referenced to 2.5 V

TLC2274Q ELECTRICAL CHARACTERISTICS

at specified free-air temperature, $V_{DD\pm} = \pm 5\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$T_A^{(1)}$	TLC2274Q			TLC2274AQ			UNIT	
			MIN	TYP	MAX	MIN	TYP	MAX		
V_{IO} Input offset voltage		25°C		300	2500		300	950	μV	
		Full range			3000			1500		
αV_{IO} Temperature coefficient of input offset voltage		25°C to 125°C		2			2	$\mu\text{V}/^\circ\text{C}$		
Input offset voltage long-term drift ⁽²⁾	$V_{IC} = 0\text{ V}$, $R_S = 50\ \Omega$	$V_O = 0\text{ V}$	25°C	0.002			0.002	$\mu\text{V}/\text{m}_o$		
I_{IO} Input offset current		25°C		0.5	60		0.5	60	pA	
		Full range			800			800		
I_{IB} Input bias current		25°C		1	60		1	60	pA	
		Full range			800			800		
V_{ICR} Common-mode input voltage range	$R_S = 50\ \Omega$	$ V_{IO} \leq 5\text{ mV}$	25°C	-5 to 4	-5.3 to 4.2		-5 to 4	-5.3 to 4.2	V	
			Full range					-5 to 3.5		
V_{OM+} Maximum positive peak output voltage	$I_O = -20\ \mu\text{A}$		25°C		4.99			4.99	V	
			25°C		4.85	4.93		4.85		4.93
	$I_O = -200\ \mu\text{A}$		Full range		4.85			4.85		
			25°C		4.25	4.65		4.25		4.65
$I_O = -1\text{ mA}$		Full range		4.25			4.25			
		25°C								
V_{OM-} Maximum negative peak output voltage	$V_{IC} = 0\text{ V}$, $I_O = 50\ \mu\text{A}$		25°C		-4.99			-4.99	V	
			25°C		-4.85	-4.91		-4.85		-4.91
	$V_{IC} = 0\text{ V}$, $I_O = 500\ \mu\text{A}$		Full range		-4.85			-4.85		
			25°C		-3.5	-4.1		-3.5		-4.1
$V_{IC} = 0\text{ V}$, $I_O = 5\text{ mA}$		Full range		-3.5			-3.5			
		25°C								
A_{VD} Large-signal differential voltage amplification	$V_O = \pm 4\text{ V}$,	$R_L = 10\text{ k}\Omega$	25°C		20	50		20	50	V/mV
			Full range		20			20		
			25°C			300			300	
r_{id} Differential input resistance			25°C		10^{12}			10^{12}	Ω	
r_i Common-mode input resistance			25°C		10^{12}			10^{12}	Ω	
c_i Common-mode input capacitance	$f = 10\text{ kHz}$,	N package	25°C		8			8	pF	
z_o Closed-loop output impedance	$f = 1\text{ MHz}$,	$AV = 10$	25°C		130			130	Ω	
CMR R Common-mode rejection ratio	$V_{IC} = -5\text{ V}$ to 2.7 V, $V_O = 0\text{ V}$,	$R_S = 50\ \Omega$	25°C	75	80		75	80	dB	
			Full range		75			75		
k_{SVR} Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = \pm 2.2\text{ V}$ to $\pm 8\text{ V}$, $V_{IC} = 0\text{ V}$,	No load	25°C	80	95		80	95	dB	
			Full range		80			80		
I_{DD} Supply current	$V_O = 0\text{ V}$,	No load	25°C	4.4	6		4.4	6	mA	
			Full range			6		6		

(1) Full range is -40°C to 125°C for Q level part.

(2) Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLC2274Q OPERATING CHARACTERISTICS

 at specified free-air temperature, $V_{DD\pm} = \pm 5\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$T_A^{(1)}$	TLC2274Q			TLC2274AQ			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain $V_O = \pm 2.3\text{ V}$, $R_L = 10\text{ k}\Omega$	$C_L = 100\text{ pF}$	25°C	2.3	3.6		2.3	3.6	V/ μs
			Full range	1.7			1.7		
V_n	Equivalent input noise voltage		25°C		50			50	$\text{nV}/\sqrt{\text{Hz}}$
					9			9	
$V_{N(\text{pp})}$	Peak-to-peak equivalent input noise voltage		25°C		1			1	μV
					1.4			1.4	
I_n	Equivalent input noise current		25°C		0.6			0.6	$\text{fA}/\sqrt{\text{Hz}}$
THD + N	Total harmonic distortion plus noise	$V_O = \pm 2.3\text{ V}$, $f = 20\text{ kHz}$, $R_L = 10\text{ k}\Omega$	25°C	$A_V = 1$	0.0011%		0.0011%		
				$A_V = 10$	0.004%		0.004%		
				$A_V = 100$	0.03%		0.03%		
	Gain-bandwidth product	$f = 10\text{ kHz}$, $C_L = 100\text{ pF}$	$R_L = 10\text{ k}\Omega$	25°C		2.25		2.25	MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(\text{pp})} = 4.6\text{ V}$, $R_L = 10\text{ k}\Omega$	$A_V = 1$, $C_L = 100\text{ pF}$	25°C		0.54		0.54	MHz
t_s	Settling time	$A_V = -1$, Step = -2.3 V to 2.3 V, $R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$	25°C	To 0.1%		1.5		1.5	μs
				To 0.01%		3.2		3.2	
Φ_m	Phase margin at unity gain	$R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$	25°C		52°			52°	
	Gain margin		25°C		10			10	dB

 (1) Full range is -40°C to 125°C for Q level part.

TYPICAL CHARACTERISTICS

Table of Graphs⁽¹⁾

		FIGURE	
V_{IO}	Input offset voltage	Distribution vs Common-mode voltage	Figure 1, Figure 2, Figure 3, Figure 4, Figure 5, Figure 6
αV_{IO}	Input offset voltage temperature coefficient	Distribution	Figure 7, Figure 8, Figure 9, Figure 10
I_{IB} / I_{IO}	Input bias and input offset current	vs Free-air temperature	Figure 11
V_I	Input voltage	vs Supply voltage	Figure 12
		vs Free-air temperature	Figure 13
V_{OH}	High-level output voltage	vs High-level output current	Figure 14
V_{OL}	Low-level output voltage	vs Low-level output current	Figure 15, Figure 16
V_{OM+}	Maximum positive peak output voltage	vs Output current	Figure 17
V_{OM-}	Maximum negative peak output voltage	vs Output current	Figure 18
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	Figure 19
I_{OS}	Short-circuit output current	vs Supply voltage	Figure 20
		vs Free-air temperature	Figure 21
V_O	Output voltage	vs Differential input voltage	Figure 22, Figure 23
A_{VD}	Large-signal differential voltage amplification	vs Load resistance	Figure 24
	Large-signal differential voltage amplification and phase margin	vs Frequency	Figure 25, Figure 26
	Large-signal differential voltage amplification	vs Free-air temperature	Figure 27, Figure 28
z_o	Output impedance	vs Frequency	Figure 29, Figure 30
		vs Frequency	Figure 31
CMRR	Common-mode rejection ratio	vs Free-air temperature	Figure 32
		vs Frequency	Figure 33, Figure 34
kSVR	Supply-voltage rejection ratio	vs Free-air temperature	Figure 35
		vs Supply voltage	Figure 36, Figure 37
I_{DD}	Supply current	vs Free-air temperature	Figure 38, Figure 39
		vs Load capacitance	Figure 40
SR	Slew rate	vs Free-air temperature	Figure 41
		Inverting large-signal pulse response	Figure 42, Figure 43
V_O	Voltage-follower large-signal pulse response		Figure 44, Figure 45
	Inverting small-signal pulse response		Figure 46, Figure 47
	Voltage-follower small-signal pulse response		Figure 48, Figure 49
	Equivalent input noise voltage	vs Frequency	Figure 50, Figure 51
	Noise voltage over a 10-second period		Figure 52
	Integrated noise voltage	vs Frequency	Figure 53
THD + N	Total harmonic distortion plus noise	vs Frequency	Figure 54
		vs Supply voltage	Figure 55
	Gain bandwidth product	vs Free-air temperature	Figure 56
Φ_m	Phase margin	vs Load capacitance	Figure 57
	Gain margin	vs Load capacitance	Figure 58

(1) For all graphs where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V.

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

DISTRIBUTION OF TLC2272 INPUT OFFSET VOLTAGE

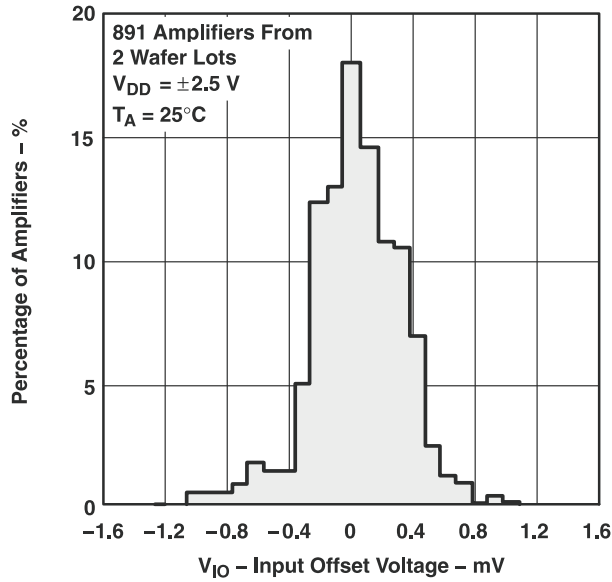


Figure 1.

DISTRIBUTION OF TLC2272 INPUT OFFSET VOLTAGE

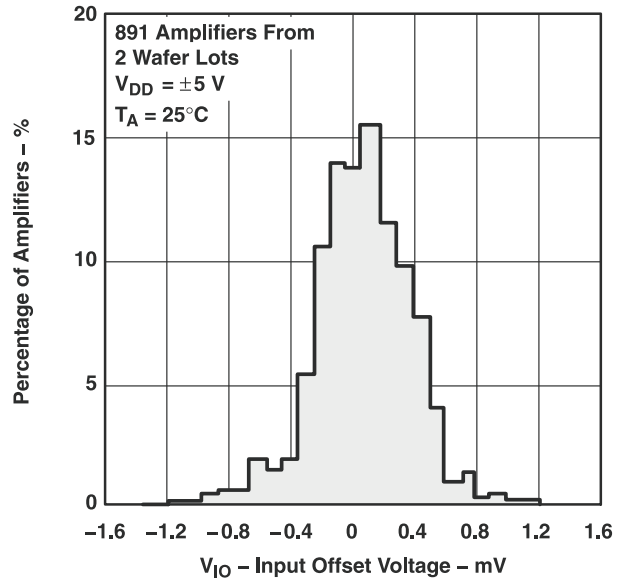


Figure 2.

DISTRIBUTION OF TLC2274 INPUT OFFSET VOLTAGE

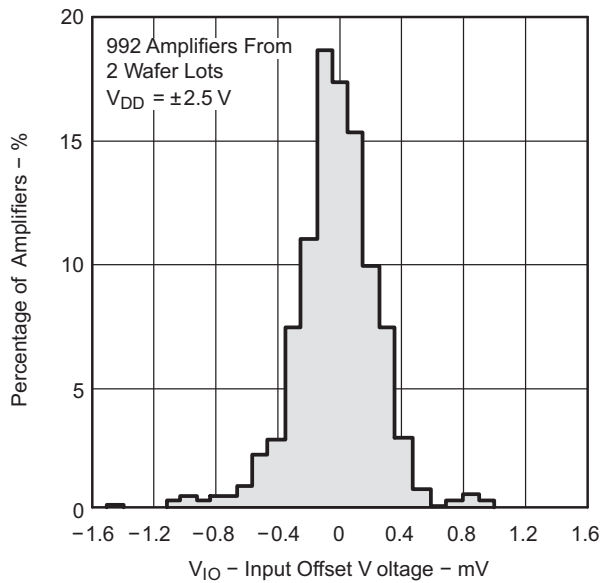


Figure 3.

DISTRIBUTION OF TLC2274A INPUT OFFSET VOLTAGE

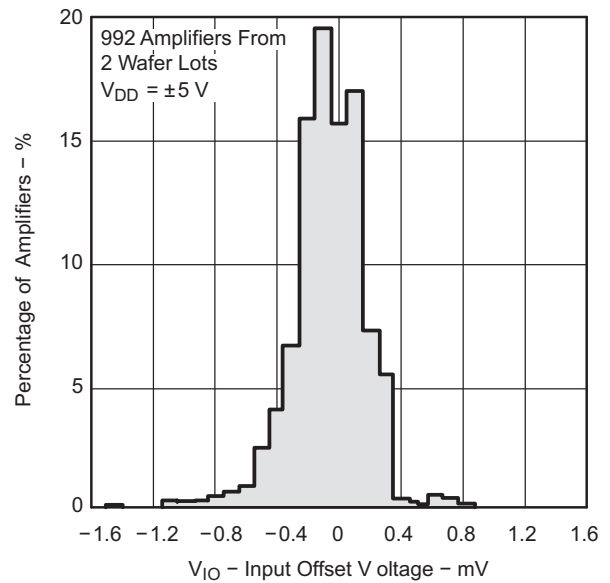
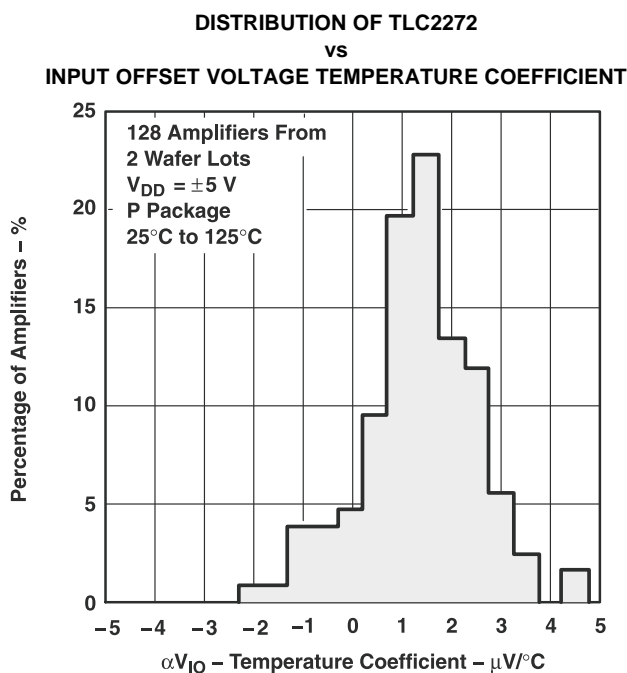
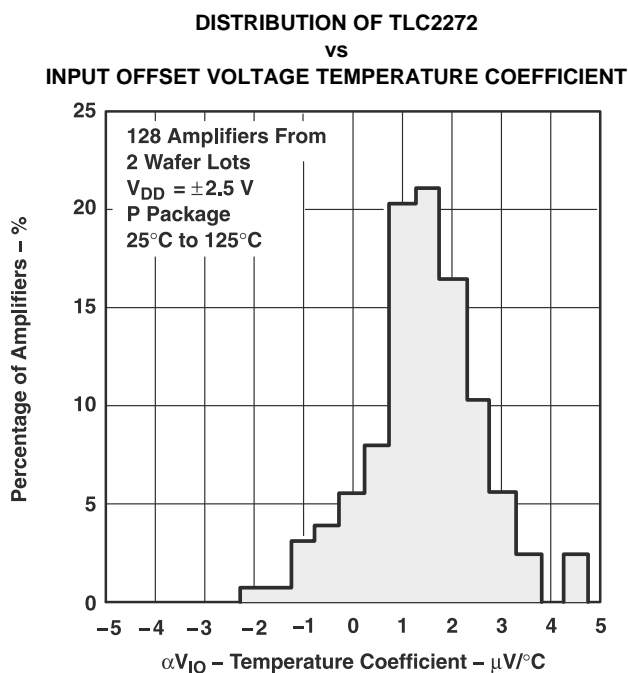
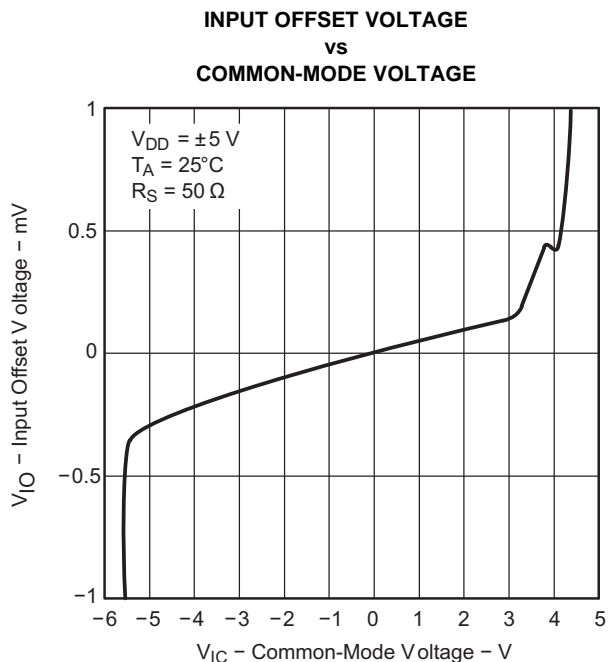
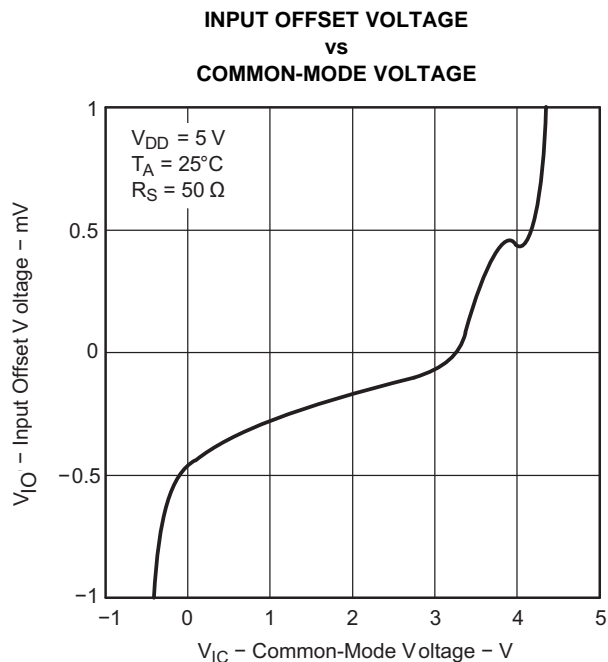


Figure 4.

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.



Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

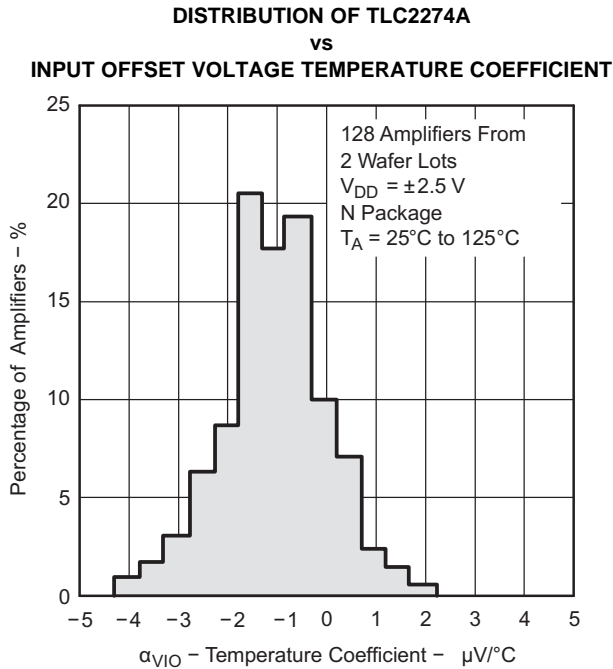


Figure 9.

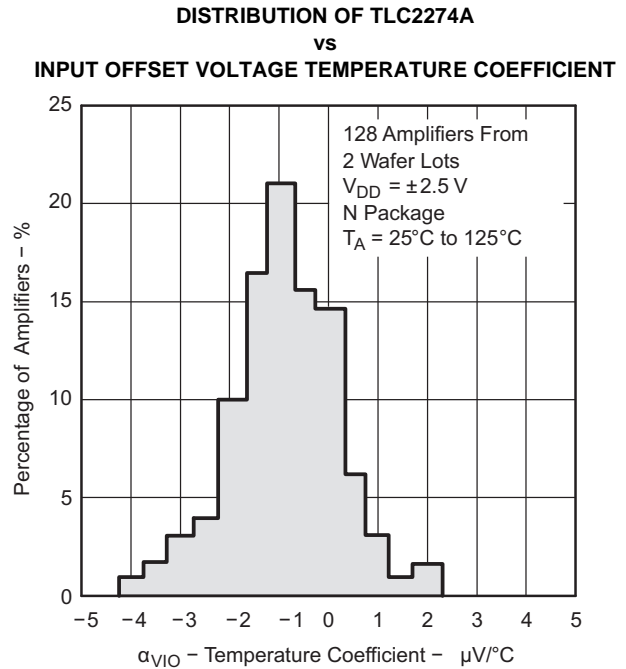


Figure 10.

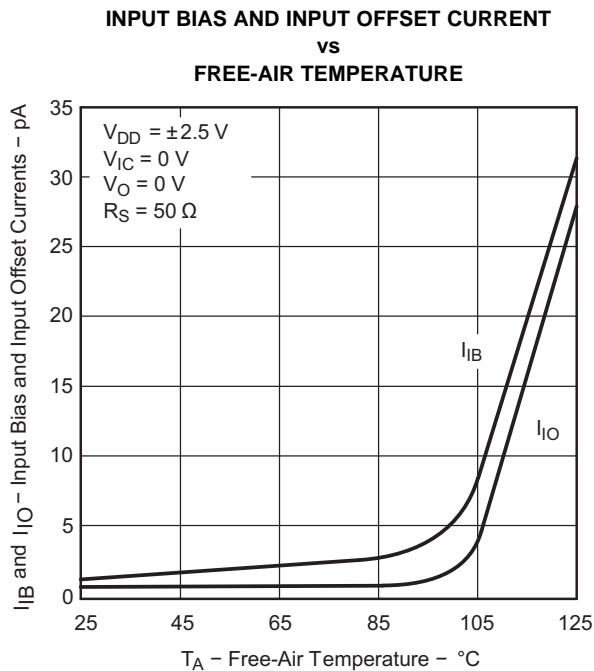


Figure 11.

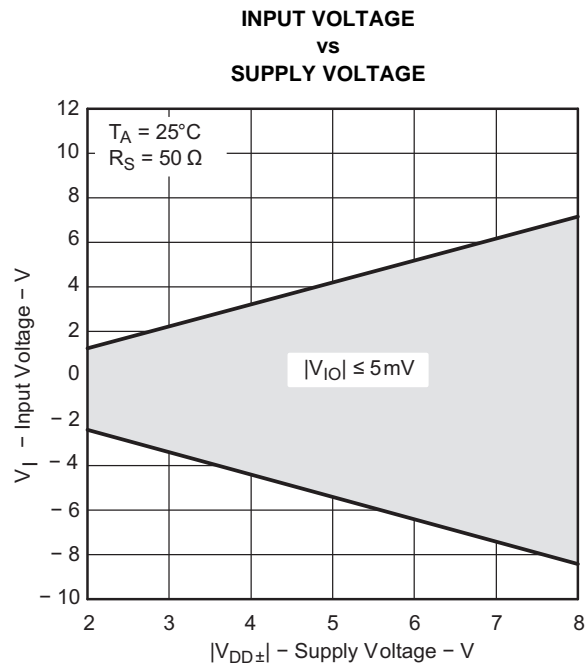


Figure 12.

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

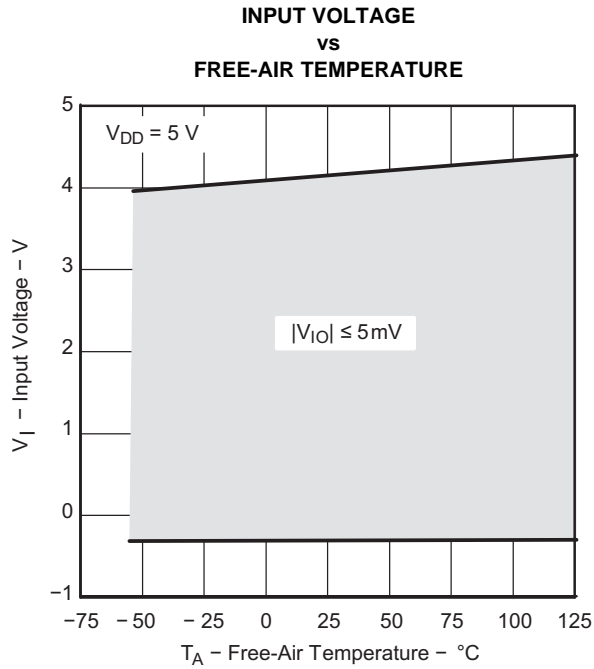


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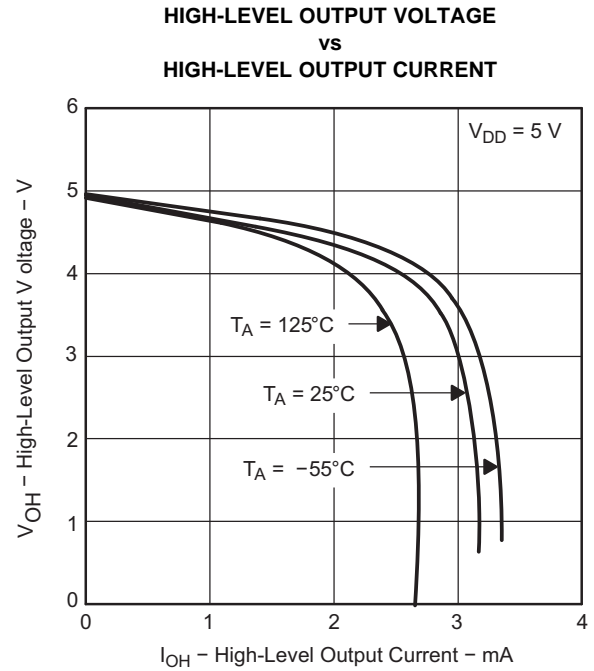


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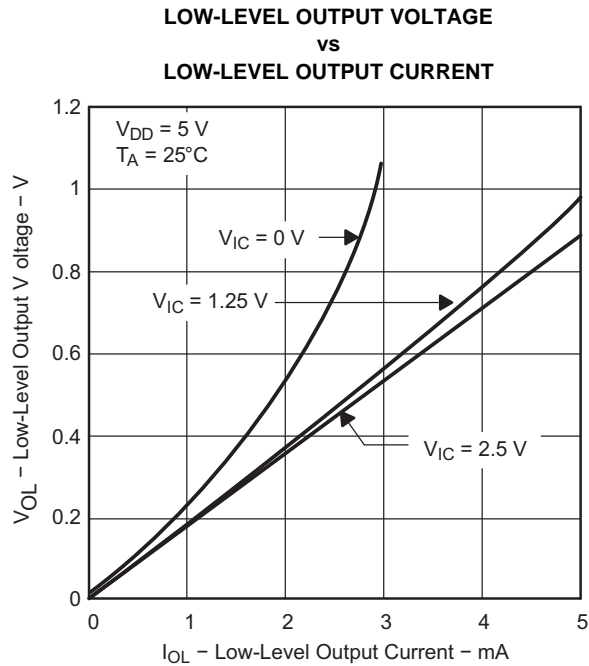


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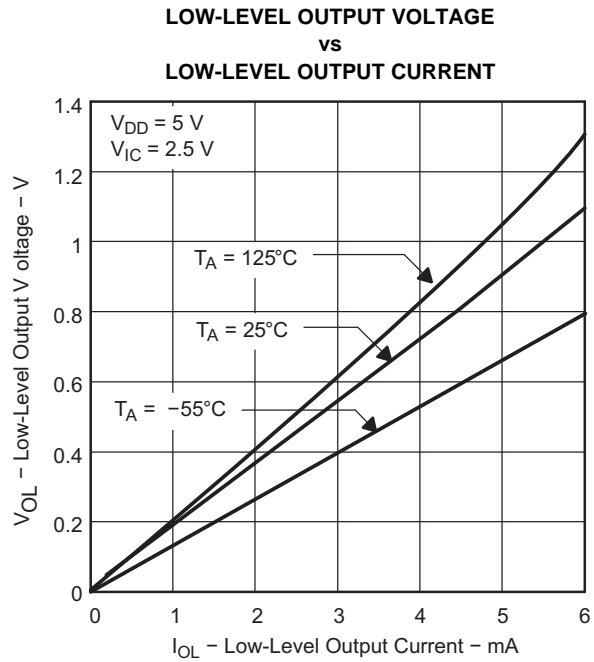
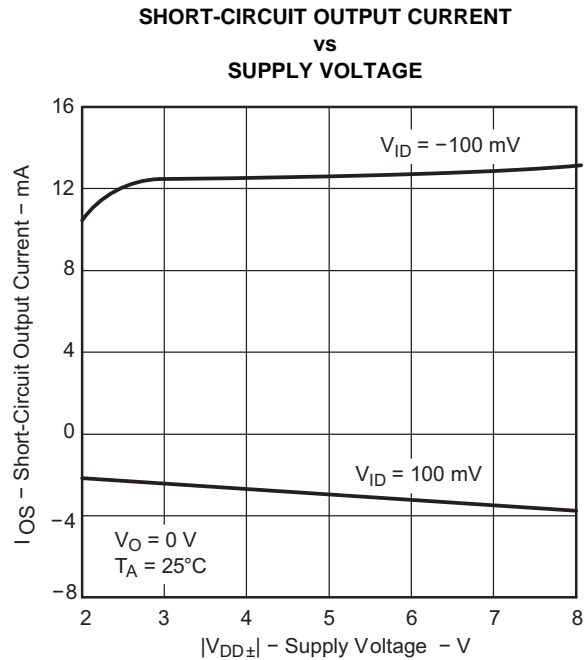
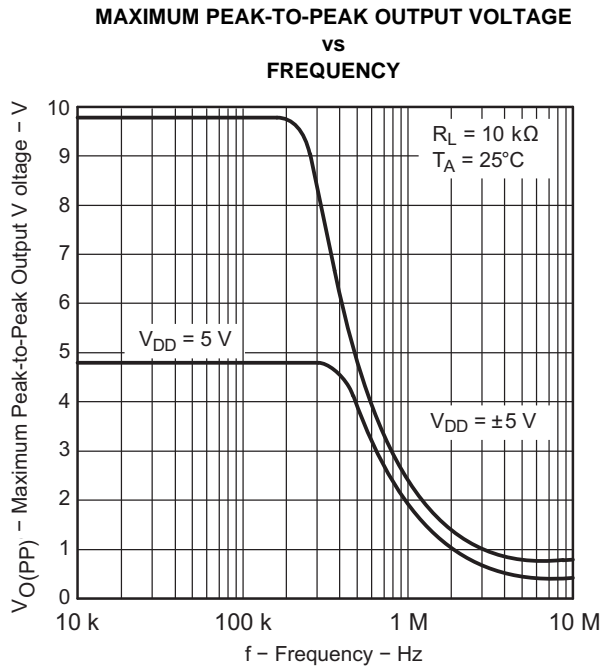
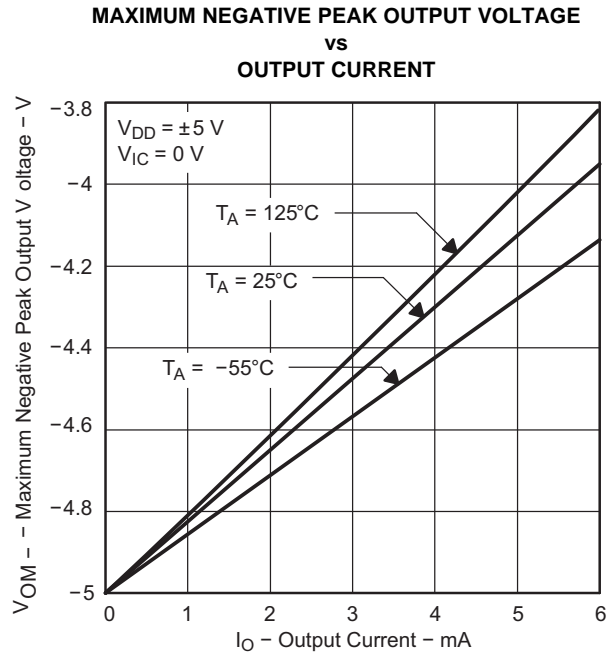
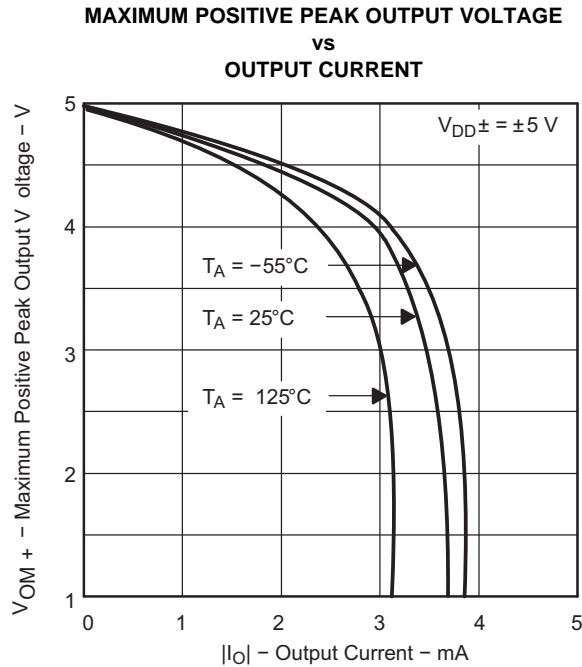
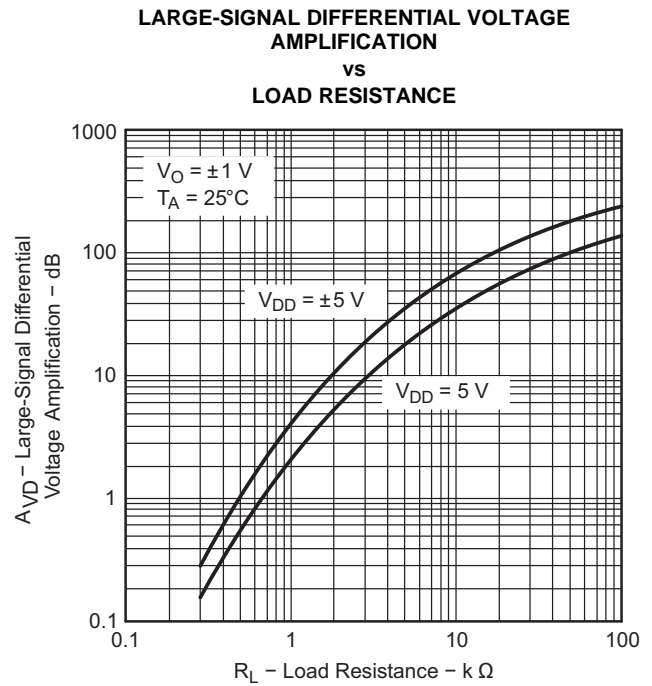
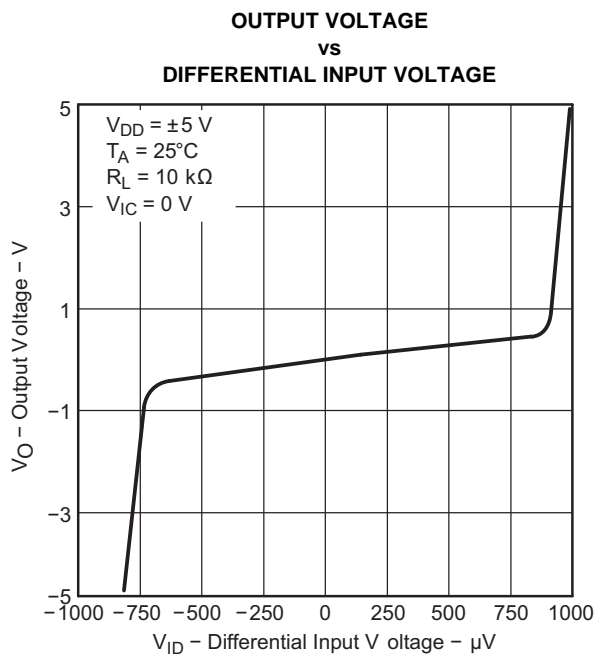
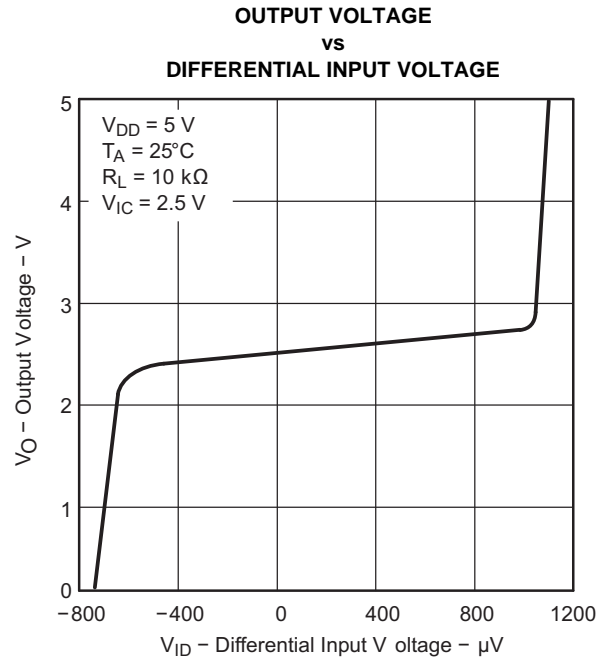
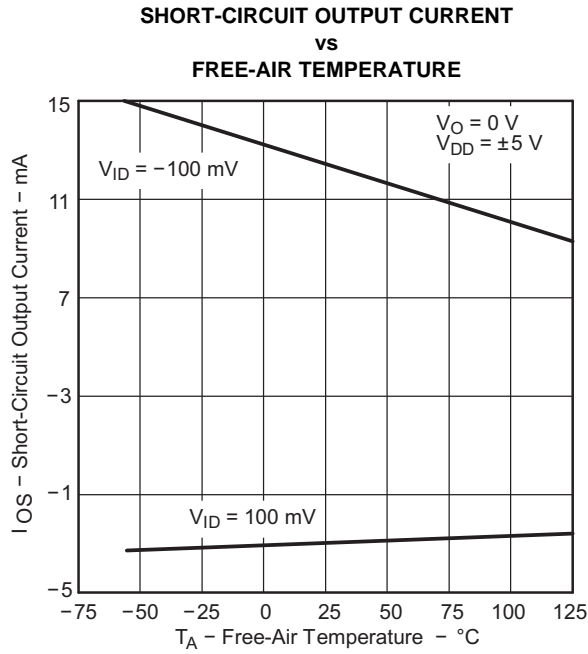


Figure 16.

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.



Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.



Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE MARGIN
vs
FREQUENCY

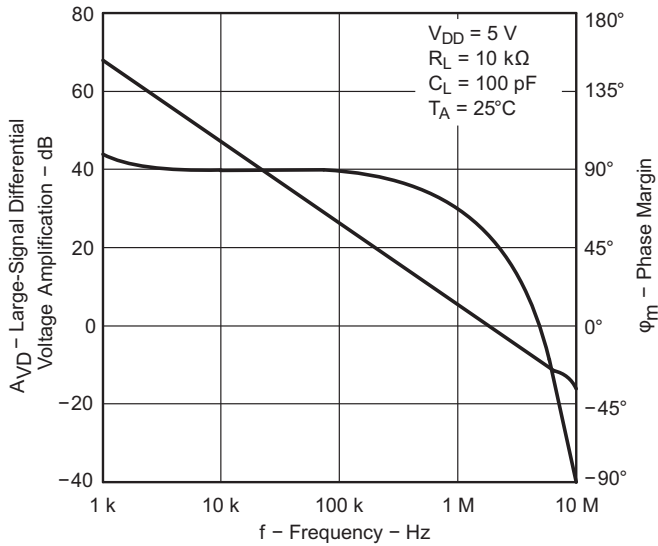


Figure 25.

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE MARGIN
vs
FREQUENCY

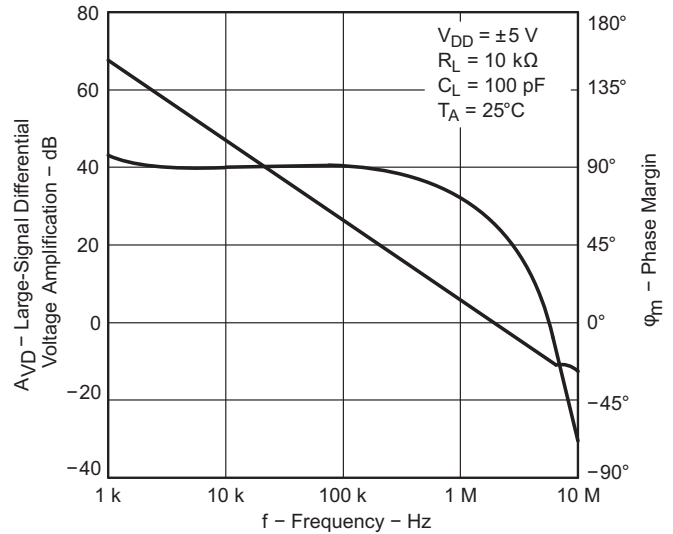


Figure 26.

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

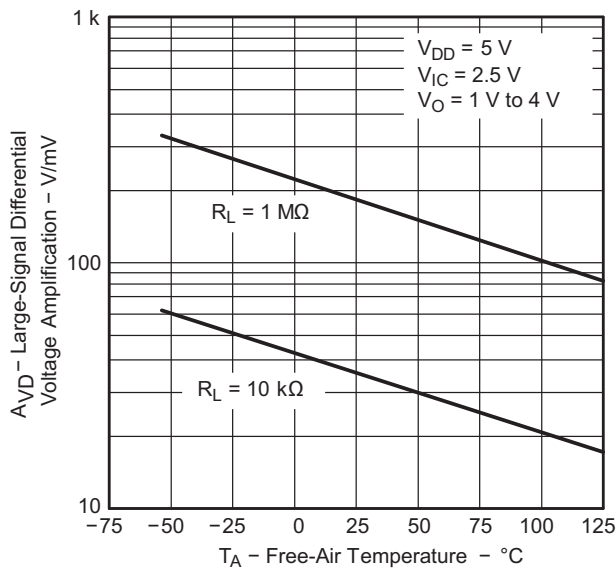


Figure 27.

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

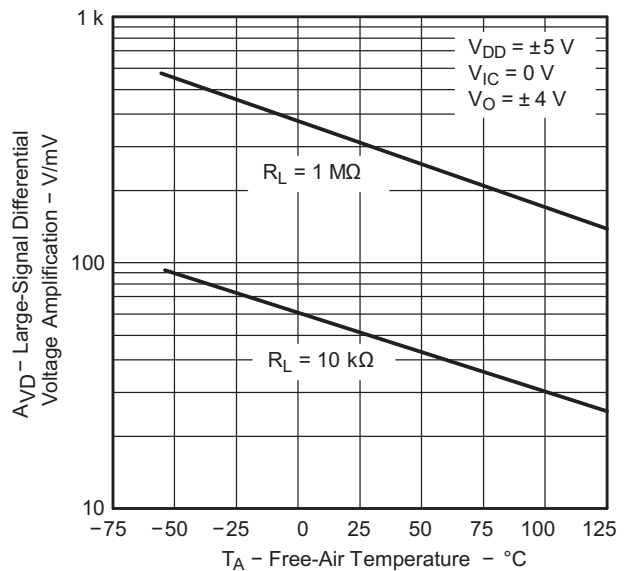


Figure 28.

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

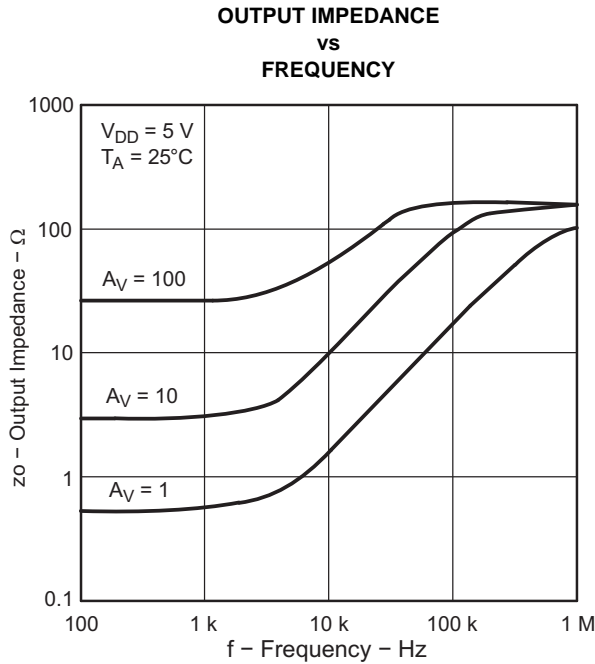


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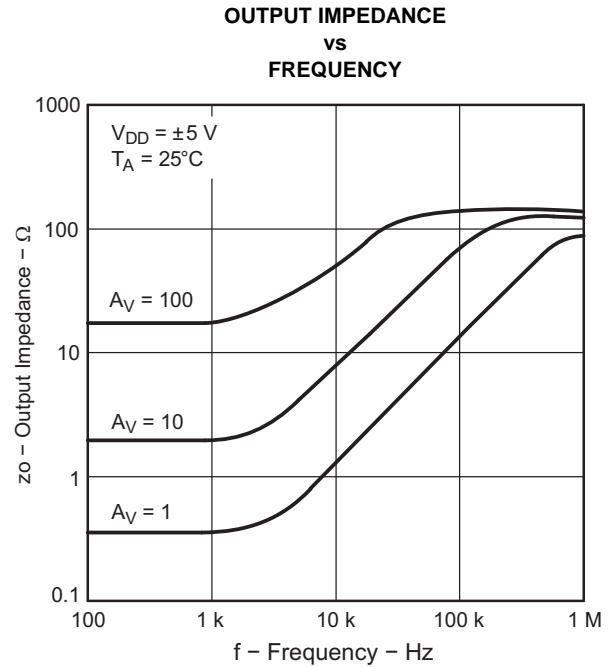


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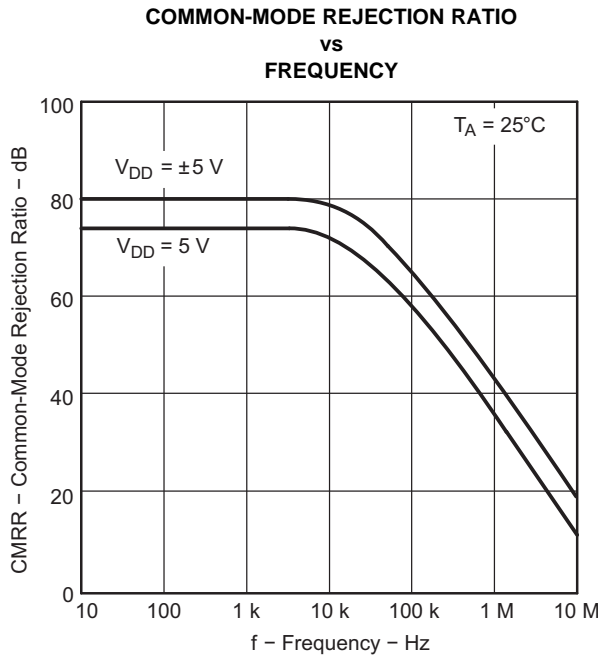


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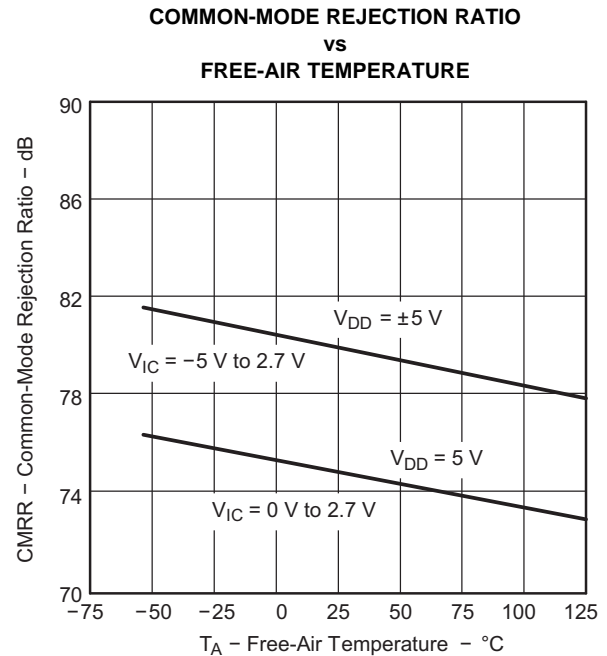


Figure 32.

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

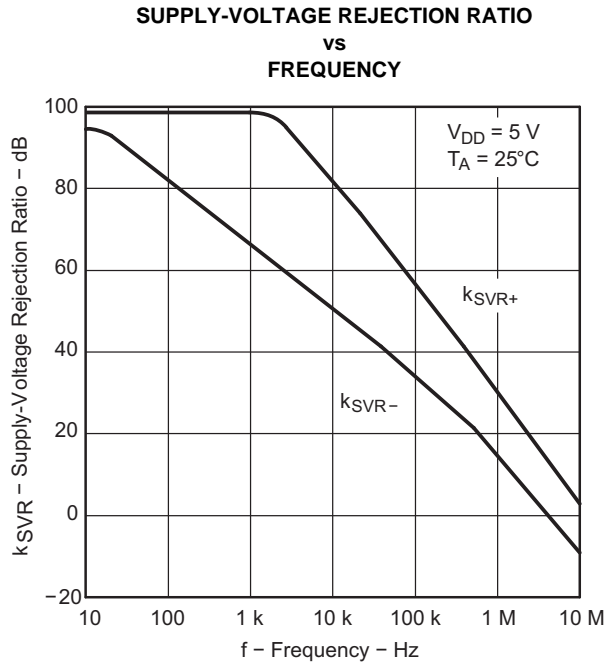


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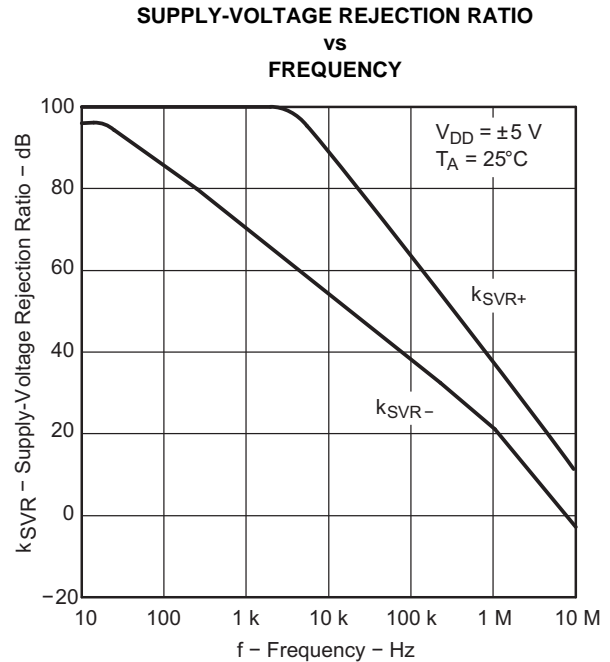


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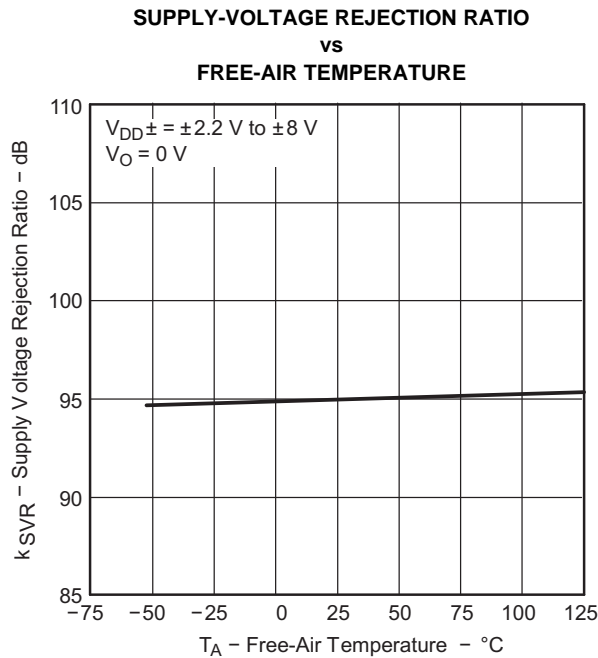


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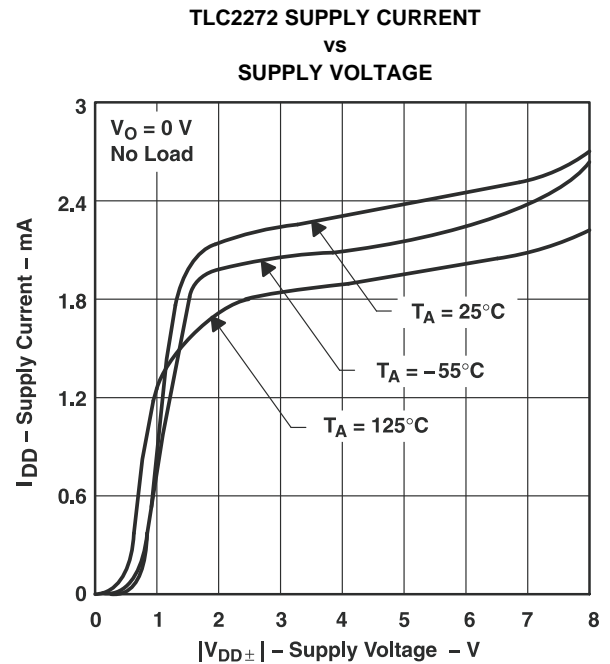
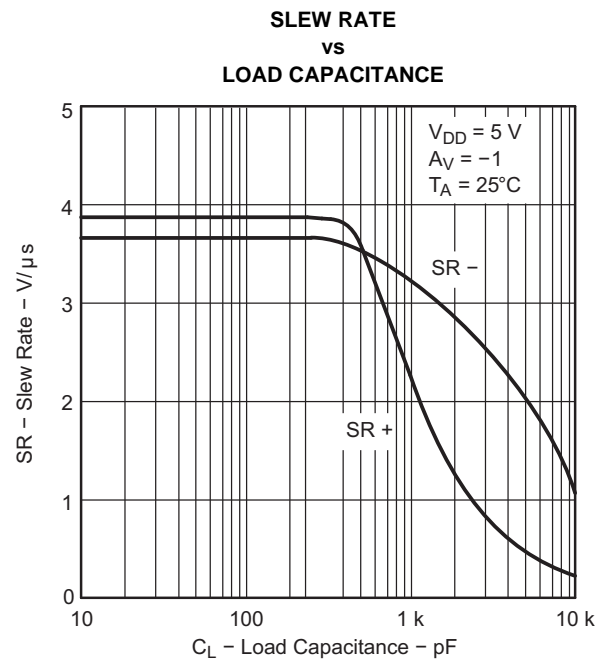
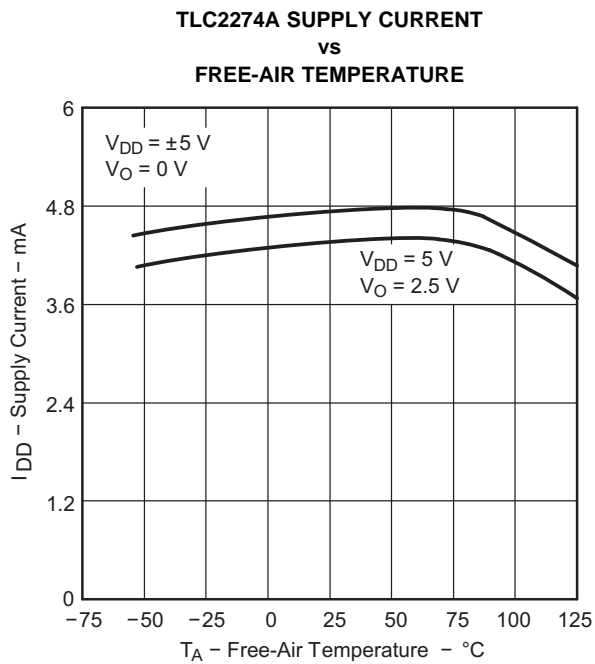
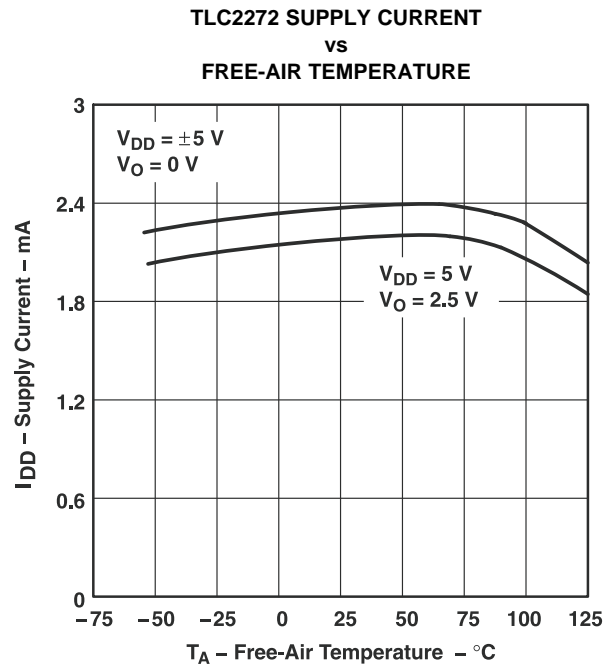
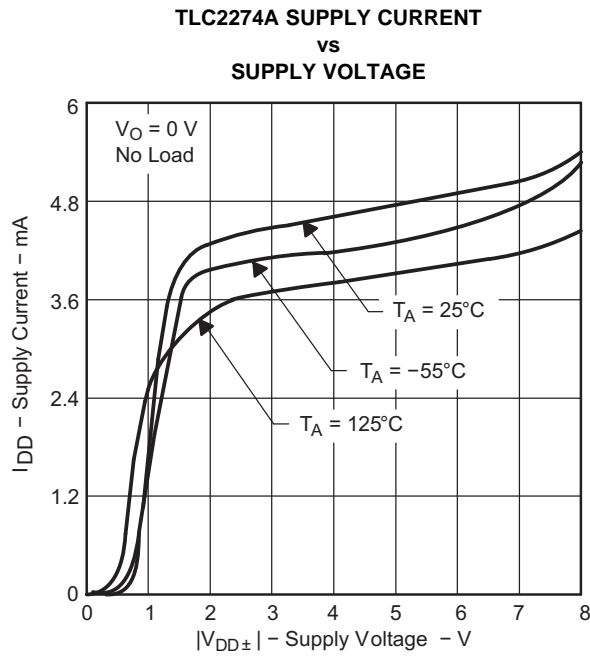
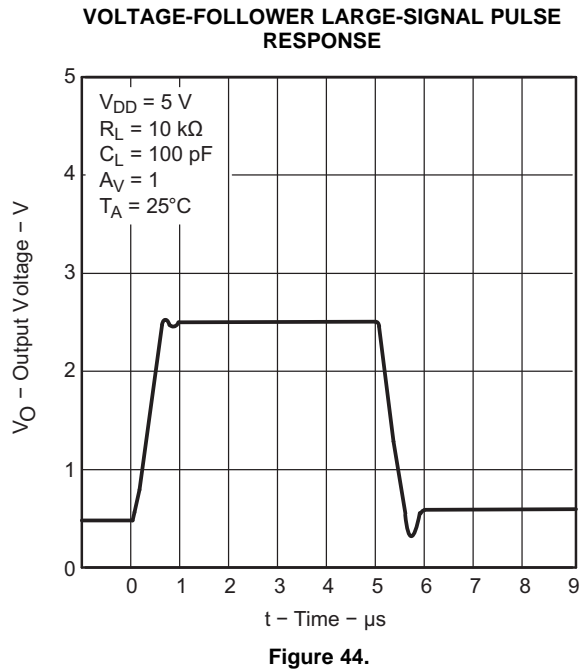
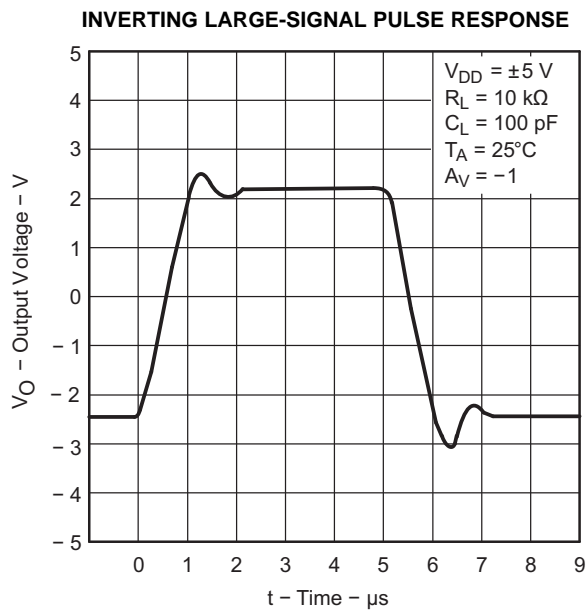
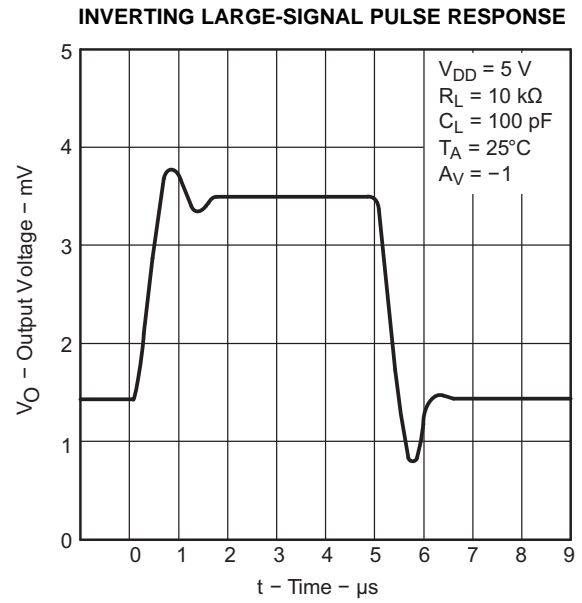
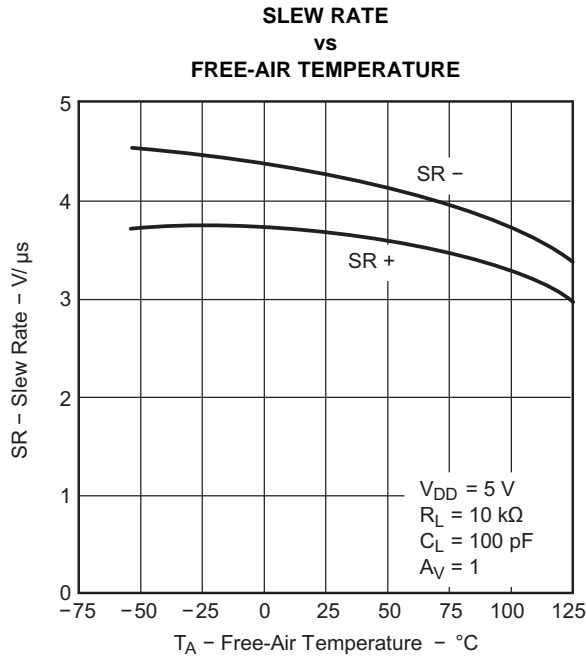


Figure 36.

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.



Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.



Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

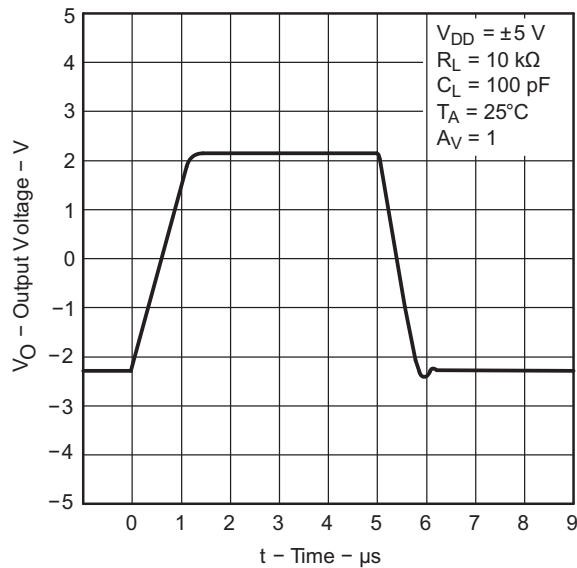


Figure 45.

INVERTING SMALL-SIGNAL PULSE RESPONSE

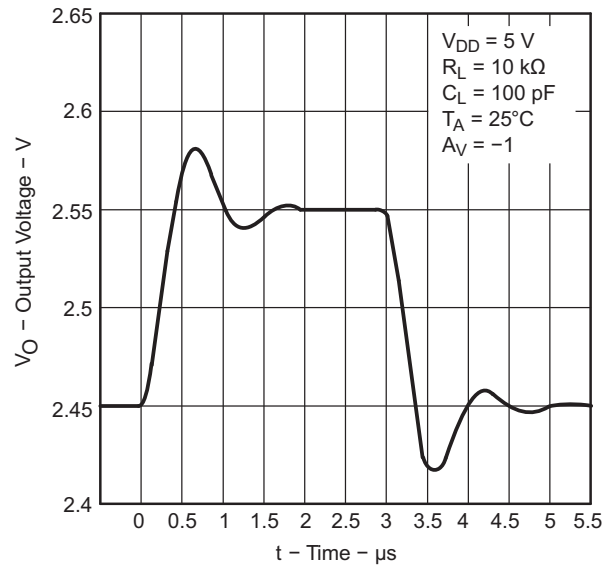


Figure 46.

INVERTING SMALL-SIGNAL PULSE RESPONSE

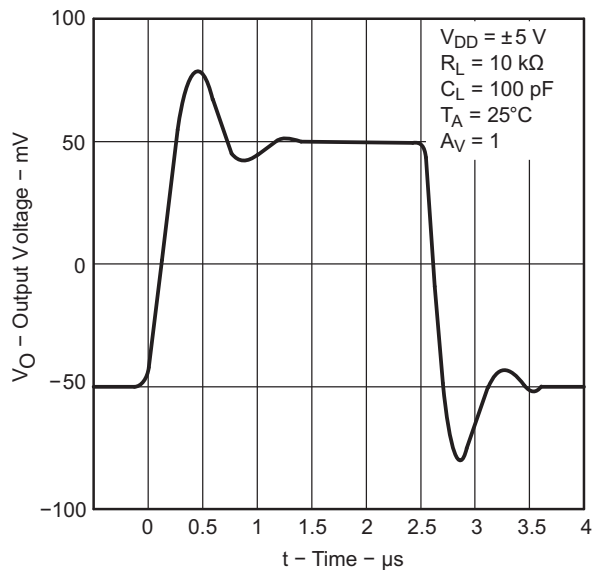


Figure 47.

VOLTAGE-FOLLOWER SMALL-SIGNAL PULSE RESPONSE

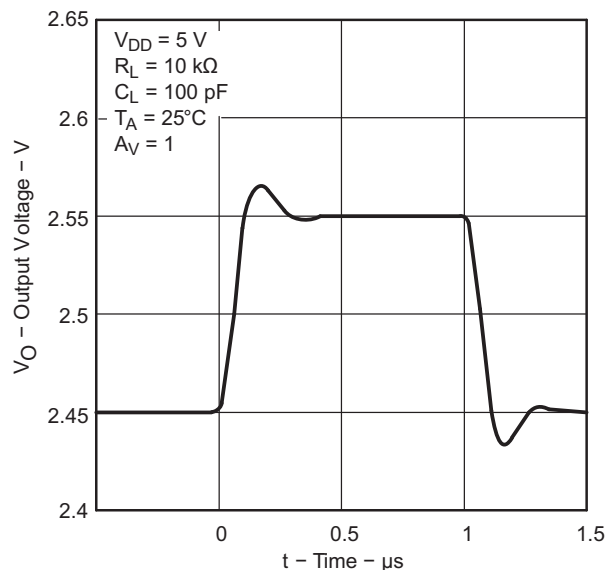


Figure 48.

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

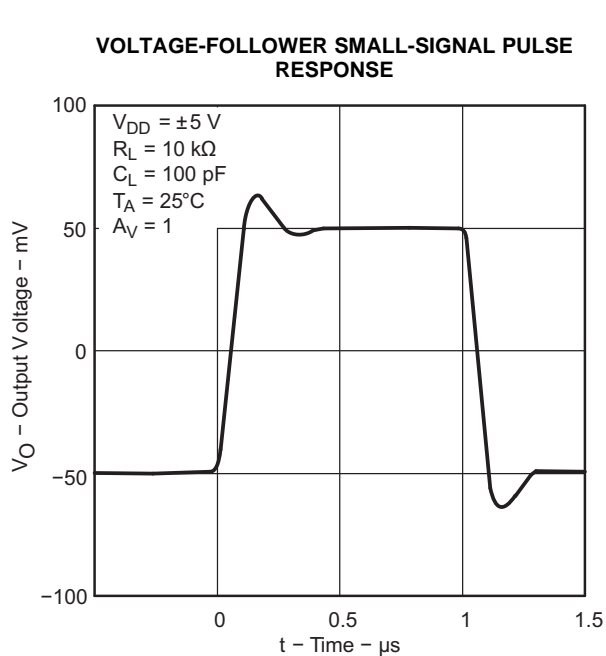


Figure 49.

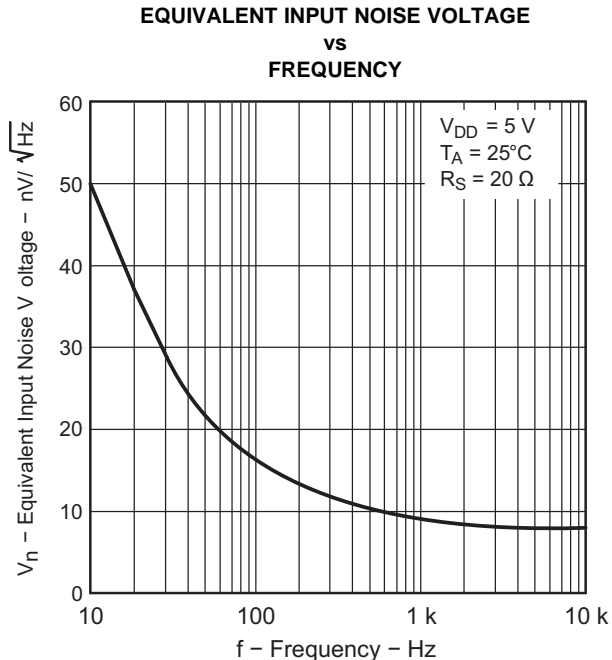


Figure 50.

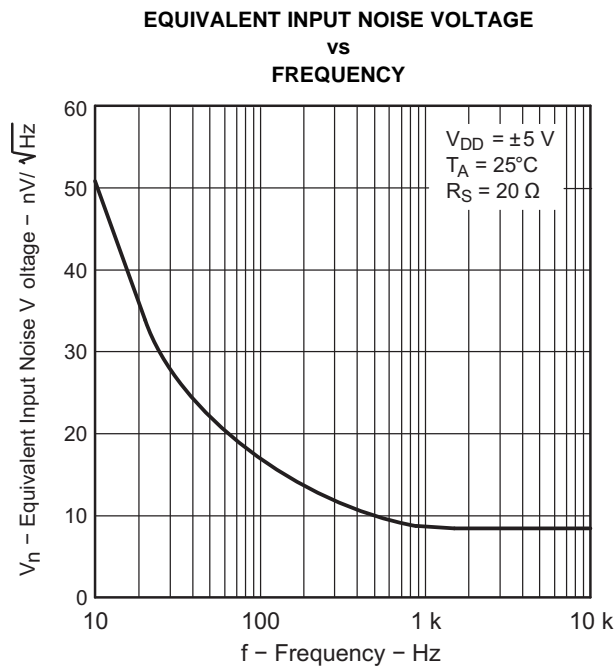


Figure 51.

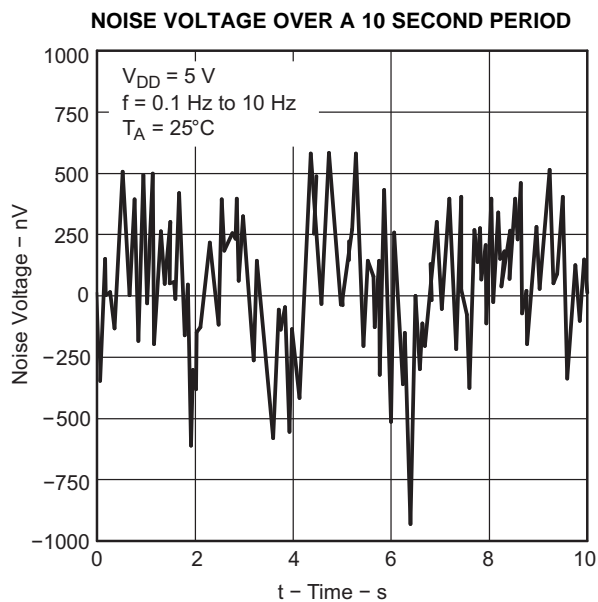


Figure 52.

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

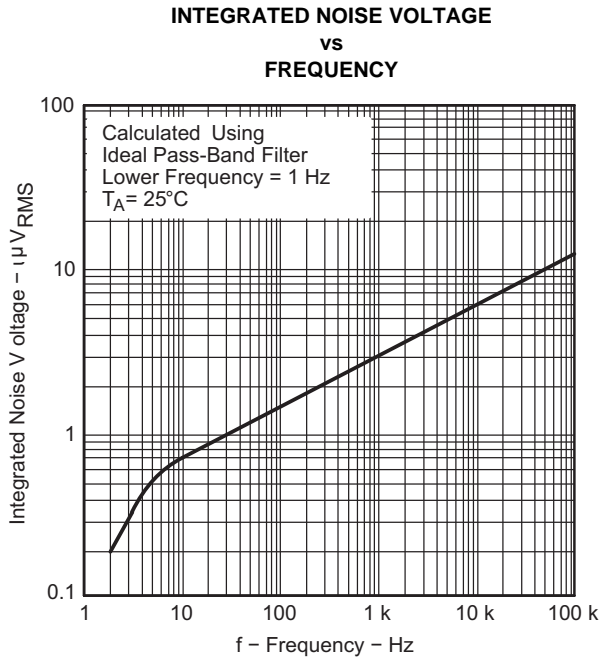


Figure 53.

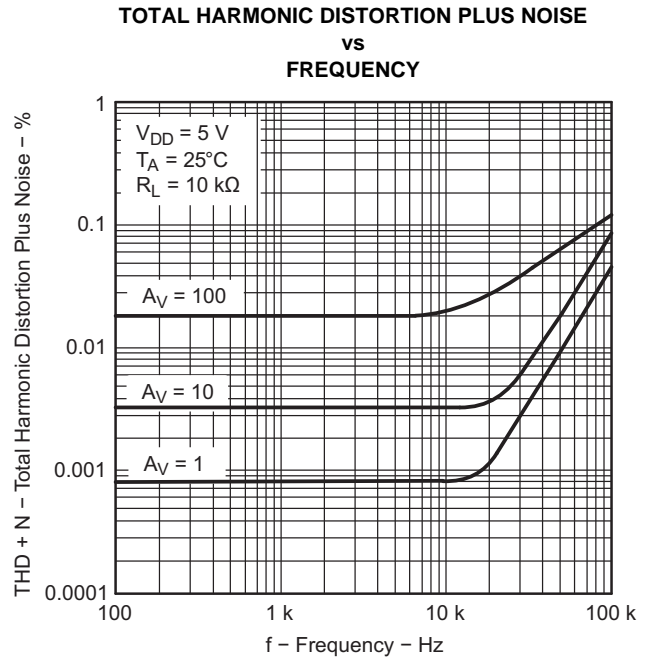


Figure 54.

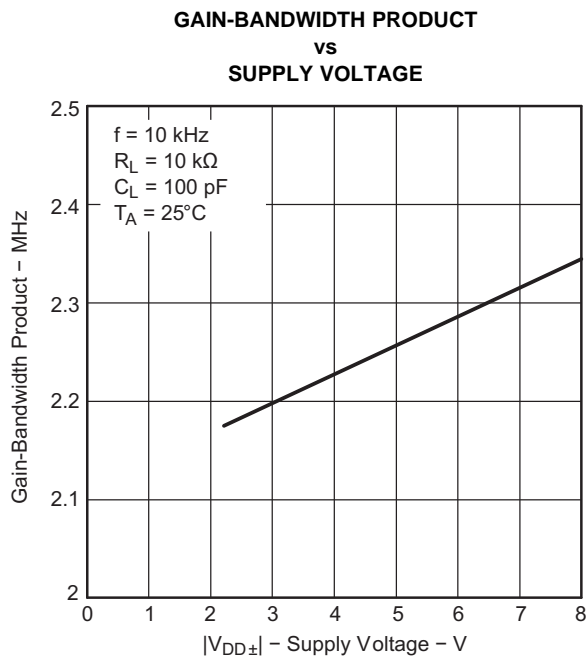


Figure 55.

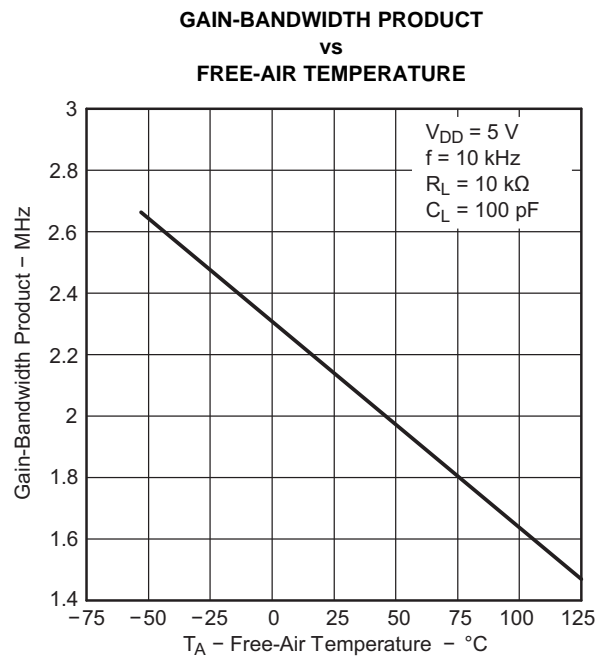
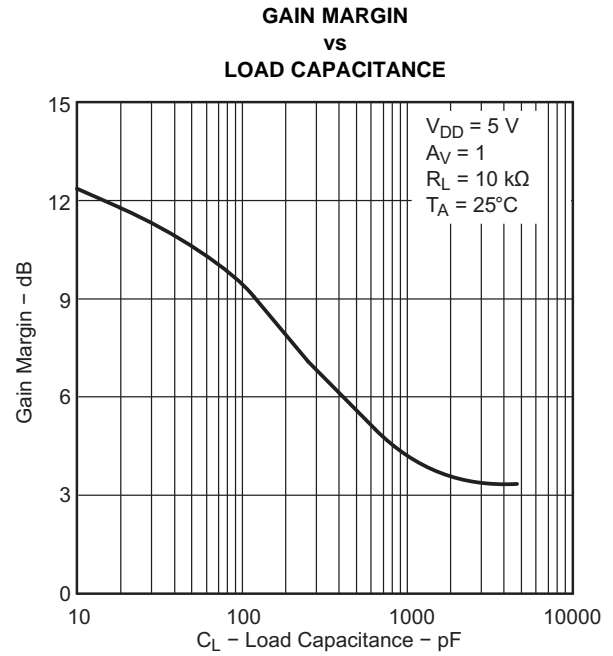
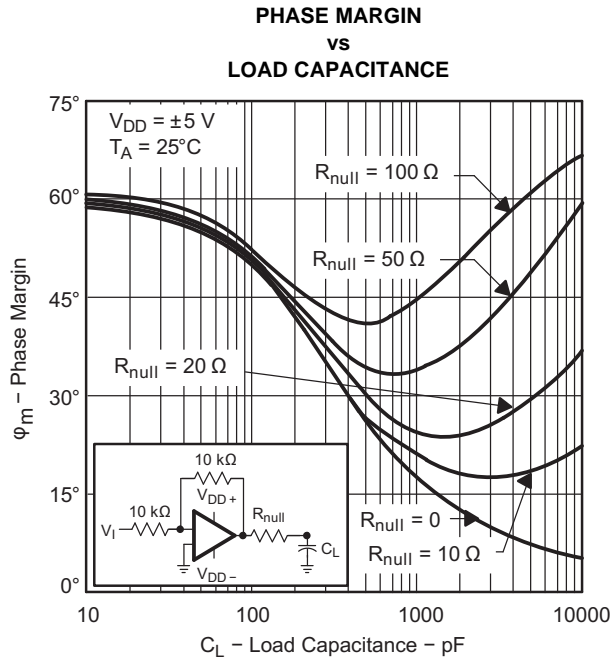


Figure 56.

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.



APPLICATION INFORMATION

Macromodel Information

Macromodel information provided was derived using Microsim Parts, the model generation software used with Microsim PSpice. The Boyle macromodel⁽²⁾ and subcircuit in Figure 59 are generated using the TLC227x typical electrical and operating characteristics at $T_A = 25^\circ\text{C}$. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

(2) G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers", IEEE Journal of Solid-State Circuits, SC-9, 353 (1974).

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

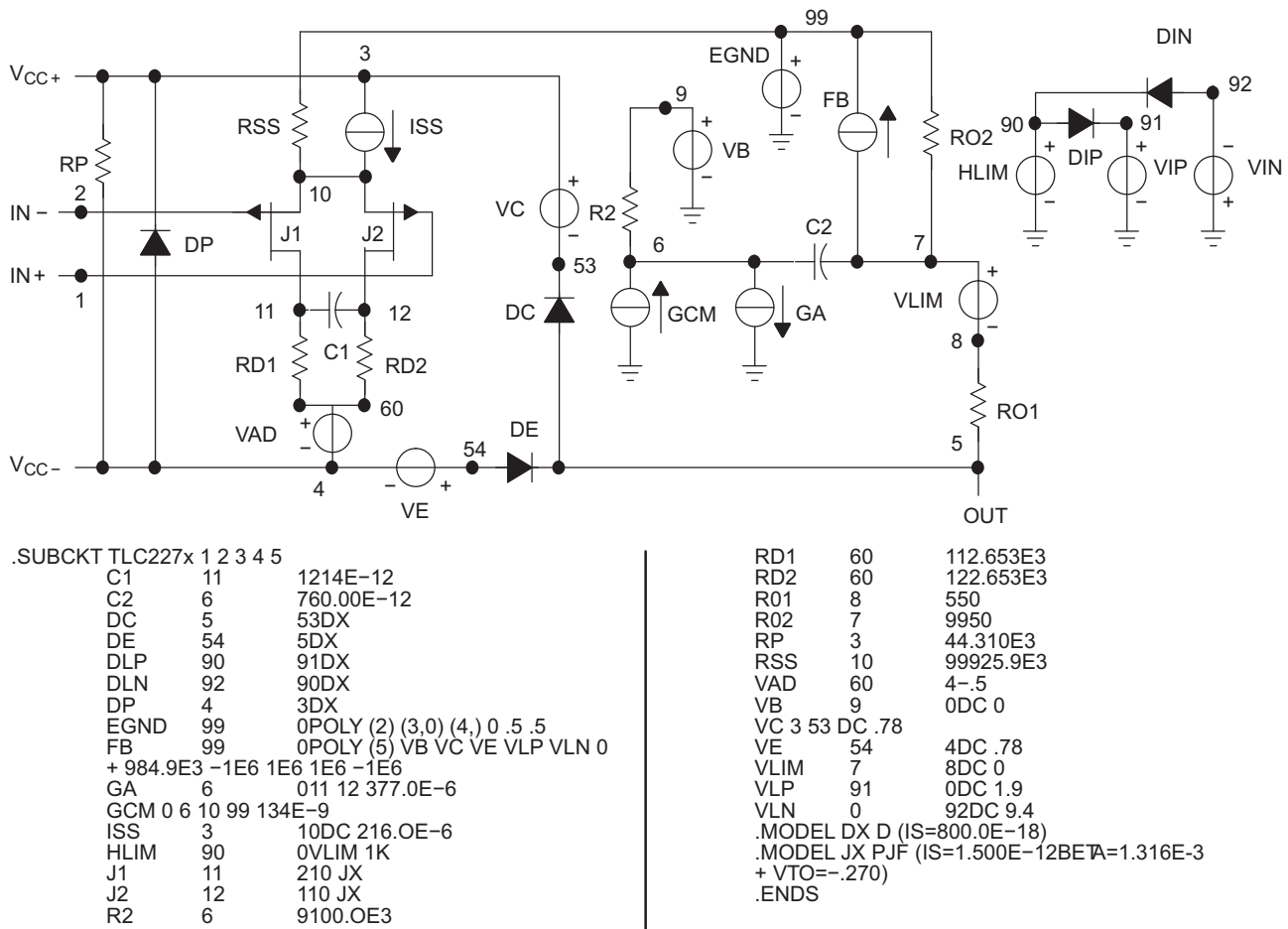


Figure 59. Boyle Macromodels and Subcircuit

REVISION HISTORY

Changes from Revision D (March 2009) to Revision E	Page
• Deleted ESD ratings table	3

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC2272AQDRG4Q1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2272AQ	Samples
TLC2272AQDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2272AQ	Samples
TLC2272AQPWRG4Q1	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2272AQ	Samples
TLC2272AQPWRQ1	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2272AQ	Samples
TLC2272QDRG4Q1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2272Q1	Samples
TLC2272QDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2272Q1	Samples
TLC2272QPWRG4Q1	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2272Q1	Samples
TLC2272QPWRQ1	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2272Q1	Samples
TLC2274AQDRG4Q1	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2274AQ1	Samples
TLC2274AQDRQ1	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2274AQ1	Samples
TLC2274AQPWRG4Q1	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2274AQ1	Samples
TLC2274AQPWRQ1	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2274AQ1	Samples
TLC2274QDRG4Q1	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2274Q1	Samples
TLC2274QDRQ1	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2274Q1	Samples
TLC2274QPWRG4Q1	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2274Q1	Samples
TLC2274QPWRQ1	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2274Q1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF TLC2272-Q1, TLC2272A-Q1, TLC2274-Q1, TLC2274A-Q1 :

● Catalog: [TLC2272](#), [TLC2272A](#), [TLC2274](#), [TLC2274A](#)

● Enhanced Product: [TLC2272A-EP](#), [TLC2274-EP](#), [TLC2274A-EP](#)

● Military: [TLC2272M](#), [TLC2272AM](#), [TLC2274M](#), [TLC2274AM](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC2274AQPWRG4Q1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLC2274AQPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLC2274QPWRG4Q1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLC2274QPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

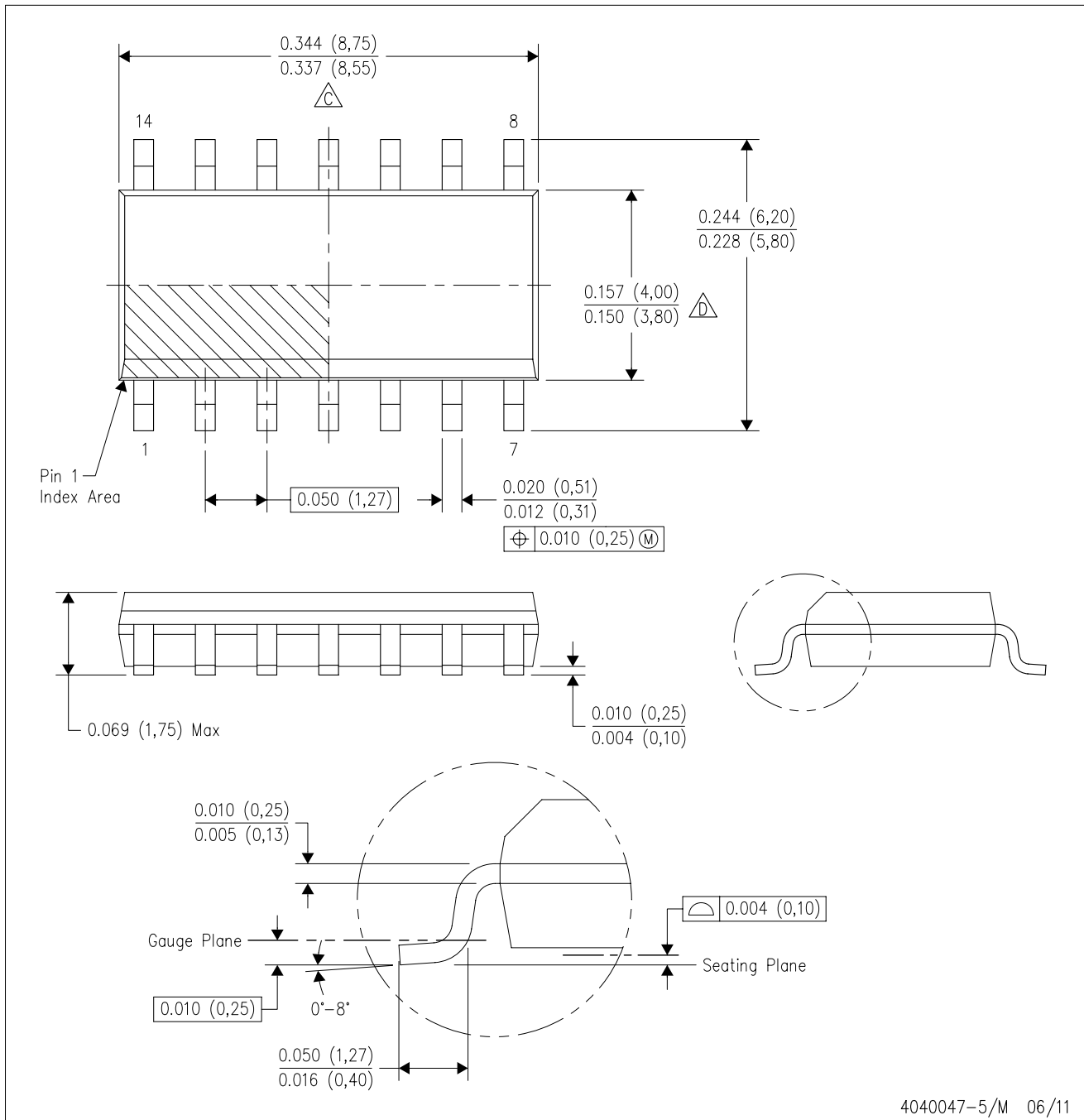
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC2274AQPWRG4Q1	TSSOP	PW	14	2000	367.0	367.0	35.0
TLC2274AQPWRQ1	TSSOP	PW	14	2000	367.0	367.0	35.0
TLC2274QPWRG4Q1	TSSOP	PW	14	2000	367.0	367.0	35.0
TLC2274QPWRQ1	TSSOP	PW	14	2000	367.0	367.0	35.0

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 -  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211284-2/G 08/15

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

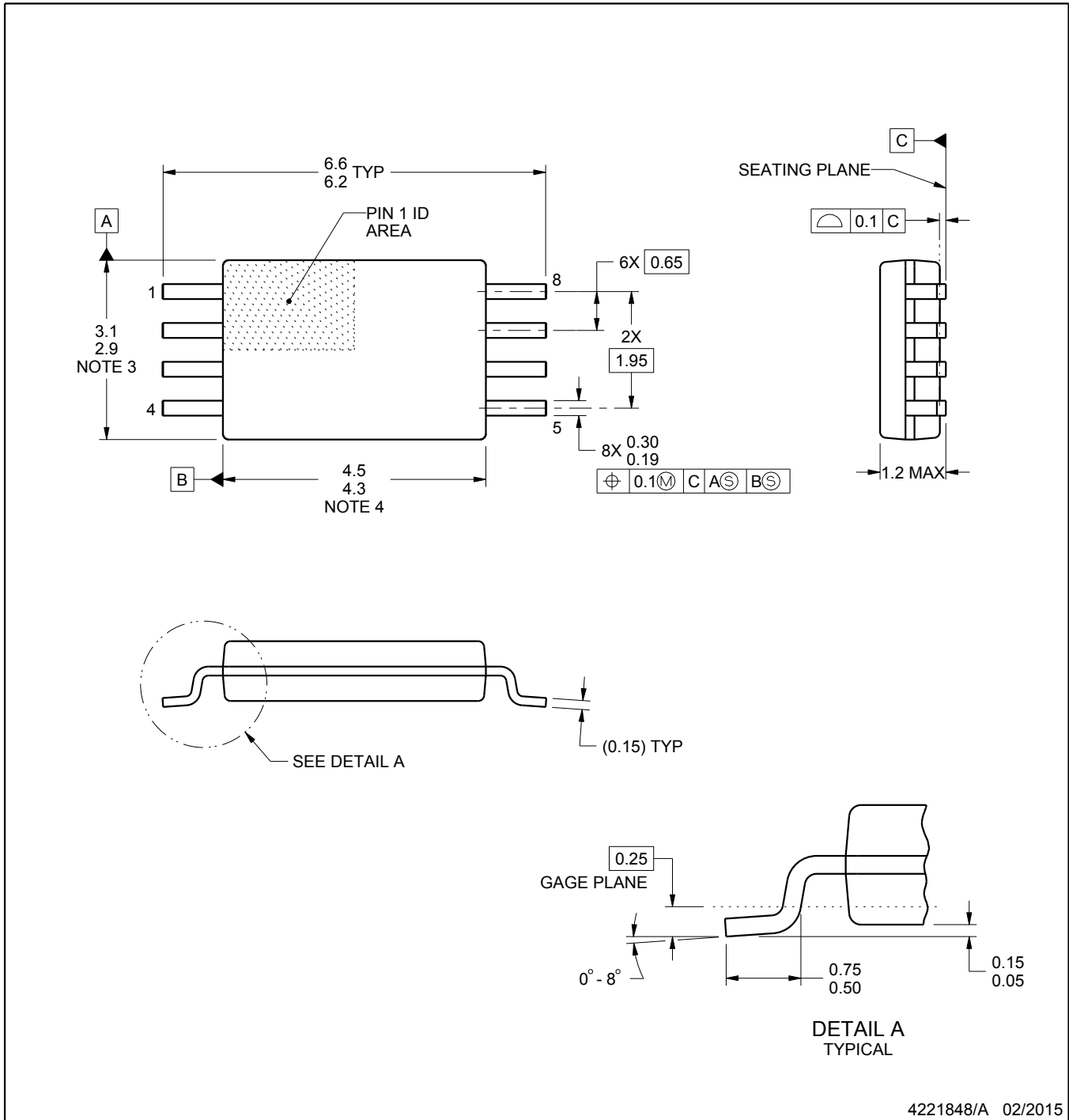
PW0008A



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4221848/A 02/2015

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.

EXAMPLE BOARD LAYOUT

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

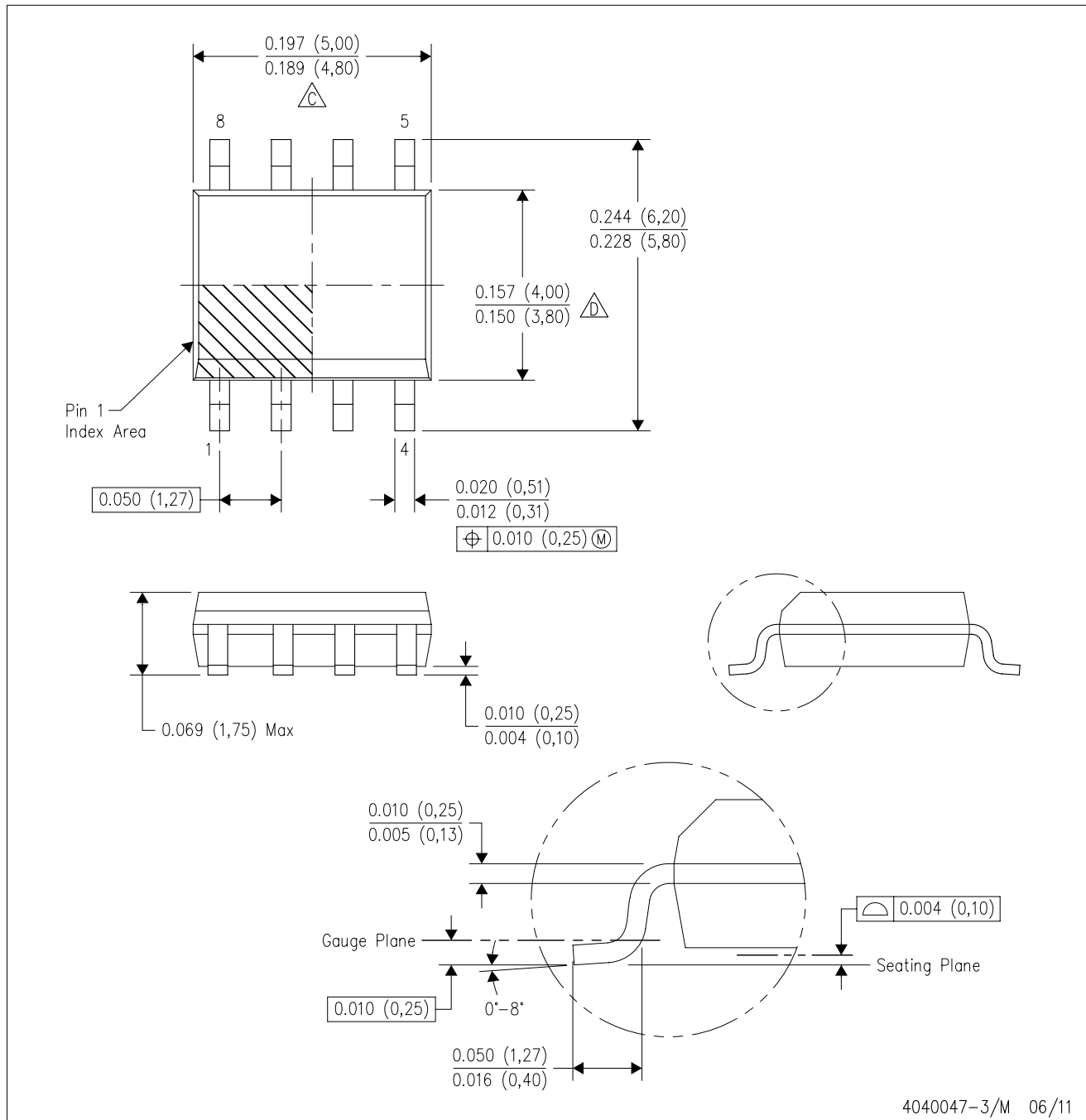
4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

D (R-PDSO-G8)

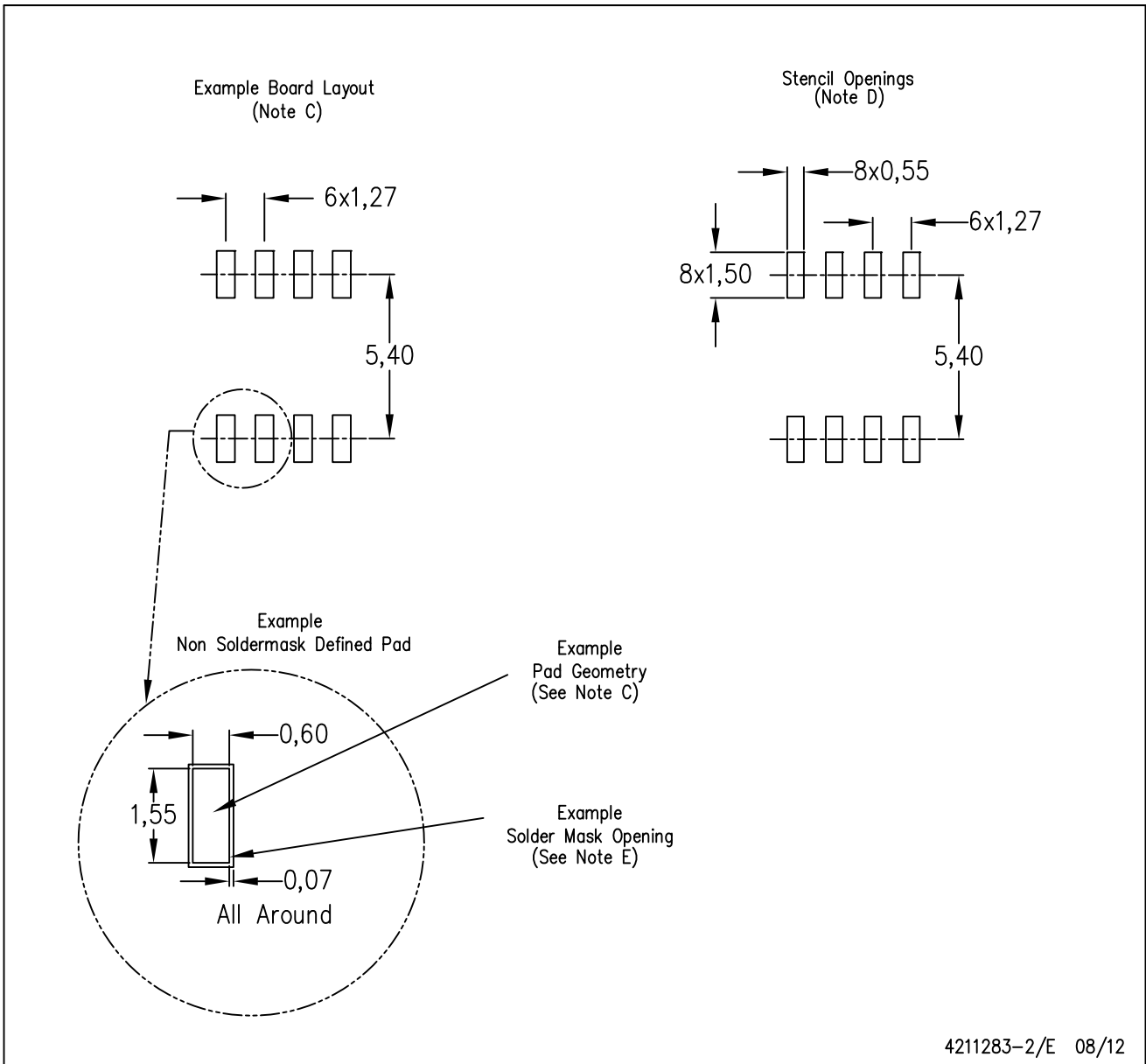
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



4211283-2/E 08/12

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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