

## 8-BIT FM+ I<sup>2</sup>C BUS LED DRIVER

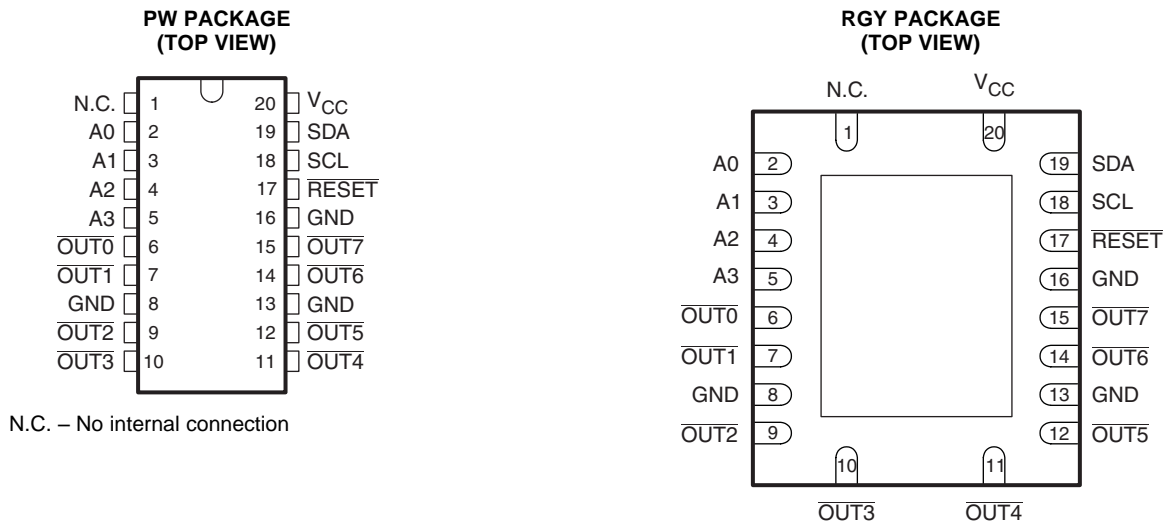
Check for Samples: [TLC59108F](#)

### FEATURES

- Eight LED Drivers (Each Output Programmable at OFF, ON, Programmable LED Brightness, Programmable Group Dimming/Blinking Mixed With Individual LED Brightness)
- Eight Open-Drain Output Channels
- 256-Step (8-Bit) Linear Programmable Brightness Per LED Output Varying From Fully Off (Default) to Maximum Brightness Using a 97-kHz PWM Signal
- 256-Step Group Brightness Control Allows General Dimming [Using a 190-Hz PWM Signal From Fully Off to Maximum Brightness (Default)]
- 256-Step Group Blinking With Frequency Programmable From 24 Hz to 10.73 s and Duty Cycle From 0% to 99.6%
- Four Hardware Address Pins Allow 14 TLC59108F Devices to be Connected to the Same I<sup>2</sup>C Bus
- Four Software Programmable I<sup>2</sup>C Bus Addresses (One LED Group Call Address and Three LED Sub Call Addresses) Allow Groups of Devices to be Simultaneously Addressed Any Combination (For Example, One Register Used for 'All Call' so That All the TLC59108Fs on the I<sup>2</sup>C Bus Can be Simultaneously Addressed and the Second Register Used for Three Different Addresses so That One Third of All Devices on the Bus Can be Simultaneously Addressed)
- Software Enable and Disable for I<sup>2</sup>C Bus Address
- Software Reset Feature (SWRST Call) Allows the Device to be Reset Through the I<sup>2</sup>C Bus
- Up to 14 Possible Hardware Adjustable Individual I<sup>2</sup>C Bus Addresses Per Device so That Each Device Can be Programmed
- Output State Change Programmable on the Acknowledge or the STOP Command to Update Outputs Byte-by-Byte or All at the Same Time (Default to 'Change on STOP')
- Maximum Output Current: 120 mA
- Maximum Output Voltage: 17 V
- 25-MHz Internal Oscillator Requires No External Components
- 1-MHz Fast-Mode Plus (FM+) Compatible I<sup>2</sup>C Bus Interface With 30 mA High Drive Capability on SDA Output for Driving High Capacitive Buses
- Internal Power-On Reset
- Noise Filter on SCL/SDA Inputs
- No Glitch on Power Up
- Active-Low Reset ( $\overline{\text{RESET}}$ )
- Supports Hot Insertion
- Low Standby Current
- 3.3-V or 5-V Supply Voltage
- 5.5-V Tolerant Inputs
- Packages Offered: 20-Pin Thin Shrink Small-Outline Package (TSSOP) (PW), 20-Pin Quad Flatpack No Lead (QFN) (RGY)
- –40°C to 85°C Operation



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



N.C. – No internal connection

**DESCRIPTION/ORDERING INFORMATION**

The TLC59108F is an I<sup>2</sup>C bus controlled 8-bit LED driver optimized for red/green/blue/amber (RGBA) color mixing applications. Each LED output has its own 8-bit resolution (256 steps) fixed frequency individual PWM controller that operates at 97 kHz with a duty cycle that is adjustable from 0% to 99.6% to allow the LED to be set to a specific brightness value. An additional 8-bit resolution (256 steps) group PWM controller has both a fixed frequency of 190 Hz and an adjustable frequency between 24 Hz to once every 10.73 seconds with a duty cycle that is adjustable from 0% to 99.6% that is used to either dim or blink all LEDs with the same value.

Each LED output can be off, on (no PWM control), set at its individual PWM controller value or at both individual and group PWM controller values. The TLC59108F operates with a supply voltage range of 3 V to 5.5 V and the outputs are 17 V tolerant. LEDs can be directly connected to the TLC59108F device outputs.

Software programmable LED group and three sub call I<sup>2</sup>C bus addresses allow all or defined groups of TLC59108F devices to respond to a common I<sup>2</sup>C bus address, allowing for example, all the same color LEDs to be turned on or off at the same time or marquee chasing effect, thus minimizing I<sup>2</sup>C bus commands.

Four hardware address pins allow up to 14 devices on the same bus.

The software reset (SWRST) call allows the master to perform a reset of the TLC59108F through the I<sup>2</sup>C bus, identical to the power-on reset (POR) that initializes the registers to their default state causing the outputs to be set high (LED off). This allows an easy and quick way to reconfigure all device registers to the same condition.

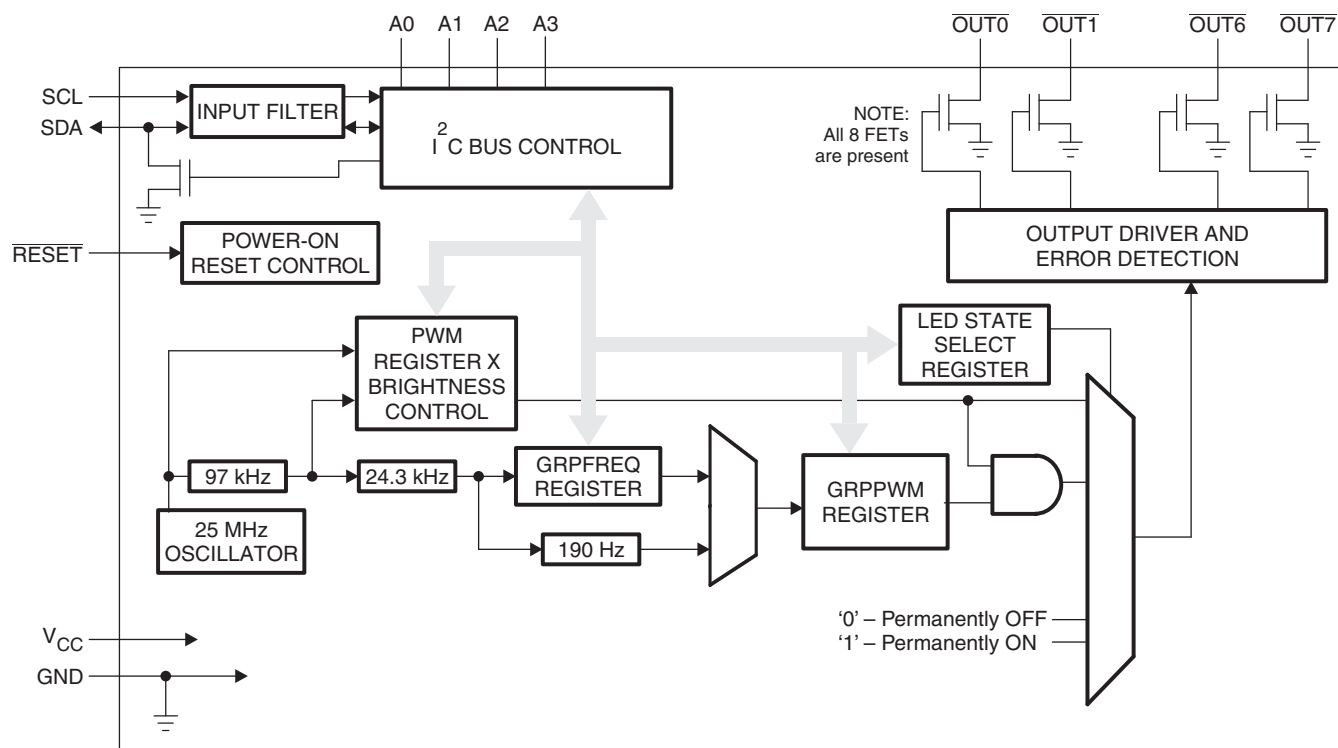
**ORDERING INFORMATION**

T <sub>A</sub>	PACKAGE <sup>(1)</sup> <sup>(2)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	QFN – RGY	Reel of 3000	TLC59108FIRGYR	Y59108F
	TSSOP – PW	Reel of 3000	TLC59108FIPWR	Y59108F

(1) Package drawings, thermal data, and symbolization are available at [www.ti.com/packaging](http://www.ti.com/packaging).

(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).

**BLOCK DIAGRAM**



NOTE: Only one PWM shown for clarity.

**TERMINAL FUNCTIONS**

TERMINAL		I/O <sup>(1)</sup>	DESCRIPTION
NAME	PW/RGY PIN NO.		
N.C.	1	I	No internal connection
A0	2	I	Address input 0
A1	3	I	Address input 1
A2	4	I	Address input 2
A3	5	I	Address input 3
$\overline{\text{OUT0}}, \overline{\text{OUT1}}, \overline{\text{OUT2}}, \overline{\text{OUT3}}, \overline{\text{OUT4}}, \overline{\text{OUT6}}, \overline{\text{OUT6}}, \overline{\text{OUT7}}$	6, 7, 9, 10, 11, 12, 14, 15	O	Constant current output 0 to 7, LED ON at low
GND	8, 13, 16	–	Ground
$\overline{\text{RESET}}$	17	I	Active-low reset input
SCL	18	I	Serial clock input
SDA	19	I/O	Serial data input/output
V <sub>CC</sub>	20	–	Power supply

(1) I = input, O = output

## THERMAL INFORMATION

THERMAL METRIC <sup>(1)</sup>	TLC59108F		UNITS
	PW	RGY	
	20 PINS	20 PINS	
$\theta_{JA}$ Junction-to-ambient thermal resistance	98.9	39.1	°C/W
$\theta_{JCTop}$ Junction-to-case (top) thermal resistance	32.9	44.7	
$\theta_{JB}$ Junction-to-board thermal resistance	49.9	14.8	
$\psi_{JT}$ Junction-to-top characterization parameter	1.7	1.0	
$\psi_{JB}$ Junction-to-board characterization parameter	49.3	14.9	
$\theta_{JCbott}$ Junction-to-case (bottom) thermal resistance	n/a	7.6	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{CC}$ Supply voltage range		0	7	V
$V_I$ Input voltage range		-0.4	7	V
$V_O$ Output voltage range		-0.5	20	V
$I_O$ Continuous output current			120	mA
$P_D$ Power dissipation, $T_A = 25\text{ }^\circ\text{C}$ , JESD 51-7	PW package		1.2	W
	RGY package		2.2	
$T_J$ Junction temperature range		-40	150	°C
$T_{stg}$ Storage temperature range		-55	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## RECOMMENDED OPERATING CONDITIONS<sup>(1)</sup>

	TEST CONDITIONS	MIN	MAX	UNIT
$V_{CC}$ Supply voltage		3	5.5	V
$V_{IH}$ High-level input voltage	SCL, SDA, $\overline{\text{RESET}}$ , A0, A1, A2, A3	$0.7 \times V_{CC}$	5.5	V
$V_{IL}$ Low-level input voltage	SCL, SDA, $\overline{\text{RESET}}$ , A0, A1, A2, A3	0	$0.3 \times V_{CC}$	V
$V_O$ Output voltage	$\overline{\text{OUT0}}$ to $\overline{\text{OUT7}}$		17	V
$I_{OL}$ Low-level output current	SDA	$V_{CC} = 3\text{ V}$	20	mA
		$V_{CC} = 4.5\text{ V}$	30	
$I_O$ Output current	$\overline{\text{OUT0}}$ to $\overline{\text{OUT7}}$	5	120	mA
$T_A$ Operating free-air temperature		-40	85	°C

(1) All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation.

**ELECTRICAL CHARACTERISTICS**
 $V_{CC} = 3\text{ V to }5.5\text{ V}$ ,  $T_A = -40^\circ\text{C to }85^\circ\text{C}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
$I_i$	Input/output leakage current	SCL, SDA, A0, A1, A2, A3, RESET $V_i = V_{CC}$ or GND			±0.3	μA
	Output leakage current	$\overline{\text{OUT0}}$ to $\overline{\text{OUT7}}$ $V_O = 17\text{ V}$ , $T_J = 25^\circ\text{C}$			0.5	μA
$V_{POR}$	Power-on reset voltage			2.5		V
$I_{OL}$	Low-level output current	SDA $V_{CC} = 3\text{ V}$ , $V_{OL} = 0.4\text{ V}$	20			mA
		$V_{CC} = 5\text{ V}$ , $V_{OL} = 0.4\text{ V}$	30			
$V_{OL}$	Low-level output voltage	$\overline{\text{OUT0}}$ to $\overline{\text{OUT7}}$ $V_{CC} = 3\text{ V}$ , $I_{OL} = 120\text{ mA}$		230	450	mV
		$V_{CC} = 4.5\text{ V}$ , $I_{OL} = 120\text{ mA}$		200	400	
$r_{ON}$	ON-state resistance	$\overline{\text{OUT0}}$ to $\overline{\text{OUT7}}$ $V_{CC} = 3\text{ V}$ , $I_{OL} = 120\text{ mA}$		1.92	3.75	Ω
		$V_{CC} = 4.5\text{ V}$ , $I_{OL} = 120\text{ mA}$		1.64	3.3	
$T_{SD}$	Overtemperature shutdown <sup>(2)</sup>		150	175	200	°C
$T_{HYS}$	Restart hysteresis			15		°C
$C_i$	Input capacitance	SCL, A0, A1, A2, A3, RESET $V_i = V_{CC}$ or GND		5		pF
$C_{io}$	Input/output capacitance	SDA $V_i = V_{CC}$ or GND		8		pF
$I_{CC}$	Supply current	$V_{CC} = 3\text{ V}$			6	mA
		$V_{CC} = 4.5\text{ V}$	$\overline{\text{OUT0}}$ to $\overline{\text{OUT7}} = \text{OFF}$		9	

- (1) All typical values are at  $T_A = 25^\circ\text{C}$ .  
 (2) Specified by design, not production tested.

## I<sup>2</sup>C INTERFACE TIMING REQUIREMENTS

 $T_A = -40^{\circ}\text{C to } 85^{\circ}\text{C}$ 

		STANDARD-MODE I <sup>2</sup> C BUS		FAST-MODE I <sup>2</sup> C BUS		FAST-MODE PLUS I <sup>2</sup> C BUS		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
<b>I<sup>2</sup>C Interface</b>								
$f_{\text{SCL}}$	SCL clock frequency	0	100	0	400	0	1000	kHz
$t_{\text{BUF}}$	I <sup>2</sup> C bus free time between Stop and Start	4.7		1.3		0.5		$\mu\text{s}$
$t_{\text{HD;STA}}$	Hold time (repeated) for Start condition	4		0.6		0.26		$\mu\text{s}$
$t_{\text{SU;STA}}$	Set-up time (repeated) for Start condition	4.7		0.6		0.26		$\mu\text{s}$
$t_{\text{SU;STO}}$	Set-up time for Stop condition	4		0.6		0.26		$\mu\text{s}$
$t_{\text{HD;DAT}}$	Data hold time	0		0		0		ns
$t_{\text{VD;ACK}}$	Data valid acknowledge time <sup>(1)</sup>	0.3	3.45	0.1	0.9	0.05	0.45	$\mu\text{s}$
$t_{\text{VD;DAT}}$	Data valid time <sup>(2)</sup>	0.3	3.45	0.1	0.9	0.05	0.45	$\mu\text{s}$
$t_{\text{SU;DAT}}$	Data set-up time	250		100		50		ns
$t_{\text{LOW}}$	Low period of the SCL clock	4.7		1.3		0.5		$\mu\text{s}$
$t_{\text{HIGH}}$	High period of the SCL clock	4		0.6		0.26		$\mu\text{s}$
$t_f$	Fall time of both SDA and SCL signals <sup>(3) (4)</sup>		300	$20+0.1C_b$ <sup>(5)</sup>	300		120	ns
$t_r$	Rise time of both SDA and SCL signals		1000	$20+0.1C_b$ <sup>(5)</sup>	300		120	ns
$t_{\text{SP}}$	Pulse width of spikes that must be suppressed by the input filter <sup>(6)</sup>		50		50		50	ns
<b>Reset</b>								
$t_{\text{W}}$	Reset pulse width	10		10		10		ns
$t_{\text{REC}}$	Reset recovery time	0		0		0		ns
$t_{\text{RESET}}$	Time to reset <sup>(7) (8)</sup>	400		400		400		ns

(1)  $t_{\text{VD;ACK}}$  = time for Acknowledgement signal from SCL low to SDA (out) low.

(2)  $t_{\text{VD;DAT}}$  = minimum time for SDA data out to be valid following SCL low.

(3) A master device must internally provide a hold time of at least 300 ns for the SDA signal (refer to the  $V_{\text{IL}}$  of the SCL signal) in order to bridge the undefined region of SCLs falling edge.

(4) The maximum  $t_f$  for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time ( $t_f$ ) for the SDA output stage is specified at 250 ns. This allows series protection resistors to be connected between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified  $t_f$ .

(5)  $C_b$  = total capacitance of one bus line in pF.

(6) Input filters on the SDA and SCL inputs suppress noise spikes less than 50 ns

(7) Resetting the device while actively communicating on the bus may cause glitches or errant Stop conditions.

(8) Upon reset, the full delay will be the sum of  $t_{\text{RESET}}$  and the RC time constant of the SDA bus.

PARAMETER MEASUREMENT INFORMATION

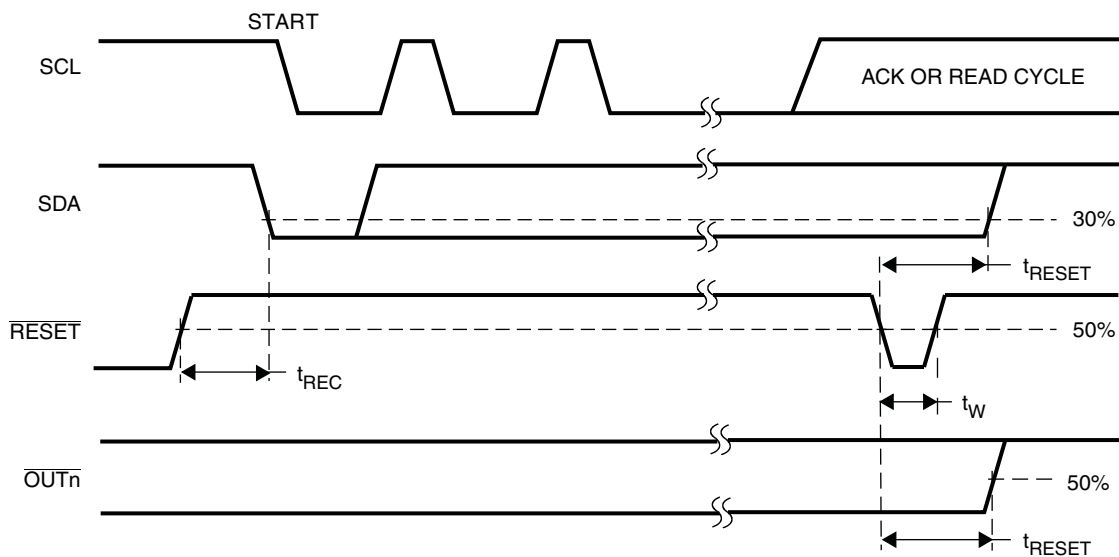


Figure 1. Definition of Reset Timing

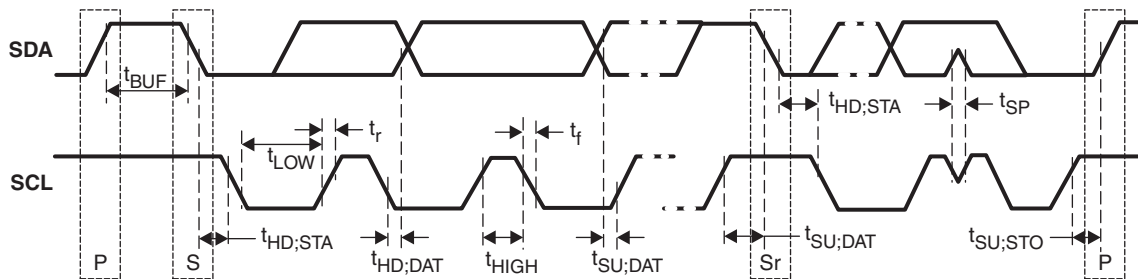
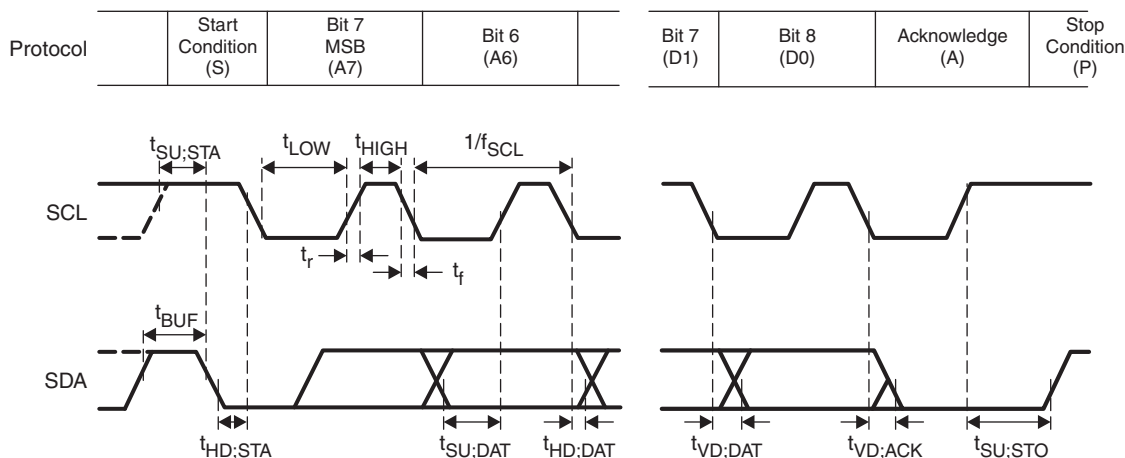


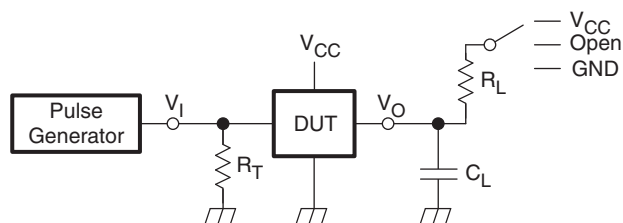
Figure 2. Definition of Timing



NOTE: Rise and fall times refer to  $V_{IL}$  and  $V_{IH}$ .

Figure 3. I<sup>2</sup>C Bus Timing

### PARAMETER MEASUREMENT INFORMATION (continued)



NOTE:  $R_L$  = Load resistance for SDA and SCL; should be  $>1\text{ k}\Omega$  at 3-mA or lower current.

$C_L$  = Load capacitance; includes jig and probe capacitance.

$R_T$  = Termination resistance; should be equal to the output impedance ( $Z_O$ ) of the pulse generator.

**Figure 4. Test Circuit for Switching Characteristics**

### APPLICATION INFORMATION

#### Typical Application Examples

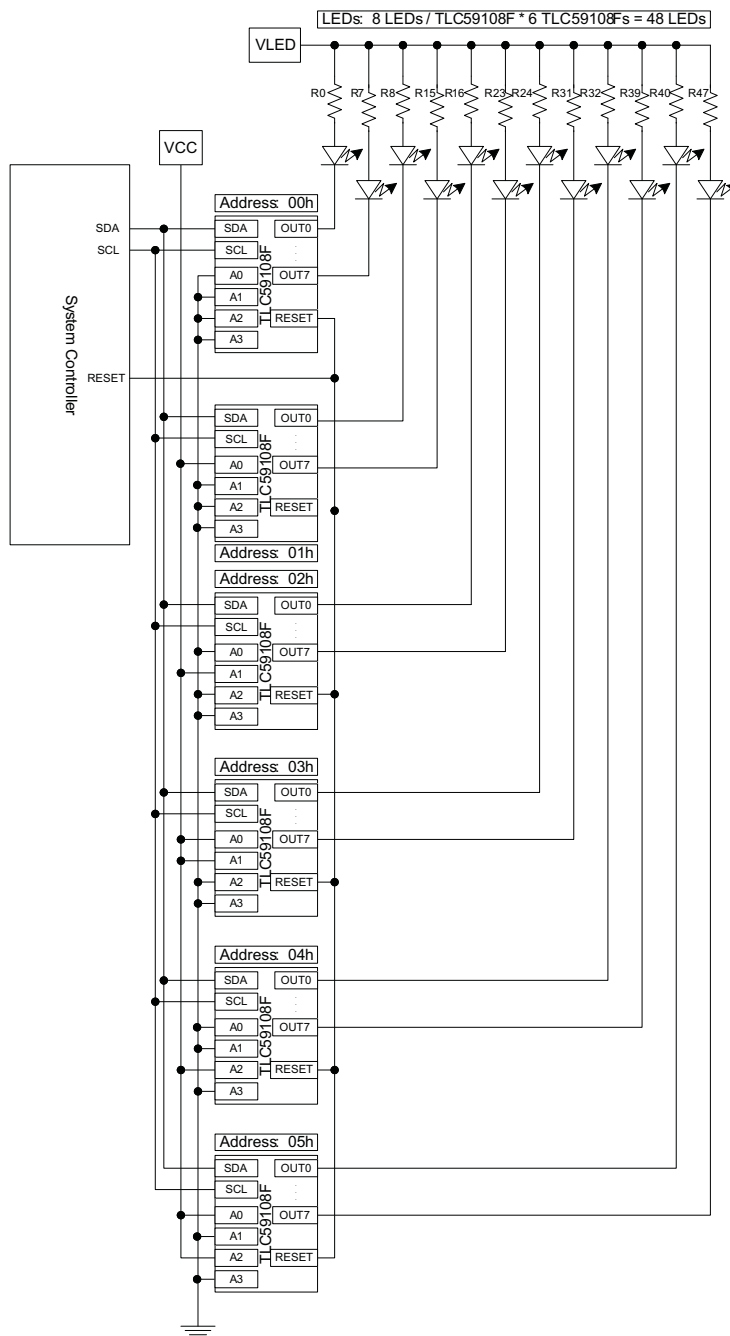


Figure 5. Six Drivers

This drawing is an example of using the TLC59108F in a system requiring up to 48 LED strings. The TLC59108F drivers share a single I2C bus. The address pins are set high or low to enable the drivers to be independently accessed (all can be written in parallel through the ALLCALLADR function). The resistors in series with the LEDs along with the VLED voltage will set the current for each string independently. Changing the resistor values allows for multi-color displays.

### TLC59108 and TLC59108F Differences

The TLC59108 and TLC59108F are similar devices with the difference being the output structure. The TLC59108 has 8 constant-current outputs while the TLC59108F has 8 open drain outputs. The REXT is used to program the current on the TLC59108 for all channels. The in-line resistors on the OUT pins are used in conjunction with the VLED to set the currents on each TLC59108F channel. Since the resistors are unique for each output, the currents can be set by output by changing the resistor value.

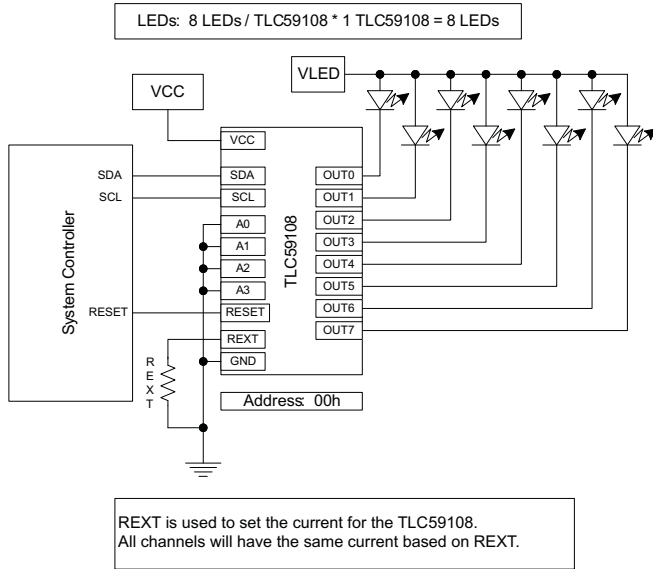


Figure 6. TLC59108 One Driver

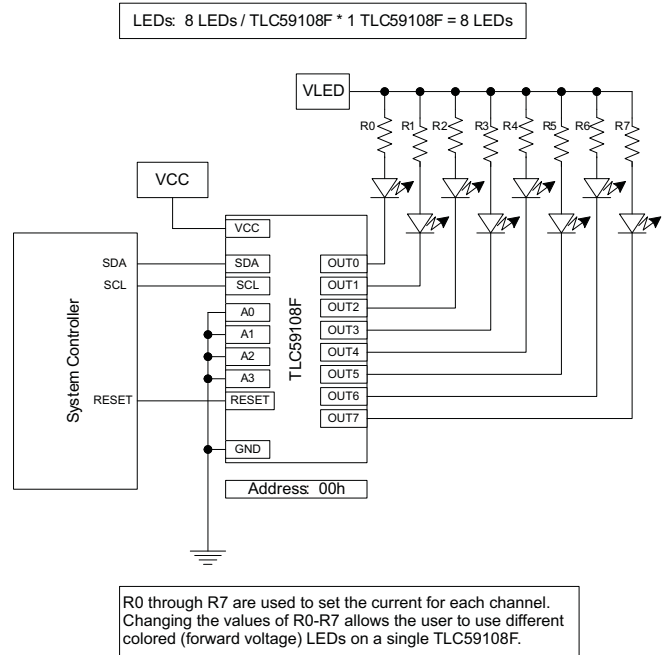


Figure 7. TLC59108F One Driver

## Functional Description

### Device Address

Following a Start condition, the bus master must output the address of the slave it is accessing.

### Regular I<sup>2</sup>C Bus Slave Address

The I<sup>2</sup>C bus slave address of the TLC59108F is shown in Figure 8. To conserve power, no internal pullup resistors are incorporated on the hardware-selectable address pins, and they must be pulled high or low. For buffer management purpose, a set of sector information data should be stored.

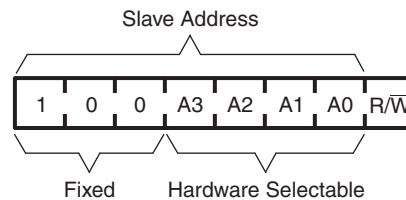


Figure 8. Slave Address

The last bit of the address byte defines the operation to be performed. When set to logic 1, a read operation is selected. When set to logic 0, a write operation is selected.

### LED All Call I<sup>2</sup>C Bus Address

- Default power-up value (ALLCALLADR address register): 90h or 1001 000
- Programmable through I<sup>2</sup>C bus (volatile programming)
- At power-up, LED All Call I<sup>2</sup>C bus address is enabled. TLC59108F sends an ACK when 90h ( $R/\overline{W} = 0$ ) or 91h ( $R/\overline{W} = 1$ ) is sent by the master.

#### NOTE

The LED All Call I<sup>2</sup>C bus address (90h or 1001 000) must not be used as a regular I<sup>2</sup>C bus slave address since this address is enabled at power-up. All the TLC59108Fs on the I<sup>2</sup>C bus will acknowledge the address if sent by the I<sup>2</sup>C bus master.

### LED Sub Call I<sup>2</sup>C Bus Address

- Three different I<sup>2</sup>C bus address can be used
- Default power-up values:
  - SUBADR1 register: 92h or 1001 001
  - SUBADR2 register: 94h or 1001 010
  - SUBADR3 register: 98h or 1001 100
- Programmable through I<sup>2</sup>C bus (volatile programming)
- At power-up, Sub Call I<sup>2</sup>C bus address is disabled. TLC59108F does not send an ACK when 92h ( $R/\overline{W} = 0$ ) or 93h ( $R/\overline{W} = 1$ ) or 94h ( $R/\overline{W} = 0$ ) or 95h ( $R/\overline{W} = 1$ ) or 98h ( $R/\overline{W} = 0$ ) or 99h ( $R/\overline{W} = 1$ ) is sent by the master.

#### NOTE

The default LED Sub Call I<sup>2</sup>C bus address may be used as a regular I<sup>2</sup>C bus slave address as long as they are disabled.

### Software Reset I<sup>2</sup>C Bus Address

The address shown in Figure 9 is used when a reset of the TLC59108F needs to be performed by the master. The software reset address (SWRST Call) must be used with  $R/\overline{W} = 0$ . If  $R/\overline{W} = 1$ , the TLC59108F does not acknowledge the SWRST. See Software Reset for more detail.



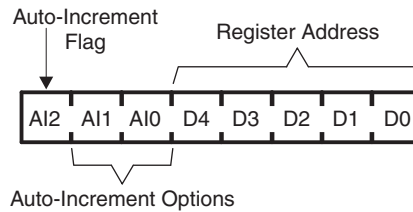
**Figure 9. Software Reset Address**

**NOTE**

The Software Reset I<sup>2</sup>C bus address is a reserved address and cannot be use as a regular I<sup>2</sup>C bus slave address.

**Control Register**

Following the successful acknowledgement of the slave address, LED All Call address or LED Sub Call address, the bus master will send a byte to the TLC59108F, which will be stored in the Control register. The lowest 5 bits are used as a pointer to determine which register will be accessed (D[4:0]). The highest 3 bits are used as Auto-Increment flag and Auto-Increment options (AI[2:0]).



**Figure 10. Control Register**

When the Auto-Increment flag is set (AI2 = logic 1), the five low order bits of the Control register are automatically incremented after a read or write. This allows the user to program the registers sequentially. Four different types of Auto-Increment are possible, depending on AI1 and AI0 values.

**Table 1. Auto-Increment Options<sup>(1)</sup>**

AI2	AI1	AI0	DESCRIPTION
0	0	0	No auto-increment
1	0	0	Auto-increment for all registers. D[4:0] roll over to '0 0000' after the last register ('1 0001') is accessed.
1	0	1	Auto-increment for individual brightness registers only. D[4:0] roll over to '0 0010' after the last register ('0 1001') is accessed.
1	1	0	Auto-increment for global control registers only. D[4:0] roll over to '0 1010' after the last register ('0 1011') is accessed.
1	1	1	Auto-increment for individual and global control registers only. D[4:0] roll over to '0 0010' after the last register ('0 1011') is accessed.

(1) Other combinations not shown in Table 1 (AI[2:0] = 001, 010, and 011) are reserved and must not be used for proper device operation.

AI[2:0] = 000 is used when the same register must be accessed several times during a single I<sup>2</sup>C bus communication, for example, changes the brightness of a single LED. Data is overwritten each time the register is accessed during a write operation.

AI[2:0] = 100 is used when all the registers must be sequentially accessed, for example, power-up programming.

AI[2:0] = 101 is used when the four LED drivers must be individually programmed with different values during the same I<sup>2</sup>C bus communication, for example, changing color setting to another color setting.

AI[2:0] = 110 is used when the LED drivers must be globally programmed with different settings during the same I<sup>2</sup>C bus communication, for example, global brightness or blinking change.

AI[2:0] = 111 is used when individually and global changes must be performed during the same I<sup>2</sup>C bus communication, for example, changing color and global brightness at the same time.

Only the 5 least significant bits D[4:0] are affected by the AI[2:0] bits.

When Control register is written, the register entry point determined by D[4:0] is the first register that will be addressed (read or write operation), and can be anywhere between 0 0000 and 1 0001 (as defined in [Table 2](#)). When AI[2] = 1, the Auto-Increment flag is set and the rollover value at which the point where the register increment stops and goes to the next one is determined by AI[2:0]. See [Table 1](#) for rollover values. For example, if the Control register = 1110 1100 (ECh), then the register addressing sequence will be (in hex):

04 → ... → 11 → 02 → ... → 11 → 02 → ... as long as the master keeps sending or reading data.

## Register Descriptions

[Table 2](#) describes the registers in the TLC59108F.

**Table 2. Register Descriptions**

REGISTER NUMBER (HEX)	NAME	ACCESS <sup>(1)</sup>	DESCRIPTION
00	MODE1	R/W	Mode register 1
01	MODE2	R/W	Mode register 2
02	PWM0	R/W	Brightness control LED0
03	PWM1	R/W	Brightness control LED1
04	PWM2	R/W	Brightness control LED2
05	PWM3	R/W	Brightness control LED3
06	PWM4	R/W	Brightness control LED4
07	PWM5	R/W	Brightness control LED5
08	PWM6	R/W	Brightness control LED6
09	PWM7	R/W	Brightness control LED7
0A	GRPPWM	R/W	Group duty cycle control
0B	GRPFREQ	R/W	Group frequency
0C	LEDOUT0	R/W	LED output state 0
0D	LEDOUT1	R/W	LED output state 1
0E	SUBADR1	R/W	I <sup>2</sup> C bus sub-address 1
0F	SUBADR2	R/W	I <sup>2</sup> C bus sub-address 2
10	SUBADR3	R/W	I <sup>2</sup> C bus sub-address 3
11	ALLCALLADR	R/W	LED all call I <sup>2</sup> C bus address

(1) R = read, W = write

## Mode Register 1 (MODE1)

Table 3 describes Mode Register 1.

**Table 3. MODE1 – Mode Register 1 (Address 00h) Bit Description**

BIT	SYMBOL	ACCESS <sup>(1)</sup>	VALUE	DESCRIPTION
7	AI2	R	0 <sup>(2)</sup>	Register auto-increment disabled
			1	Register auto-increment enabled
6	AI1	R	0 <sup>(2)</sup>	Auto-increment bit 1 = 0
			1	Auto-increment bit 1 = 1
5	AI0	R	0 <sup>(2)</sup>	Auto-increment bit 0 = 0
			1	Auto-increment bit 0 = 1
4	OSC	R/W	0	Normal mode <sup>(3)</sup>
			1 <sup>(2)</sup>	Oscillator off <sup>(4)</sup> .
3	SUB1	R/W	0 <sup>(2)</sup>	Device does not respond to I <sup>2</sup> C bus sub-address 1.
			1	Device responds to I <sup>2</sup> C bus sub-address 1.
2	SUB2	R/W	0 <sup>(2)</sup>	Device does not respond to I <sup>2</sup> C bus sub-address 2.
			1	Device responds to I <sup>2</sup> C bus sub-address 2.
1	SUB3	R/W	0 <sup>(2)</sup>	Device does not respond to I <sup>2</sup> C bus sub-address 3.
			1	Device responds to I <sup>2</sup> C bus sub-address 3.
0	ALLCALL	R/W	0	Device does not respond to LED All Call I <sup>2</sup> C bus address.
			1 <sup>(2)</sup>	Device responds to LED All Call I <sup>2</sup> C bus address.

(1) R = read, W = write

(2) Default value

(3) It takes 500  $\mu$ s max. for the oscillator to be up and running once SLEEP bit has been set from logic 1 to 0. Timings on LEDn outputs are not guaranteed if PWMx, GRPPWM, or GRPFREQ registers are accessed within the 500  $\mu$ s window.

(4) No LED control (on, off, blinking, or dimming) is possible when the oscillator is off. Write to a register cannot be accepted during SLEEP mode. When you change the LED condition, SLEEP bit must be set to logic 0.

## Mode Register 2 (MODE2)

Table 4 describes Mode Register 2.

**Table 4. MODE2 – Mode Register 2 (Address 01h) Bit Description**

BIT	SYMBOL	ACCESS <sup>(1)</sup>	VALUE	DESCRIPTION
7:6		R	0 <sup>(2)</sup>	Reserved
5	DMBLNK	R/W	0 <sup>(2)</sup>	Group control = dimming
			1	Group control = blinking
4		R	0 <sup>(2)</sup>	Reserved
3	OCH	R/W	0 <sup>(2)</sup>	Outputs change on Stop command <sup>(3)</sup> .
			1	Outputs change on ACK.
2:0		R	000 <sup>(2)</sup>	Reserved

(1) R = read, W = write

(2) Default value

(3) Change of the outputs at the STOP command allows synchronizing outputs of more than one TLC59108F. Applicable to registers from 02h (PWM0) to 0Dh (LEDOUT) only.

## Individual Brightness Control Registers (PWM0–PWM7)

Table 5 describes the Individual Brightness Control Registers.

**Table 5. PWM0–PWM7 – Individual Brightness Control Registers (Addresses 02h–09h) Bit Description**

ADDRESS	REGISTER	BIT	SYMBOL	ACCESS <sup>(1)</sup>	VALUE	DESCRIPTION
02h	PWM0	7:0	IDC0[7:0]	R/W	0000 0000 <sup>(2)</sup>	PWM0 individual duty cycle

(1) R = read, W = write

(2) Default value

**Table 5. PWM0–PWM7 – Individual Brightness Control Registers (Addresses 02h–09h) Bit Description (continued)**

ADDRESS	REGISTER	BIT	SYMBOL	ACCESS <sup>(1)</sup>	VALUE	DESCRIPTION
03h	PWM1	7:0	IDC1[7:0]	R/W	0000 0000 <sup>(2)</sup>	PWM1 individual duty cycle
04h	PWM2	7:0	IDC2[7:0]	R/W	0000 0000 <sup>(2)</sup>	PWM2 individual duty cycle
05h	PWM3	7:0	IDC3[7:0]	R/W	0000 0000 <sup>(2)</sup>	PWM3 individual duty cycle
06h	PWM4	7:0	IDC4[7:0]	R/W	0000 0000 <sup>(2)</sup>	PWM4 individual duty cycle
07h	PWM5	7:0	IDC5[7:0]	R/W	0000 0000 <sup>(2)</sup>	PWM5 individual duty cycle
08h	PWM6	7:0	IDC6[7:0]	R/W	0000 0000 <sup>(2)</sup>	PWM6 individual duty cycle
09h	PWM7	7:0	IDC7[7:0]	R/W	0000 0000 <sup>(2)</sup>	PWM7 individual duty cycle

A 97-kHz fixed-frequency signal is used for each output. Duty cycle is controlled through 256 linear steps from 00h (0% duty cycle = LED output off) to FFh (99.6% duty cycle = LED output at maximum brightness). Applicable to LED outputs programmed with LDRx = 10 or 11 (LEDOUT0 and LEDOUT1 registers).

$$\text{duty cycle} = \frac{\text{IDCx}[7:0]}{256}$$

### Group Duty Cycle Control Register (GRPPWM)

Table 6 describes the Group Duty Cycle Control Register .

**Table 6. GRPPWM – Group Duty Cycle Control Register (Address 0Ah) Bit Description**

ADDRESS	REGISTER	BIT	SYMBOL	ACCESS <sup>(1)</sup>	VALUE	DESCRIPTION
0Ah	GRPPWM	7:0	GDC0[7:0]	R/W	1111 1111 <sup>(2)</sup>	GRPPWM register

(1) R = read, W = write

(2) Default value

When DMBLNK bit (MODE2 register) is programmed with logic 0, a 190 Hz fixed frequency signal is superimposed with the 97 kHz individual brightness control signal. GRPPWM is then used as a global brightness control allowing the LED outputs to be dimmed with the same value. The value in GRPFREQ is then a 'Don't care'.

General brightness for the 8 outputs is controlled through 256 linear steps from 00h (0% duty cycle = LED output off) to FFh (99.6% duty cycle = maximum brightness). Applicable to LED outputs programmed with LDRx = 11 (LEDOUT0 and LEDOUT1 registers).

When DMBLNK bit is programmed with logic 1, GRPPWM and GRPFREQ registers define a global blinking pattern, where GRPPWM and GRPFREQ registers define a global blinking pattern, where GRPFREQ contains the blinking period (from 24 Hz to 10.73 s) and GRPPWM the duty cycle (ON/OFF ratio in %).

$$\text{duty cycle} = \frac{\text{GDC}[7:0]}{256}$$

### Group Frequency Register (GRPFREQ)

Table 7 describes the Group Frequency Register.

**Table 7. GRPFREQ – Group Frequency Register (Address 0Bh) Bit Description**

ADDRESS	REGISTER	BIT	SYMBOL	ACCESS <sup>(1)</sup>	VALUE	DESCRIPTION
0Bh	GRPFREQ	7:0	GFRQ[7:0]	R/W	0000 0000 <sup>(2)</sup>	GRPFREQ register

(1) R = read, W = write

(2) Default value

GRPFREQ is used to program the global blinking period when DMBLNK bit (MODE2 register) is equal to 1. Value in this register is a ‘Don’t care’ when DMBLNK = 0. Applicable to LED output programmed with LDRx = 11 (LEDOUT0 and LEDOUT1 registers).

Blinking period is controlled through 256 linear steps from 00h (41 ms, frequency 24 Hz) to FFh (10.73 s).

$$\text{globalblinkingperiod} = \frac{\text{GFRQ}[7:0] + 1}{24} (\text{s})$$

**LED Driver Output State Registers (LEDOUT0, LEDOUT1)**

Table 8 describes the LED Driver Output State Registers.

**Table 8. LEDOUT0 and LEDOUT1 – LED Driver Output State Registers (Address 0Ch and 0Dh) Bit Descriptions**

ADDRESS	REGISTER	BIT	SYMBOL	ACCESS <sup>(1)</sup>	VALUE	DESCRIPTION
0Ch	LEDOUT0	7:6	LDR3[1:0]	R/W	00 <sup>(2)</sup>	LED3 output state control
		5:4	LDR2[1:0]		00 <sup>(2)</sup>	LED2 output state control
		3:2	LDR1[1:0]		00 <sup>(2)</sup>	LED1 output state control
		1:0	LDR0[1:0]		00 <sup>(2)</sup>	LED0 output state control
0Dh	LEDOUT1	7:6	LDR7[1:0]	R/W	00 <sup>(2)</sup>	LED7 output state control
		5:4	LDR6[1:0]		00 <sup>(2)</sup>	LED6 output state control
		3:2	LDR4[1:0]		00 <sup>(2)</sup>	LED5 output state control
		1:0	LDR4[1:0]		00 <sup>(2)</sup>	LED4 output state control

- (1) R = read, W = write
- (2) Default value

LDRx = 00 : LED driver x is off (default power-up state).

LDRx = 01 : LED driver x is fully on (individual brightness and group dimming/blinking not controlled).

LDRx = 10 : LED driver x is individual brightness can be controlled through its PWMx register.

LDRx = 11 : LED driver x is individual brightness and group dimming/blinking can be controlled through its PWMx register and the GRPPWM registers.

**I<sup>2</sup>C Bus Sub-Address Registers 1 to 3 (SUBADR1–SUBADR3)**

Table 9 describes the Output Gain Control Register.

**Table 9. SUBADR1–SUBADR3 – I<sup>2</sup>C Bus Sub-Address Registers 1 to 3 (Addresses 0Eh–10h) Bit Descriptions**

ADDRESS	REGISTER	BIT	SYMBOL	ACCESS <sup>(1)</sup>	VALUE	DESCRIPTION
0Eh	SUBADR1	7:5	A1[7:5]	R	100 <sup>(2)</sup>	Reserved
		4:1	A1[4:1]	R/W	1001 <sup>(2)</sup>	I <sup>2</sup> C bus sub-address 1
		0	A1[0]	R	0 <sup>(2)</sup>	Reserved
0Fh	SUBADR2	7:5	A2[7:5]	R	100 <sup>(2)</sup>	Reserved
		4:1	A2[4:1]	R/W	1010 <sup>(2)</sup>	I <sup>2</sup> C bus sub-address 2
		0	A2[0]	R	0 <sup>(2)</sup>	Reserved
10h	SUBADR3	7:5	A3[7:5]	R	100 <sup>(2)</sup>	Reserved
		4:1	A3[4:1]	R/W	1100 <sup>(2)</sup>	I <sup>2</sup> C bus sub-address 3
		0	A3[0]	R	0 <sup>(2)</sup>	Reserved

- (1) R = read, W = write
- (2) Default value

Sub-addresses are programmable through the I<sup>2</sup>C bus. Default power-up values are 92h, 94h, 98h and the device(s) will not acknowledge these addresses right after power-up (the corresponding SUBx bit in MODE1 register is equal to 0).

Once sub-addresses have been programmed to their right values, SUBx bits need to be set to 1 in order to have the device acknowledging these addresses (MODE1 register).

Only the 7 MSBs representing the I<sup>2</sup>C bus sub-address are valid. The LSB in SUBADR<sub>x</sub> register is a read-only bit (0).

When SUBx is set to 1, the corresponding I<sup>2</sup>C bus sub-address can be used during either an I<sup>2</sup>C bus read or write sequence.

### LED All Call I<sup>2</sup>C Bus Address Register (ALLCALLADR)

Table 10 describes the LED All Call I<sup>2</sup>C Bus Address Register.

**Table 10. ALLCALLADR – LED All Call I<sup>2</sup>C Bus Address Register Addresses 11h) Bit Description**

ADDRESS	REGISTER	BIT	SYMBOL	ACCESS <sup>(1)</sup>	VALUE	DESCRIPTION
11h	ALLCALLADR	7:5	AC[7:5]	R	100 <sup>(2)</sup>	Reserved
		4:1	AC[4:1]	R/W	1000 <sup>(2)</sup>	ALLCALL I <sup>2</sup> C bus address
		0	AC[0]	R	0 <sup>(2)</sup>	Reserved

(1) R = read, W = write

(2) Default value

The LED All Call I<sup>2</sup>C-bus address allows all the TLC59108Fs in the bus to be programmed at the same time (ALLCALL bit in register MODE1 must be equal to 1 (power-up default state)). This address is programmable through the I<sup>2</sup>C-bus and can be used during either an I<sup>2</sup>C-bus read or write sequence. The register address can also be programmed as a Sub Call.

Only the 7 MSBs representing the All Call I<sup>2</sup>C-bus address are valid. The LSB in ALLCALLADR register is a read-only bit (0).

If ALLCALL bit = 0 (MODE1 register), the device does not acknowledge the address programmed in register ALLCALLADR.

### Power-On Reset

When power is applied to V<sub>CC</sub>, an internal power-on reset holds the TLC59108F in a reset condition until V<sub>CC</sub> has reached V<sub>POR</sub>. At this point, the reset condition is released and the TLC59108F registers and I<sup>2</sup>C bus state machine are initialized to their default states causing all the channels to be deselected. Thereafter, V<sub>CC</sub> must be lowered below 0.2 V to reset the device.

### External Reset

A reset can be accomplished by holding the  $\overline{\text{RESET}}$  pin low for a minimum of t<sub>w</sub>. The TLC59108F registers and I<sup>2</sup>C state machine will be held in their default state until the  $\overline{\text{RESET}}$  input is once again high.

This input requires a pull-up resistor to V<sub>CC</sub> if no active connection is used.

### Software Reset

The Software Reset Call (SWRST Call) allows all the devices in the I<sup>2</sup>C bus to be reset to the power-up state value through a specific I<sup>2</sup>C bus command. To be performed correctly, the I<sup>2</sup>C bus must be functional and there must be no device hanging the bus.

The SWRST Call function is defined as the following:

1. A Start command is sent by the I<sup>2</sup>C bus master.
2. The reserved SWRST I<sup>2</sup>C bus address 1001 011 with the R $\overline{\text{W}}$  bit set to 0 (write) is sent by the I<sup>2</sup>C bus master.
3. The TLC59108F device(s) acknowledge(s) after seeing the SWRST Call address 1001 0110 (96h) only. If the R $\overline{\text{W}}$  bit is set to 1 (read), no acknowledge is returned to the I<sup>2</sup>C bus master.

4. Once the SWRST Call address has been sent and acknowledged, the master sends two bytes with two specific values (SWRST data byte 1 and byte 2):
  - (a) Byte1 = A5h: the TLC59108F acknowledges this value only. If byte 1 is not equal to A5h, the TLC59108F does not acknowledge it.
  - (b) Byte 2 = 5Ah: the TLC59108F acknowledges this value only. If byte 2 is not equal to 5Ah, the TLC59108F does not acknowledge it.

If more than two bytes of data are sent, the TLC59108F does not acknowledge any more.

5. Once the correct two bytes (SWRST data byte 1 and byte 2 only) have been sent and correctly acknowledged, the master sends a Stop command to end the SWRST Call. The TLC59108F then resets to the default value (power-up value) and is ready to be addressed again within the specified bus free time ( $t_{BUF}$ ).

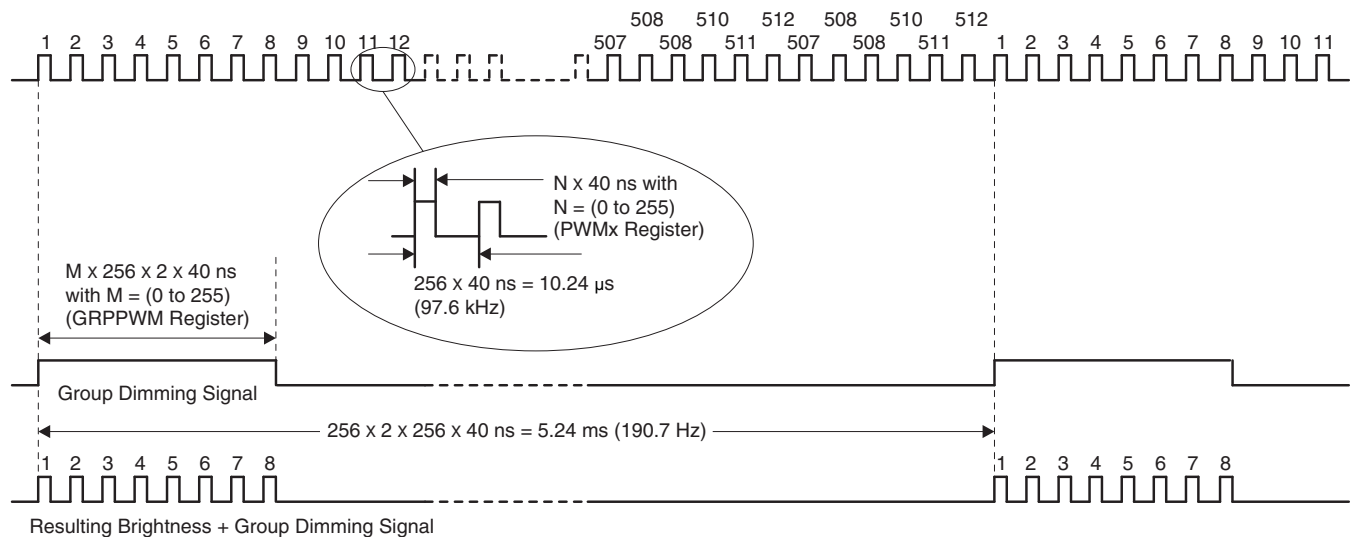
The I<sup>2</sup>C bus master may interpret a non-acknowledge from the TLC59108F (at any time) as a SWRST Call Abort. The TLC59108F does not initiate a reset of its registers. This happens only when the format of the Start Call sequence is not correct.

### Individual Brightness Control With Group Dimming/Blinking

A 97 kHz fixed frequency signal with programmable duty cycle (8 bits, 256 steps) is used to control individually the brightness for each LED.

On top of this signal, one of the following signals can be superimposed (this signal can be applied to the 4 LED outputs):

- A lower 190 Hz fixed frequency signal with programmable duty cycle (8 bits, 256 steps) is used to provide a global brightness control.
- A programmable frequency signal from 24 Hz to 1/10.73 s (8 bits, 256 steps) is used to provide a global blinking control.



- A. Minimum pulse width for LEDn brightness control is 40 ns.
- B. Minimum pulse width for group dimming is 20.48  $\mu\text{s}$ .
- C. When  $M = 1$  (GRPPWM register value), the resulting LEDn brightness control and group dimming signal will have two pulses of the LED brightness control signal (pulse width =  $N \times 40 \text{ ns}$ , with  $N$  defined in the PWMx register).
- D. The resulting brightness plus group dimming signal shown above demonstrate a resulting control signal with  $M = 4$  (8 pulses).

**Figure 11. Brightness + Group Dimming Signals**

## Characteristics of the I<sup>2</sup>C Bus

The I<sup>2</sup>C bus is for two-way two-line communication between different devices or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pullup resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

### Bit Transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high period of the clock pulse as changes in the data line at this time will be interpreted as control signals (see Figure 12).

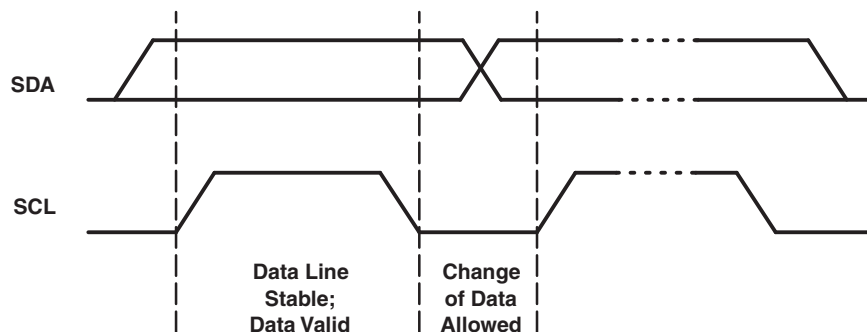


Figure 12. Bit Transfer

### Start and Stop Conditions

Both data and clock lines remain high when the bus is not busy. A high-to-low transition of the data line while the clock is high is defined as the Start condition (S). A low-to-high transition of the data line while the clock is high is defined as the Stop condition (P) (see Figure 13).

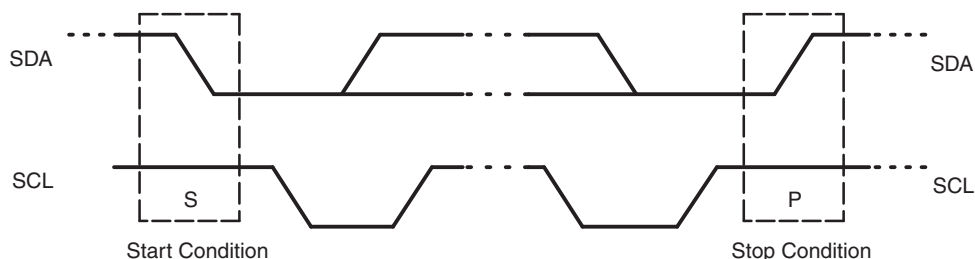


Figure 13. Start and Stop Conditions

### System Configuration

A device generating a message is a transmitter; a device receiving is the receiver. The device that controls the message is the master and the devices which are controlled by the master are the slaves (see Figure 14).

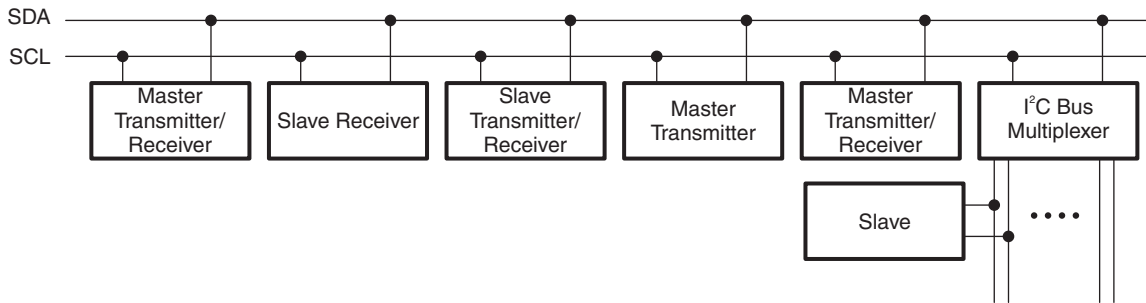


Figure 14. System Configuration

### Acknowledge

The number of data bytes transferred between the Start and the Stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a high level put on the bus by the transmitter, whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge related clock pulse, so that the SDA line is stable low during the high period of the acknowledge related clock pulse; set-up time and hold time must be taken into account.

A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line high to enable the master to generate a Stop condition.

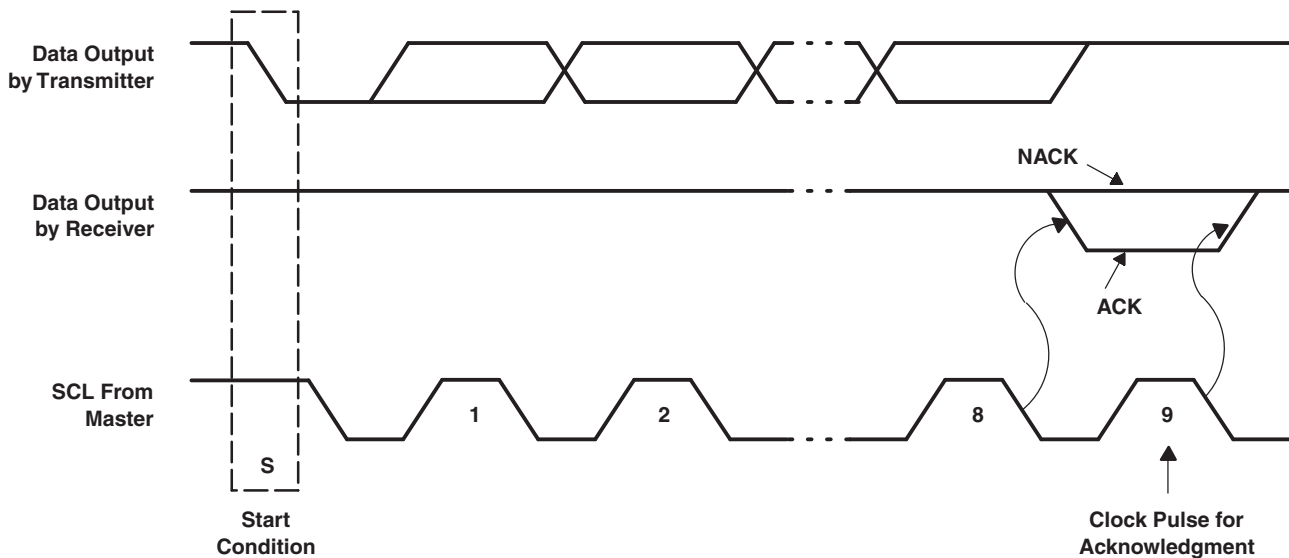


Figure 15. Acknowledge on I²C Bus

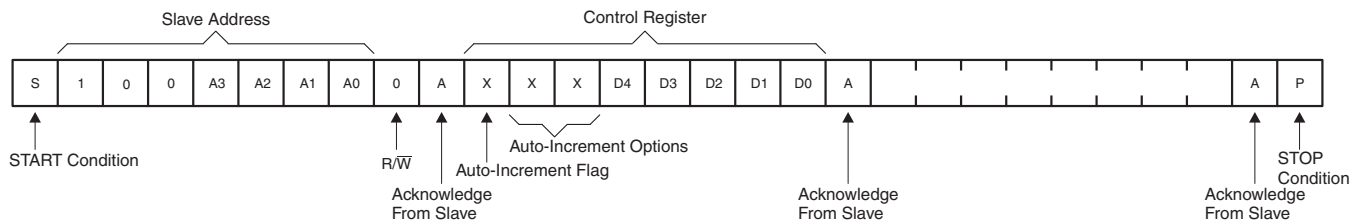


Figure 16. Write to a Specific Register

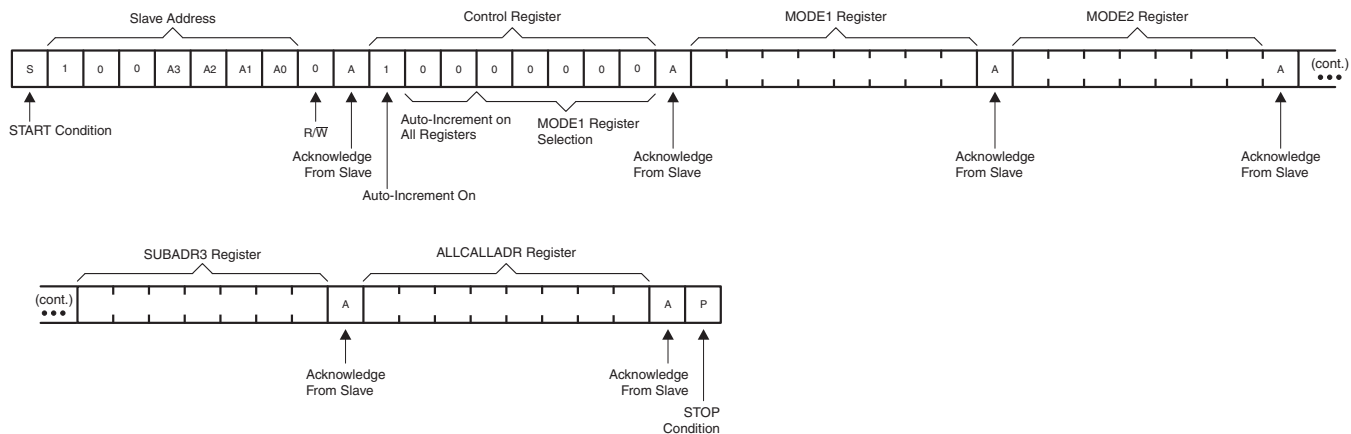


Figure 17. Write to All Registers Using Auto-Increment

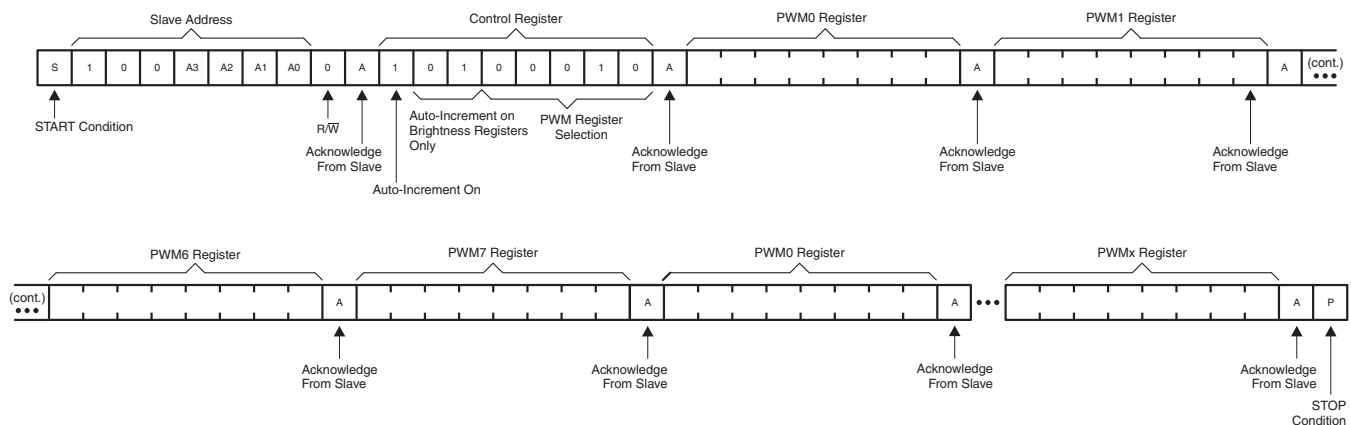


Figure 18. Multiple Writes to Individual Brightness Registers Only Using the Auto-Increment Feature



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**Changes from Original (November 2011) to Revision A****Page**

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• Added Typical Application Examples section. ....	9
• Added TLC59108 and TLC59108F Differences section. ....	10
• Changed SLEEP Symbol to OSC and removed the "Low power mode" description to clarify functionality. ....	14
• Fixed address typo in the Software Reset Section .....	17

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**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TLC59108FIPWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	Y59108F	Samples
TLC59108FIRGYR	PREVIEW	VQFN	RGY	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FL108F	

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC59108FIPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TLC59108FIRGYR	VQFN	RGY	20	3000	330.0	12.4	3.8	4.8	1.6	8.0	12.0	Q1

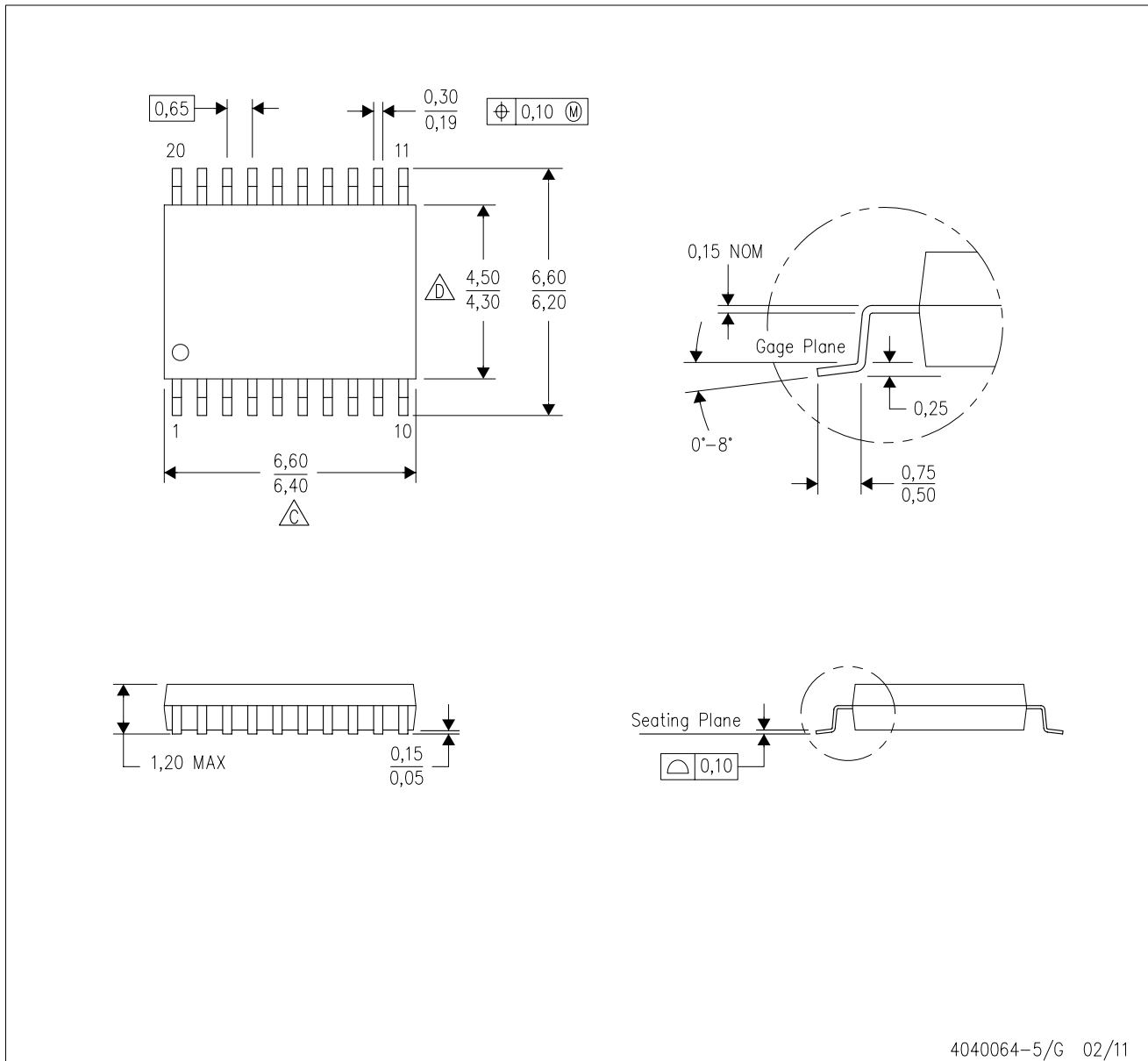
**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC59108FIPWR	TSSOP	PW	20	2000	367.0	367.0	38.0
TLC59108FIRGYR	VQFN	RGY	20	3000	367.0	367.0	35.0

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



4040064-5/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G20)

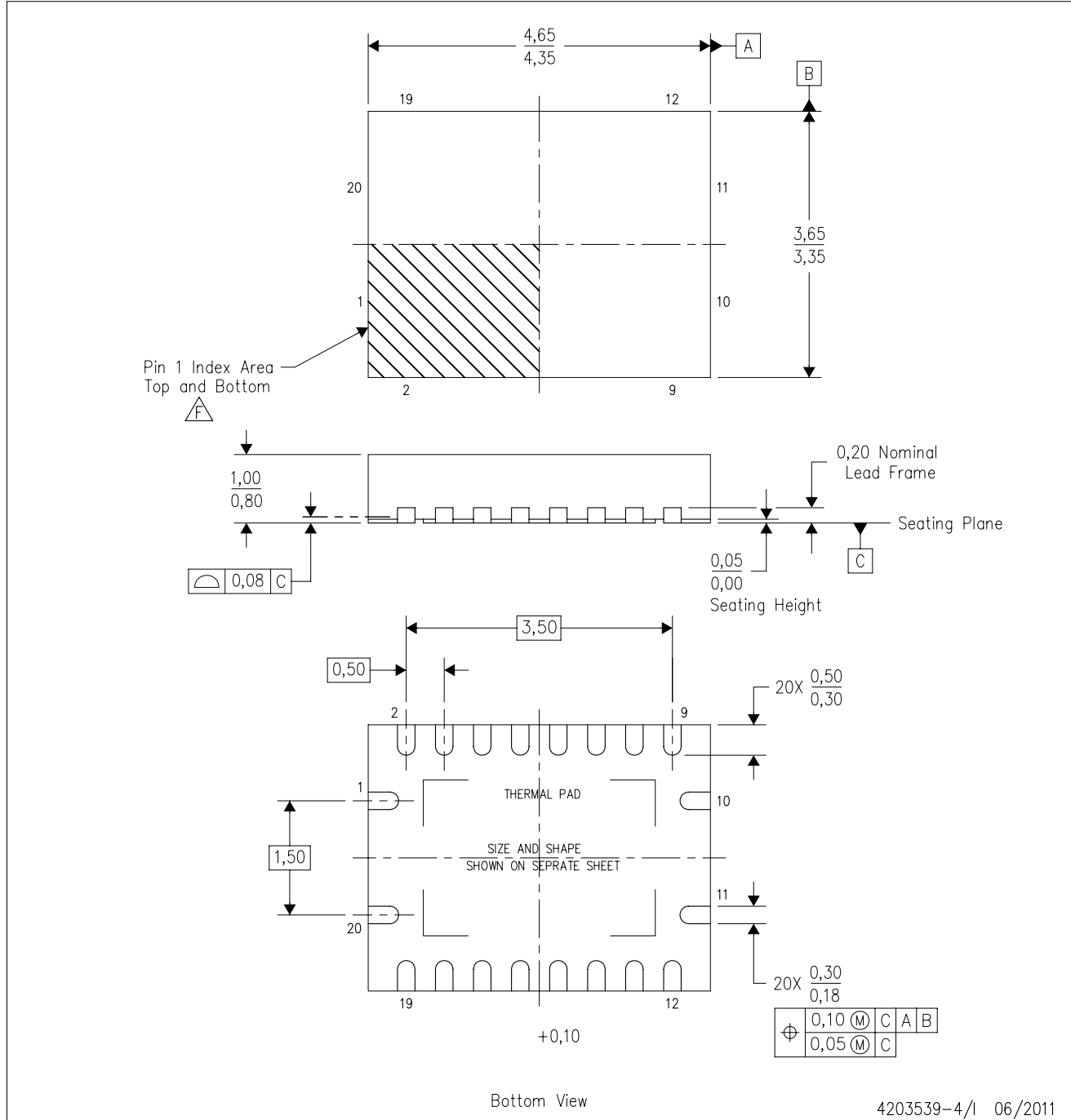
PLASTIC SMALL OUTLINE




- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

RGY (R-PVQFN-N20)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. QFN (Quad Flatpack No-Lead) package configuration.
  - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  -  Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
  - G. Package complies to JEDEC MO-241 variation BA.

RGY (R-PVQFN-N20)

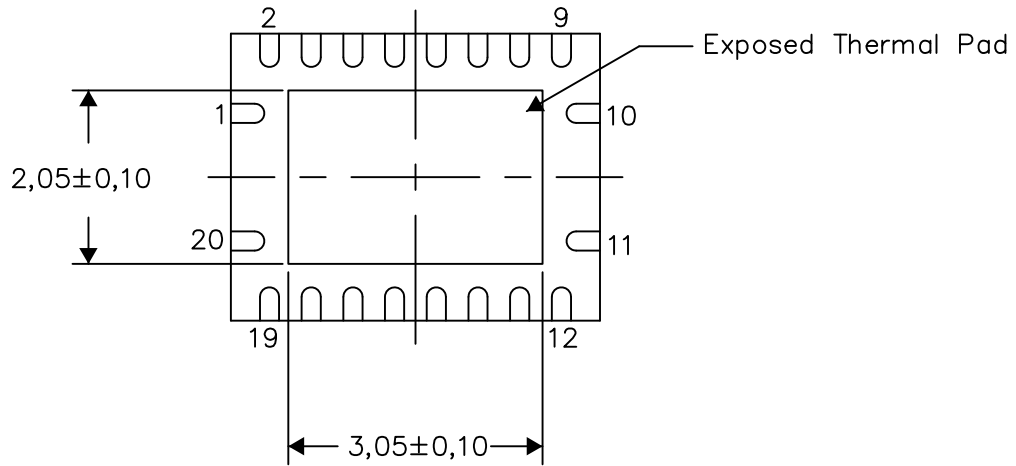
PLASTIC QUAD FLATPACK NO-LEAD

**THERMAL INFORMATION**

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

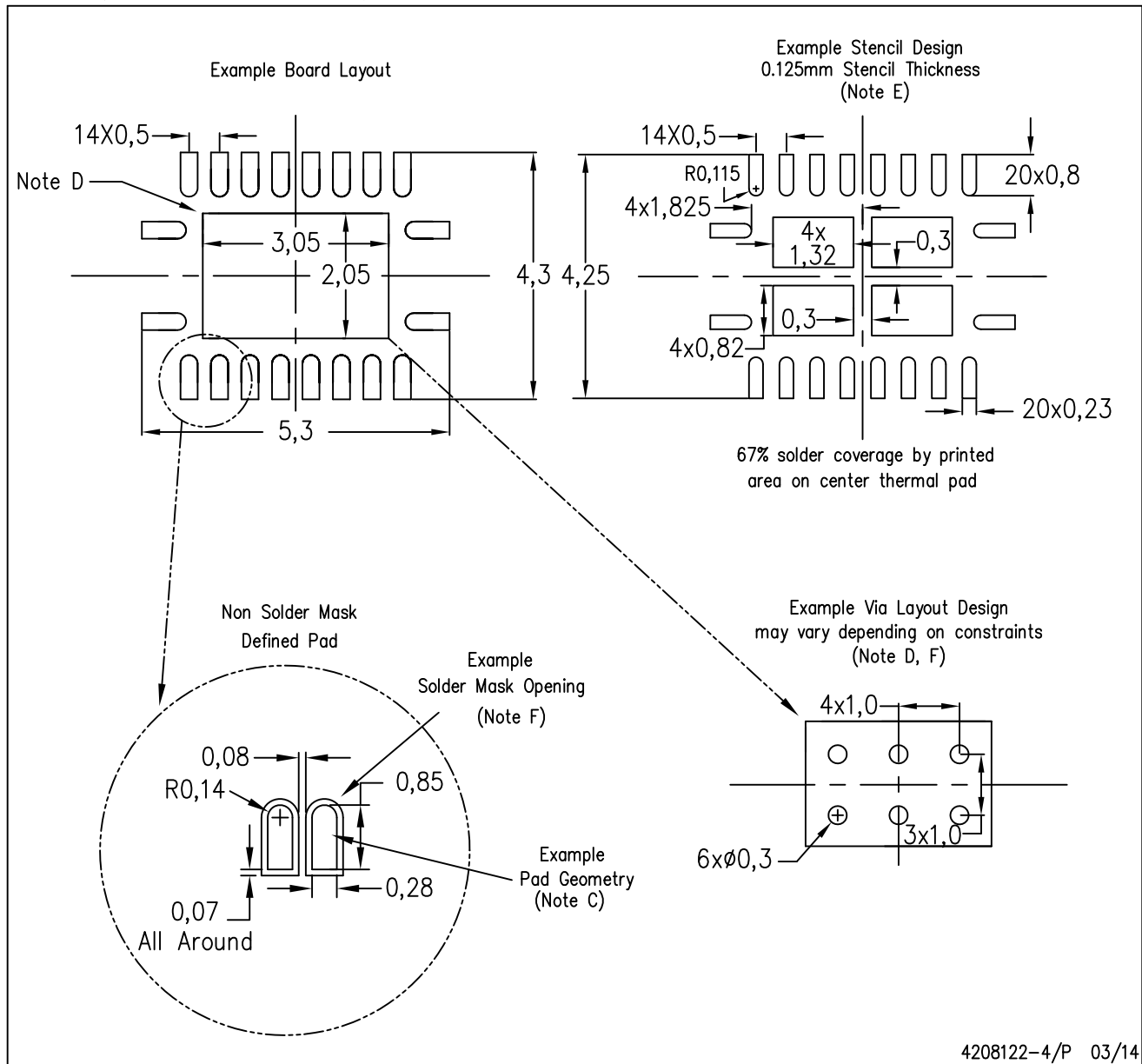
Exposed Thermal Pad Dimensions

4206353-4/P 03/14

NOTE: All linear dimensions are in millimeters

RGY (R-PVQFN-N20)

PLASTIC QUAD FLATPACK NO-LEAD



4208122-4/P 03/14

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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