16-Channel, 12-Bit PWM LED Driver with 7-Bit Dot Correction

FEATURES

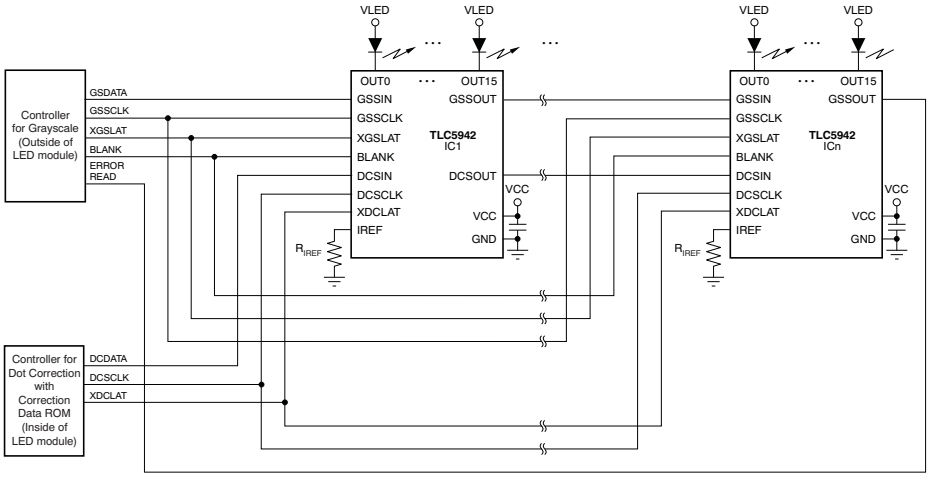
- 16 Channels, Constant Current Sink Output
- 50-mA Capability (Constant Current Sink)
- 12-Bit (4096 Steps) Grayscale Control with PWM
- 7-Bit (128 Steps) Dot Correction with Sink Current
- LED Power-Supply Voltage up to 17 V
- Constant Current Accuracy:
  - Channel-to-Channel = ±1.5%
  - Device-to-Device = ±3%
- VCC = 3.0 V to 5.5 V
- CMOS Level I/O
- 30-MHz Data Transfer Rate
- 30-MHz Grayscale Control Clock
- Dedicated Ports for Grayscale and Dot Correction
- Continuous Base LED Open Detection (LOD)
- Thermal Shutdown (TSD):
  - Automatic shutdown at high temperature conditions
  - Restart under normal temperature
- Readable Error Information:
  - LED Open Detection
  - Thermal Error Flag (TEF)
- Noise Reduction:
  - 4-Channel grouped delay to prevent inrush current
- Operating Temperature: –40°C to +85°C

APPLICATIONS

- Monochrome, Multicolor, Full-Color LED Displays
- LED Signboards
- Display Backlighting

DESCRIPTION

The TLC5942 is a 16-channel, constant current sink driver. Each channel is individually adjustable with 4096 pulse-width modulated (PWM) steps and 128 constant current sink steps for dot correction. Dot correction adjusts the brightness variations between LEDs. Both grayscale control and dot correction are accessible via separate, dedicated serial interface ports. The maximum current value of all 16 channels can be set by a single external resistor.



Typical Application Circuit (Multiple Daisy-Chained TLC5942s)

DESCRIPTION, CONTINUED

The TLC5942 has two error detection circuits for LED open detection (LOD) and a thermal error flag (TEF). LOD detects a broken or disconnected LED during the display period. TEF indicates an over-temperature condition; when a TEF is set, all output drivers are turned off. When the TEF is cleared, all output drivers are restarted.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
TLC5942	HTSSOP-28 PowerPAD™	TLC5942PWPR	Tape and Reel, 2000
		TLC5942PWP	Tube, 50
TLC5942	5 mm × 5 mm QFN-32	TLC5942RHBR	Tape and Reel, 3000
		TLC5942RHBT	Tape and Reel, 250

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)(2)

Over operating free-air temperature range, unless otherwise noted.

PARAMETER			TLC5942	UNIT
VCC	Supply voltage, VCC		–0.3 to +6.0	V
I_{OUT}	Output current (dc): OUT0 to OUT15		60	mA
V_{IN}	Input voltage range: GSSIN, GSSCLK, XGSLAT, DCSIN, DCSCLK, XDCLAT, BLANK, IREF		–0.3 to VCC + 0.3	V
V_{OUT}	Output voltage range	GSSOUT, DCSOUT	–0.3 to VCC + 0.3	V
		OUT0 to OUT15	–0.3 to +18	
$T_{J(max)}$	Maximum operating junction temperature		+150	°C
T_{STG}	Storage temperature range		–55 to +150	
	ESD rating	Human body model (HBM)	2	kV
		Charged device model (CDM)	500	V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.
(2) All voltage values are with respect to network ground terminal.

RECOMMENDED OPERATING CONDITIONS

At T_A= –40°C to +85°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	TLC5942			UNIT
			MIN	NOM	MAX	
DC Characteristics: VCC = 3 V to 5.5 V						
VCC	Supply voltage		3.0		5.5	V
V_O	Voltage applied to output	OUT0 to OUT15			17	V
V_{IH}	High-level input voltage		0.7 × VCC		VCC	V
V_{IL}	Low-level input voltage		GND		0.3 × VCC	V
I_{OH}	High-level output current	GSSOUT, DCSOUT			–1	mA
I_{OL}	Low-level output current	GSSOUT, DCSOUT			1	mA
I_{OLC}	Constant output sink current	OUT0 to OUT15			50	mA
T_A	Operating free-air temperature		–40		+85	°C
T_J	Operating junction temperature		–40		+125	°C
AC Characteristics: VCC = 3 V to 5.5 V						
$f_{CLK\ (dcsclk)}$	Data shift clock frequency	DCSCLK			30	MHz
$f_{CLK\ (gssclk)}$	Data shift/grayscale control clock frequency	GSSCLK			30	MHz
T_{WH0} / T_{WL0}	Pulse duration	GSSCLK (see Figure 9), DCSCLK (see Figure 10)	10			ns
T_{WH1}		XGSLAT, BLANK (see Figure 9), XDCLAT (see Figure 10)	30			ns
T_{SU0}	Setup time	GSSIN–GSSCLK ↑ (see Figure 9), DCSIN–DCSCLK ↑ (see Figure 10)	3			ns
T_{SU1}		BLANK ↓– GSSCLK ↑ (see Figure 9)	10			ns
T_{SU2}		XGSLAT ↑ – GSSCLK↑ (see Figure 9), XDCLAT ↑ – DCSCLK↑ (see Figure 10)	100			ns
T_{SU3}		XGSLAT ↓ – GSSCLK↑ (see Figure 9 and Figure 11)	15			ns
T_{H0}	Hold time	GSSIN–GSSCLK ↑ (see Figure 9), DCSIN–DCSCLK ↑ (see Figure 10)	3			ns
T_{H1}		XGSLAT ↑ – GSSCLK↑ (see Figure 9), XDCLAT ↑ – DCSCLK↑ (see Figure 10)	30			ns

DISSIPATION RATINGS

PACKAGE	DERATING FACTOR ABOVE T_A = +25°C	T_A < +25°C POWER RATING	T_A = +70°C POWER RATING	T_A = +85°C POWER RATING
HTSSOP-28 with PowerPAD soldered(1)	31.67 mW/°C	3958 mW	2533 mW	2058 mW
HTSSOP-28 with PowerPAD not soldered(2)	16.21 mW/°C	2026 mW	1296 mW	1053 mW
QFN-32(3)	27.86 mW/°C	3482 mW	2228 mW	1811 mW

(1) With PowerPAD soldered onto copper area on printed circuit board (PCB); 2 oz. copper. For more information, see SLMA002 (available for download at www.ti.com).
(2) With PowerPAD not soldered onto copper area on PCB.
(3) The package thermal impedance is calculated in accordance with JESD51-5.

ELECTRICAL CHARACTERISTICS

At VCC = 3.0 V to 5.5 V, and T_A = –40°C to +85°C. Typical values at VCC = 3.3 V and T_A = +25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	TLC5942			UNIT
			MIN	TYP	MAX	
V_{OH}	High-level output voltage	I_{OH} = –1 mA at GSSOUT, DCSOUT	VCC – 0.4		VCC	V
V_{OL}	Low-level output voltage	I_{OL} = 1 mA at GSSOUT, DCSOUT	0		0.4	V
I_{IN}	Input current	V_{IN} = VCC or GND at GSSIN, GSSCLK, XGSLAT, DCSIN, DCSCLK, XDCLAT, BLANK	–1		1	µA
I_{CC1}	Supply current	No data transfer, all OUTn = OFF, DCn = 7Fh, V_{OUTn} = 1 V, R_{IREF} = 10 kΩ		1	3	mA
I_{CC2}		No data transfer, all OUTn = OFF, DCn = 7Fh, V_{OUTn} = 1 V, R_{IREF} = 2 kΩ		4	8	
I_{CC3}		Data transfer 30 MHz, all OUTn = ON, DCn = 7Fh, V_{OUTn} = 1 V, R_{IREF} = 2 kΩ		14	30	
I_{CC4}		Data transfer 30 MHz, all OUTn = ON, DCn = 7Fh, V_{OUTn} = 1 V, R_{IREF} = 1 kΩ		27	50	
$I_{O(LC)}$	Constant output current	All OUTn = ON, DCn = 7Fh, V_{OUTn} = 1 V, V_{OUTfix} = 1 V, R_{IREF} = 1 kΩ	43	49	55	mA
$I_{O(LKG)}$	Leakage output current	All OUTn = OFF, DCn = 7Fh, V_{OUTn} = 17 V, R_{IREF} = 1 kΩ			0.1	µA
$\Delta I_{O(LC)}$	Constant current error (channel-to-channel)(1)	All OUTn = ON, DCn = 7Fh, V_{OUTn} = 1 V, V_{OUTfix} = 1 V, R_{IREF} = 1 kΩ		±1.5	±5	%
$\Delta I_{O(LC1)}$	Constant current error (device-to-device)(2)	All OUTn = ON, DCn = 7Fh, V_{OUTn} = 1 V, V_{OUTfix} = 1 V, R_{IREF} = 1 kΩ		±3	±8	%
$\Delta I_{O(LC2)}$	Line regulation(3)	All OUTn = ON, DCn = 7Fh, V_{OUTn} = 1 V, V_{OUTfix} = 1 V, R_{IREF} = 1 kΩ, VCC = 3 V to 5.5 V		±1	±4	%/V
$\Delta I_{O(LC3)}$	Load regulation(4)	All OUTn = ON, DCn = 7Fh, V_{OUTn} = 1 V to 3 V, V_{OUTfix} = 1 V, R_{IREF} = 1 kΩ		±1	±3	%/V
$T_{(TEF)}$	Thermal error flag threshold	Junction temperature(5)	+150	+162	+175	°C
$T_{(HYS)}$	Thermal error hysteresis	Junction temperature(5)	+5	+10	+20	°C
V_{LOD}	LED open detection threshold	All OUTn = ON	0.2	0.3	0.4	V
V_{IREF}	Reference voltage output	R_{IREF} = 1 kΩ	1.16	1.20	1.24	V

(1) The deviation of each output from the average of OUT0–OUT15 constant current. Deviation is calculated by the formula:

$$\Delta\,(\%) = \left(\frac{I_{OUTn}}{\frac{(I_{OUT0} + I_{OUT1} + \ldots + I_{OUT15})}{16}} - 1 \right) \times 100$$

(2) The deviation of the OUT0–OUT15 constant current average from the ideal constant current value.

$$\Delta\,(\%) = \left(\frac{\frac{(I_{OUT0} + I_{OUT1} + \ldots I_{OUT14} + I_{OUT15})}{16} - (\text{Ideal Output Current})}{\text{Ideal Output Current}} \right) \times 100$$

Deviation is calculated by the following formula:

$$I_{OUT(IDEAL)} = 41 \times \left(\frac{1.20}{R_{IREF}} \right)$$

Ideal current is calculated by the formula:

(3) Line regulation is calculated by this equation:

$$\Delta\,(\%/V) = \left(\frac{(I_{OUTn} \text{ at } V_{CC} = 5.5 \text{ V}) - (I_{OUTn} \text{ at } V_{CC} = 3.0 \text{ V})}{(I_{OUTn} \text{ at } V_{CC} = 3.0 \text{ V})} \right) \times \frac{100}{5.5 \text{ V} - 3 \text{ V}}$$

(4) Load regulation is calculated by the equation:

$$\Delta\,(\%/V) = \left(\frac{(I_{OUTn} \text{ at } V_{OUTn} = 3 \text{ V}) - (I_{OUTn} \text{ at } V_{OUTn} = 1 \text{ V})}{(I_{OUTn} \text{ at } V_{OUTn} = 1 \text{ V})} \right) \times \frac{100}{3 \text{ V} - 1 \text{ V}}$$

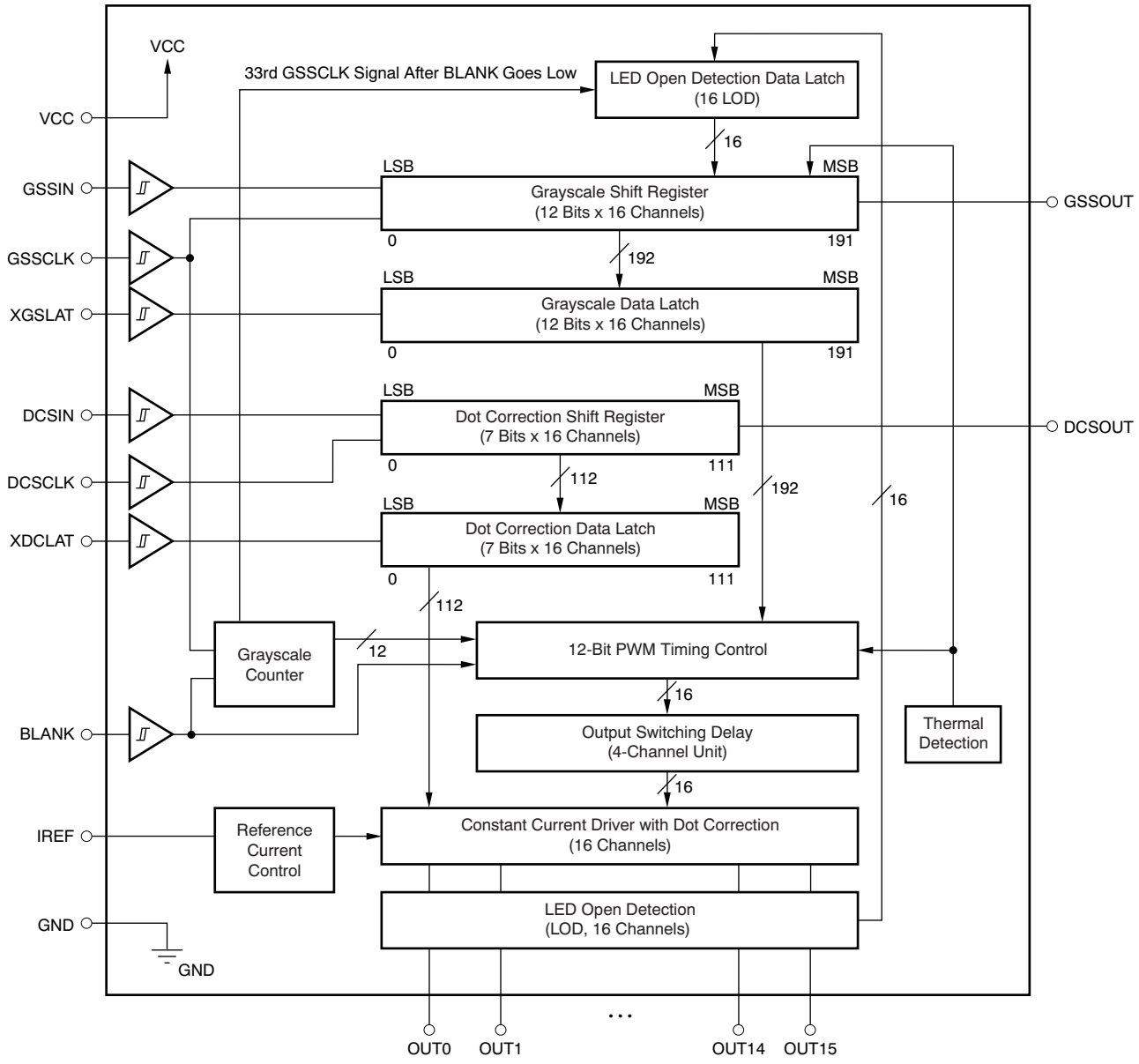
(5) Not tested; specified by design.

SWITCHING CHARACTERISTICS

At VCC = 3.0 V to 5.5 V, T_A = –40°C to +85°C, C_L = 15 pF, R_L = 82 Ω, R_{IREF} = 1 kΩ, and V_{LED} = 5.0 V. Typical values at VCC = 3.3 V and T_A = +25°C, unless otherwise noted.

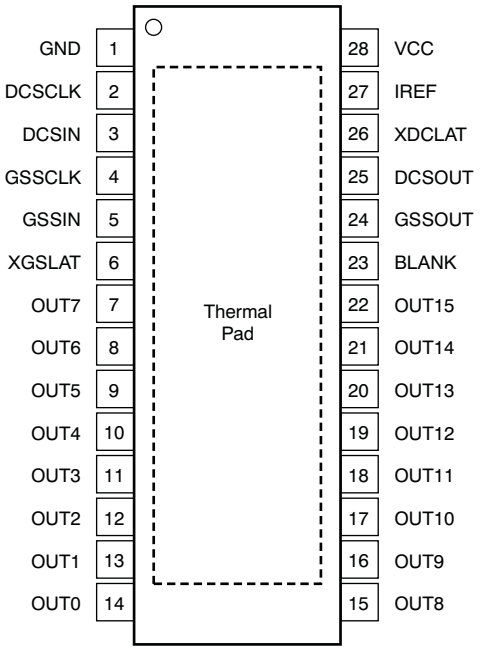
PARAMETER		TEST CONDITIONS	TLC5942			UNIT
			MIN	TYP	MAX	
t_{R0}	Rise time	GSSOUT (see Figure 9) DCSOUT (see Figure 10)			16	ns
t_{R1}		OUTn, DCn = 7Fh (see Figure 9)		10	30	
t_{F0}	Fall time	GSSOUT (see Figure 9) DCSOUTn (see Figure 10)			16	ns
t_{F1}		OUTn, DCn = 7Fh (see Figure 9)		10	30	
t_{D0}	Propagation delay time	GSSCLK ↑ – GSSOUT (see Figure 9) DCSCLK ↑ – DCSOUT (see Figure 10)			25	ns
t_{D1}		BLANK ↑ – OUT0 current sink off (see Figure 9)		20	40	ns
t_{D2}		GSSCLK ↑ – OUT0, 4, 8, 12 (see Figure 9)	5	18	40	ns
t_{D3}		GSSCLK ↑ – OUT1, 5, 9, 13 (see Figure 9)	20	42	73	ns
t_{D4}		GSSCLK ↑ – OUT2, 6, 10, 14 (see Figure 9)	35	66	106	ns
t_{D5}		GSSCLK ↑ – OUT3, 7, 11, 15 (see Figure 9)	50	90	140	ns
t_{ON_ERR}	Output on-time error	t_{OUTON} – T_{GSSCLK}, GSn = 001h, GSSCLK = 30 MHz (see Figure 9)	–20		10	ns

FUNCTIONAL BLOCK DIAGRAM

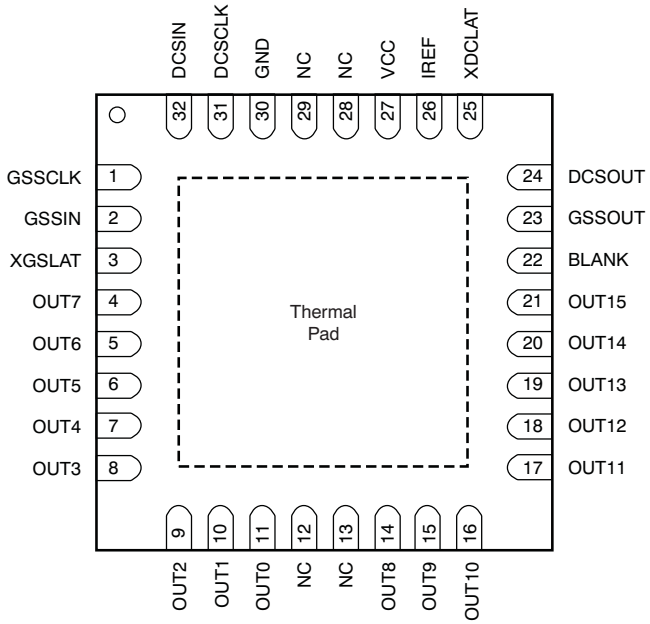


DEVICE INFORMATION

PWP PACKAGE
(Top View)



RHB PACKAGE
(Top View)



NC = No connection.

TERMINAL FUNCTIONS

TERMINAL			I/O	DESCRIPTION
NAME	PWP	RHB		
GSSIN	5	2	I	Serial data input for grayscale.
GSSCLK	4	1	I	Serial data shift clock for grayscale and reference clock for Grayscale PWM control. Data present on the GSSIN pin are shifted into the Grayscale Shift Register with each rising edge of the GSSCLK pin. Data are shifted into the LSB of the register with each rising edge. The MSB of the register is shifted to the GSSOUT pin with each rising edge. If BLANK is low, then each rising edge of GSSCLK increments the grayscale counter for PWM control.
XGSLAT	6	3	I	Data in the shift register are moved to the grayscale data latch with a low-to-high transition of this pin.
GSSOUT	24	23	O	Serial data output for Grayscale/Status information data. This signal is connected to MSB of Grayscale Shift Register.
DCSIN	3	32	I	Serial data input for Dot Correction.
DCSCLK	2	31	I	Serial data shift clock for dot correction. Data present on the DCSIN pin are shifted into the dot correction shift register with each rising edge of the DCSCLK pin. Data are shifted into the LSB of the register with each rising edge. The MSB of the register is shifted to the DCSOUT pin with each rising edge.
XDCLAT	26	25	I	Data in the shift register are moved to the dot correction data latch with a low-to-high transition of this pin.
DCSOUT	25	24	O	Serial data output for dot correction. This signal is connected to the MSB of the Dot Correction Shift Register.
BLANK	23	22	I	Blank (all constant current outputs off). When BLANK is high, all constant current outputs (OUT0 through OUT15) are forced off, the Grayscale counter is reset to '0', and the Grayscale PWM timing controller is initialized. When BLANK is low, all constant current outputs are controlled by the Grayscale PWM timing controller.
IREF	27	26	I/O	Constant current value setting. OUT0 through OUT15 sink constant current is set to desired value by connecting an external resistor between IREF and GND.
OUT0	14	11	O	Constant current output
OUT1	13	10	O	Constant current output
OUT2	12	9	O	Constant current output
OUT3	11	8	O	Constant current output
OUT4	10	7	O	Constant current output
OUT5	9	6	O	Constant current output
OUT6	8	5	O	Constant current output
OUT7	7	4	O	Constant current output
OUT8	15	14	O	Constant current output
OUT9	16	15	O	Constant current output
OUT10	17	16	O	Constant current output
OUT11	18	17	O	Constant current output
OUT12	19	18	O	Constant current output
OUT13	20	19	O	Constant current output
OUT14	21	20	O	Constant current output
OUT15	22	21	O	Constant current output
VCC	28	27	—	Power-supply voltage
GND	1	30	—	Power ground
NC	—	12, 13, 28, 29	—	No internal connection

PARAMETER MEASUREMENT INFORMATION

PIN EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS

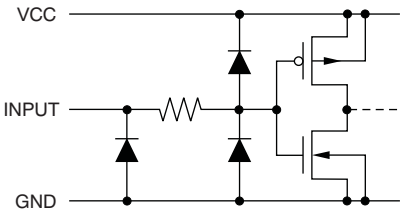


Figure 1. GSSIN, GSSCLK, XGSLAT, DCSIN, DCSCLK, XDCLAT, BLANK

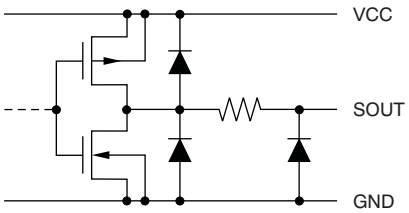


Figure 2. SOUT

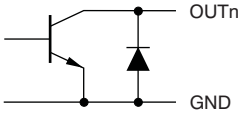
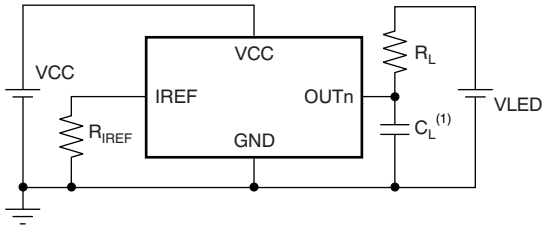


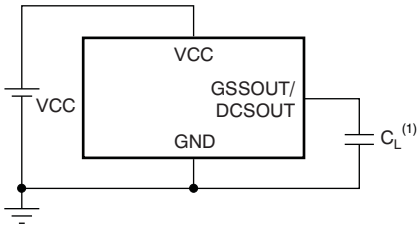
Figure 3. OUT0 Through OUT15

TEST CIRCUITS



(1) C_L includes measurement probe and jig capacitance.

Figure 4. Rise Time and Fall Time Test Circuit for OUTn



(1) C_L includes measurement probe and jig capacitance.

Figure 5. Rise Time and Fall Time Test Circuit for GSSOUT/DCSOUT

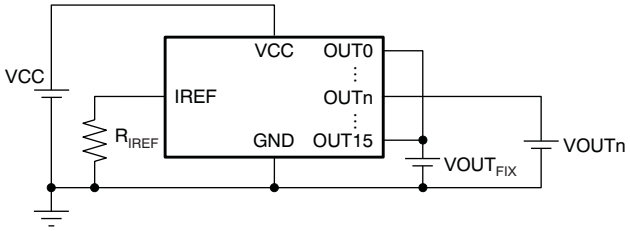
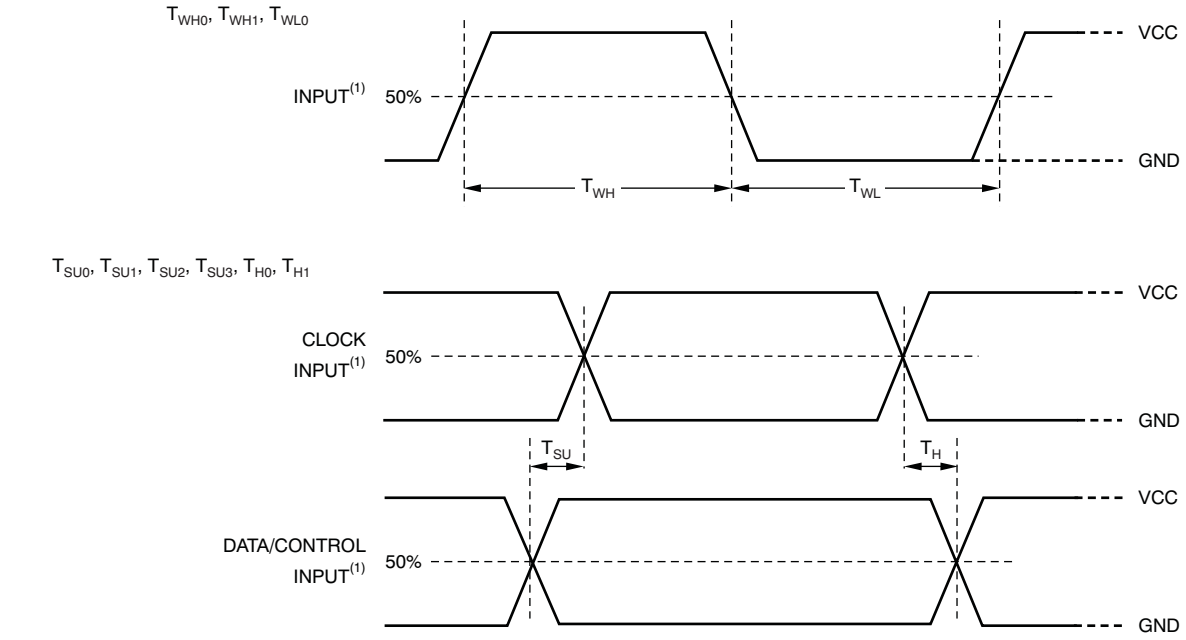


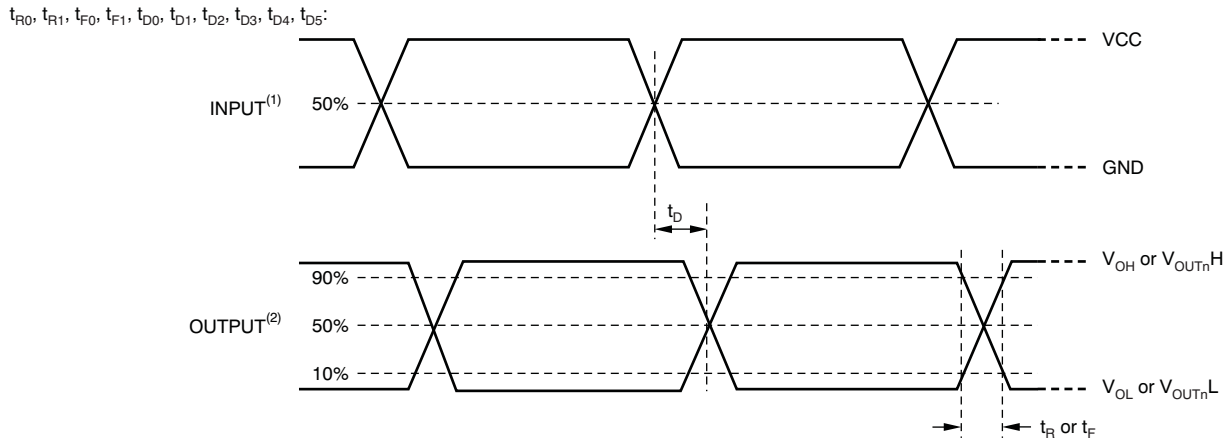
Figure 6. Test Circuit for OUTn

TIMING DIAGRAMS



(1) Input pulse rise and fall time is 1 ns to 3 ns.

Figure 7. Input Timing



(1) Input pulse rise and fall time is 1 ns to 3 ns.

(2) Input pulse high level is VCC and low level is GND.

Figure 8. Output Timing

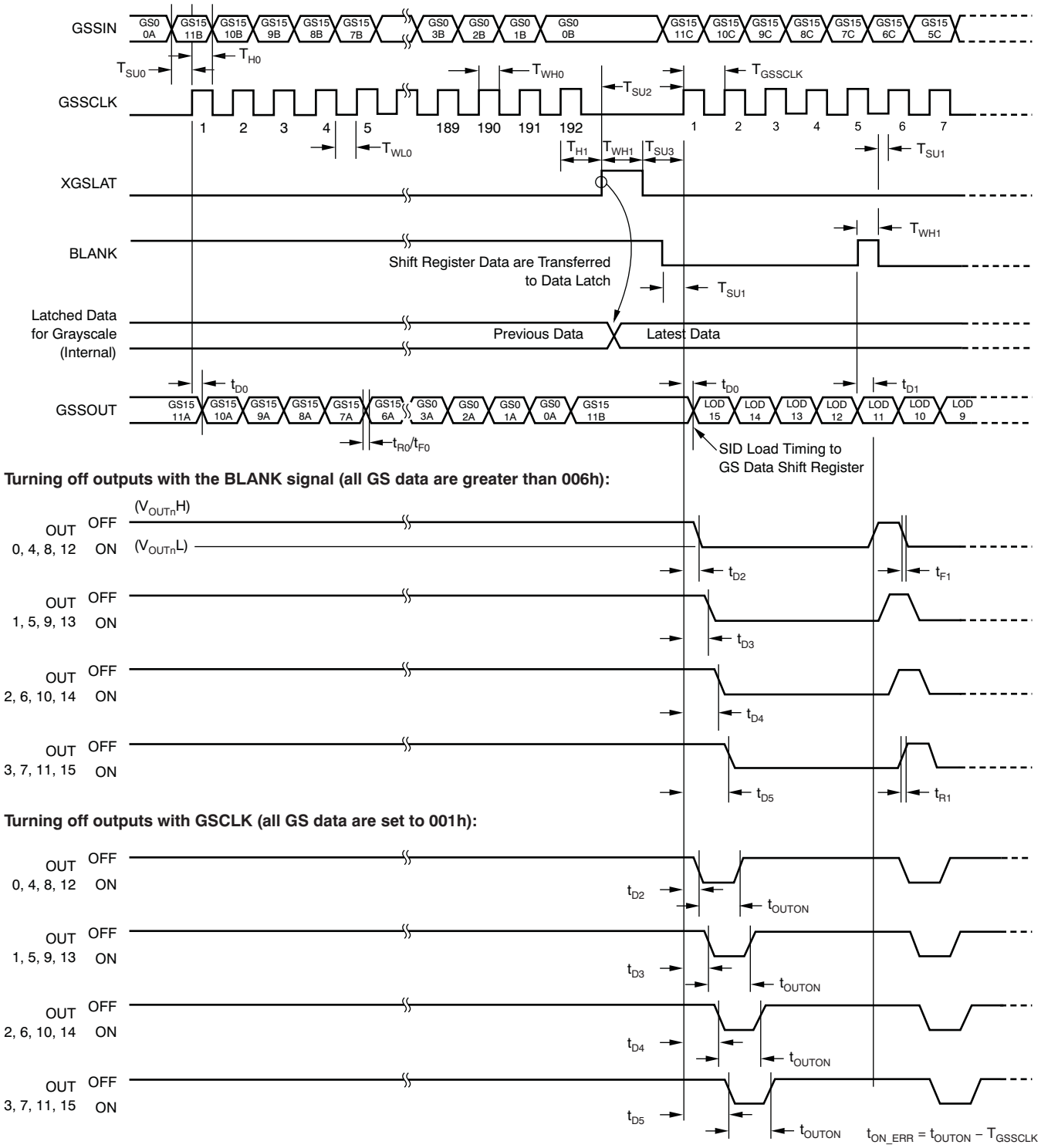


Figure 9. Grayscale Data Write Timing

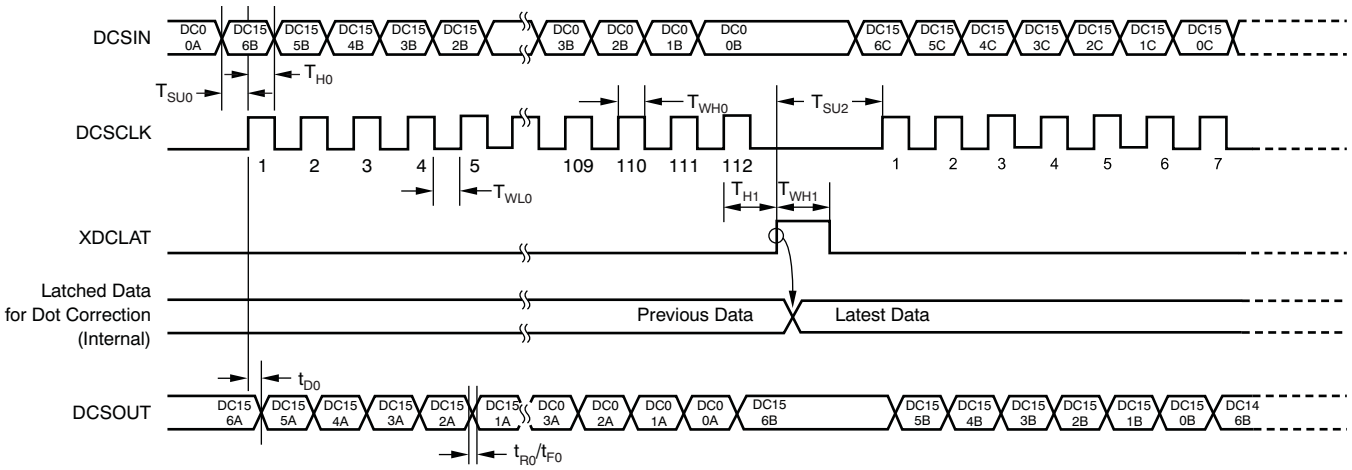
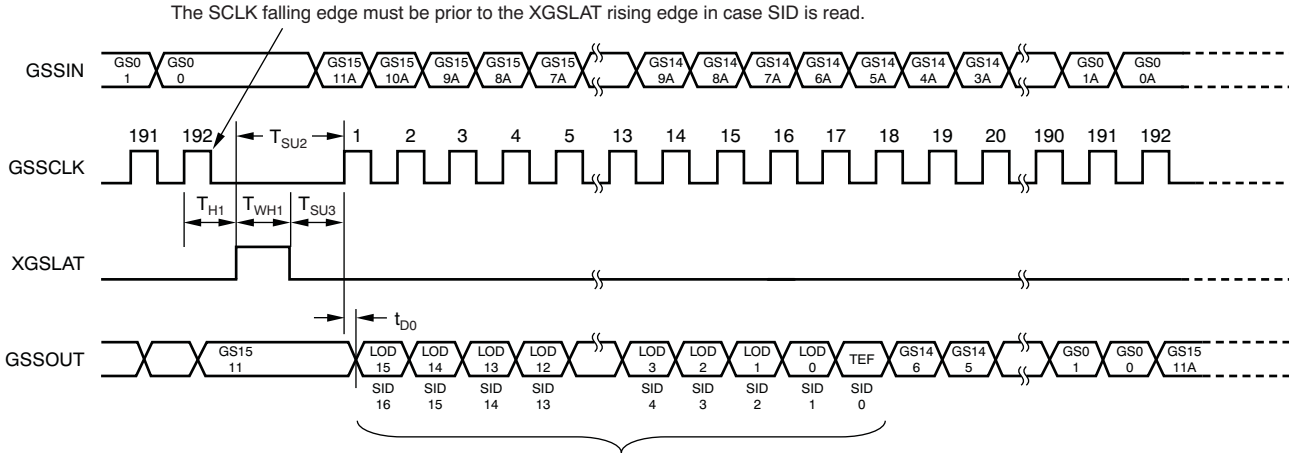


Figure 10. Dot Correction Data Write Timing



SID are entered in the GS shift register at the first rising edge of GSSCLK after XGSLAT goes low.
The SID readout consists of the saved LOD result at the 33rd GSSCLK rising edge in the previous display period and the TEF data at the rising edge of the first GSCLK after XGSLAT goes low.

Figure 11. Status Information Data Read Timing

TYPICAL CHARACTERISTICS

At VCC = 3.3 V and T_A = +25°C, unless otherwise noted.

REFERENCE RESISTOR vs OUTPUT CURRENT

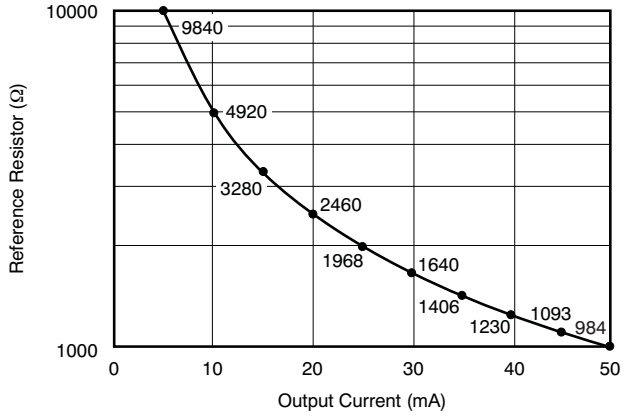


Figure 12.

POWER DISSIPATION RATE vs FREE-AIR TEMPERATURE

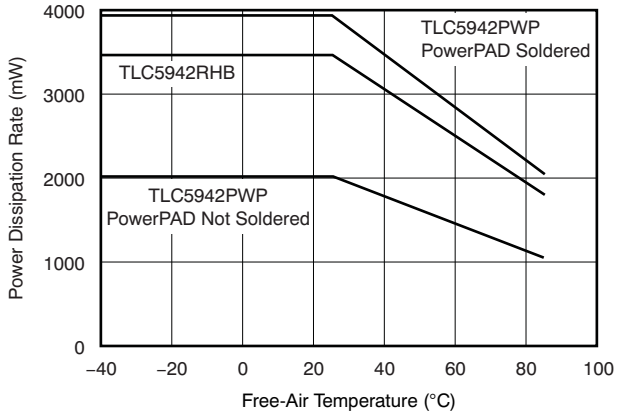


Figure 13.

OUTPUT CURRENT vs OUTPUT VOLTAGE

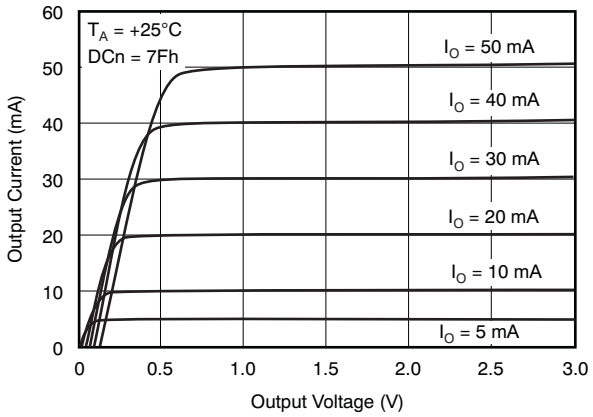


Figure 14.

OUTPUT CURRENT vs OUTPUT VOLTAGE

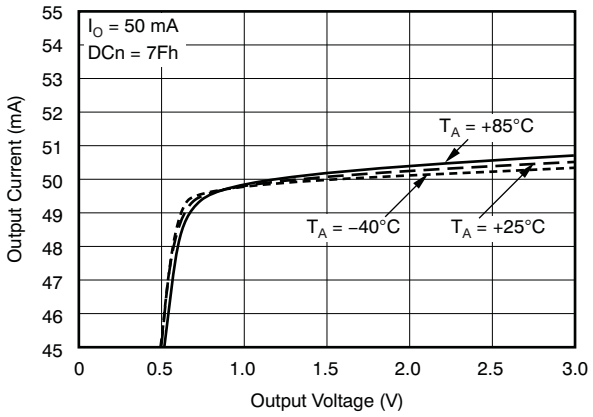


Figure 15.

ΔI_{OLC} vs AMBIENT TEMPERATURE

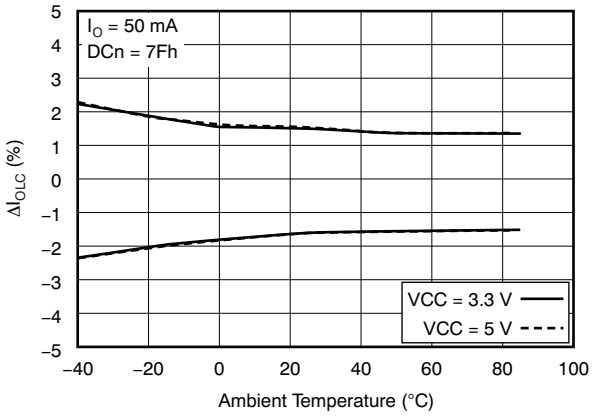


Figure 16.

ΔI_{OLC} vs OUTPUT CURRENT

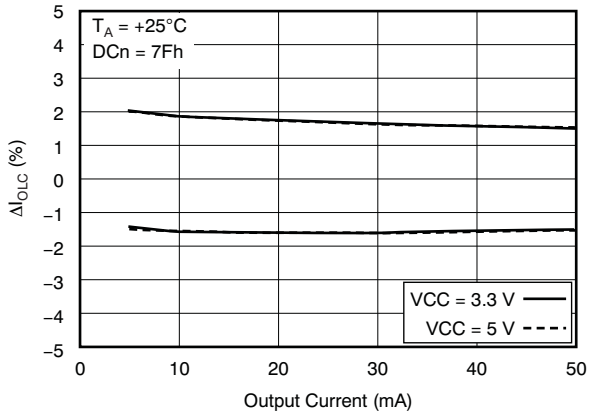


Figure 17.

TYPICAL CHARACTERISTICS (continued)

At VCC = 3.3 V and T_A = +25°C, unless otherwise noted.

DOT CORRECTION LINEARITY

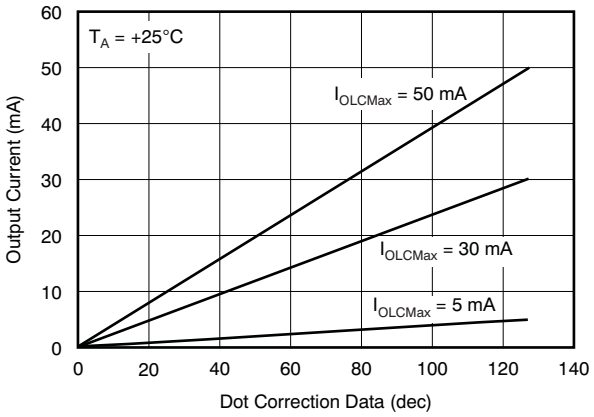


Figure 18.

DOT CORRECTION LINEARITY

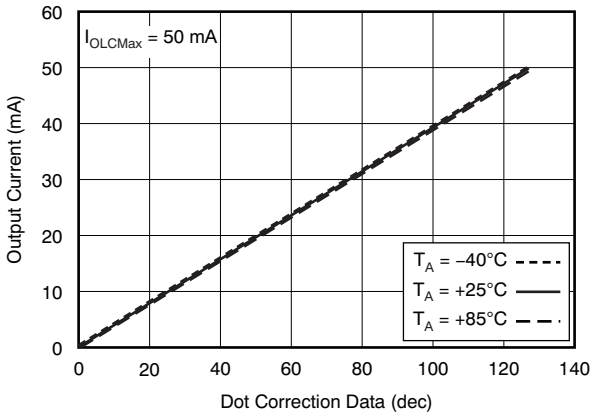


Figure 19.

CONSTANT CURRENT OUTPUT VOLTAGE WAVEFORM

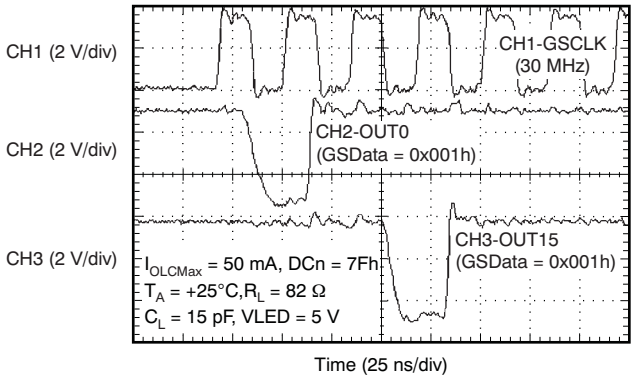


Figure 20.

DETAILED DESCRIPTION

Setting for the Maximum Constant Sink Current Value

On the TLC5942, the maximum constant current sink value for each channel, I_{OLCMax}, is determined by an external resistor, R_{IREF}, placed between the IREF and GND pins. The R_{IREF} resistor value is calculated with Equation 1:

$$R_{IREF}\ (k\Omega) = \frac{V_{IREF}\ (V)}{I_{OLCMax}\ (mA)} \times 41 \quad (1)$$

Where:

V_{IREF} = the internal reference voltage on the IREF pin (typically 1.20 V)

I_{OLCMax} is the largest current for all outputs. Each output sinks the I_{OLCMax} current when it is turned on and its dot correction is set to the maximum value of 7Fh (127d). The sink current for each output can be reduced by lowering the respective output dot correction value.

R_{IREF} must be between 984 Ω (typ) and 9.84 kΩ (typ) in order to keep I_{OLCMax} between 5 mA and 50 mA. The output may become unstable when I_{OLCMax} is set lower than 5 mA. However, output currents lower than 5 mA can be achieved by setting I_{OLCMax} to 5 mA or higher, and then using dot correction to lower the output current.

Figure 12 in the Typical Characteristics and Table 1 show the characteristics of the constant sink current versus external resistor, R_{IREF}.

Table 1. Maximum Constant Current Output versus External Resistor Value

I_{OLCMax} (mA, typical)	R_{IREF} (Ω)
50	984
45	1093
40	1230
35	1406
30	1640
25	1968
20	2460
15	3280
10	4920
5	9840

Dot Correction (DC) Function

The TLC5942 is able to individually adjust the output current of each channel (OUT0 to OUT15). This function is called *dot correction* (DC). The DC function allows users to individually adjust the brightness and color deviations of LEDs connected to the outputs OUT0 to OUT15. Each respective channel output current can be adjusted in 128 steps from 0% to 100% of the maximum output current, I_{OLCMax}. The dot correction data are entered into the TLC5942 via the serial interface.

Equation 2 determines the sink current for each output (OUTn):

$$I_{OUTn}\ (mA) = I_{OLCMax}\ (mA) \times \left(\frac{DCn}{127d}\right) \quad (2)$$

Where:

I_{OLCMax} = the maximum channel current for each channel determined by R_{IREF}

DCn = the programmed dot correction value for OUTn (DCn = 0 to 127d)

When the IC is powered on, the data in the Dot Correction Shift Register and data latch are not set to any default values. Therefore, DC data must be written to the DC latch before turning on the constant current output.

Table 2 summarizes the DC data versus current ratio and set current value.

Table 2. DC Data versus Current Ratio and Set Current Value

DC DATA (Binary)	DC DATA (Decimal)	DC DATA (Hex)	SET CURRENT RATIO TO MAX CURRENT (%)	OUTPUT CURRENT (mA, typical) AT I_{OLCMax} = 50 mA	OUTPUT CURRENT (mA, typical) AT I_{OLCMax} = 5 mA
000 0000	0	00	0.0	0.0	0.00
000 0001	1	01	0.8	0.4	0.04
000 0010	2	02	1.6	0.8	0.08
... ...	... ...	... ...	... ...	... ...	... ...
111 1101	125	7D	98.4	49.2	4.92
111 1110	126	7E	99.2	49.6	4.96
111 1111	127	7F	100.0	50.0	5.00

Grayscale (GS) Function (PWM Operation)

The pulse width modulation (PWM) operation is controlled by a 12-bit grayscale counter that is clocked on each rising edge of the grayscale reference clock, GSSCLK. The counter is reset to zero when the BLANK signal is set high. The counter value is held at zero while BLANK is high, even if the GSSCLK input toggles high and low. After the falling edge of BLANK, the counter increments with each rising edge of GSSCLK. Any constant current sink output (OUT0 through OUT15) with a nonzero value in its corresponding grayscale latch starts to sink current after the first rising edge of GSSCLK following a high-to-low transition of BLANK. The internal counter keeps track of the number of GSSCLK pulses. Each output channel stays on as long as the internal counter is equal to or less than the respective output GSSCLK. Each channel turns off at the rising edge of GSSCLK when the grayscale counter value is larger than the grayscale latch value.

For example, an output that has a grayscale latch value of '1' turns on at the first rising edge of GSSCLK after BLANK goes low. It turns off at the second rising edge of GSSCLK. Figure 21 shows the PWM timing diagram.

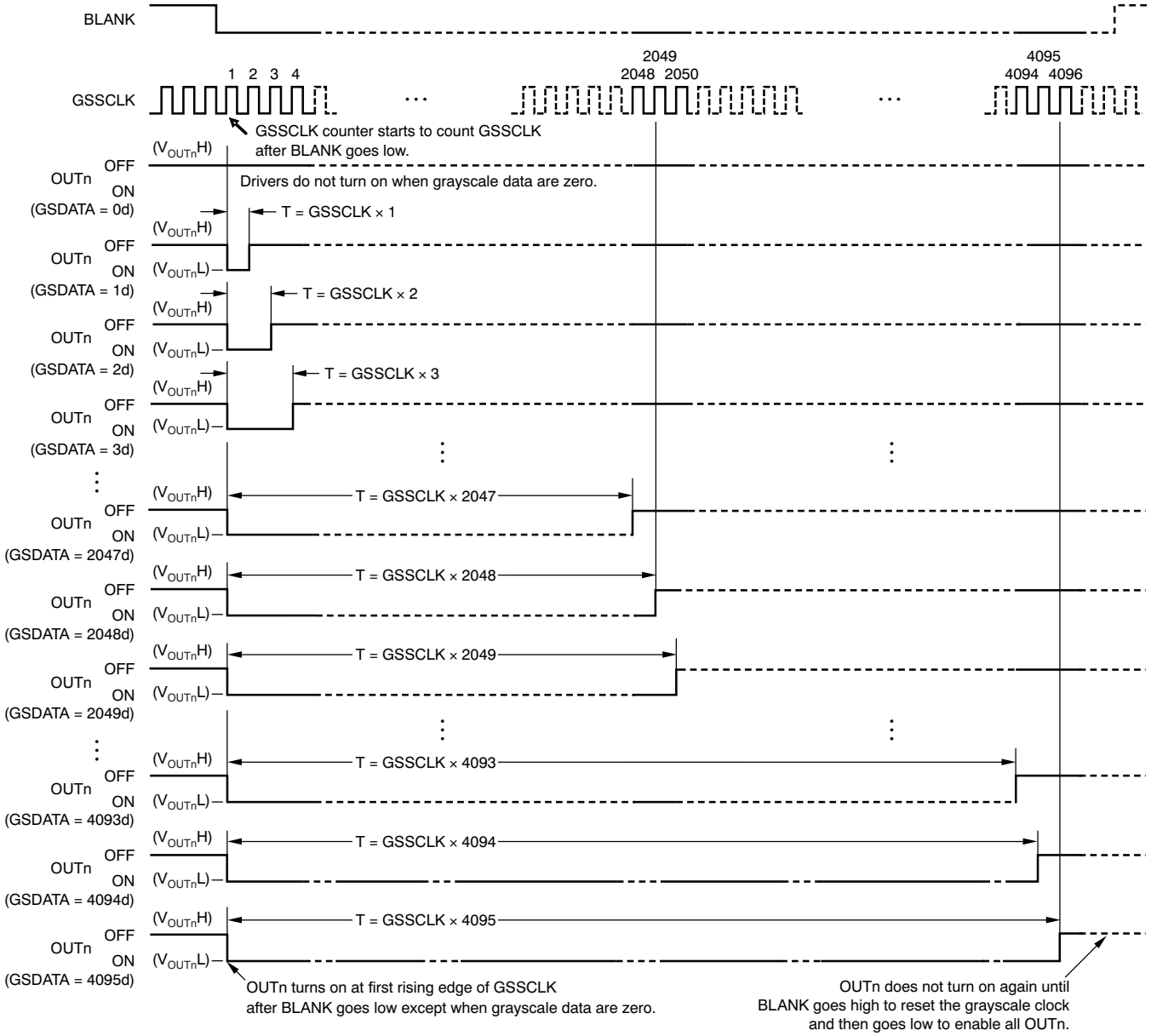


Figure 21. PWM Operation Timing

When the IC is powered on, the data in the Grayscale Shift Register and latch are not set to any default value. Therefore, Grayscale data must be written to the Grayscale latch before turning the constant current output on. Additionally, BLANK should be high when the device turns on, to prevent the outputs from turning on before the proper grayscale and dot correction values can be written. All constant current outputs are always off when BLANK is high. Equation 3 determines each output (OUTn) on time (t_{OUTON}):

$$t_{OUTON}\ (ns) = T_{GSSCLK}\ (ns) \times GSn \quad (3)$$

Where:

T_{GSSCLK} = the period of GSSCLK

GSn = the programmed grayscale value for OUTn (GSn = 0 to 4095d)

If there are any unconnected output LED lamps (including connection failures or short-circuits), the grayscale data corresponding to the unconnected output should be set to '0' before turning on the LEDs. Otherwise, the supply current (I_{VCC}) increases while the LEDs are on. If GS data changes during a GS period because XLAT goes high, and latches new GS data, the internal data latch registers are immediately updated. This action can cause the outputs to turn on or off unexpectedly. For proper operation, GS data should only be latched into the IC at the end of a GS period when BLANK is high. Table 3 summarizes the GS data versus OUTn on duty and on time.

Table 3. GS Data versus OUTn On Duty and OUTn On Time

GS DATA (Binary)	GS DATA (Decimal)	GS DATA (Hex)	OUTn ON DUTY (%)	OUTn ON TIME (ns, typical) AT 30 MHz GSSCLK
0000 0000 0000	0	000	0.00	0
0000 0000 0001	1	001	0.02	33
0000 0000 0010	2	002	0.05	67
0000 0000 0011	3	003	0.07	100
... ...	... ...	... ...	... ...	... ...
0111 1111 1111	2047	7FF	49.99	68263
1000 0000 0000	2048	800	50.01	68267
1000 0000 0001	2049	801	50.04	68300
... ...	... ...	... ...	... ...	... ...
1111 1111 1101	4093	FFD	99.95	136433
1111 1111 1110	4094	FFE	99.98	135467
1111 1111 1111	4095	FFF	100.00	136500

Grayscale Shift Register and Data Latch

The Grayscale (GS) Shift Registers and data latches are each 192 bits in length, and are used to set the PWM timing for each constant current driver. See Table 3 for the ON time duty of each GS data bit. Figure 22 shows the shift register and latch configuration. Refer to Figure 9 for the timing diagram for writing data into the GS shift register and latch. The driver on time is set by the data in the GS data latch. GS data present on the GSSIN pin are clocked into the GS Shift Register with each rising edge of the GSSCLK pin. Data are shifted in MSB first. Data are latched from the shift register into the GS data latch with a rising edge on the XGSLAT pin.

When the IC is powered on, the data in Grayscale Shift Register and data latch are not set to any default value. Therefore, grayscale data must be written to the GS latch before turning on the constant current output. Also, BLANK should be high when powered on because the constant current may also turn on. All constant current outputs are off when BLANK is high.

The Status Information Data (SID) byte is overwritten on the most significant 17 bits of the Grayscale Shift Register at the rising edge of the first GSSCLK after XGSLAT goes low.

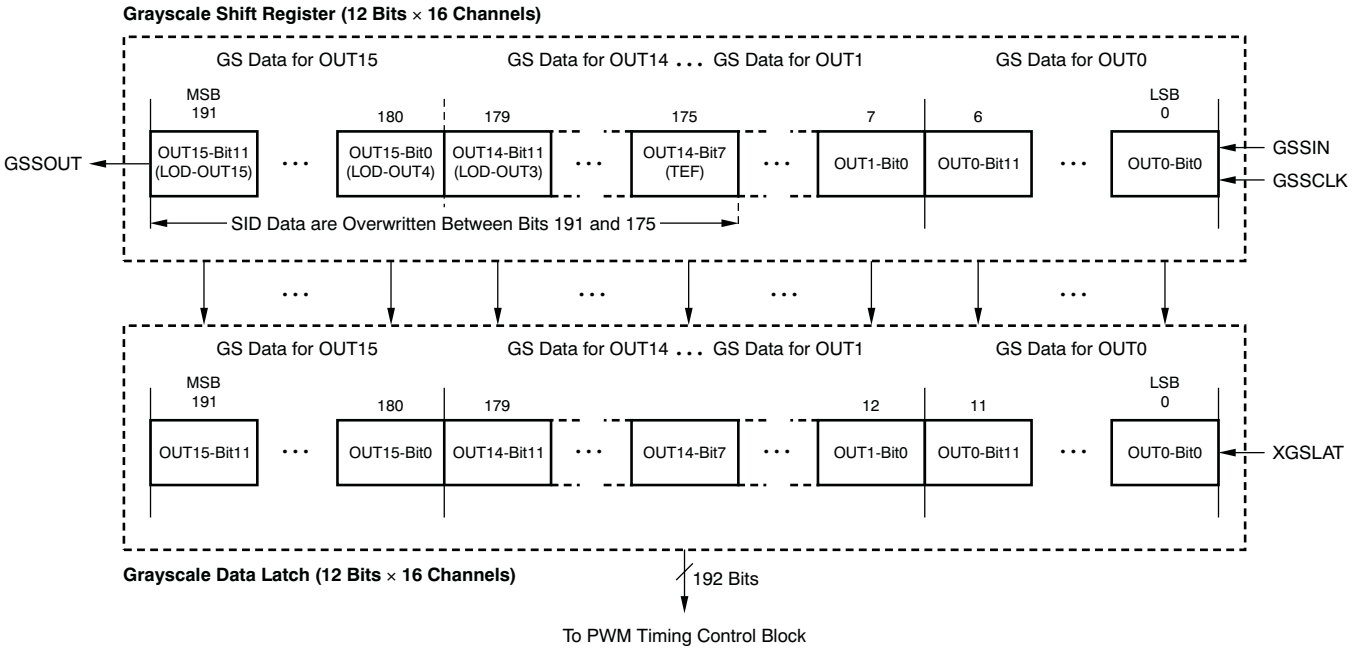


Figure 22. Grayscale Shift Register and Data Latch Configuration

Dot Correction Shift Register and Data Latch

The Dot Correction (DC) Shift Registers and latches are each 112 bits in length and are used to individually adjust the constant current values for each constant current driver. Each channel can be adjusted from 0% to 100% of the maximum LED current with 7-bit resolution. Table 2 describes the percentage of the maximum current for each dot correction data. See Figure 23 for the Dot Correction Shift Register and data latch configuration. Figure 10 illustrates the timing chart for writing data into the DC Shift Registers and latches. Each channel LED current is dot-corrected by the percentage corresponding to the data in its DC data latch. DC data present on the DCSIN pin are clocked into the DC Shift Register with each rising edge of the DCSCLK pin. Data are shifted in MSB first. The data are latched from the shift register into the DC data latch with a rising edge on the XDCLAT pin.

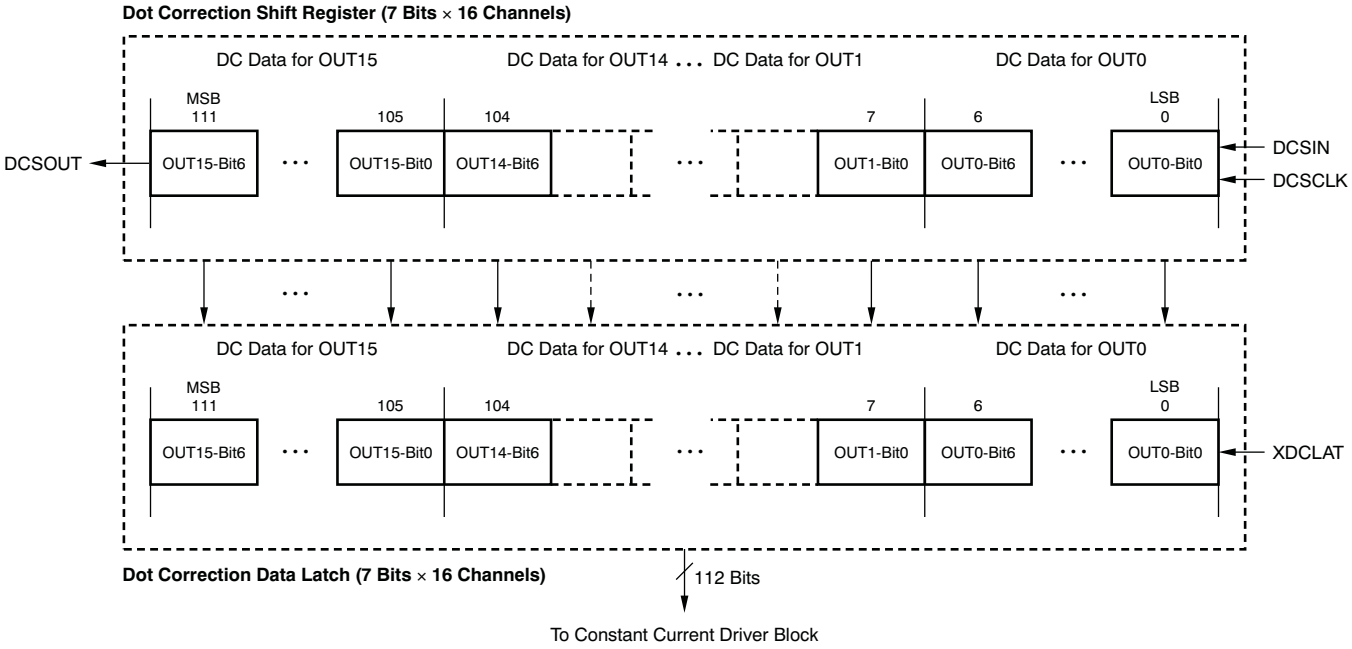


Figure 23. Dot Correction Shift Register and Latch Configuration

When the IC is powered on, the data in the Dot Correction Shift Register and data latch are not set to a specific default value. Therefore, dot correction data must be written to the DC latch before turning on the constant current output.

Status Information Data (SID)

Status information data (SID) are 17-bit, read-only data. Both the LED open detection (LOD) error and the thermal error flag (TEF) are shifted out of the GSSOUT pin with each rising edge of the grayscale clock, GSSCLK. The 16 LOD bits for each channel and the TEF bit are written into the 17 most significant bits of the Grayscale Shift Register at the rising edge of the first GSSCLK after XGSLAT goes low. As a result, the previous data in the 17 most significant bits are lost at the same time. No data are loaded into the other 175 bits. Figure 24 shows the bit assignments. Figure 11 illustrates the read timing for the status information data.

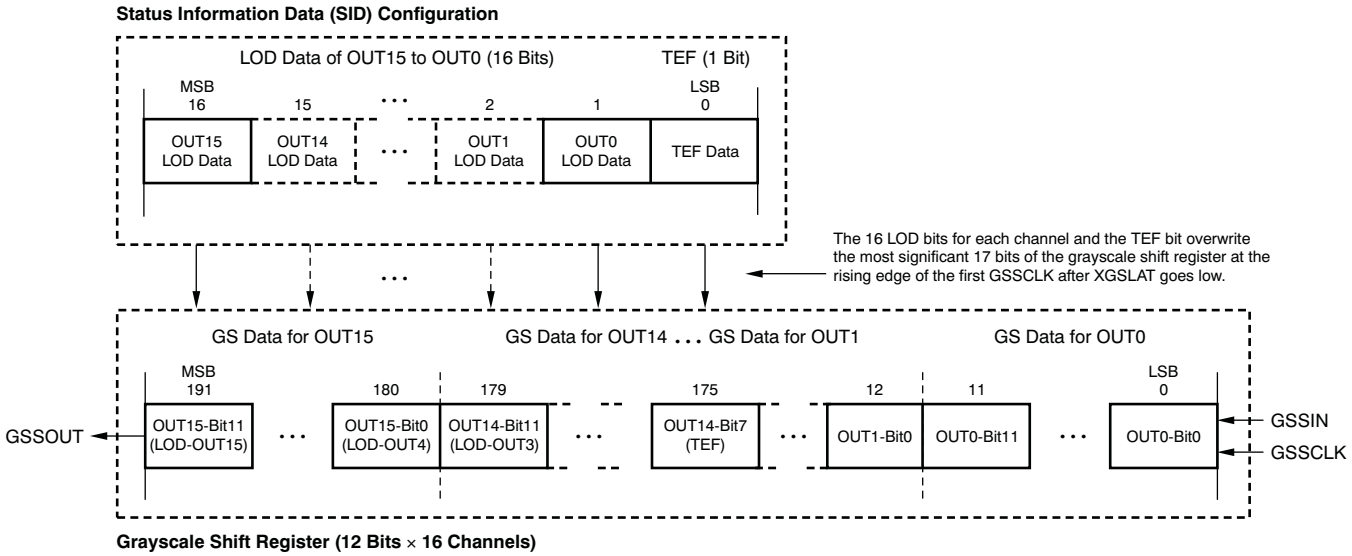


Figure 24. Status Information Data Configuration

The LOD data are updated at the rising edge of the 33rd GSSCLK pulse after BLANK goes low; the LOD data are retained until the next 33rd GSSCLK. LOD data are only checked for outputs that are turned on during the rising edge of the 33rd GSSCLK pulse. A '1' in an LOD bit indicates an open LED condition for the corresponding channel. A '0' indicates normal operation. It is possible for LOD data to show a '0' even if the LED is open when the grayscale data are less than 20h (32d). Therefore, the GS data must be set to 21h (33d) or higher to get updated LOD data beyond 20h (32d).

The TEF bit indicates that the IC temperature is too high. The flag also indicates that the IC has turned off all drivers to avoid damage by overheating the device. A '1' in the TEF bit means that the IC temperature has exceeded the detect temperature threshold (T_{TEF}) and the driver is turned off. A '0' in the TEF bit indicates normal operating temperature conditions. The IC automatically turns the drivers back on when the IC temperature decreases to less than $T_{TEF-THYS}$. When the IC is powered on, LOD data do not show correct values. Therefore, LOD data must be read from the 33rd GSSCLK pulse input after BLANK goes low. Table 4 shows a truth table for both LOD and TEF.

Table 4. LOD and TEF Truth Table

SID DATA	CONDITION	
	LED OPEN DETECTION (LODn)	THERMAL ERROR FLAG (TEF)
0	LED is connected ($V_{OUTn} > V_{IOD}$)	Device temperature is low (temp ≤ $T_{TEF–THYS}$)
1	LED is open or shorted to GND ($V_{OUTn} \le V_{IOD}$)	Device temperature is high (temp > T_{TEF})

Continuous Base LED Open Detection

The LED Open Detection (LOD) circuit checks the voltage of each active (that is, on) constant current sink output (OUT0 through OUT15) at the rising edge of the 33rd GSSCLK after the falling edge of BLANK to detect open and short LEDs to GND. The channels corresponding to the LOD bit in the Status Information Data register (SID) are set to a '1' if the voltage of the OUTn pin is less than the LED open detection threshold (V_{LOD} = 0.3 V_{TYP}). This status information can be read from the GSSOUT pin. No special test sequence is required for LED open detection.

The LOD function automatically checks for open and short LEDs to GND during each grayscale PWM cycle. The SID information of the LOD is latched into the LED Open Detection data latch and does not change until the rising edge of the 33rd GSSCLK pulse following the next falling edge of BLANK. To eliminate false detection of open LEDs, the LED driver design must ensure that the TLC5942 output voltage is greater than V_{LOD} when the outputs are on. The GS data must be 21h (33d) or more to get the LOD result.

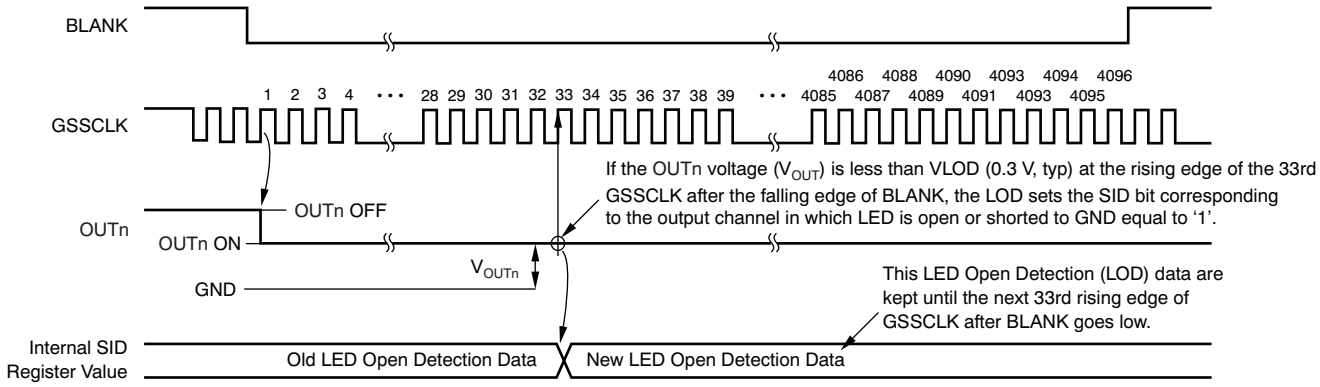


Figure 25. LED Open Detection (LOD) Timing

Thermal Shutdown and Thermal Error Flag

The Thermal Shutdown (TSD) function turns off all of the constant current outputs on the IC when the junction temperature (T_J) exceeds the threshold (T_{TEF} = +162°C, typ) and sets the thermal error flag (TEF) to '1'. All outputs are latched off when TEF is set to '1' and remain off until the next grayscale cycle after the junction temperature drops below ($T_{(TEF)} - T_{(HYS)}$). TEF is set to '0' once the junction temperature drops below ($T_{(TEF)} - T_{(HYS)}$), but the outputs do not turn on until the first GSSCLK after BLANK goes low while TEF is set to '0'.

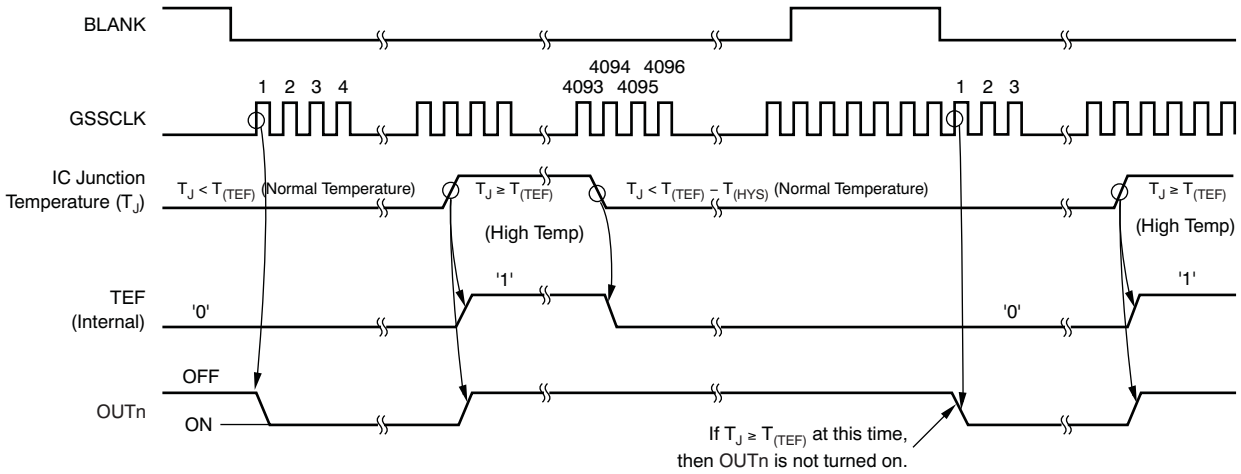


Figure 26. TEF/TSD Timing

Noise Reduction

Large surge currents may flow through the IC and the board on which the device is mounted if all 16 LED channels turn on simultaneously at the start of each grayscale cycle. These large current surges could introduce detrimental noise and electromagnetic interference (EMI) into other circuits. The TLC5942 turns on the LED channels in a series delay, to provide a current soft-start feature. The output current sinks are grouped into four groups of four channels each. The first group is OUT0, 4, 8, 12; the second group is OUT1, 5, 9, 13; the third group is OUT2, 6, 10, 14; and the fourth group is OUT3, 7, 11, 15. Each group turns on sequentially with a small delay between groups; see Figure 9. Both turn-on and turn-off are delayed.

POWER DISSIPATION CALCULATION

The device power dissipation must be below the power dissipation rate of the device package illustrated in Figure 13 to ensure correct operation. Equation 4 calculates the power dissipation of the device:

$$P_D = (V_{CC} \times I_{CC}) + \left(V_{OUT} \times I_{MAX} \times N \times \frac{DCn}{127d} \times d_{PWM} \right) \quad (4)$$

Where:

V_{CC} = device supply voltage
I_{CC} = device supply current
V_{OUT} = OUTn voltage when driving LED current
I_{MAX} = LED current adjusted by $R_{(IREF)}$ resistor
DCn = maximum dot correction value for OUTn (decimal)
N = number of OUTn driving LED at the same time
d_{PWM} = duty ratio defined by BLANK pin or GS PWM value

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (October 2007) to Revision B	Page
• Changed Figure 11.	12

Changes from Original (October 2007) to Revision A	Page
• Changed release date for QFN package	2

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC5942PWP	NRND	HTSSOP	PWP	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLC5942	
TLC5942PWPG4	NRND	HTSSOP	PWP	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLC5942	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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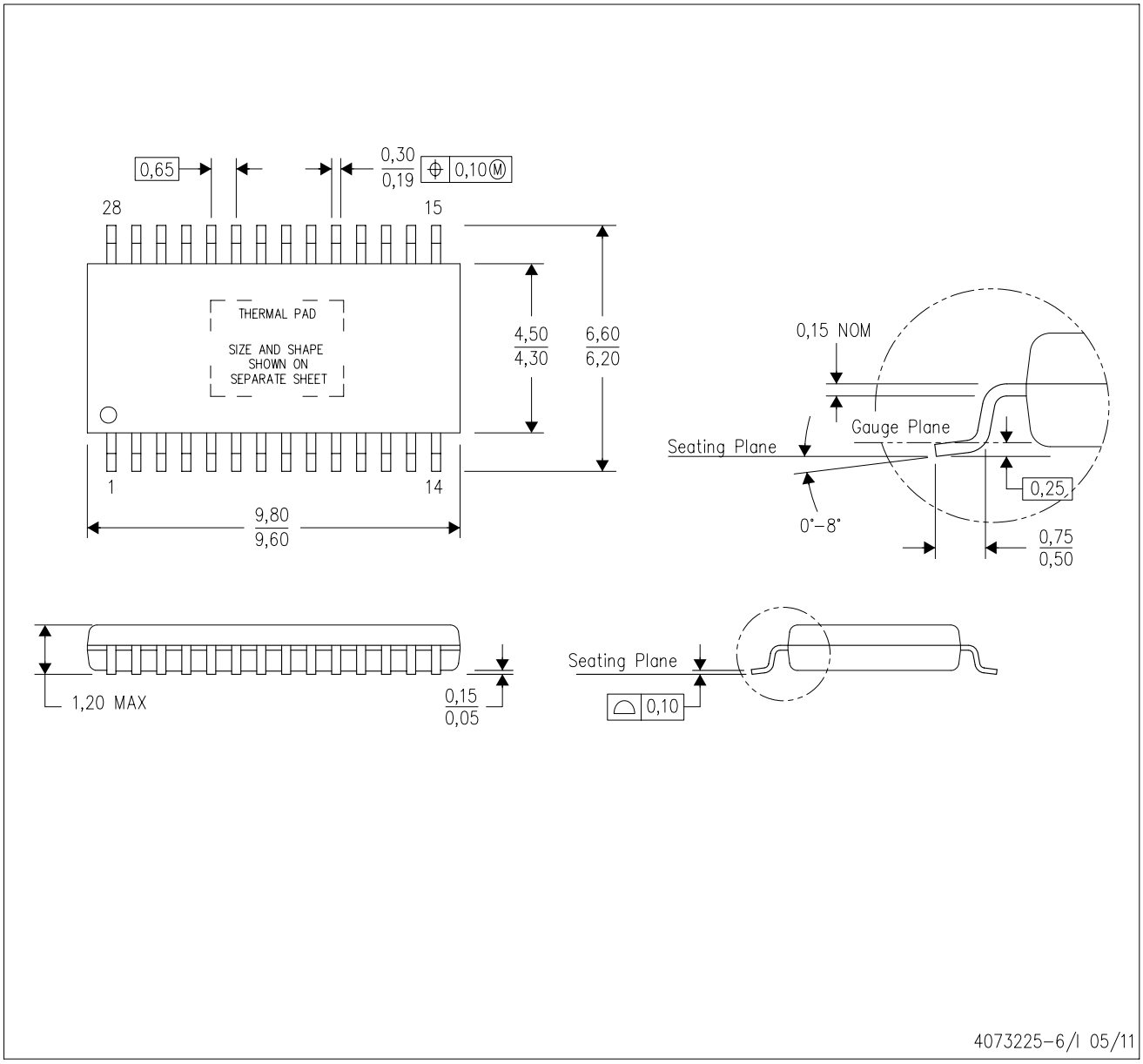
PWP (R–PDSO–G28) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

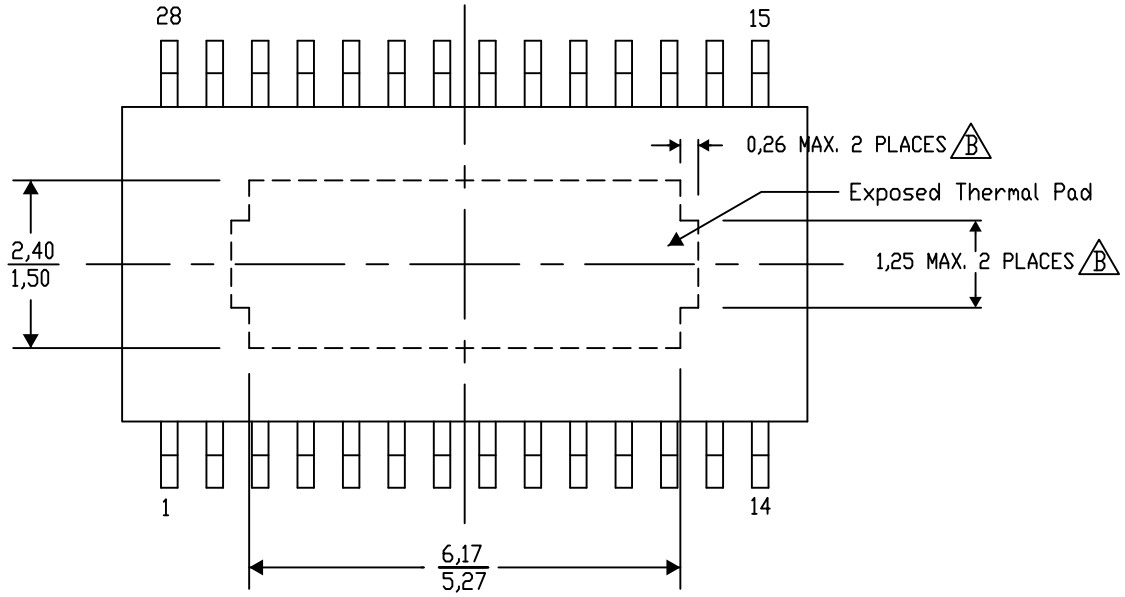
PWP (R–PDSO–G28) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206332–33/AI 09/14

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

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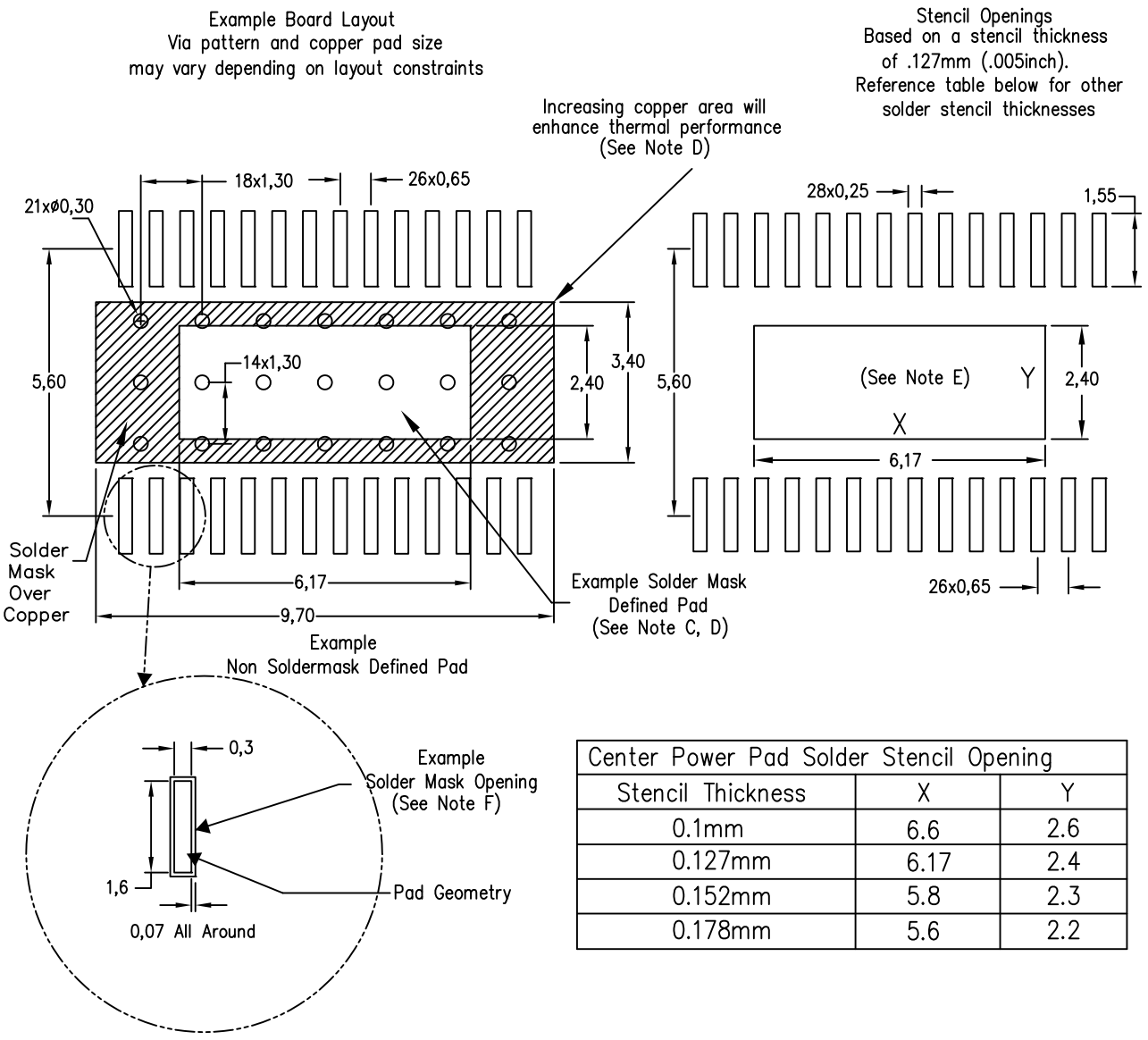
PWP (R–PDSO–G28) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	6.6	2.6
0.127mm	6.17	2.4
0.152mm	5.8	2.3
0.178mm	5.6	2.2

4207609–19/T 08/13

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets.
E. For specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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