

# LinCMOS™ DUAL LOW-VOLTAGE DIFFERENTIAL COMPARATORS

TLV2352, TLV2352Y

SLCS011B – MAY 1992 – REVISED MARCH 1999

- Wide Range of Supply Voltages  
2 V to 8 V
- Fully Characterized at 3 V and 5 V
- Very-Low Supply-Current Drain  
120  $\mu$ A Typ at 3 V
- Output Compatible With TTL, MOS, and CMOS
- Fast Response Time . . . 200 ns Typ for TTL-Level Input Step
- High Input Impedance . . .  $10^{12} \Omega$  Typ
- Extremely Low Input Bias Current  
5 pA Typ
- Common-Mode Input Voltage Range  
Includes Ground
- Built-In ESD Protection

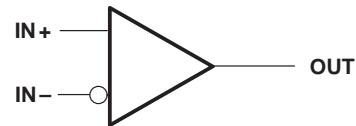
## description

The TLV2352 consists of two independent, low-power comparators specifically designed for single power-supply applications and operates with power-supply rails as low as 2 V. When powered from a 3-V supply, the typical supply current is only 120  $\mu$ A.

The TLV2352 is designed using the Texas Instruments LinCMOS™ technology and therefore features an extremely high input impedance (typically greater than  $10^{12} \Omega$ ), which allows direct interfacing with high-impedance sources. The outputs are N-channel open-drain configurations that require an external pullup resistor to provide a positive output voltage swing, and they can be connected to achieve positive-logic wired-AND relationships. The TLV2352I is fully characterized at 3 V and 5 V for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ . The TLV2352M is fully characterized at 3 V and 5 V for operation from  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ .

The TLV2352 has internal electrostatic-discharge (ESD)-protection circuits and has been classified with a 1000-V ESD rating using Human Body Model testing. However, care should be exercised in handling this device as exposure to ESD may result in degradation of the device parametric performance.

## symbol (each comparator)



## AVAILABLE OPTIONS

T <sub>A</sub>	V <sub>IO</sub> max at 25°C	PACKAGED DEVICES						CHIP FORM (Y)
		SMALL OUTLINE (D) <sup>†</sup>	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)	TSSOP (PW) <sup>‡</sup>	PLASTIC DIP (U)	
$-40^{\circ}\text{C}$ to $85^{\circ}\text{C}$	5 mV	TLV2352ID	—	—	TLV2352IP	TLV2352IPWLE	—	TLV2352Y
$-55^{\circ}\text{C}$ to $125^{\circ}\text{C}$	5 mV	—	TLV2352MFK	TLV2352MJG	—	—	TLV2352MU	

<sup>†</sup> The D package is available taped and reeled. Add the suffix R to the device type (e.g., TLV2352IDR).

<sup>‡</sup> The PW packages are only available left-ended taped and reeled (e.g., TLV2352IPWLE)



These devices have limited built-in protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

LinCMOS is a trademark of Texas Instruments Incorporated.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

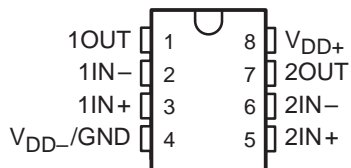
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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

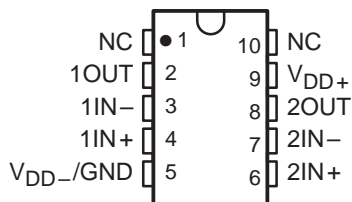
# TLV2352, TLV2352Y LinCMOS™ DUAL LOW-VOLTAGE DIFFERENTIAL COMPARATORS

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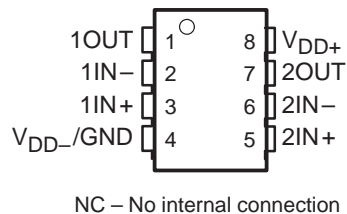
**TLV2352I . . . D OR P PACKAGE  
TLV2352M . . . JG PACKAGE  
(TOP VIEW)**



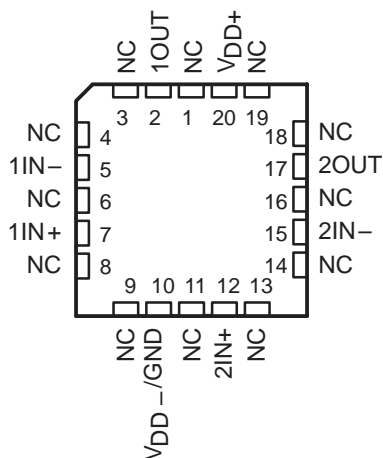
**TLV2254M  
U PACKAGE  
(TOP VIEW)**



**TLV2352I . . . PW PACKAGE  
(TOP VIEW)**

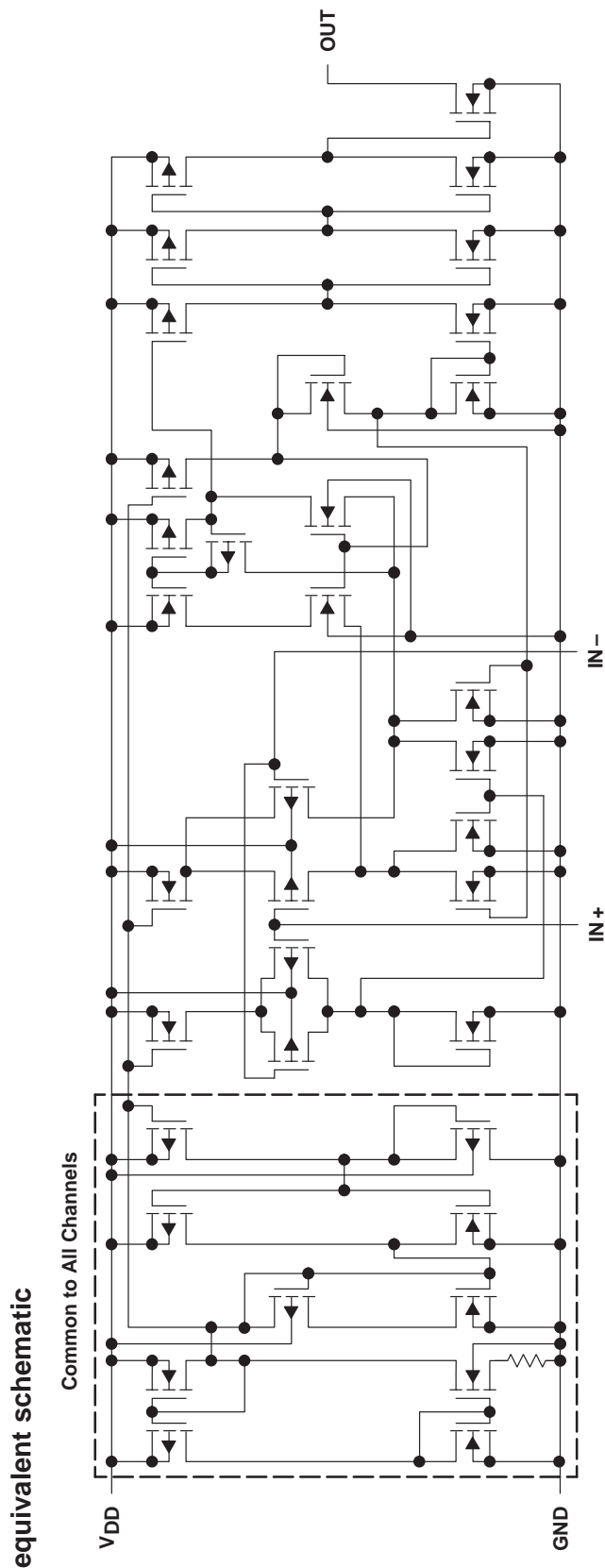


**TLV2352M  
FK PACKAGE  
(TOP VIEW)**



# TLV2352, TLV2352Y LinCMOS™ DUAL LOW-VOLTAGE DIFFERENTIAL COMPARATORS

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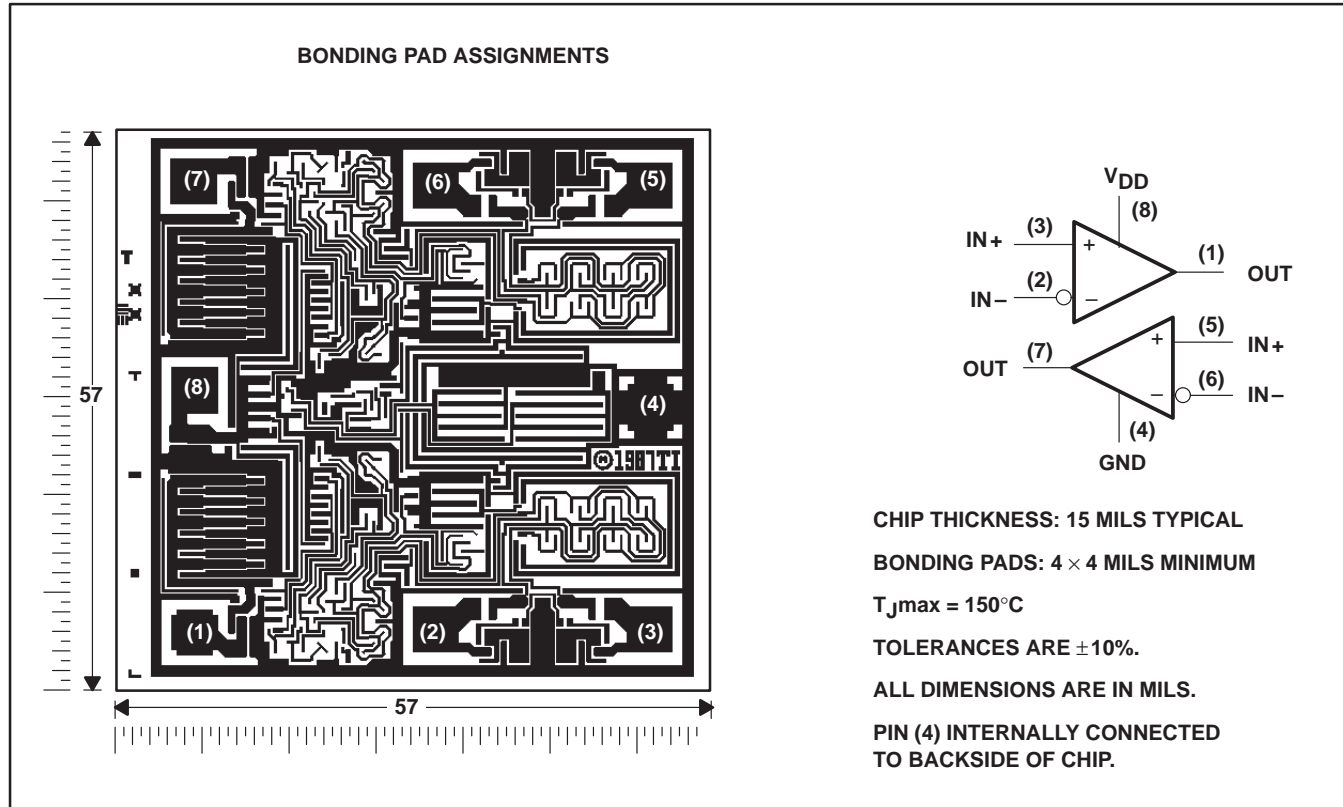


# TLV2352, TLV2352Y LinCMOS™ DUAL LOW-VOLTAGE DIFFERENTIAL COMPARATORS

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## TLV2352Y chip information

These chips, when properly assembled, display characteristics similar to the TLV2352. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. This chip can be mounted with conductive epoxy or a gold-silicon preform.



# TLV2352, TLV2352Y

## LinCMOS™ DUAL LOW-VOLTAGE DIFFERENTIAL COMPARATORS

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### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, $V_{DD}$ (see Note 1)	8 V
Differential input voltage, $V_{ID}$ (see Note 2)	$\pm 8$ V
Input voltage range, $V_I$	–0.3 to 8 V
Output voltage, $V_O$	8 V
Input current, $I_I$	$\pm 5$ mA
Output current, $I_O$	20 mA
Duration of output short-circuit current to GND (see Note 3)	unlimited
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, $T_A$ : TLV2352I	–40°C to 85°C
TLV2352M	–55°C to 125°C
Storage temperature range, $T_{stg}$	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, P, and PW Packages	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: FK, JG, and U Packages	300°C

† Stress beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.  
 2. Differential voltages are at  $IN+$  with respect to  $IN-$ .  
 3. Short circuits from outputs to  $V_{DD}$  can cause excessive heating and eventual device destruction.

**DISSIPATION RATING TABLE**

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR	$T_A = 85^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING
D	725 mW	5.8 mW/°C	377 mW	—
FK	1375 mW	11.0 mW/°C	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	546 mW	210 mW
P	1000 mW	8.0 mW/°C	520 mW	—
PW	525 mW	4.2 mW/°C	273 mW	—
U	700 mW	5.5 mW/°C	370 mW	150 mW

### recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, $V_{DD}$		2	8	V
Common-mode input voltage, $V_{IC}$	$V_{DD} = 3$ V	0	1.75	V
	$V_{DD} = 5$ V	0	3.75	
Operating free-air temperature, $T_A$	TLV2352I	–40	85	°C
	TLV2352M	–55	125	



# TLV2352, TLV2352Y LinCMOS™ DUAL LOW-VOLTAGE DIFFERENTIAL COMPARATORS

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## electrical characteristics at specified free-air temperature†

PARAMETER	TEST CONDITIONS	T <sub>A</sub> ‡	TLV2352I						UNIT
			V <sub>DD</sub> = 3 V			V <sub>DD</sub> = 5 V			
			MIN	TYP	MAX	MIN	TYP	MAX	
V <sub>IO</sub> Input offset voltage	V <sub>IC</sub> = V <sub>ICRmin</sub> , See Note 4	25°C	1		5	1		5	mV
		Full range	7			7			
I <sub>IO</sub> Input offset current		25°C	1			1			pA
		85°C			1			1	nA
I <sub>IB</sub> Input bias current		25°C	5			5			pA
		85°C			2			2	nA
V <sub>ICR</sub> Common-mode input voltage range		25°C	0 to 2			0 to 4			V
		Full range	0 to 1.75			0 to 3.75			
I <sub>OH</sub> High-level output current	V <sub>ID</sub> = 1 V	25°C	0.1			0.1			nA
		Full range	1			1			μA
V <sub>OL</sub> Low-level output voltage	V <sub>ID</sub> = -1 V, I <sub>OL</sub> = 2 mA	25°C	115		300	150		400	mV
		Full range	600			700			
I <sub>OL</sub> Low-level output current	V <sub>ID</sub> = -1 V, V <sub>OL</sub> = 1.5 V	25°C	6	16		6	16		mA
I <sub>DD</sub> Supply current	V <sub>ID</sub> = 1 V, No load	25°C	120		250	140		300	μA
		Full range	350			400			

† All characteristics are measured with zero common-mode input voltages unless otherwise noted.

‡ Full range is -40°C to 85°C. IMPORTANT: See *Parameter Measurement Information*.

NOTE 4: The offset voltage limits given are the maximum values required to drive the output above 4 V with V<sub>DD</sub> = 5 V, 2 V with V<sub>DD</sub> = 3 V, or below 400 mV with a 10-kΩ resistor between the output and V<sub>DD</sub>. They can be verified by applying the limit value to the input and checking for the appropriate output state.

## switching characteristics, V<sub>DD</sub> = 3 V, T<sub>A</sub> = 25°C

PARAMETER	TEST CONDITIONS	TLV2352I			UNIT
		MIN	TYP	MAX	
Response time	R <sub>L</sub> = 5.1 kΩ, C <sub>L</sub> = 15 pF§, See Note 5	100-mV input step with 5-mV overdrive		640	ns

§ C<sub>L</sub> includes probe and jig capacitance.

NOTE 5: The response time specified is the interval between the input step function and the instant when the output crosses V<sub>O</sub> = 1 V with V<sub>DD</sub> = 3 V or V<sub>O</sub> = 1.4 V with V<sub>DD</sub> = 5 V.

## switching characteristics, V<sub>DD</sub> = 5 V, T<sub>A</sub> = 25°C

PARAMETER	TEST CONDITIONS	TLV2352I			UNIT
		MIN	TYP	MAX	
Response time	R <sub>L</sub> = 5.1 kΩ, C <sub>L</sub> = 15 pF§, See Note 5	100-mV input step with 5-mV overdrive		650	ns
		TTL-level input step		200	

§ C<sub>L</sub> includes probe and jig capacitance.

NOTE 5: The response time specified is the interval between the input step function and the instant when the output crosses V<sub>O</sub> = 1 V with V<sub>DD</sub> = 3 V or V<sub>O</sub> = 1.4 V with V<sub>DD</sub> = 5 V.



# TLV2352, TLV2352Y

## LinCMOS™ DUAL LOW-VOLTAGE DIFFERENTIAL COMPARATORS

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### electrical characteristics at specified free-air temperature†

PARAMETER	TEST CONDITIONS	T <sub>A</sub> ‡	TLV2352M						UNIT
			V <sub>DD</sub> = 3 V			V <sub>DD</sub> = 5 V			
			MIN	TYP	MAX	MIN	TYP	MAX	
V <sub>IO</sub> Input offset voltage	V <sub>IC</sub> = V <sub>ICRmin</sub> , See Note 4	25°C	1		5	1		5	mV
		Full range				10			
I <sub>IO</sub> Input offset current		25°C	1			1			pA
		125°C				10			nA
I <sub>IB</sub> Input bias current		25°C	5			5			pA
		125°C				20			nA
V <sub>ICR</sub> Common-mode input voltage range		25°C	0 to 2			0 to 4			V
		Full range	0 to 1.75			0 to 3.75			
I <sub>OH</sub> High-level output current	V <sub>ID</sub> = 1 V	25°C	0.1			0.1			nA
		Full range				1			μA
V <sub>OL</sub> Low-level output voltage	V <sub>ID</sub> = -1 V, I <sub>OL</sub> = 2 mA	25°C	115		300	150		400	mV
		Full range				700			
I <sub>OL</sub> Low-level output current	V <sub>ID</sub> = -1 V, V <sub>OL</sub> = 1.5 V	25°C	6	16		6	16	mA	
I <sub>DD</sub> Supply current	V <sub>ID</sub> = 1 V, No load	25°C	120		250	140		300	μA
		Full range				400			

† All characteristics are measured with zero common-mode input voltages unless otherwise noted.

‡ Full range is -55°C to 125°C. IMPORTANT: See *Parameter Measurement Information*.

NOTE 4: The offset voltage limits given are the maximum values required to drive the output above 4 V with V<sub>DD</sub> = 5 V, 2 V with V<sub>DD</sub> = 3 V, or below 400 mV with a 10-kΩ resistor between the output and V<sub>DD</sub>. They can be verified by applying the limit value to the input and checking for the appropriate output state.

### switching characteristics, V<sub>DD</sub> = 3 V, T<sub>A</sub> = 25°C

PARAMETER	TEST CONDITIONS	TLV2352M			UNIT
		MIN	TYP	MAX	
Response time	R <sub>L</sub> = 5.1 kΩ, C <sub>L</sub> = 100 pF§, See Note 5   100-mV input step with 5-mV overdrive	1400			ns

§ C<sub>L</sub> includes probe and jig capacitance.

NOTE 5: The response time specified is the interval between the input step function and the instant when the output crosses V<sub>O</sub> = 1 V with V<sub>DD</sub> = 3 V or V<sub>O</sub> = 1.4 V with V<sub>DD</sub> = 5 V.

### switching characteristics, V<sub>DD</sub> = 5 V, T<sub>A</sub> = 25°C

PARAMETER	TEST CONDITIONS	TLV2352M			UNIT
		MIN	TYP	MAX	
Response time	R <sub>L</sub> = 5.1 kΩ, C <sub>L</sub> = 100 pF§, See Note 5	100-mV input step with 5-mV overdrive			ns
		TTL-level input step			

§ C<sub>L</sub> includes probe and jig capacitance.

NOTE 5: The response time specified is the interval between the input step function and the instant when the output crosses V<sub>O</sub> = 1 V with V<sub>DD</sub> = 3 V or V<sub>O</sub> = 1.4 V with V<sub>DD</sub> = 5 V.



# TLV2352, TLV2352Y

## LinCMOS™ DUAL LOW-VOLTAGE DIFFERENTIAL COMPARATORS

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### electrical characteristics at specified free-air temperature, $T_A = 25^\circ\text{C}^\dagger$

PARAMETER	TEST CONDITIONS	TLV2352Y						UNIT
		$V_{DD} = 3\text{ V}$			$V_{DD} = 5\text{ V}$			
		MIN	TYP	MAX	MIN	TYP	MAX	
$V_{IO}$ Input offset voltage	$V_{IC} = V_{ICRmin}$ , See Note 4		1	5		1	5	mV
$I_{IO}$ Input offset current			1			1		pA
$I_{IB}$ Input bias current			5			5		pA
$V_{ICR}$ Common-mode input voltage range		0 to 2			0 to 4			V
$I_{OH}$ High-level output current	$V_{ID} = 1\text{ V}$		0.1			0.1		nA
$V_{OL}$ Low-level output voltage	$V_{ID} = -1\text{ V}$ , $I_{OL} = 2\text{ mA}$		115	300		150	400	mV
$I_{OL}$ Low-level output current	$V_{ID} = -1\text{ V}$ , $V_{OL} = 1.5\text{ V}$	6	16		6	16		mA
$I_{DD}$ Supply current	$V_{ID} = 1\text{ V}$ No load		120	250		140	300	$\mu\text{A}$

<sup>†</sup> All characteristics are measured with zero common-mode input voltages unless otherwise noted.

NOTE 4: The offset voltage limits given are the maximum values required to drive the output above 4 V with  $V_{DD} = 5\text{ V}$ , 2 V with  $V_{DD} = 3\text{ V}$ , or below 400 mV with a 10-k $\Omega$  resistor between the output and  $V_{DD}$ . They can be verified by applying the limit value to the input and checking for the appropriate output state.

TYPICAL CHARACTERISTICS

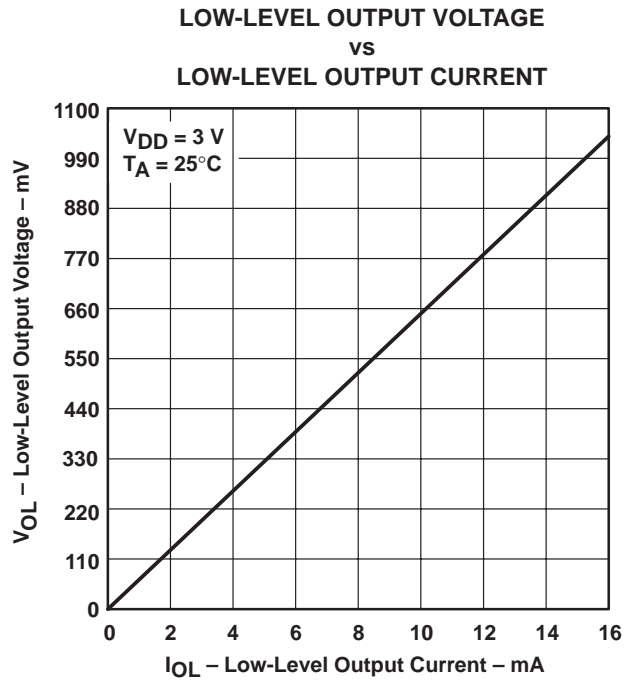


Figure 1

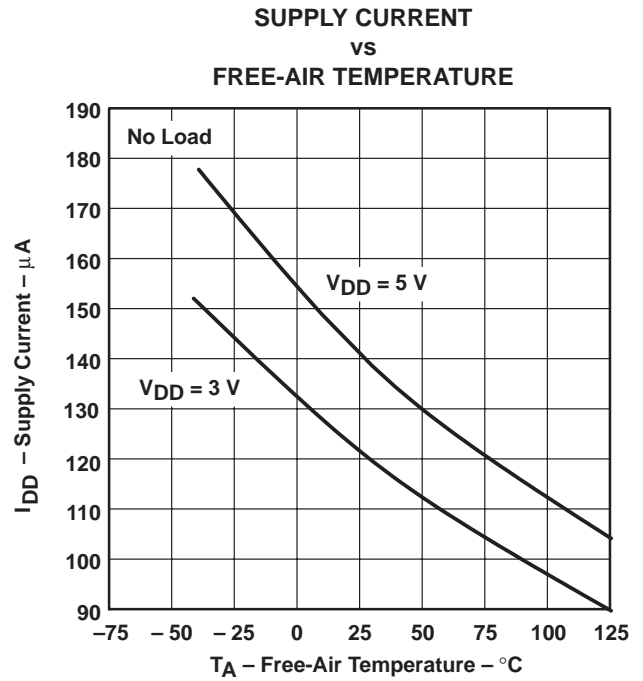


Figure 2

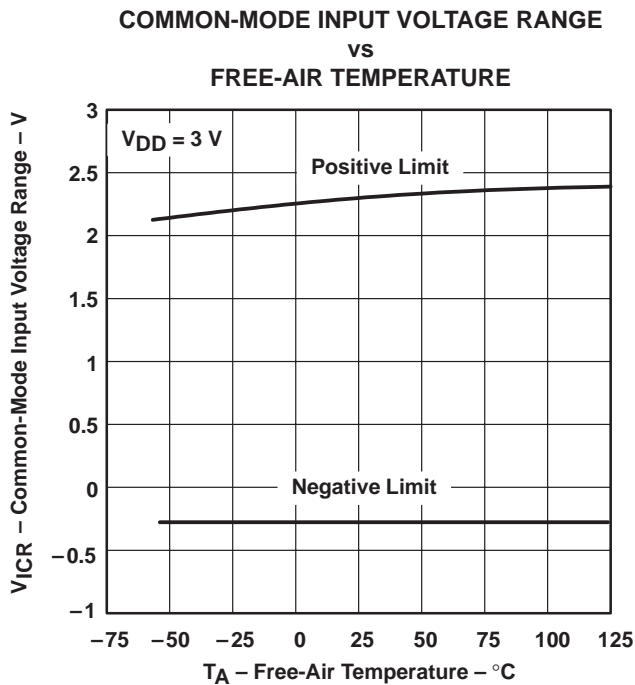


Figure 3

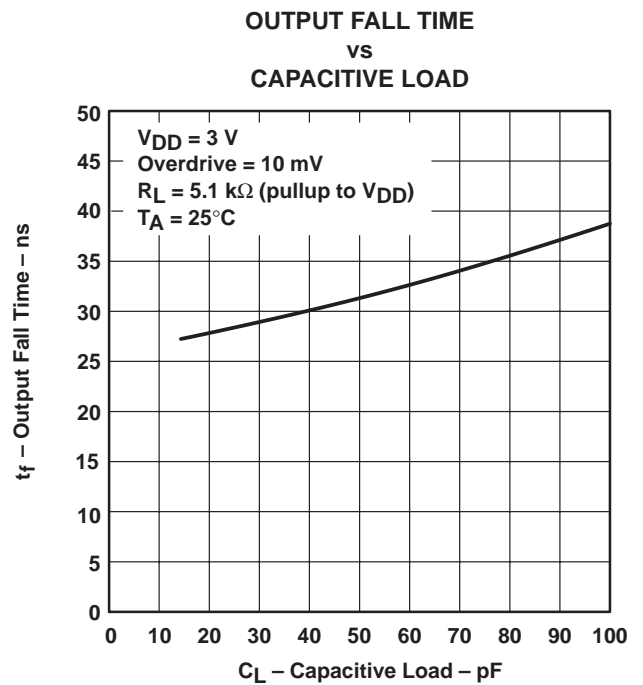


Figure 4

TYPICAL CHARACTERISTICS

HIGH-TO-LOW-LEVEL OUTPUT  
 PROPAGATION DELAY  
 FOR VARIOUS OVERDRIVE VOLTAGES

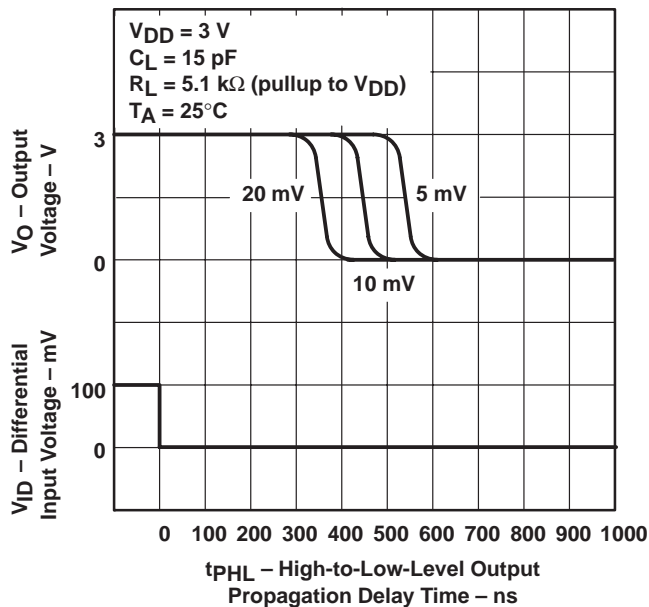


Figure 5

HIGH-TO-LOW-LEVEL OUTPUT  
 PROPAGATION DELAY  
 FOR VARIOUS CAPACITIVE LOADS

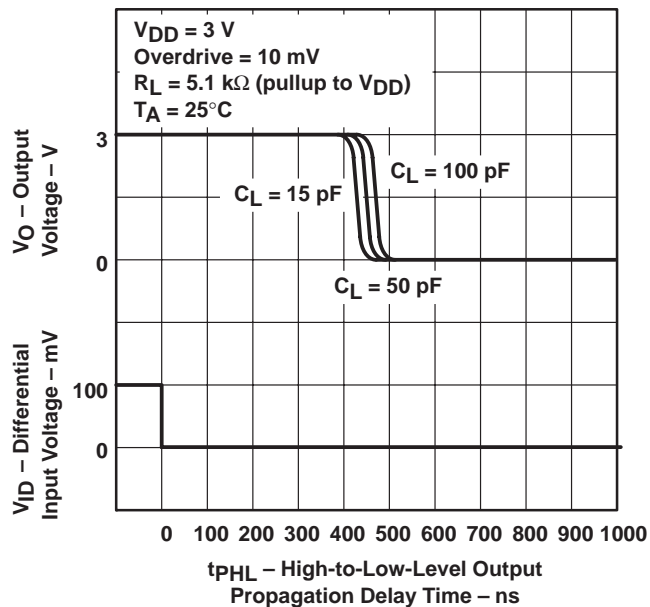


Figure 6

LOW-TO-HIGH-LEVEL OUTPUT  
 PROPAGATION DELAY  
 FOR VARIOUS OVERDRIVE VOLTAGES

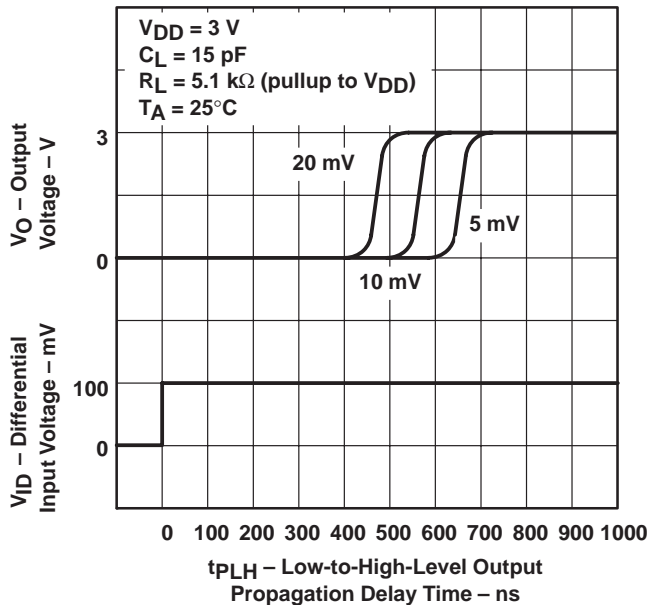


Figure 7

LOW-TO-HIGH-LEVEL OUTPUT  
 PROPAGATION DELAY  
 FOR VARIOUS CAPACITIVE LOADS

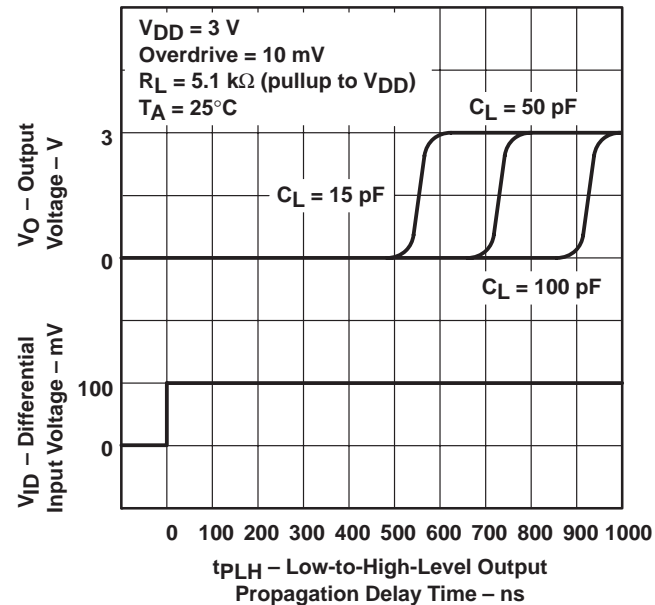


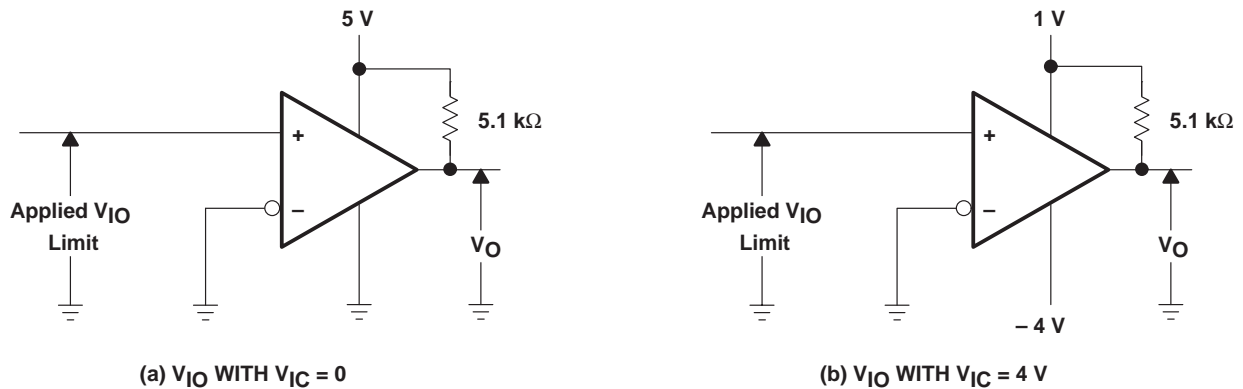
Figure 8

**PARAMETER MEASUREMENT INFORMATION**

The digital output stage of the TLV2352 can be damaged if it is held in the linear region of the transfer curve. Conventional operational amplifier/comparator testing incorporates the use of a servo loop that is designed to force the device output to a level within this linear region. Since the servo-loop method of testing cannot be used, the following alternatives for measuring parameters such as input offset voltage, common-mode rejection, etc., are offered.

To verify that the input offset voltage falls within the limits specified, the limit value is applied to the input as shown in Figure 9(a). With the noninverting input positive with respect to the inverting input, the output should be high. With the input polarity reversed, the output should be low.

A similar test can be made to verify the input offset voltage at the common-mode extremes. The supply voltages can be slewed as shown in Figure 9(b) for the  $V_{ICR}$  test, rather than changing the input voltages to provide greater accuracy.



**Figure 9. Method for Verifying That Input Offset Voltage Is Within Specified Limits**

A close approximation of the input offset voltage can be obtained by using a binary search method to vary the differential input voltage while monitoring the output state. When the applied input voltage differential is equal but opposite in polarity to the input offset voltage, the output changes states.

PARAMETER MEASUREMENT INFORMATION

Figure 10 illustrates a practical circuit for direct dc measurement of input offset voltage that does not bias the comparator in the linear region. The circuit consists of a switching-mode servo loop in which U1a generates a triangular waveform of approximately 20-mV amplitude. U1b acts as a buffer with C2 and R4 removing any residual dc offset. The signal is then applied to the inverting input of the comparator under test while the noninverting input is driven by the output of the integrator formed by U1c through the voltage divider formed by R9 and R10. The loop reaches a stable operating point when the output of the comparator under test has a duty cycle of exactly 50%, which can only occur when the incoming triangle wave is sliced symmetrically or when the voltage at the noninverting input exactly equals the input offset voltage.

Voltage dividers R9 and R10 provide a step up of the input offset voltage by a factor of 100 to make measurement easier. The values of R5, R8, R9, and R10 can significantly influence the accuracy of the reading; therefore, it is suggested that their tolerance level be 1% or lower.

Measuring the extremely low values of input current requires isolation from all other sources of leakage current and compensation for the leakage of the test socket and board. With a good picoammeter, the socket and board leakage can be measured with no device in the socket. Subsequently, this open-socket leakage value can be subtracted from the measurement obtained with a device in the socket to obtain the actual input current of the device.

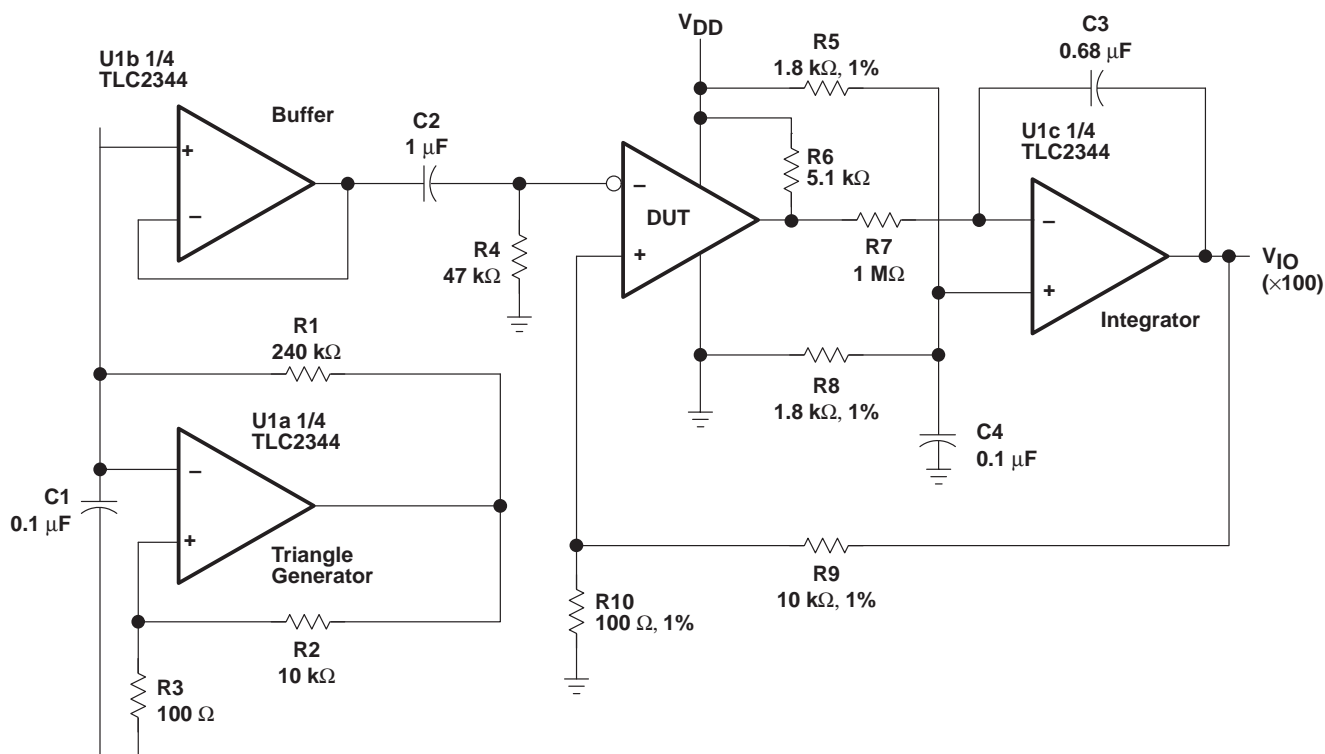
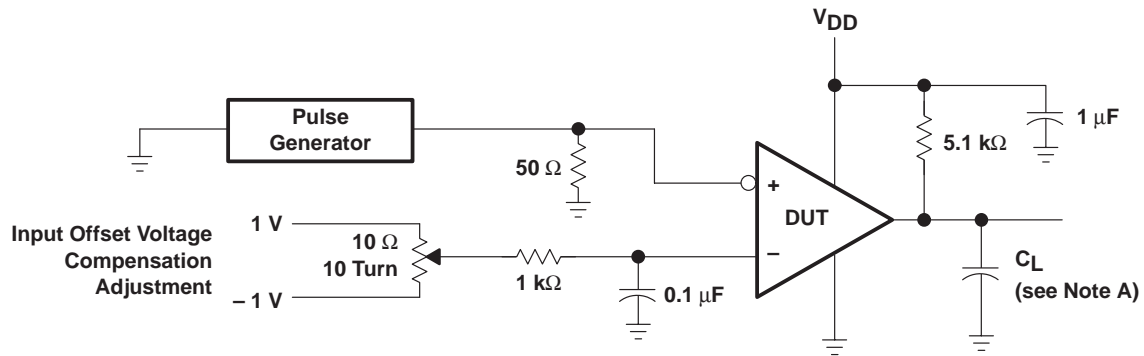


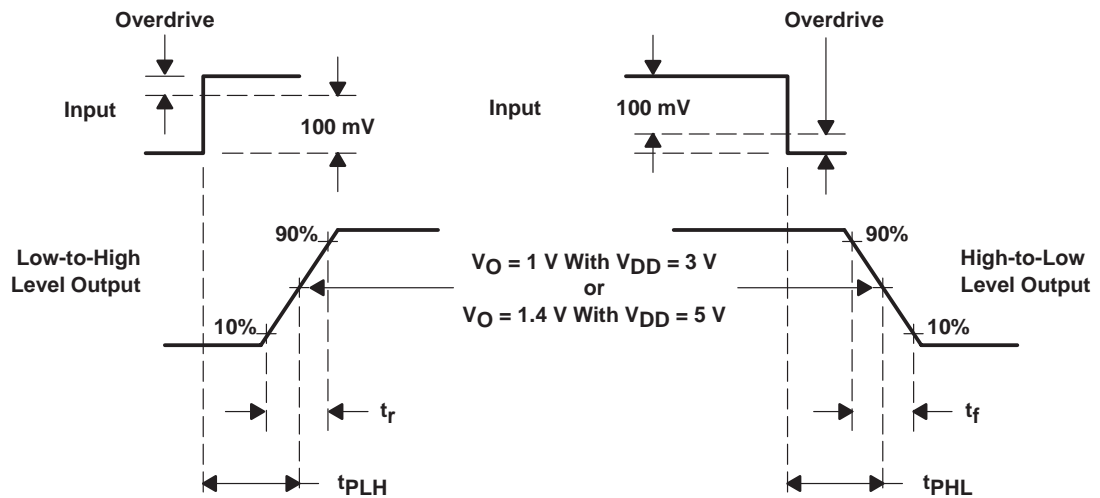
Figure 10. Circuit for Input Offset Voltage Measurement

### PARAMETER MEASUREMENT INFORMATION

Propagation delay time is defined as the interval between the application of an input step function and the instant when the output crosses  $V_O = 1\text{ V}$  with  $V_{DD} = 3\text{ V}$  or when the output crosses  $V_O = 1.4\text{ V}$  with  $V_{DD} = 5\text{ V}$ . Propagation delay time, low-to-high-level output, is measured from the leading edge of the input pulse while propagation delay time, high-to-low-level output, is measured from the trailing edge of the input pulse. Propagation-delay-time measurement at low input signal levels can be greatly affected by the input offset voltage. The offset voltage should be balanced by the adjustment at the inverting input (as shown in Figure 11) so that the circuit is just at the transition point. Then a low signal, for example 105-mV or 5-mV overdrive, causes the output to change states.



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTE A:  $C_L$  includes probe and jig capacitance.

**Figure 11. Propagation Delay, Rise, and Fall Times Test Circuit and Voltage Waveforms**

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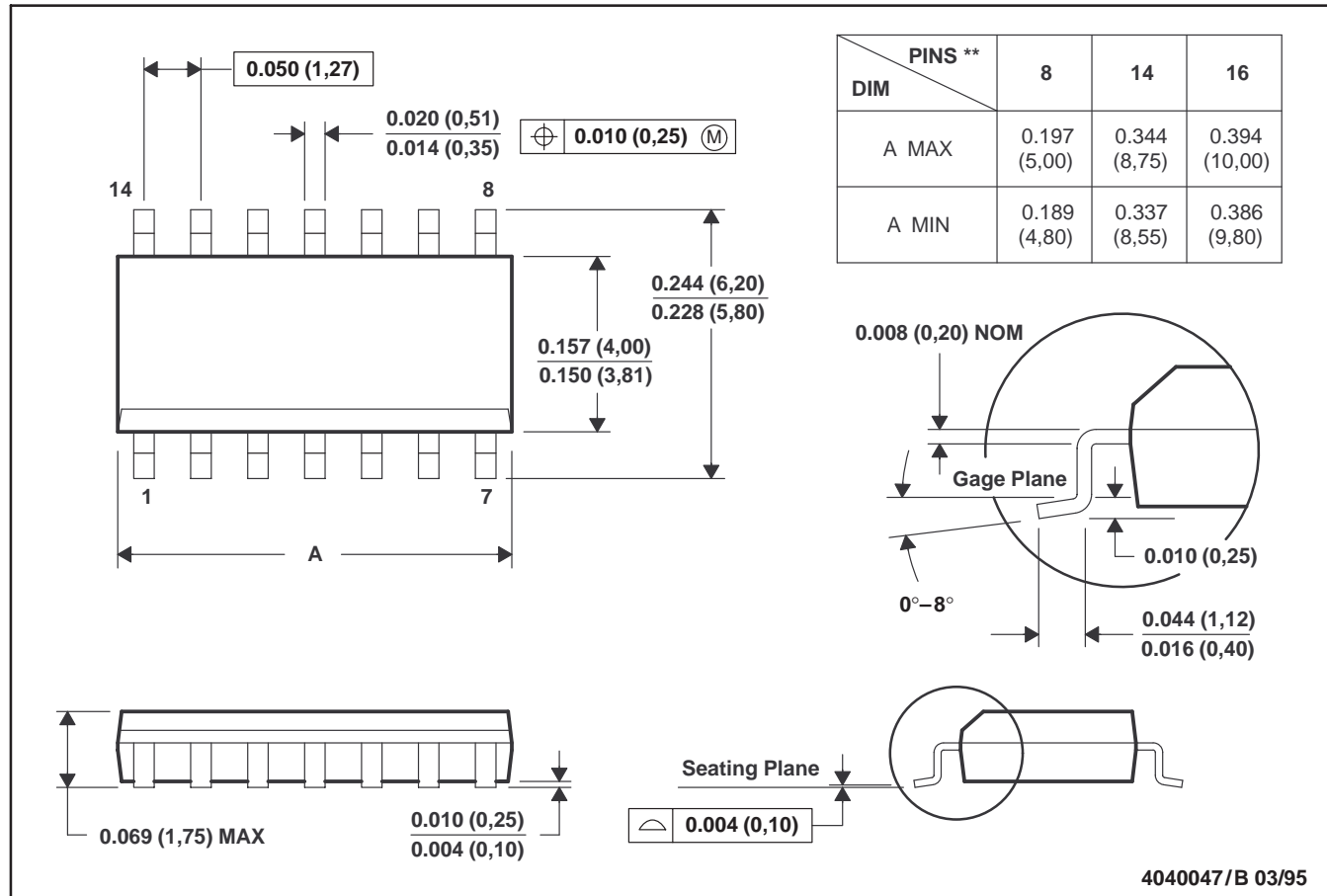
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## MECHANICAL INFORMATION

D (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14 PIN SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
  - D. Four center pins are connected to die mount pad.
  - E. Falls within JEDEC MS-012

# TLV2352, TLV2352Y

## LinCMOS™ DUAL LOW-VOLTAGE DIFFERENTIAL COMPARATORS

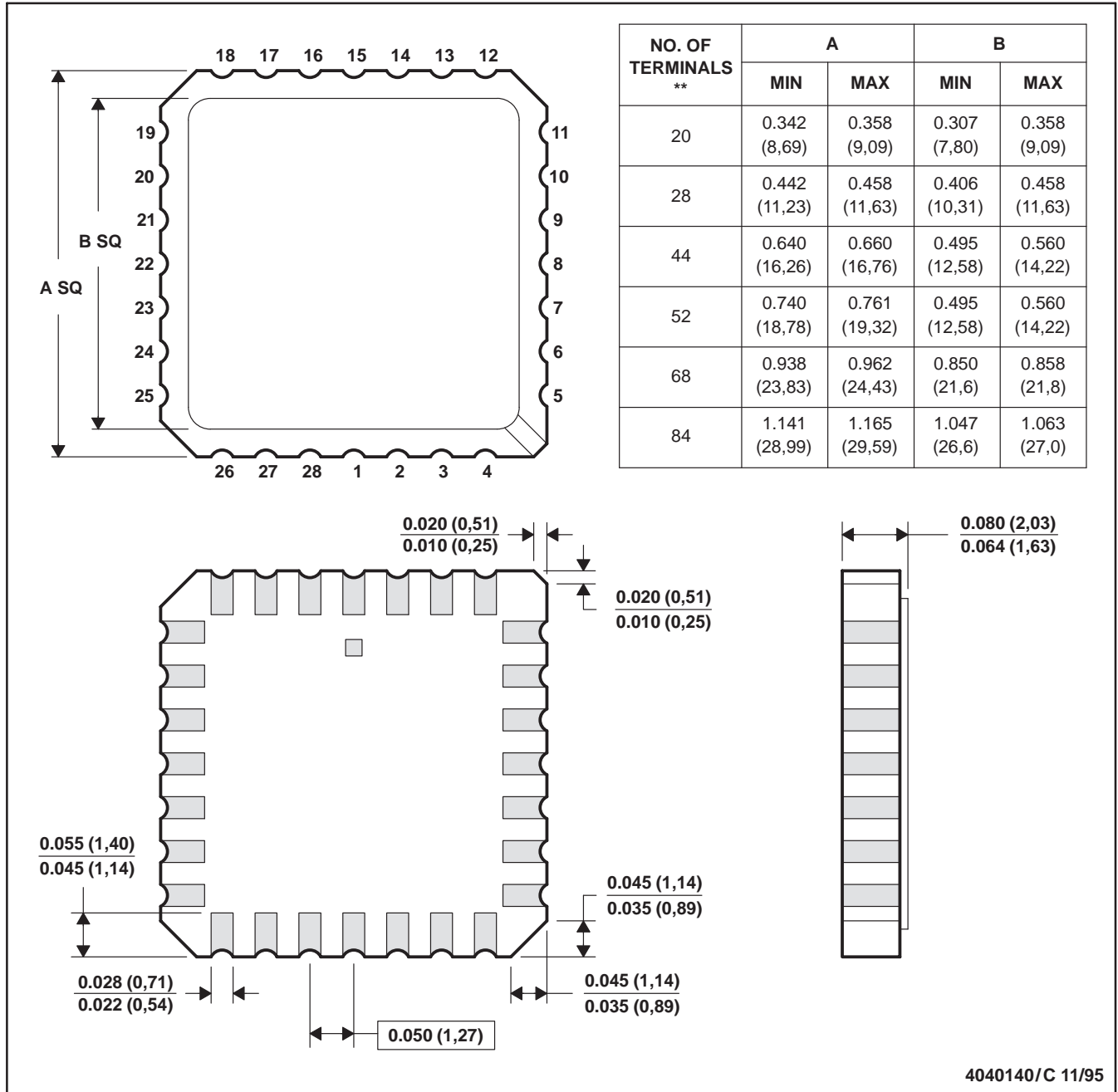
SLCS011B – MAY 1992 – REVISED MARCH 1999

### MECHANICAL INFORMATION

**FK (S-CQCC-N\*\*)**

**LEADLESS CERAMIC CHIP CARRIER**

28 TERMINAL SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a metal lid.
  - D. The terminals are gold plated.
  - E. Falls within JEDEC MS-004

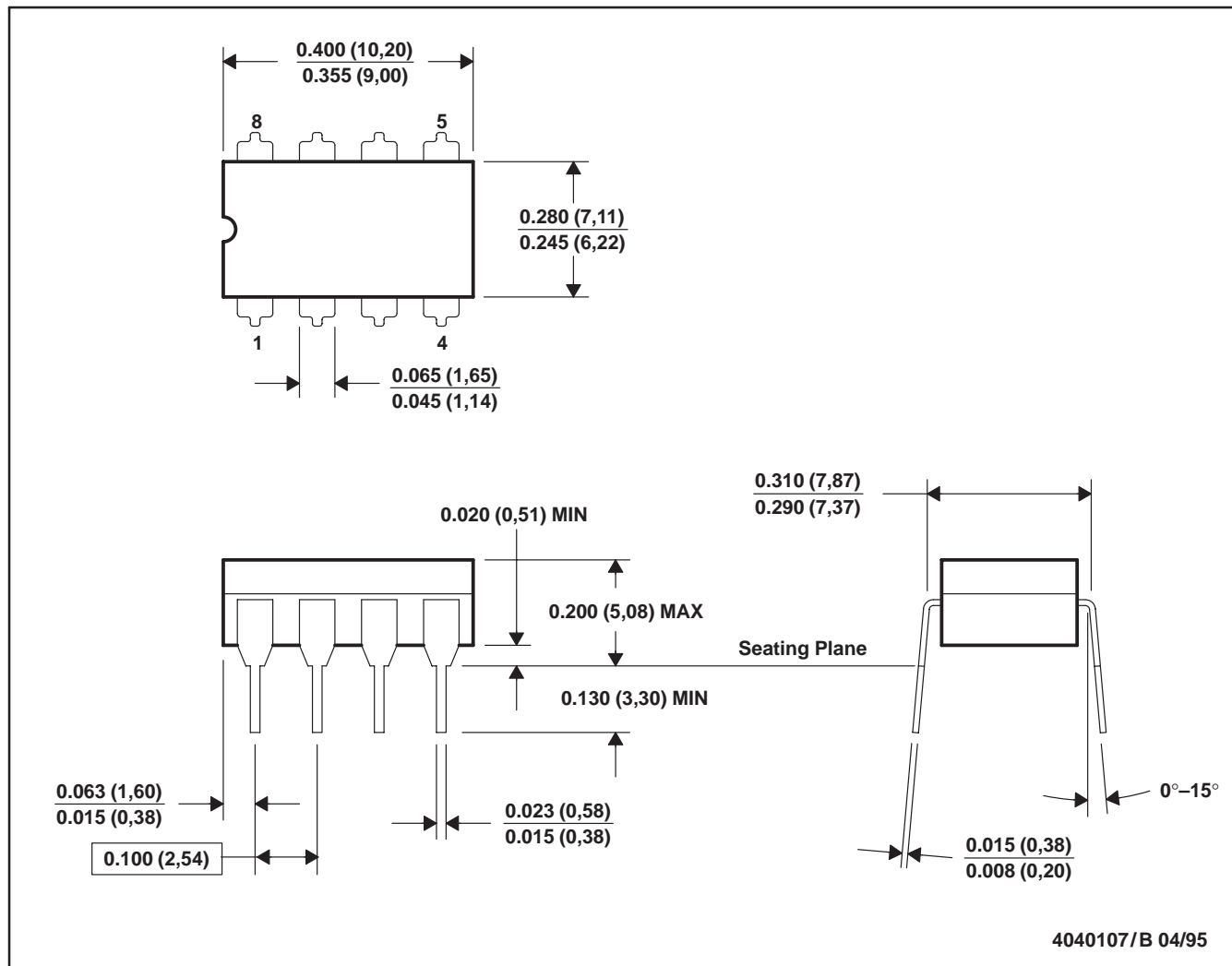
# TLV2352, TLV2352Y LinCMOS™ DUAL LOW-VOLTAGE DIFFERENTIAL COMPARATORS

SLCS011B – MAY 1992 – REVISED MARCH 1999

## MECHANICAL INFORMATION

JG (R-GDIP-T8)

CERAMIC DUAL-IN-LINE PACKAGE

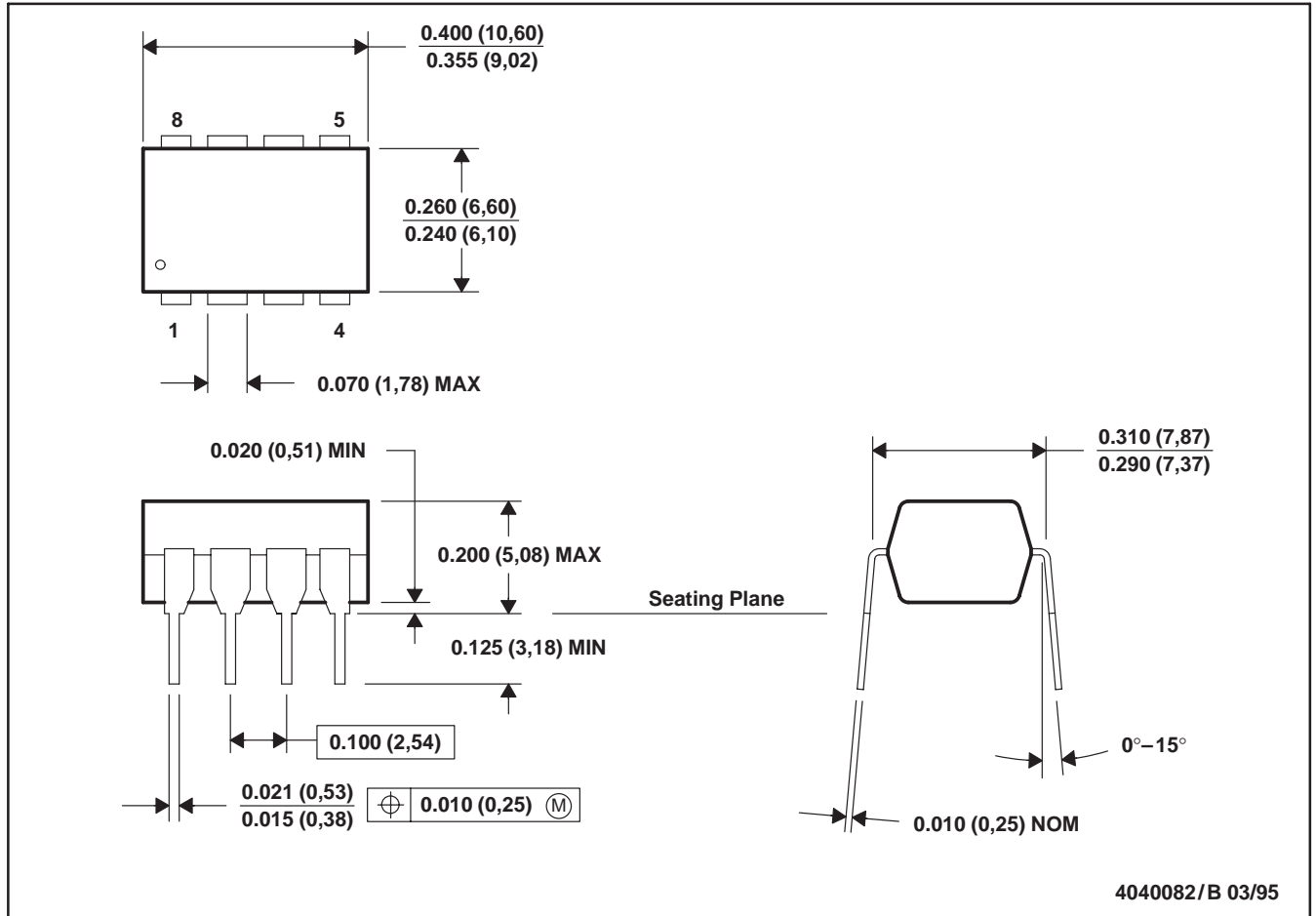


- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. This package can be hermetically sealed with a ceramic lid using glass frit.  
 D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only  
 E. Falls within MIL-STD-1835 GDIP1-T8

MECHANICAL INFORMATION

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Falls within JEDEC MS-001

# TLV2352, TLV2352Y LinCMOS™ DUAL LOW-VOLTAGE DIFFERENTIAL COMPARATORS

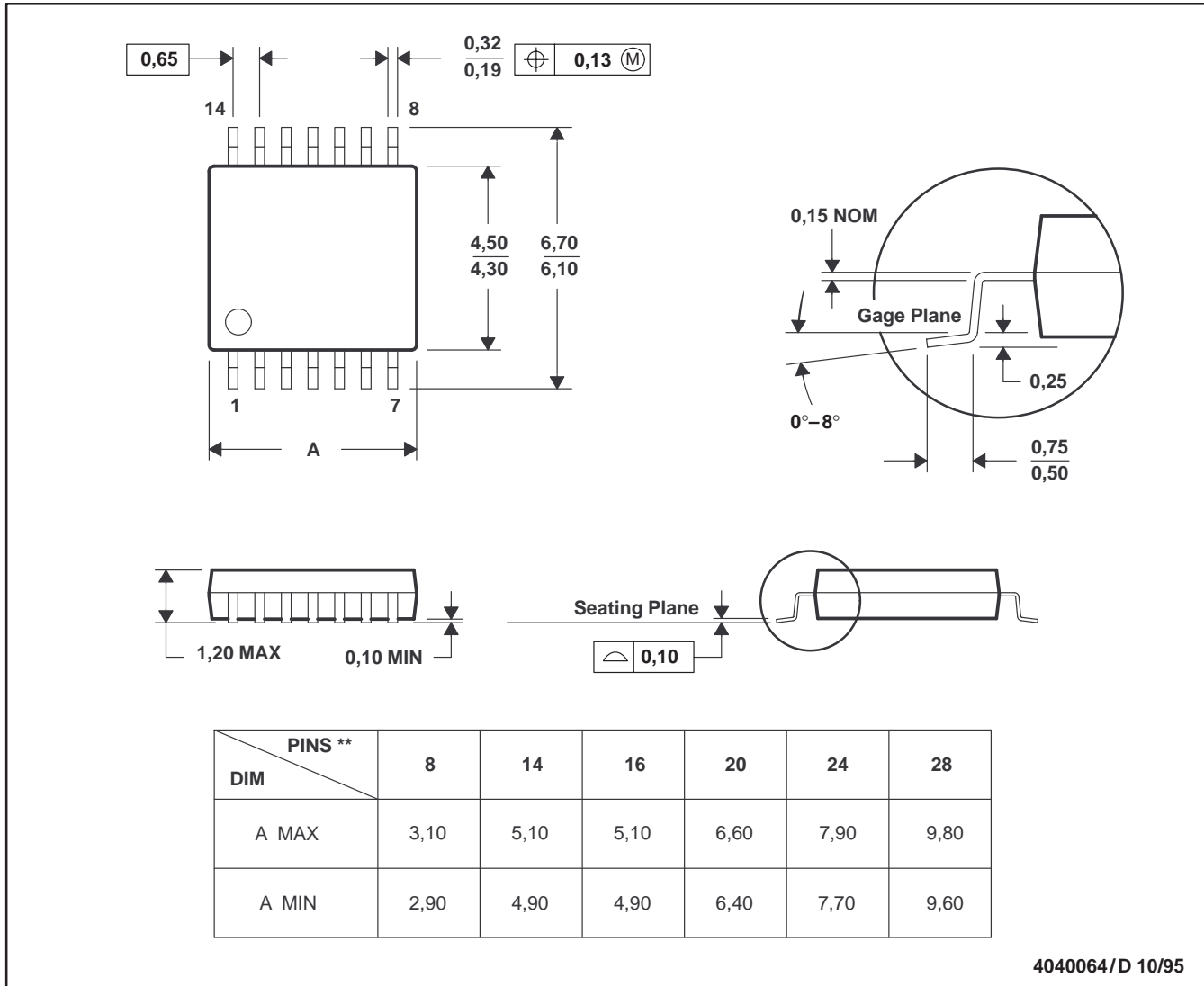
SLCS011B – MAY 1992 – REVISED MARCH 1999

## MECHANICAL INFORMATION

PW (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14 PIN SHOWN



4040064/D 10/95

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

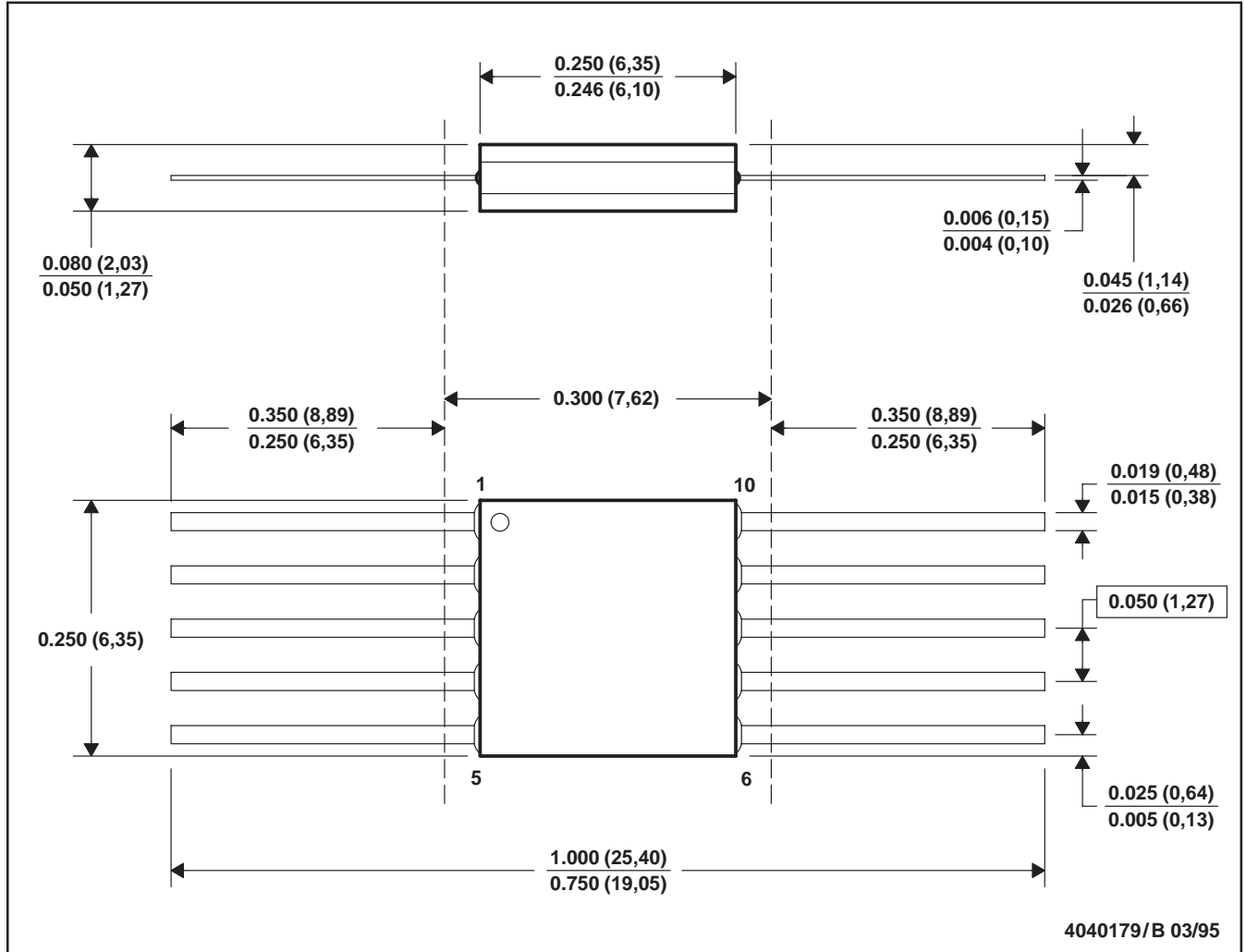
# TLV2352, TLV2352Y LinCMOS™ DUAL LOW-VOLTAGE DIFFERENTIAL COMPARATORS

SLCS011B – MAY 1992 – REVISED MARCH 1999

## MECHANICAL INFORMATION

U (S-GDFP-F10)

CERAMIC DUAL FLATPACK



- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only.
  - Falls within MIL STD 1835 GDFP1-F10 and JEDEC MO-092AA

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9688101Q2A	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI	-55 to 125	5962- 9688101Q2A TLV2352 MFKB	
5962-9688101QHA	OBSOLETE	CFP	U	10		TBD	Call TI	Call TI	-55 to 125	9688101QHA TLV2352M	
5962-9688101QPA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	9688101QPA TLV2352M	<a href="#">Samples</a>
TLV2352ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2352I	<a href="#">Samples</a>
TLV2352IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2352I	<a href="#">Samples</a>
TLV2352IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2352I	<a href="#">Samples</a>
TLV2352IP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	TLV2352IP	<a href="#">Samples</a>
TLV2352IPW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TY2352	<a href="#">Samples</a>
TLV2352IPWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TY2352	<a href="#">Samples</a>
TLV2352IPWLE	OBSOLETE	TSSOP	PW	8		TBD	Call TI	Call TI	-40 to 85		
TLV2352IPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TY2352	<a href="#">Samples</a>
TLV2352IPWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TY2352	<a href="#">Samples</a>
TLV2352MFKB	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI	-55 to 125	5962- 9688101Q2A TLV2352 MFKB	
TLV2352MJG	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	TLV2352MJG	<a href="#">Samples</a>
TLV2352MJGB	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	9688101QPA TLV2352M	<a href="#">Samples</a>
TLV2352MUB	OBSOLETE	CFP	U	10		TBD	Call TI	Call TI	-55 to 125	9688101QHA TLV2352M	

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF TLV2352, TLV2352M :**

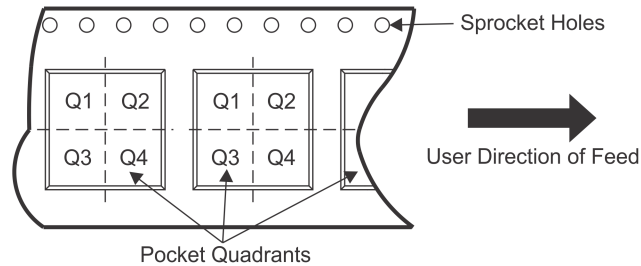
● Catalog: [TLV2352](#)

● Military: [TLV2352M](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV2352IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2352IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV2352IDR	SOIC	D	8	2500	340.5	338.1	20.6
TLV2352IPWR	TSSOP	PW	8	2000	367.0	367.0	35.0

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