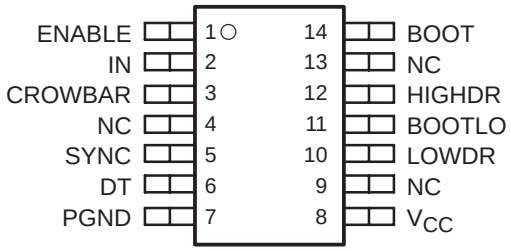
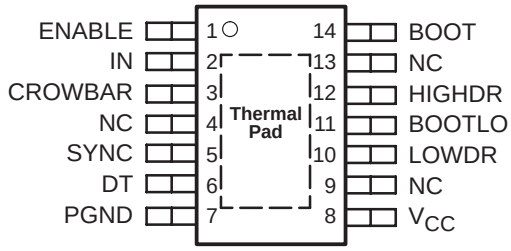
- **Floating Bootstrap or Ground-Reference High-Side Driver**
- **Adaptive Dead-Time Control**
- **50-ns Max Rise/Fall Times With 3.3-nF Load**
- **2.4-A Typical Output Current**
- **4.5-V to 15-V Supply Voltage Range**
- **TTL-Compatible Inputs**
- **Internal Schottky Bootstrap Diode**
- **SYNC Control for Synchronous or Nonsynchronous Operation**
- **CROWBAR for OVP, Protects Against Faulted High-Side Power FETs**
- **Low Supply Current....3 mA Typical**
- **Ideal for High-Current Single or Multiphase Power Supplies**
- **−40°C to 125°C Operating Virtual Junction Temperature Range**
- **Available in SOIC and TSSOP PowerPAD Packages**

D PACKAGE
(TOP VIEW)



PWP PACKAGE
(TOP VIEW)



NC − No internal connection

description

The TPS2834 and TPS2835 are MOSFET drivers for synchronous-buck power stages. These devices are ideal for designing a high-performance power supply using switching controllers that do not include on-chip MOSFET drivers. The drivers are designed to deliver minimum 2-A peak currents into large capacitive loads. The high-side driver can be configured as ground-reference or as floating-bootstrap. An adaptive dead-time control circuit eliminates shoot-through currents through the main power FETs during switching transitions, and provides high efficiency for the buck regulator. The TPS2834 and TPS2835 have additional control functions: ENABLE, SYNC, and CROWBAR. Both high-side and low-side drivers are off when ENABLE is low. The driver is configured as a nonsynchronous-buck driver disabling the low-side driver when SYNC is low. The CROWBAR function turns on the low-side power FET, overriding the IN signal, for overvoltage protection against faulted high-side power FETs.

The TPS2834 has a noninverting input, while the TPS2835 has an inverting input. These drivers are available in 14-terminal SOIC and thermally enhanced TSSOP PowerPAD™ packages and operate over a junction temperature range of −40°C to 125°C.

Related Synchronous MOSFET Drivers

DEVICE NAME	ADDITIONAL FEATURES	INPUTS	
TPS2830	ENABLE, SYNC, and CROWBAR	CMOS	Noninverted
TPS2831			Inverted
TPS2832	W/O ENABLE, SYNC, and CROWBAR	CMOS	Noninverted
TPS2833			Inverted
TPS2836	W/O ENABLE, SYNC, and CROWBAR	TTL	Noninverted
TPS2837			Inverted

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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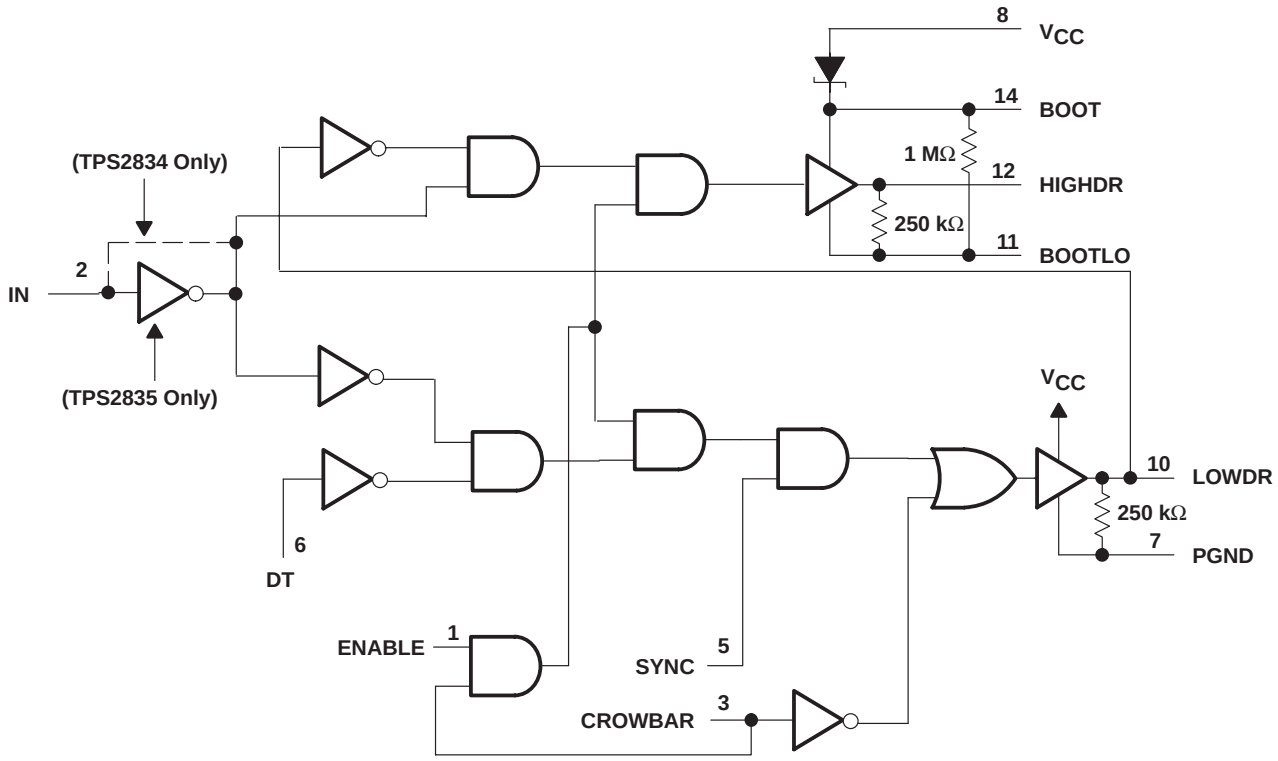
AVAILABLE OPTIONS

T_J	PACKAGED DEVICES	
	SOIC (D)	TSSOP (PWP)
− 40°C to 125°C	TPS2834D TPS2835D	TPS2834PWP TPS2835PWP

The D and PWP packages are available taped and reeled. Add R suffix to device type (e.g., TPS2834DR)

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
BOOT	14	I	Bootstrap terminal. A ceramic capacitor is connected between BOOT and BOOTLO to develop the floating bootstrap voltage for the high-side MOSFET. The capacitor value is typically between 0.1 µF and 1 µF.
BOOTLO	11	O	This terminal connects to the junction of the high-side and low-side MOSFETs.
CROWBAR	3	I	CROWBAR can to be driven by an external OVP circuit to protect against a short across the high-side MOSFET. If CROWBAR is driven low, the low-side driver will be turned on and the high-side driver will be turned off, independent of the status of all other control terminals.
DT	6	I	Dead-time control terminal. Connect DT to the junction of the high-side and low-side MOSFETs.
ENABLE	1	I	If ENABLE is low, both drivers are off.
HIGHDR	12	O	Output drive for the high-side power MOSFET
IN	2	I	Input signal to the MOSFET drivers (noninverting input for the TPS2834; inverting input for the TPS2835).
LOWDR	10	O	Output drive for the low-side power MOSFET
NC	4, 9, 13		No internal connection
PGND	7		Power ground. Connect to the FET power ground.
SYNC	5	I	Synchronous rectifier enable terminal. If SYNC is low, the low-side driver is always off; If SYNC is high, the low-side driver provides gate drive to the low-side MOSFET.
V_{CC}	8	I	Input supply. Recommended that a 1-µF capacitor be connected from V_{CC} to PGND.

detailed description

low-side driver

The low-side driver is designed to drive low $r_{DS(on)}$ N-channel MOSFETs. The current rating of the driver is 2 A, source and sink.

high-side driver

The high-side driver is designed to drive low $r_{DS(on)}$ N-channel MOSFETs. The current rating of the driver is 2 A, source and sink. The high-side driver can be configured as a GND-reference driver or as a floating bootstrap driver. The internal bootstrap diode is a Schottky, for improved drive efficiency. The maximum voltage that can be applied from BOOT to ground is 30 V.

dead-time (DT) control

Dead-time control prevents shoot-through current from flowing through the main power FETs during switching transitions by controlling the turnon times of the MOSFET drivers. The high-side driver is not allowed to turn on until the gate drive voltage to the low-side FET is low, and the low-side driver is not allowed to turn on until the voltage at the junction of the power FETs (Vdrain) is low; the TTL-compatible DT terminal connects to the junction of the power FETs.

ENABLE

The ENABLE terminal enables the drivers. When enable is low, the output drivers are low. ENABLE is a TTL-compatible digital terminal.

IN

The IN terminal is a TTL-compatible digital terminal that is the input control signal for the drivers. The TPS2834 has a noninverting input; the TPS2835 has an inverting input.

detailed description (continued)

SYNC

The SYNC terminal controls whether the drivers operate in synchronous or nonsynchronous mode. In synchronous mode, the low-side FET is operated as a synchronous rectifier. In nonsynchronous mode, the low-side FET is always off. SYNC is a TTL-compatible digital terminal.

CROWBAR

The CROWBAR terminal overrides the normal operation of the driver. When CROWBAR is low, the low-side FET turns on to act as a clamp, protecting the output voltage of the dc/dc converter against overvoltages due to a short across the high-side FET. V_{IN} should be fused to protect the low-side FET. CROWBAR is a TTL-compatible digital terminal.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1)		−0.3 V to 16 V
Input voltage range:	BOOT to PGND (high-side driver ON)	−0.3 V to 30 V
	BOOTLO to PGND	−0.3 V to 16 V
	BOOT to BOOTLO	−0.3 V to 16 V
	ENABLE, SYNC, and CROWBAR	−0.3 V to 16 V
	IN	−0.3 V to 16 V
	DT	−0.3 V to 30 V
Continuous total power dissipation		See Dissipation Rating Table
Operating virtual junction temperature range, T_J		−40°C to 125°C
Storage temperature range, T_{stg}		−65°C to 150°C
Lead temperature soldering 1,6 mm (1/16 inch) from case for 10 seconds		260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Unless otherwise specified, all voltages are with respect to PGND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$	DERATING FACTOR	$T_A = 70°C$	$T_A = 85°C$
PWP with solder‡	2668	26.68 mW/°C	1467	1067
PWP without solder‡	1024	10.24 mW/°C	563	409
D	749	7.49 mW/°C	412	300

JUNCTION-CASE THERMAL RESISTANCE TABLE

PWP	Junction-case thermal resistance	2.07 °C/W

‡ Test Board Conditions:
1. Thickness: 0.062″
2. 3″ × 3″ (for packages <27 mm long)
3. 4″ × 4″ (for packages >27 mm long)
4. 2-oz copper traces located on the top of the board (0.071 mm thick)
5. Copper areas located on the top and bottom of the PCB for soldering
6. Power and ground planes, 1-oz copper (0.036 mm thick)
7. Thermal vias, 0.33 mm diameter, 1.5 mm pitch
8. Thermal isolation of power plane

For more information, refer to TI technical brief literature number SLMA002.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.5		15	V
Input voltage	BOOT to PGND	4.5		28	V

electrical characteristics over recommended operating virtual junction temperature range, V_{CC} = 6.5 V, ENABLE = High, C_L = 3.3 nF (unless otherwise noted)

supply current

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage range			4.5		15	V
V_{CC}	Quiescent current	$V_{(ENABLE)}$ = LOW,	V_{CC} =15 V			100	µA
		$V_{(ENABLE)}$ = HIGH,	V_{CC} =15 V		300	400	µA
		$V_{(ENABLE)}$ = HIGH, $f_{(SWX)}$ = 200 kHz, $C_{(HIGHDR)}$ = 50 pF, See Note 2	V_{CC} =12 V, BOOTLO grounded, $C_{(LOWDR)}$ = 50 pF,		3		mA

NOTE 2: Ensured by design, not production tested.

electrical characteristics over recommended operating virtual junction temperature range, V_{CC} = 6.5 V, ENABLE = High, C_L = 3.3 nF (unless otherwise noted) (continued)

output drivers

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
Peak output current	High-side sink (see Note 3)	Duty cycle < 2%, t_{pw} < 100 µs (see Note 2)	$V_{(BOOT)} - V_{(BOOTLO)}$ = 4.5 V, $V_{(HIGHDR)}$ = 4 V	0.7	1.1		A
			$V_{(BOOT)} - V_{(BOOTLO)}$ = 6.5 V, $V_{(HIGHDR)}$ = 5 V	1.1	1.5		
			$V_{(BOOT)} - V_{(BOOTLO)}$ = 12 V, $V_{(HIGHDR)}$ = 10.5 V	2	2.4		
	High-side source (see Note 3)	Duty cycle < 2%, t_{pw} < 100 µs (see Note 2)	$V_{(BOOT)} - V_{(BOOTLO)}$ = 4.5 V, $V_{(HIGHDR)}$ = 0.5V	1.2	1.4		A
			$V_{(BOOT)} - V_{(BOOTLO)}$ = 6.5 V, $V_{(HIGHDR)}$ = 1.5 V	1.3	1.6		
			$V_{(BOOT)} - V_{(BOOTLO)}$ = 12 V, $V_{(HIGHDR)}$ = 1.5 V	2.3	2.7		
	Low-side sink (see Note 3)	Duty cycle < 2%, t_{pw} < 100 µs (see Note 2)	V_{CC} = 4.5 V, $V_{(LOWDR)}$ = 4 V	1.3	1.8		A
			V_{CC} = 6.5 V, $V_{(LOWDR)}$ = 5 V	2	2.5		
			V_{CC} = 12 V, $V_{(LOWDR)}$ = 10.5 V	3	3.5		
	Low-side source (see Note 3)	Duty cycle < 2%, t_{pw} < 100 µs (see Note 2)	V_{CC} = 4.5 V, $V_{LOWDR))}$ = 0.5V	1.4	1.7		A
			V_{CC} = 6.5 V, $V_{(LOWDR))}$ = 1.5 V	2	2.4		
			V_{CC} = 12 V, $V_{(LOWDR0)}$ = 1.5 V	2.5	3		
Output resistance	High-side sink (see Note 3)		$V_{(BOOT)} - V_{(BOOTLO)}$ = 4.5 V, $V_{(HIGHDR)}$= 0.5 V			5	Ω
			$V_{(BOOT)} - V_{(BOOTLO)}$ = 6.5 V, $V_{(HIGHDR)}$ = 0.5 V			5	
			$V_{(BOOT)} - V_{(BOOTLO)}$ = 12 V, $V_{(HIGHDR)}$ = 0.5 V			5	
	High-side source (see Note 3)		$V_{(BOOT)} - V_{(BOOTLO)}$ = 4.5 V, $V_{(HIGHDR)}$ = 4 V			75	Ω
			$V_{(BOOT)} - V_{(BOOTLO)}$ = 6.5 V, $V_{(HIGHDR)}$= 6 V			75	
			$V_{(BOOT)} - V_{(BOOTLO)}$ = 12 V, $V_{(HIGHDR)}$ =11.5 V			75	
	Low-side sink (see Note 3)		$V_{(DRV)}$ = 4.5 V, $V_{(LOWDR)}$= 0.5 V			9	Ω
			$V_{(DRV)}$ = 6.5 V, $V_{(LOWDR)}$ = 0.5 V			7.5	
			$V_{(DRV)}$ = 12 V, $V_{(LOWDR)}$ = 0.5 V			6	
	Low-side source (see Note 3)		$V_{(DRV)}$ = 4.5 V, $V_{(LOWDR)}$ = 4 V			75	Ω
			$V_{(DRV)}$ = 6.5 V, $V_{(LOWDR)}$= 6 V			75	
			$V_{(DRV)}$ = 12 V, $V_{(LOWDR)}$ = 11.5 V			75	

NOTES: 2: Ensured by design, not production tested.
3. The pullup/pulldown circuits of the drivers are bipolar and MOSFET transistors in parallel. The peak output current rating is the combined current from the bipolar and MOSFET transistors. The output resistance is the $r_{DS(on)}$ of the MOSFET transistor when the voltage on the driver output is less than the saturation voltage of the bipolar transistor.

electrical characteristics over recommended operating virtual junction temperature range, V_{CC} = 6.5 V, ENABLE = High, C_L = 3.3 nF (unless otherwise noted) (continued)

dead-time control

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage	LOWDR	Over the V_{CC} range (see Note 2)	$0.7V_{CC}$			V
V_{IL}	Low-level input voltage					1	
V_{IH}	High-level input voltage	DT	Over the V_{CC} range	2			V
V_{IL}	Low-level input voltage					1	V

NOTE 2: Ensured by design, not production tested.

digital control terminals (IN, CROWBAR, SYNC, ENABLE)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage	Over the V_{CC} range	2			V
V_{IL}	Low-level input voltage				1	V

switching characteristics over recommended operating virtual junction temperature range, ENABLE = High, C_L = 3.3 nF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Rise time	HIGHDR output (see Note 2)	$V_{(BOOT)}$ = 4.5 V, $V_{(BOOTLO)}$ = 0 V			60	ns
		$V_{(BOOT)}$ = 6.5 V, $V_{(BOOTLO)}$ = 0 V			50	
		$V_{(BOOT)}$ = 12 V, $V_{(BOOTLO)}$ = 0 V			50	
	LOWDR output (see Note 2)	V_{CC} = 4.5 V			40	ns
		V_{CC} = 6.5 V			30	
		V_{CC} = 12 V			30	
Fall time	HIGHDR output (see Note 2)	$V_{(BOOT)}$ = 4.5 V, $V_{(BOOTLO)}$ = 0 V			50	ns
		$V_{(BOOT)}$ = 6.5 V, $V_{(BOOTLO)}$ = 0 V			40	
		$V_{(BOOT)}$ = 12 V, $V_{(BOOTLO)}$ = 0 V			40	
	LOWDR output (see Note 2)	V_{CC} = 4.5 V			40	ns
		V_{CC} = 6.5 V			30	
		V_{CC} = 12 V			30	
Propagation delay time	HIGHDR going low (excluding dead time) (see Note 2)	$V_{(BOOT)}$ = 4.5 V, $V_{(BOOTLO)}$ = 0 V			95	ns
		$V_{(BOOT)}$ = 6.5 V, $V_{(BOOTLO)}$ = 0 V			80	
		$V_{(BOOT)}$ = 12 V, $V_{(BOOTLO)}$ = 0 V			70	
	LOWDR going high (excluding dead time) (see Note 2)	$V_{(BOOT)}$ = 4.5 V, $V_{(BOOTLO)}$ = 0 V			80	ns
		$V_{(BOOT)}$ = 6.5 V, $V_{(BOOTLO)}$ = 0 V			70	
		$V_{(BOOT)}$ = 12 V, $V_{(BOOTLO)}$ = 0 V			60	
Propagation delay time	LOWDR going low (excluding dead time) (see Note 2)	V_{CC} = 4.5 V			80	ns
		V_{CC} = 6.5 V			70	
		V_{CC} = 12 V			60	
Driver nonoverlap time	DT to LOWDR and LOWDR to HIGHDR (see Note 2)	V_{CC} = 4.5 V	40		170	ns
		V_{CC} = 6.5 V	25		135	
		V_{CC} = 12 V	15		85	

NOTE 2: Ensured by design, not production tested.

TYPICAL CHARACTERISTICS

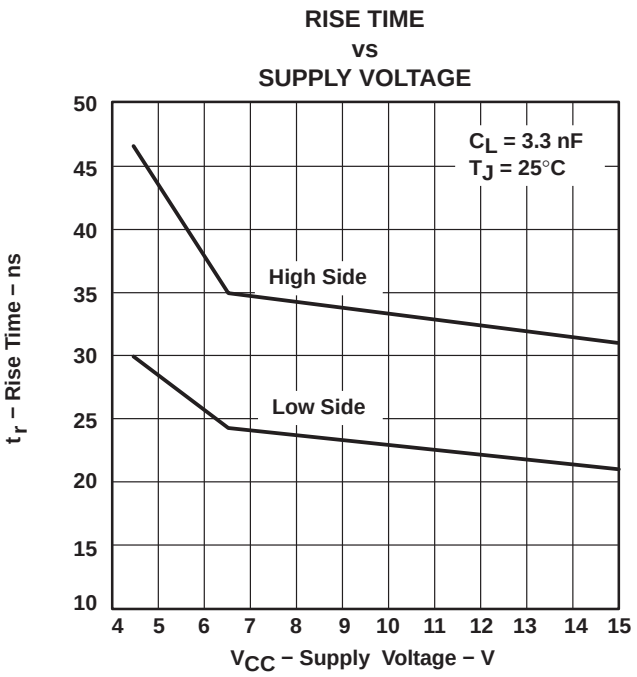


Figure 1

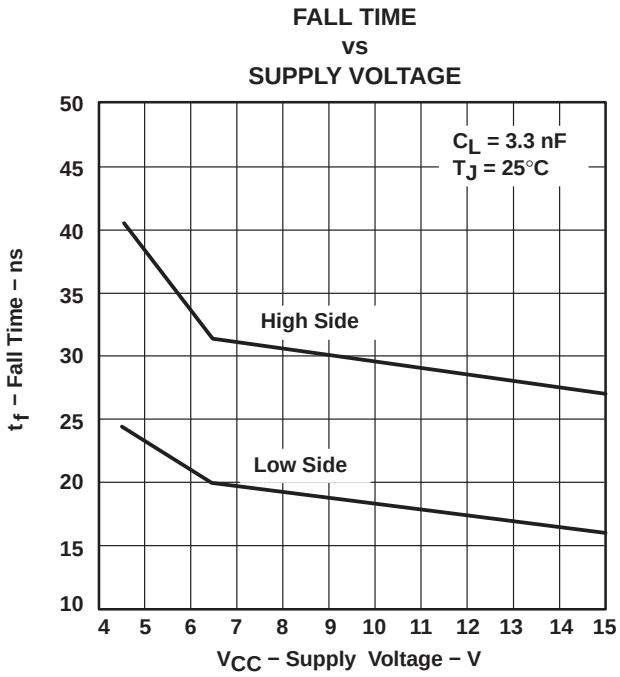


Figure 2

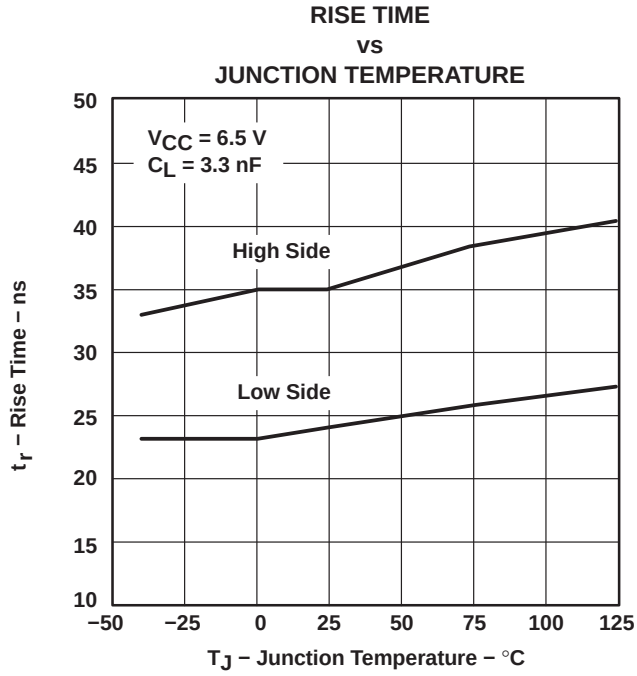


Figure 3

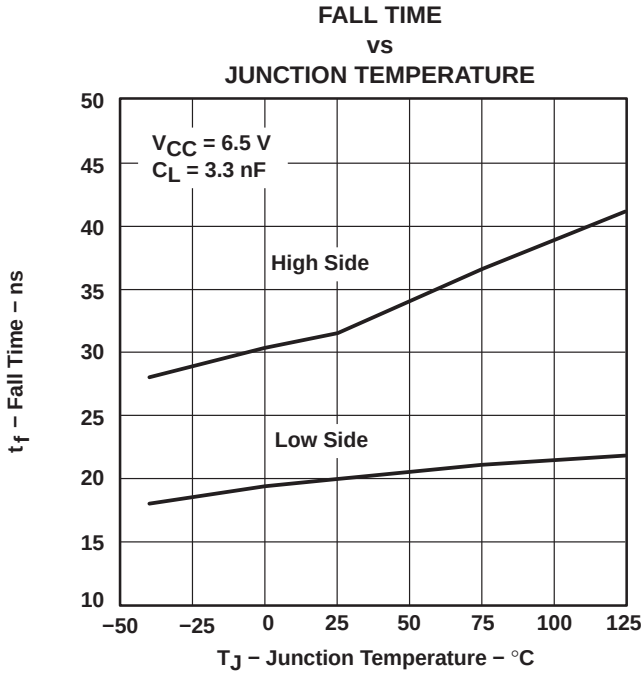
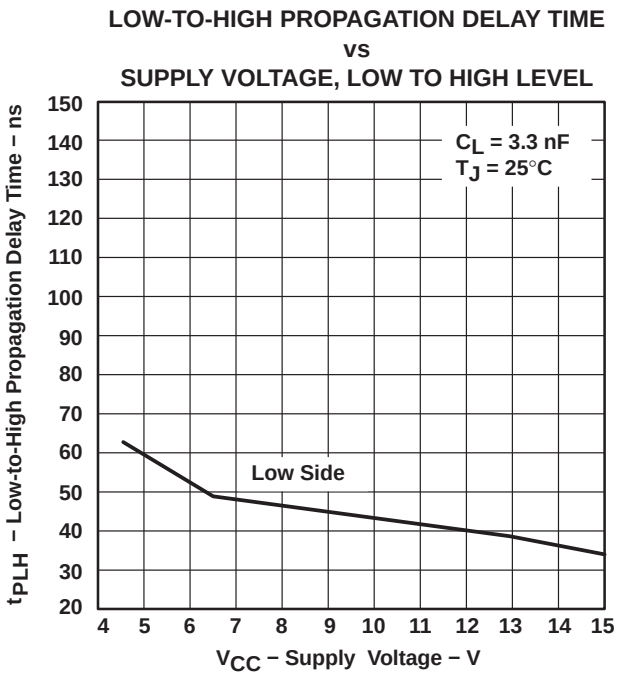


Figure 4

TYPICAL CHARACTERISTICS



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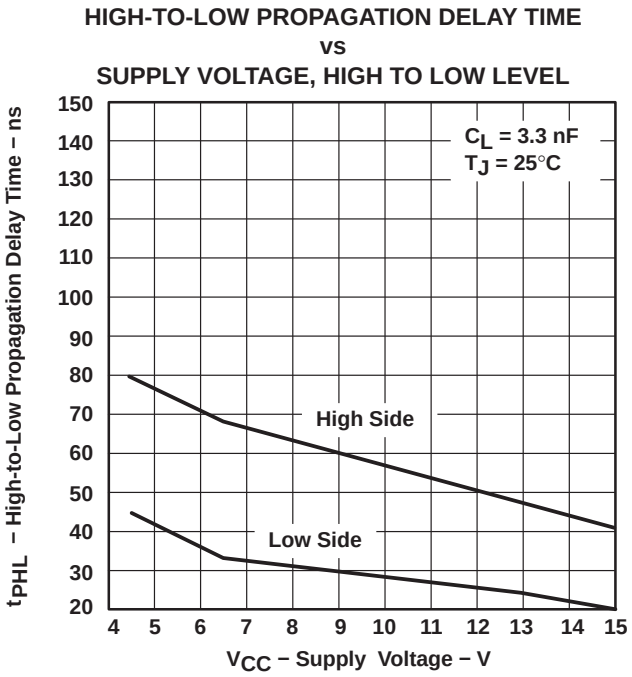

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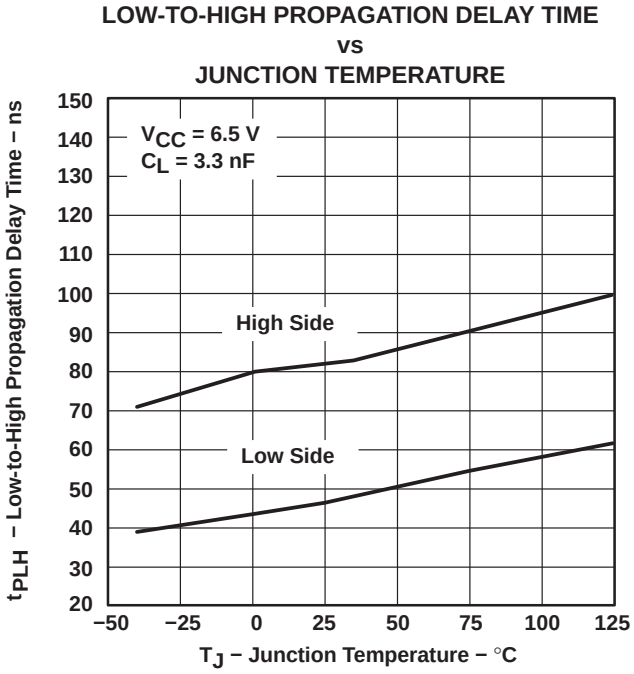

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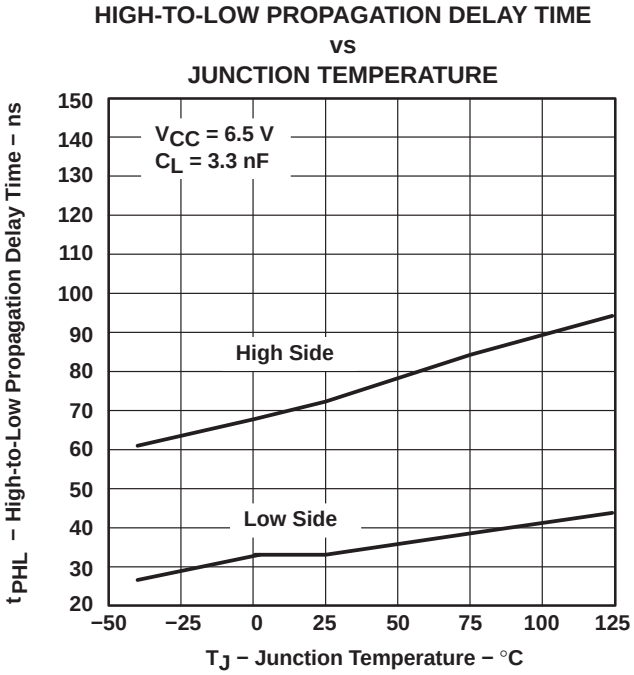

Figure 8

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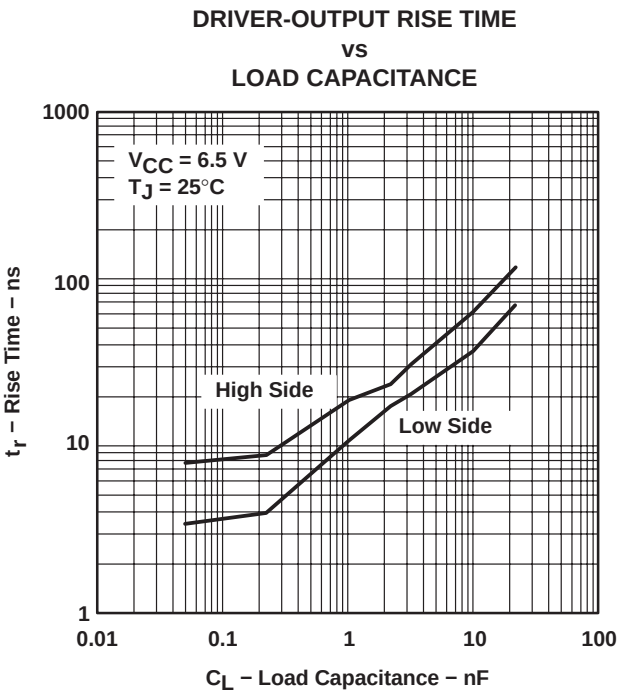

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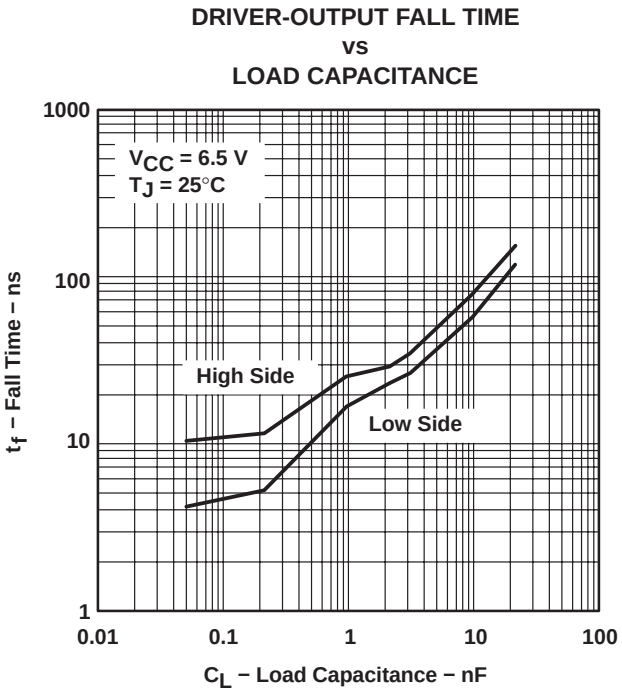

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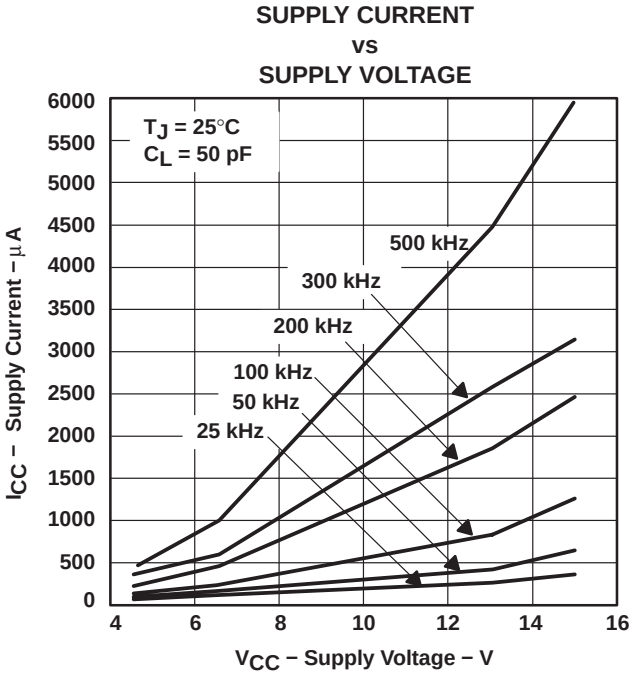


Figure 11

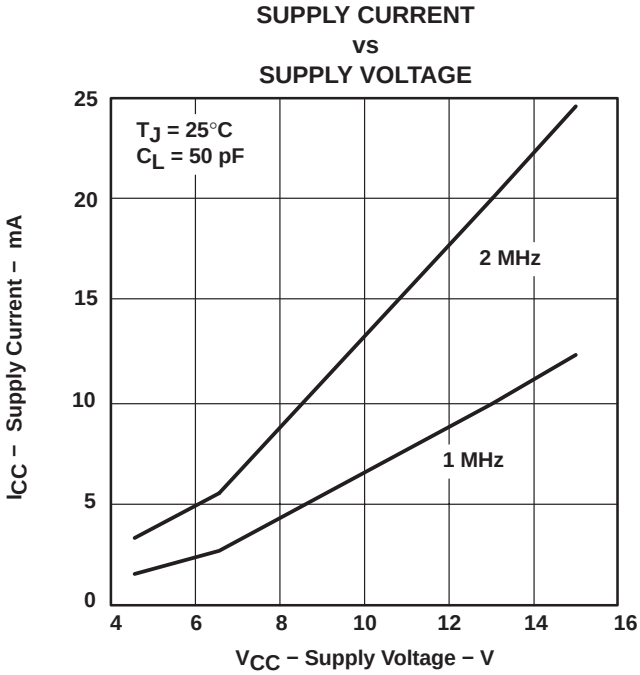
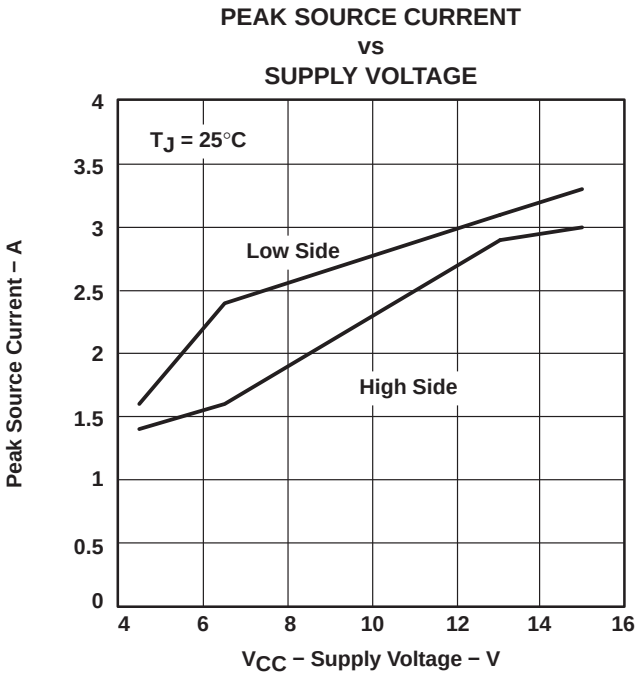


Figure 12

TYPICAL CHARACTERISTICS



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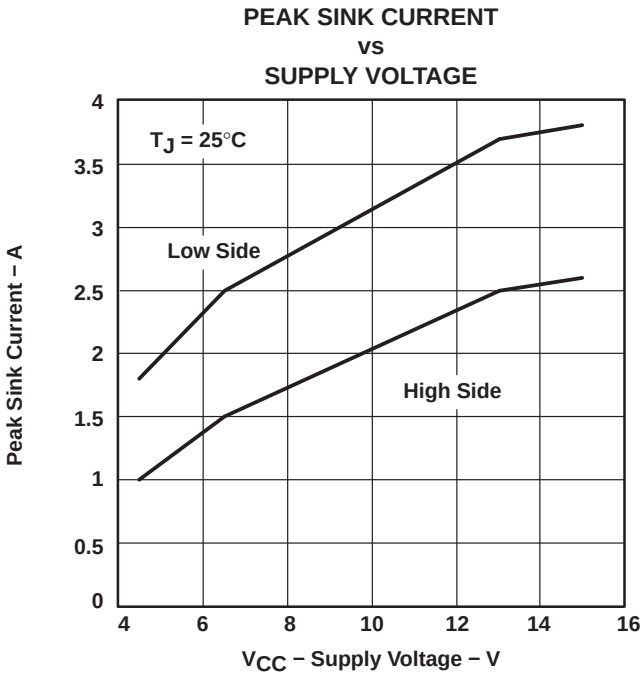

Figure 14

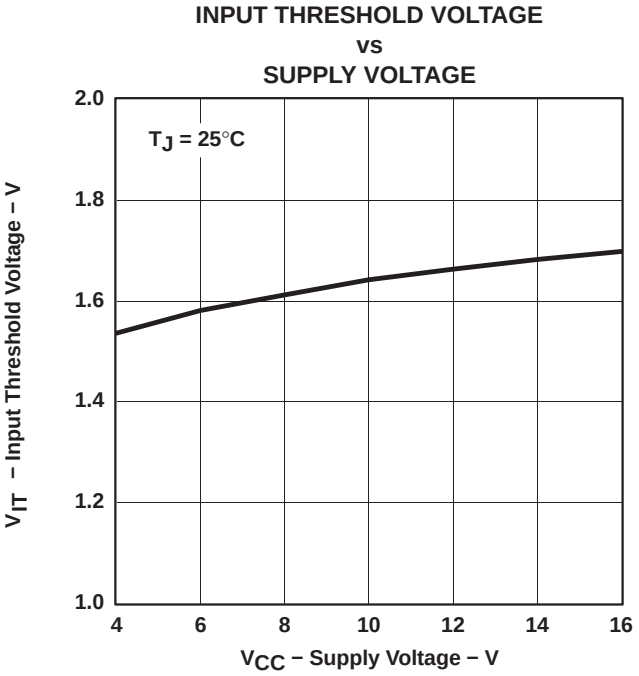

Figure 15

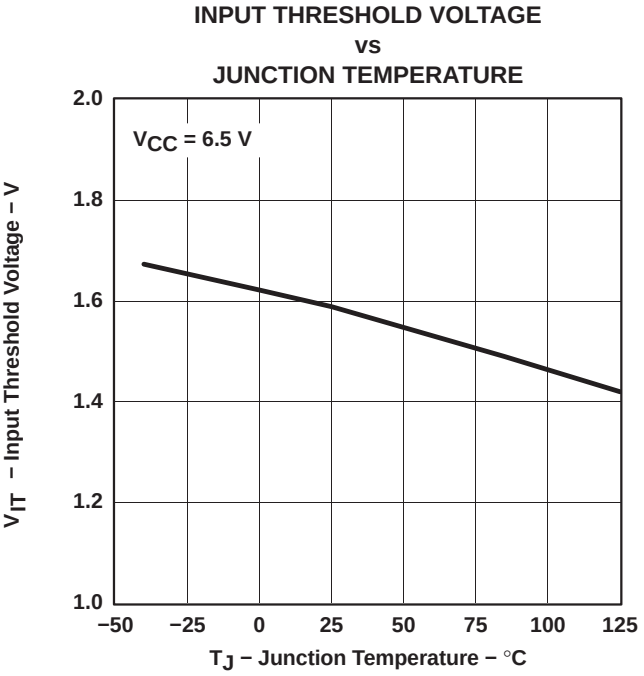

Figure 16

APPLICATION INFORMATION

Figure 17 shows the circuit schematic of a 100-kHz synchronous-buck converter implemented with a TL5001A pulse-width-modulation (PWM) controller and a TPS2835 driver. The converter operates over an input range from 4.5 V to 12 V and has a 3.3-V output. The circuit can supply 3 A continuous load. The converter achieves an efficiency of 94% for V_{IN} = 5 V, I_{load}=1 A, and 93% for V_{IN} = 5 V, I_{load} = 3 A.

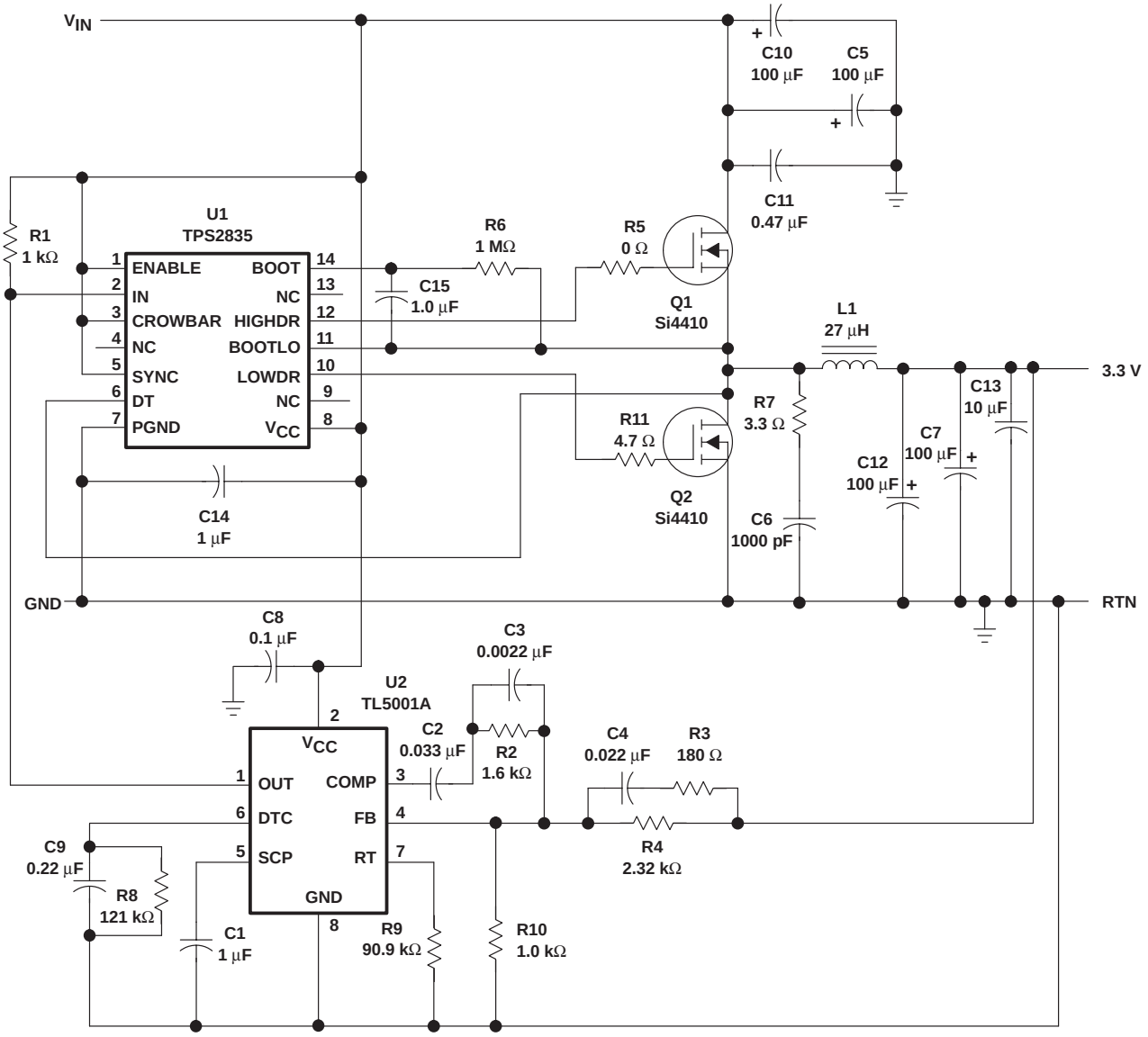

Figure 17. 3.3-V 3-A Synchronous-Buck Converter Circuit

APPLICATION INFORMATION

Great care should be taken when laying out the PC board. The power-processing section is the most critical and will generate large amounts of EMI if not properly configured. The junction of Q1, Q2, and L1 should be very tight. The connection from Q1 drain to the positive sides of C5, C10, and C11 and the connection from Q2 source to the negative sides of C5, C10, and C11 should be as short as possible. The negative terminals of C7 and C12 should also be connected to Q2 source.

Next, the traces from the MOSFET driver to the power switches should be considered. The BOOTLO signal from the junction of Q1 and Q2 carries the large gate drive current pulses and should be as heavy as the gate drive traces. The bypass capacitor (C14) should be tied directly across V_{CC} and PGND.

The next most sensitive node is the FB node on the controller (terminal 4 on the TL5001A). This node is very sensitive to noise pickup and should be isolated from the high-current power stage and be as short as possible. The ground around the controller and low-level circuitry should be tied to the power ground as the output. If these three areas are properly laid out, the rest of the circuit should not have other EMI problems and the power supply will be relatively free of noise.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS2834D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2834	Samples
TPS2834DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2834	Samples
TPS2834DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2834	Samples
TPS2834PWP	ACTIVE	HTSSOP	PWP	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS2834	Samples
TPS2834PWPR	ACTIVE	HTSSOP	PWP	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS2834	Samples
TPS2835D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	2835	Samples
TPS2835PWP	ACTIVE	HTSSOP	PWP	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS2835	Samples
TPS2835PWPR	OBSOLETE	HTSSOP	PWP	14		TBD	Call TI	Call TI	-40 to 125	TPS2835	
TPS2835PWPRG4	OBSOLETE	HTSSOP	PWP	14		TBD	Call TI	Call TI	-40 to 125		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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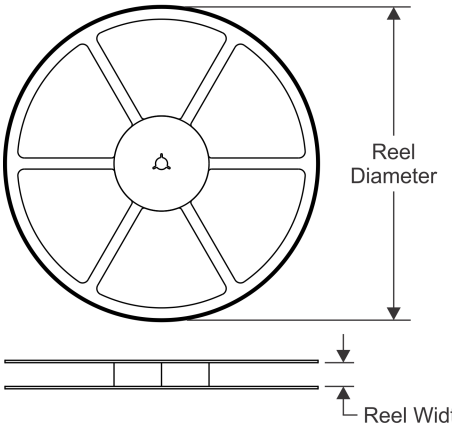
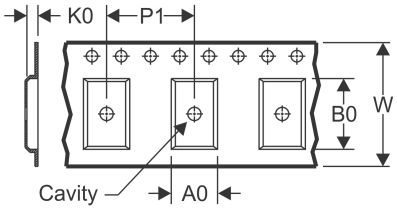
TAPE AND REEL INFORMATION

REEL DIMENSIONS

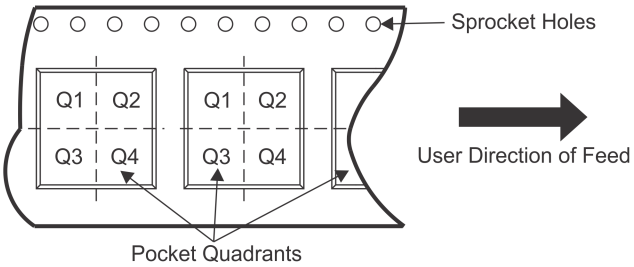


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

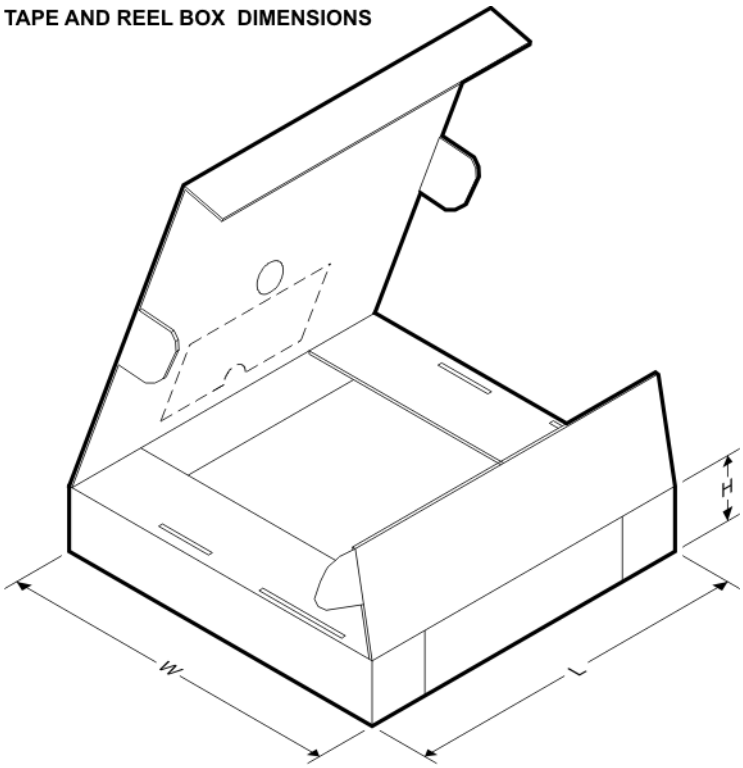
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2834DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TPS2834PWPR	HTSSOP	PWP	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

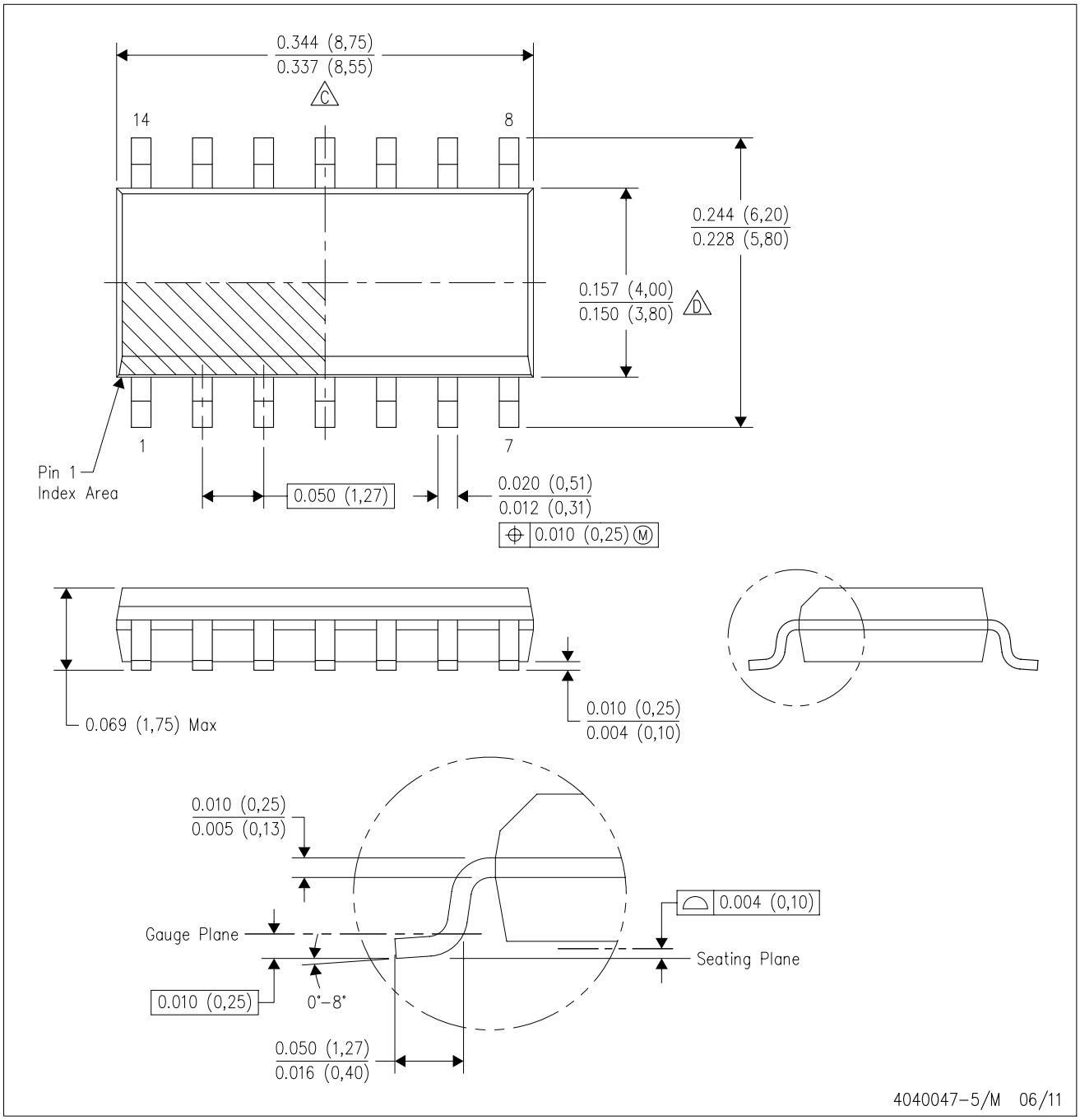
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

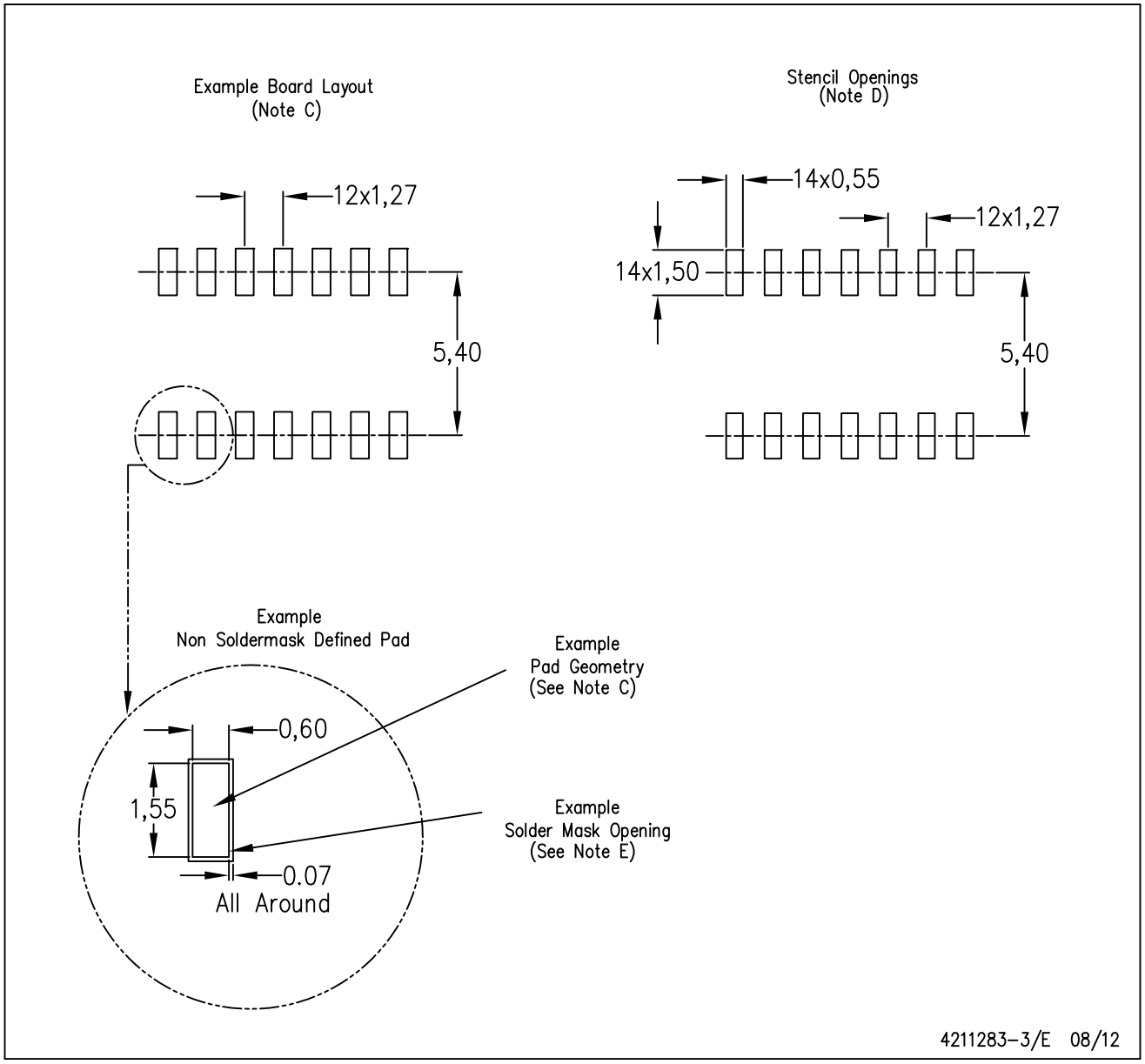
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2834DR	SOIC	D	14	2500	367.0	367.0	38.0
TPS2834PWPR	HTSSOP	PWP	14	2000	367.0	367.0	35.0

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



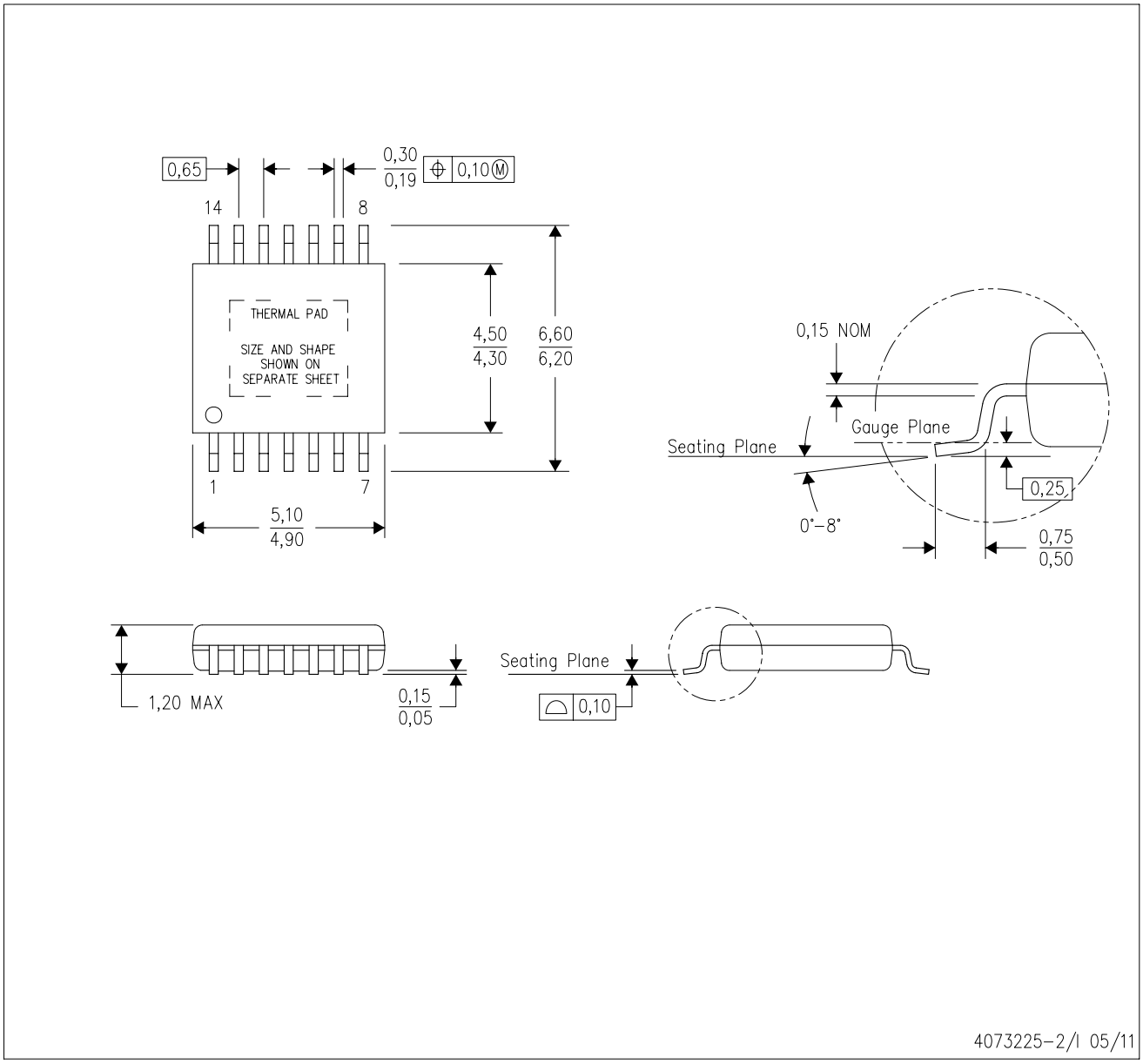
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PWP (R-PDSO-G14) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO-153

PowerPAD is a trademark of Texas Instruments.

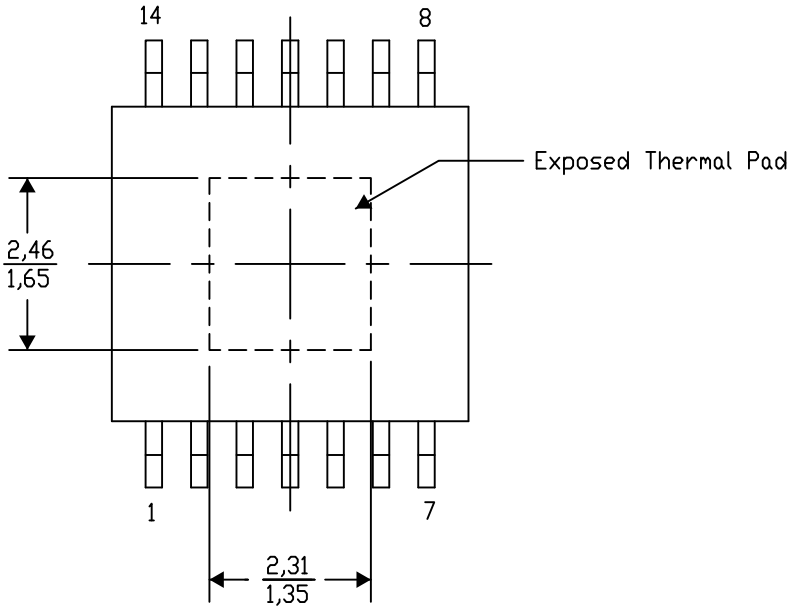
PWP (R-PDSO-G14) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

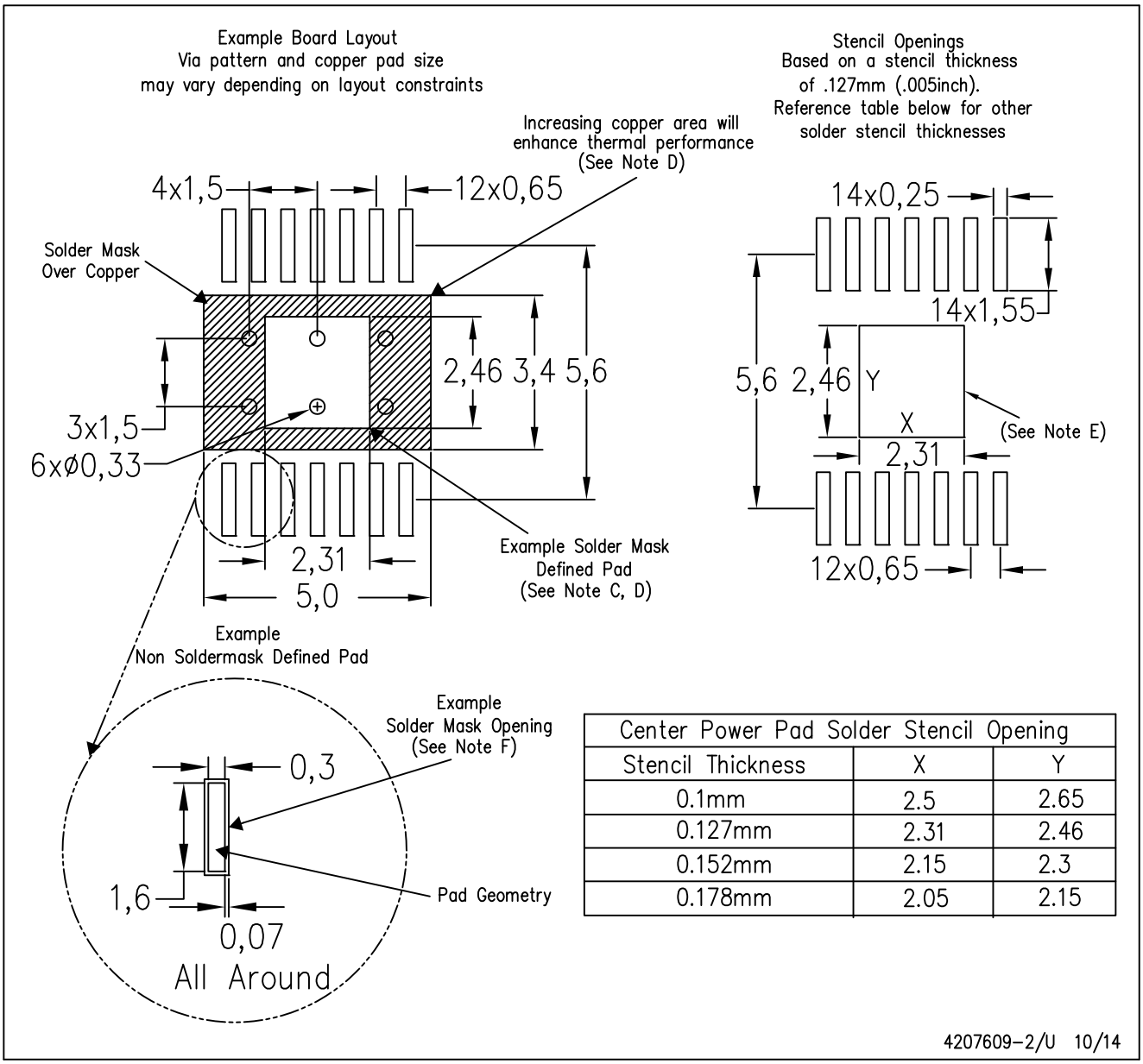
Exposed Thermal Pad Dimensions

4206332-2/AJ 10/14

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

PWP (R–PDSO–G14) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.5	2.65
0.127mm	2.31	2.46
0.152mm	2.15	2.3
0.178mm	2.05	2.15

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PWP (R-PDSO-G14) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

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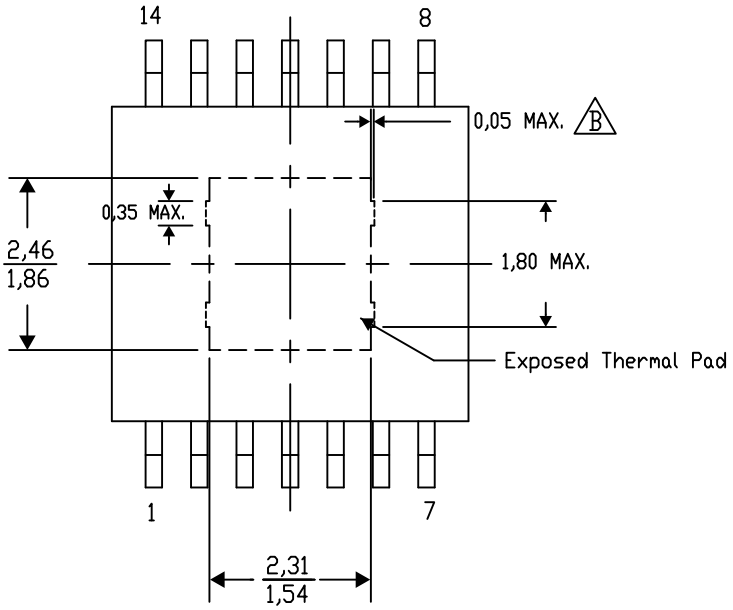

Top View

Exposed Thermal Pad Dimensions

4206332-44/AJ 10/14

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

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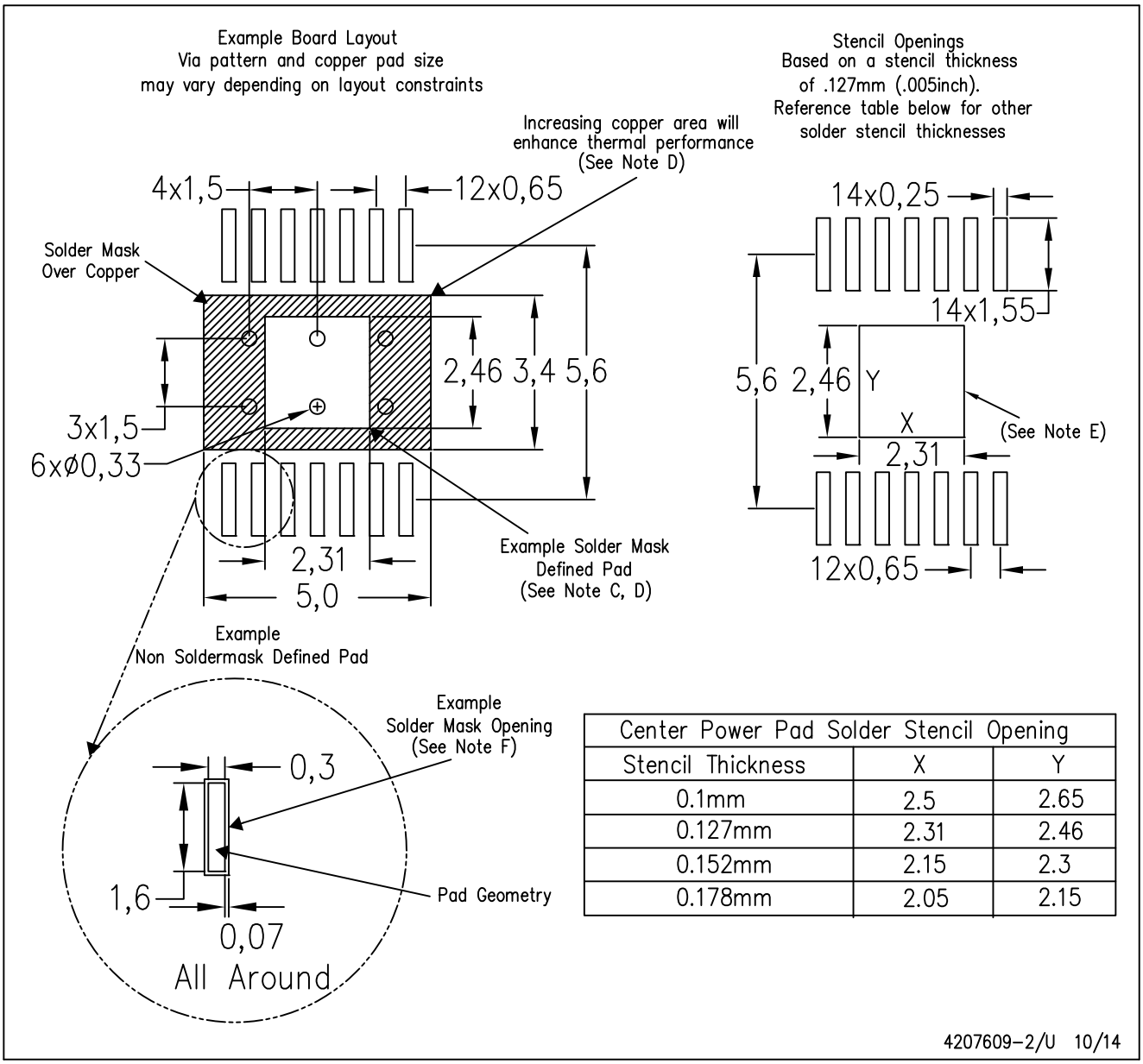
PWP (R–PDSO–G14) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.5	2.65
0.127mm	2.31	2.46
0.152mm	2.15	2.3
0.178mm	2.05	2.15

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
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F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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