VRM10.0 COMPLIANT PROGRAMMABLE FEEDBACK DIVIDER

FEATURES

- **VRM 10.x VID Code Table**
- **14-Pin TSSOP**

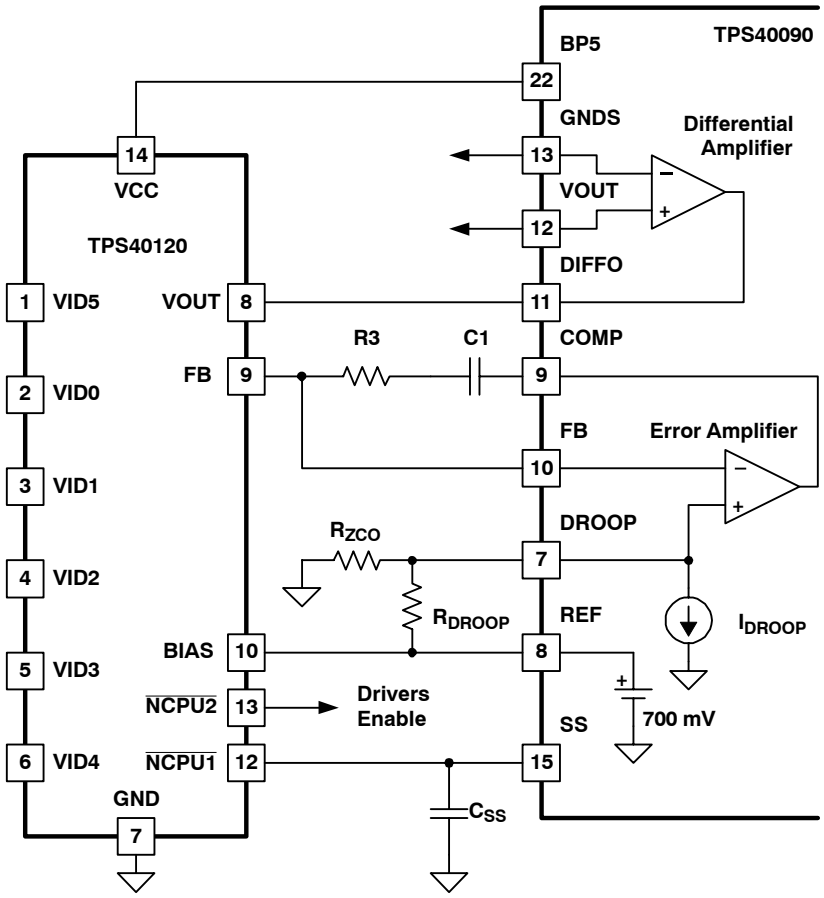
APPLICATIONS

- **Voltage Regulator Modules VRM/EVRD 10.x**
- **Multiphase Processor Power Supplies**

DESCRIPTION

The TPS40120 is a 6-bit digitally programmed feedback divider designed to work with TPS40090 multiphase controller or other controllers having 0.7-V internal reference to support VRM 10.x compliant power supplies. The TPS40120 is designed to support discrete DC/DC converters for Intel® processors using 5-bit (Pentium® 4 or Xeon™) or 6-bit VID codes with 12.5 mV steps.

TYPICAL APPLICATION



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOSFET gates.

ORDERING INFORMATION

T_A	PLASTIC HTTSOP(1)
-40°C to 85°C	TPS40120PW

(1) The PW package is available taped and reeled. Add an R suffix to the device type (i.el TPS40120PWR).

ABSOLUTE MAXIMUM RATING(1)

over operating free-air temperature range unless otherwise noted

			TPS40120	UNITS
V_{IN}	Input voltage range	VID0, VID1, VID2, VID3, VID4, VID5, VOUT	-0.3 to 5.5	V
V_{OUT}	Output voltage range	FB, $\overline{NCPU2}$	-0.3 to 5.5	V
		VCC, $\overline{NCPU1}$	-0.3 to 7.0	
T_A	Operating ambient temperature range		-40 to 85	°C
T_{stg}	Storage temperature		-55 to 150	

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to the network ground terminal unless otherwise noted.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply voltage, VCC		4.3	5.0	5.5	V
I/O voltage range	VID0, VID1, VID2, VID3, VID4, VID5, VOUT	-0.1		5.5	
Operating free-air temperature, T_A		-40		85	°C

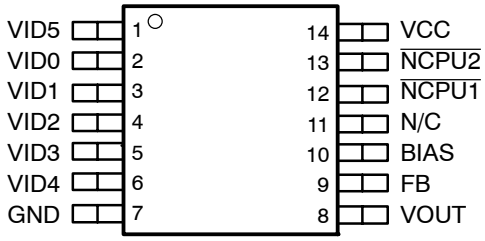
ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{VCC}	Supply voltatge		4.3	5.0	5.5	V
I_{VCC}	Supply current	All VID inputs low			1	mA
R_{FB}	Resistance between FB and OUT		7.5	10	14.5	kΩ
	Divider accuracy		-0.5%		0.5%	
VID_{THD}	VID input logic high		0.85			V
VID_{THD}	VID input logic low				0.3	
I_{BIAS}	BIAS input leakage	V_{BIAS} = 0.7 V			100	μA
	Logic low voltage	I_{PULLUP}= 1 mA			0.8	V
	Logic high leakage current				1	μA
	No CPU output voltage	$I_{L(SNK)}$= 0.5 mA, $I_{L(SRC)}$= 0.5 mA	V_{VSS}+ 0.5		V_{VCC} - 0.5	V

DEVICE INFORMATION

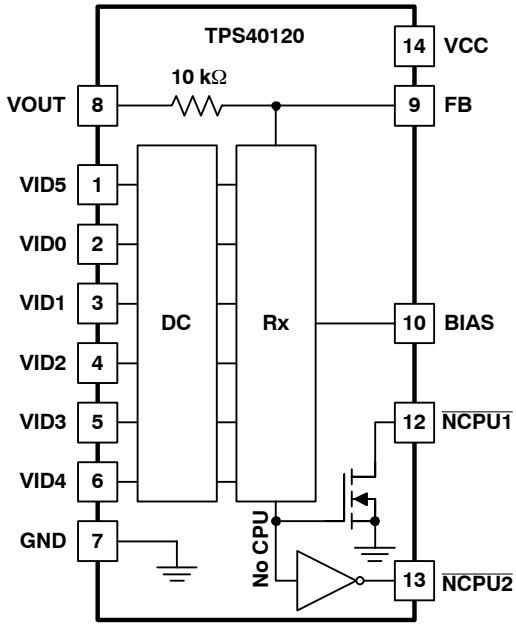
PW PACKAGE
(TOP VIEW)



TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
BIAS	10	I	Provides controller's reference voltage into the divider for improved tolerance.
FB	9	O	Middle point of the feedback divider connected to the inverting input of the controller's error amplifier
GND	7	-	Signal ground pin.
$\overline{\text{NCPU1}}$	12	O	Signals no CPU state. VID = x11111. Open drain output.
$\overline{\text{NCPU2}}$	13	O	Signals no CPU state. VID = x11111. TTL logic output.
VCC	14	I	Power to the device.
VID0	2	I	Voltage identification inputs. V_{REF} voltage is set in accordance with VRM 10.x codes applied to these pins.
VID1	3	I	
VID2	4	I	
VID3	5	I	
VID4	6	I	
VID5	1	I	
VOUT	8	I	This pin is connected to the output of the VR module or to the output of the differential amplifier of the TPS40090 controller.

FUNCTIONAL BLOCK DIAGRAM



DETAILED DESCRIPTION

Operation

The digitally programmed feedback divider TPS40120 substitutes for a discrete output voltage set-divider and allows for multiphase PWM controllers such as the TPS4009x, TPS40130 and with internal reference of 0.7 V to provide voltage identification (VID) feature to power supply designs.

The TPS40120 operates as a resistive divider with constant value of the upper resistor and variable and code determined value of the lower resistor, refer to the functional block diagram. The VID code truth table is presented in Table 1.

Dynamic VID

Most modern processors adjust their core voltage depending on the workload and clock frequency by commanding voltage identification (VID) codes to the power supply.The power supply reads these VID codes and adjusts the output voltage in a control manner per processor requirements. To provide safe transition from one VID code to another (and to ensure that no erroneous output voltage is produced by the power supply), the TPS40120 VID inputs have internal anti-skew circuit with approximately 500 ns of filtering time. With a rate of change of 12.5 mV in 5 μs, nothing else is required to achieve smooth upward and downward core voltage transitions. See Figure 1 and Figure 2.

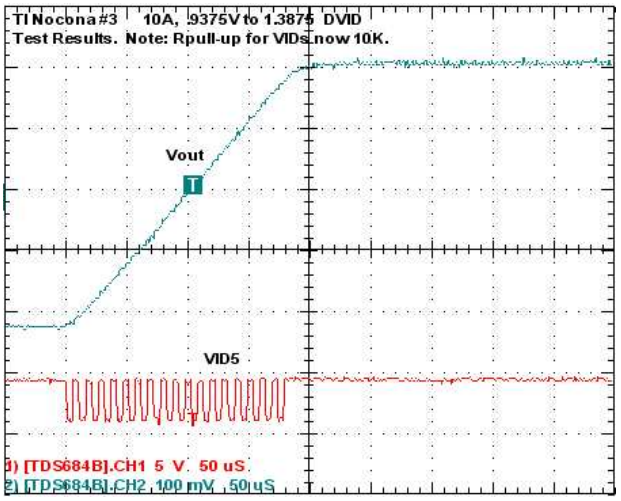


Figure 1. VID Step-Up Transition

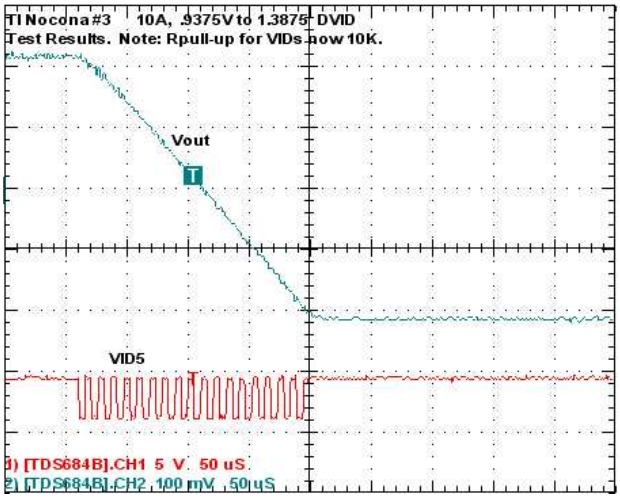


Figure 2. VID Step-Down Transition

DETAILED DESCRIPTION (continued)

Table 1. Voltage Identification (VID)

PROCESSOR PINS (0=LOW, 1=HIGH)						V_{REF} (V)
VID4	VID3	VID2	VID1	VID0	VID5	
0	1	0	1	0	0	0.8375
0	1	0	0	1	1	0.8500
0	1	0	0	1	0	0.8625
0	1	0	0	0	1	0.8750
0	1	0	0	0	0	0.8875
0	0	1	1	1	1	0.9000
0	0	1	1	1	0	0.9125
0	0	1	1	0	1	0.9250
0	0	1	1	0	0	0.9375
0	0	1	0	1	1	0.9500
0	0	1	0	1	0	0.9625
0	0	1	0	0	1	0.9750
0	0	1	0	0	0	0.9875
0	0	0	1	1	1	1.0000
0	0	0	1	1	0	1.0125
0	0	0	1	0	1	1.0250
0	0	0	1	0	0	1.0375
0	0	0	0	1	1	1.0500
0	0	0	0	1	0	1.0625
0	0	0	0	0	1	1.075
0	0	0	0	0	0	1.0875
1	1	1	1	1	1	OFF (1)
1	1	1	1	1	0	OFF (1)
1	1	1	1	0	1	1.1000
1	1	1	1	0	0	1.1125
1	1	1	0	1	1	1.1250
1	1	1	0	1	0	1.1375
1	1	1	0	0	1	1.1500
1	1	1	0	0	0	1.1625
1	1	0	1	1	1	1.1750
1	1	0	1	1	0	1.1875
1	1	0	1	0	1	1.2000
1	1	0	1	0	0	1.2125
1	1	0	0	1	1	1.2250
1	1	0	0	1	0	1.2375
1	1	0	0	0	1	1.2500
1	1	0	0	0	0	1.2625
1	0	1	1	1	1	1.2750
1	0	1	1	1	0	1.2875
1	0	1	1	0	1	1.3000
1	0	1	1	0	0	1.3125
1	0	1	0	1	1	1.3250
1	0	1	0	1	0	1.3375
1	0	1	0	0	1	1.3500

(1) $\overline{\text{NCPU1}}$ and $\overline{\text{NCPU2}}$ outputs go low.

DETAILED DESCRIPTION (continued)

Table 1. Voltage Identification (VID) (continued)

PROCESSOR PINS (0=LOW, 1=HIGH)						V_{REF} (V)
VID4	VID3	VID2	VID1	VID0	VID5	
1	0	1	0	0	0	1.3625
1	0	0	1	1	1	1.3750
1	0	0	1	1	0	1.3875
1	0	0	1	0	1	1.4000
1	0	0	1	0	0	1.4125
1	0	0	0	1	1	1.4250
1	0	0	0	1	0	1.4375
1	0	0	0	0	1	1.4500
1	0	0	0	0	0	1.4625
0	1	1	1	1	1	1.4750
0	1	1	1	1	0	1.4875
0	1	1	1	0	1	1.500
0	1	1	1	0	0	1.5125
0	1	1	0	1	1	1.5250
0	1	1	0	1	0	1.5375
0	1	1	0	0	1	1.5500
0	1	1	0	0	0	1.5625
0	1	0	1	1	1	1.5750
0	1	0	1	1	0	1.5875
0	1	0	1	0	1	1.6000

APPLICATION INFORMATION

Typical application circuit for TPS40120 and TPS40090 combination is presented on the front page. Normally, the TPS40120 accepts power from the BP5 pin of the TPS40090 multiphase controller which simplifies its enable/disable control. The upper resistor of the programmable divider (pin 8) is connected to the output of the differential amplifier DIFFO. The center tap of the divider (pin 9) is connected to the joint point of the FB pin of the multi-phase controller and error amplifier compensation network. TPS40120 has two logic $\overline{\text{NCPUx}}$ outputs that can be used to control output and the gate drivers in a multi-phase power supply when no-CPU code is asserted. The $\overline{\text{NCPU1}}$ output is an open drain that can be useful by discharging the soft-start capacitor and bringing the output voltage down. The push-pull $\overline{\text{NCPU2}}$ output can be used to control gate drivers to provide high impedance of the power supply output in off state.

The application circuit for a four-phase 105-A CPU VRM10.x compliant power supply is shown in Figure 3.

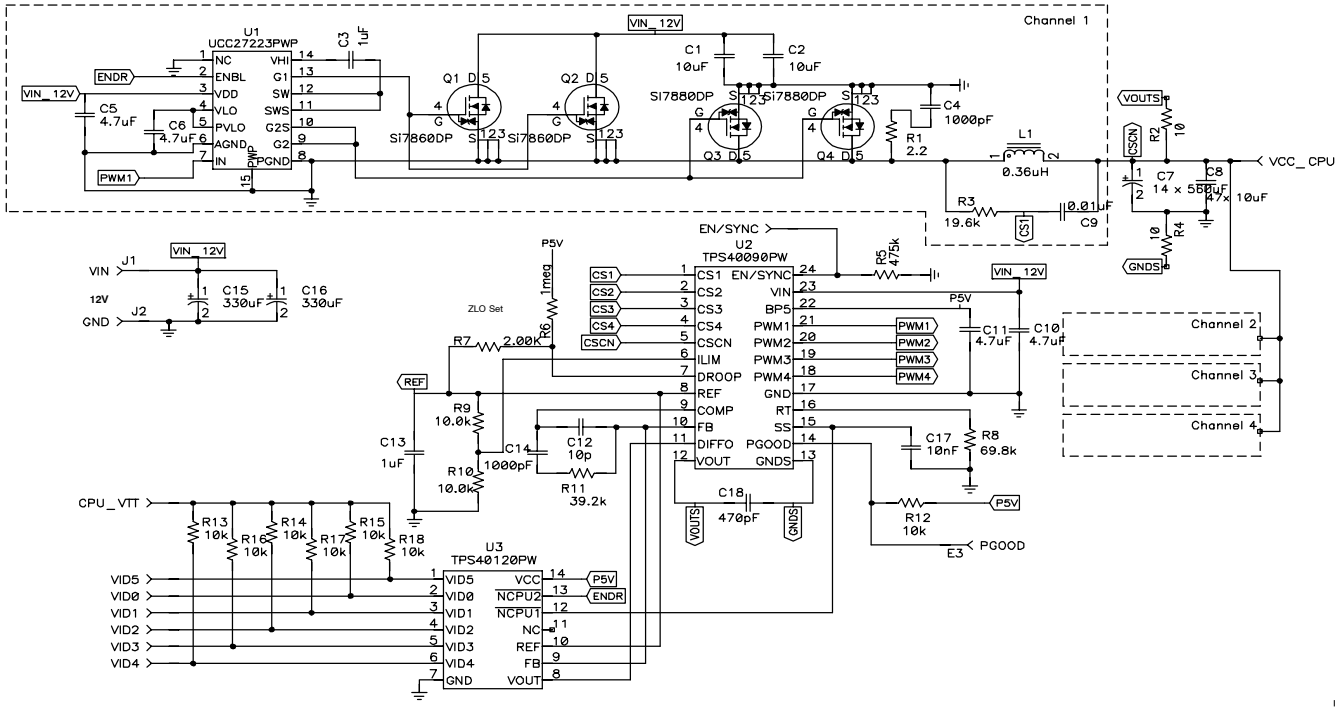


Figure 3. VRM 10.x Compliant CPU Power Supply

For detailed information on TPS40090 multiphase controller and design example request the TPS4009x datasheet (SLUS578) and the user's guide (SLUU026).

11-Apr-2013

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TPS40120PW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	40120	Samples
TPS40120PWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	40120	Samples
TPS40120PWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	40120	Samples
TPS40120PWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	40120	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

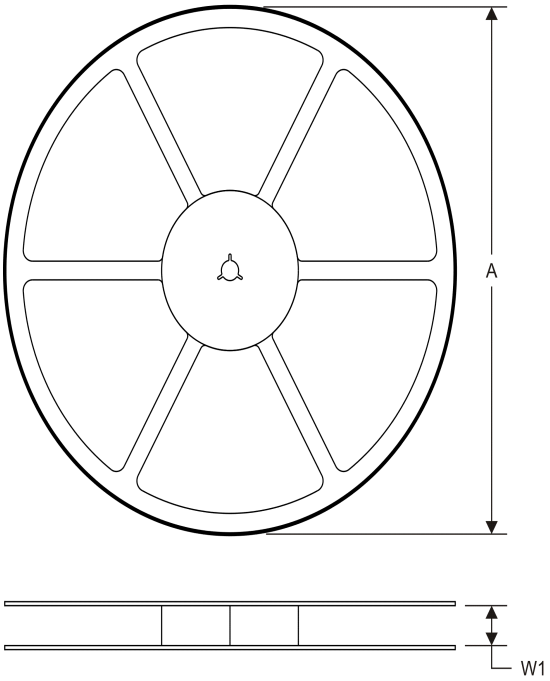
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

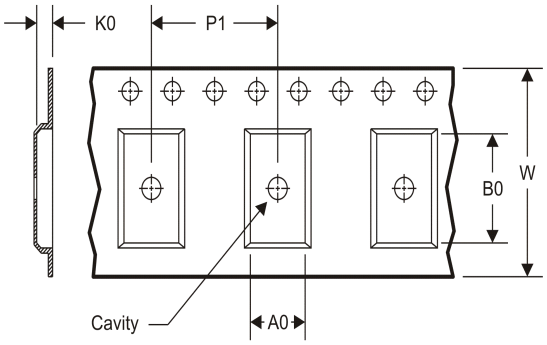
11-Apr-2013

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

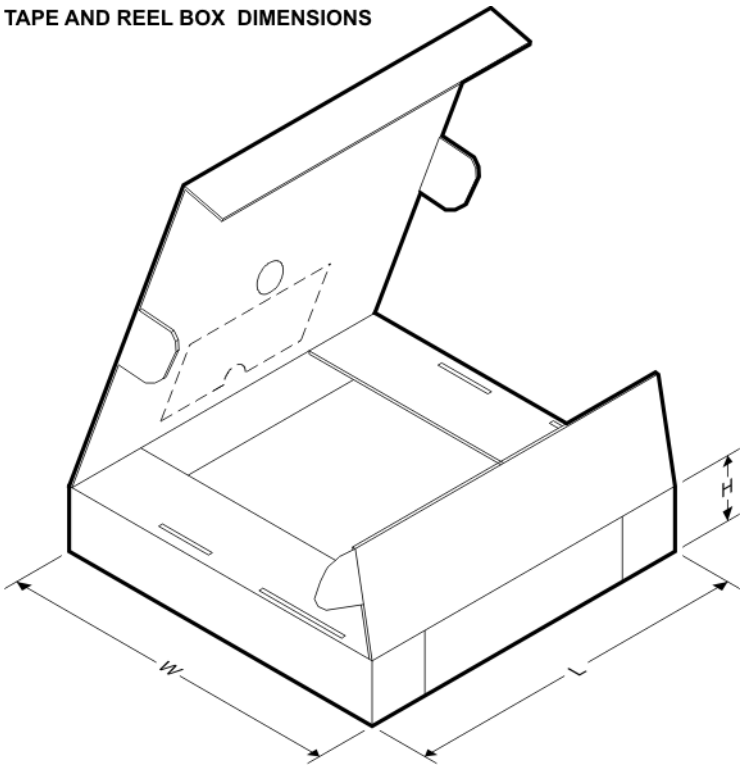
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS40120PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

PACKAGE MATERIALS INFORMATION

14-Jul-2012

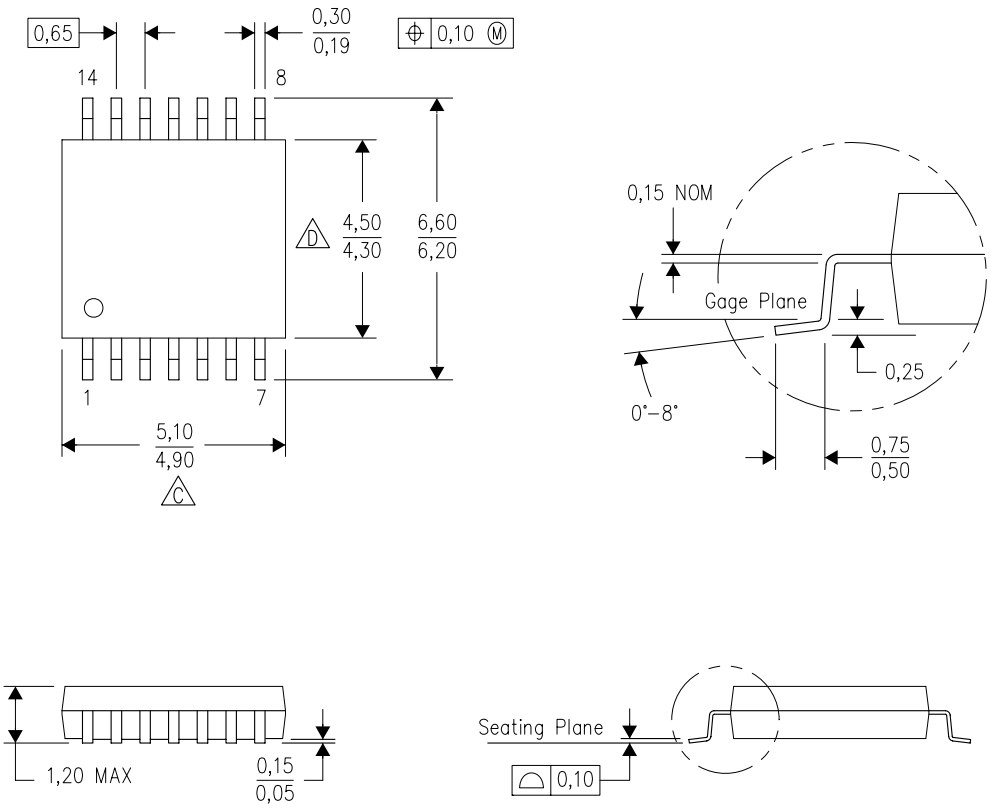
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS40120PWR	TSSOP	PW	14	2000	367.0	367.0	35.0

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



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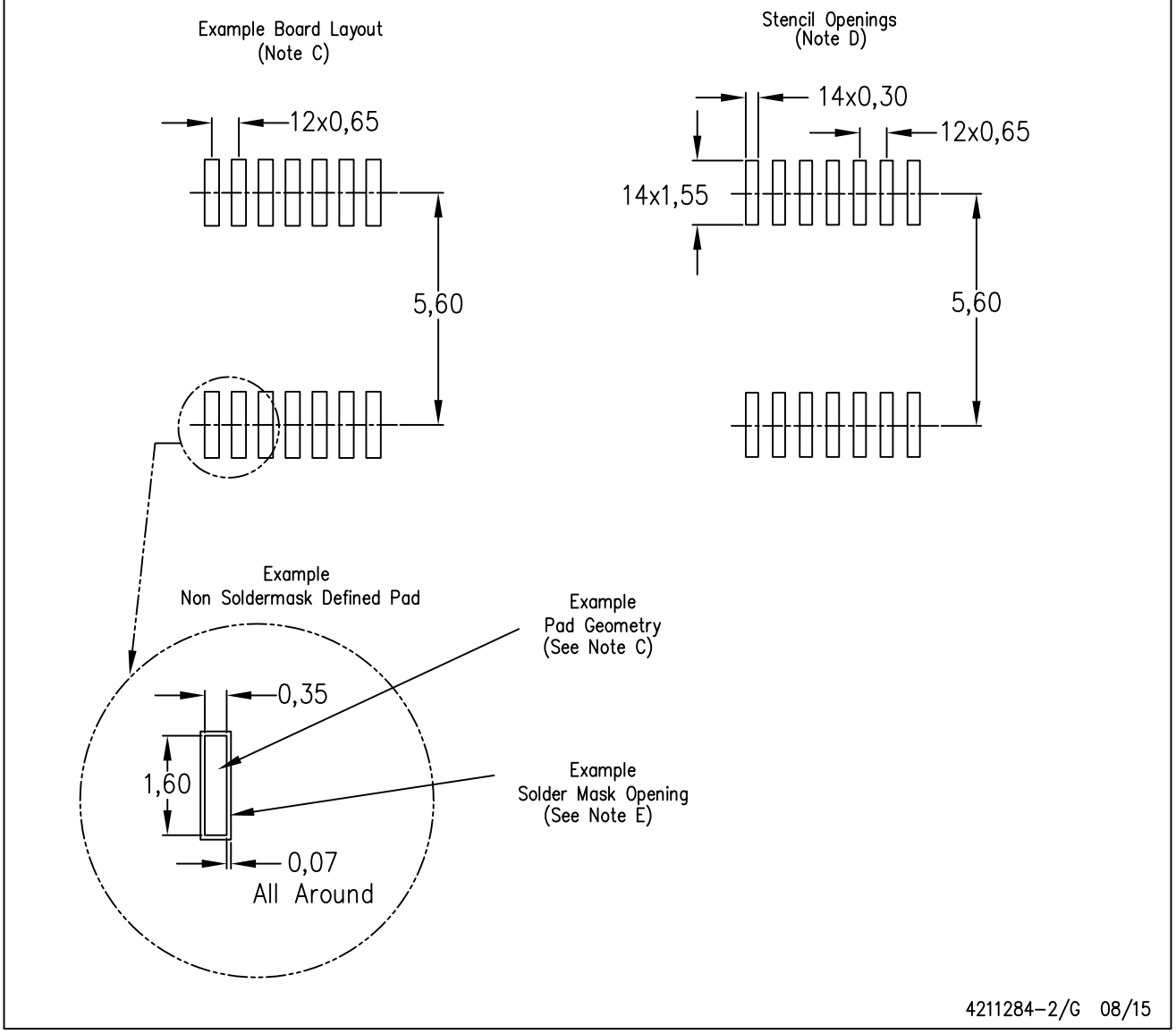
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.