Dual Output or Two-Phase Synchronous Buck Controller

FEATURES

- **Dual-Output or Two-Phase Synchronous Buck Controller**
- **180° Out-of-Phase Reduces Input Ripple**
- **Input Voltage Range from 3 V to 20 V**
- **Output Voltage Range: 0.6 V to 5.6 V**
- **Adjustable Frequency 100 kHz to 1 MHz**
- **Bidirectional SYNC Pin with 0°/180° or 90°/270° Phase Shift**
- **Voltage Mode Control With Input Feed-Forward**
- **Accurate Current Sharing for Two-Phase Operation**
- **Individual PowerGood Outputs**
- **Individual Enable and Programmable Soft Start, With Pre-Bias Start-up**
- **±0.5%, 600-mV Reference**
- **Output UV/OV Protection and Input Undervoltage Lockout**
- **Individual Overcurrent Limit Setting**
- **Hiccup Overcurrent Protection**
- **Accurate Inductor DCR or Resistive Current Sensing**
- **Remote Sense for Two-Phase Applications**
- **Internal N-Channel FET Drivers**
- **Integrated Bootstrap Switches**
- **Available in 5 mm × 5 mm 32-Pin QFN Package**

APPLICATIONS

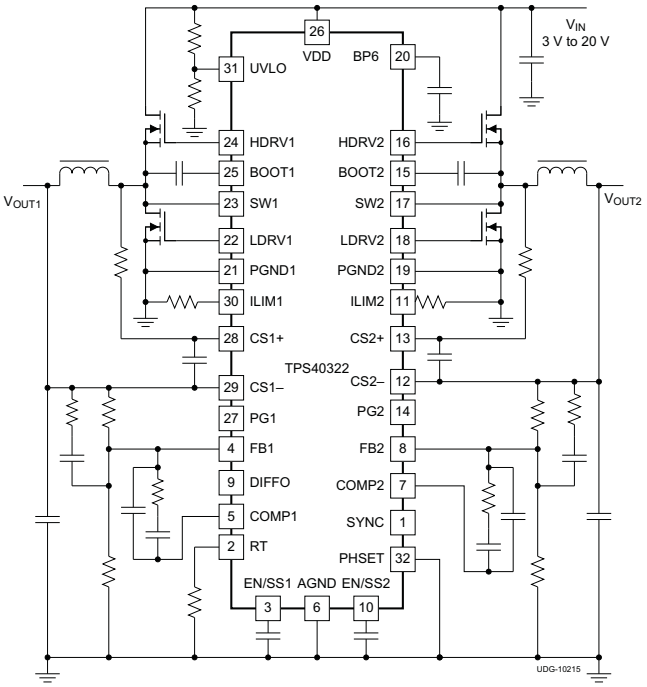
- **Multiple Rail Systems**
- **Telecom Base Station**
- **Switcher/Router Networking**
- **xDSL Broadband Access**
- **Server and Storage System**

DESCRIPTION

The TPS40322 is a dual-output, synchronous buck controller. It can also be configured as a single-output, two-phase controller. The 180° out-of-phase operation reduces the input current ripple and extends the input capacitor lifetime. Bi-directional master/slave synchronization function provides evenly distributed phase shift for a four-output system that reduces input ripple further and attenuates the system noise.

The wide input range can support 3.3-V, 5-V, and 12-V buses. The accurate reference voltage satisfies the precision voltage needed by ASICs and potentially reduces the output capacitance requirement. Separate PGOOD signals provide flexibility for system monitoring and sequencing. The two channels are independently controlled and each soft-start time is programmable. Voltage mode control is implemented to reduce noise sensitivity and also ensures low duty ratio conversion.

SIMPLIFIED APPLICATION CIRCUIT



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION(1)

TEMPERATURE RANGE	PINS	PACKAGE	ORDERING NUMBER
–40°C to 125°C	32	QFN	TPS40322RHB

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS (1)

Over operating free-air temperature range, all voltages are with respect to GND (unless otherwise noted)

		VALUE		UNIT
		MIN	MAX	
Voltage Range	VDD	–0.3	22	V
	SW1, SW2	–3	27	
	SW1, SW2 (< 100 ns pulse width)		–5	
	SW1, SW2 (< 10 ns pulse width)	–7.5	30	
	BOOT1, BOOT2	–0.3	30	
	BOOT1, BOOT2 (< 10 ns pulse width)	–0.5	33	
	BP6	–0.3	7	
	HDRV1, HDRV2	–2	30	
	BOOT1-SW1, BOOT2-SW2, HDRV1-SW1, HDRV2-SW2 (differential from BOOT or HDRV to SW)	–0.3	7	
	All other pins	–0.3	7	
Temperature	T_J Operating temperature	–40	145	°C
	T_{stg} Storage temperature	–55	150	°C
Electrostatic disharge	Human Body Model (HBM)	2000		V
	Charged Device Model (CDM)	1500		V

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
V_{VDD}	Input operating voltage	3	20	V
T_J	Operating junction temperature	–40	125	°C

THERMAL INFORMATION

THERMAL METRIC(1)		TPS40322 QFN 32 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(2)	37.3	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	28.6	
θ_{JB}	Junction-to-board thermal resistance(4)	10.0	
ψ_{JT}	Junction-to-top characterization parameter(5)	0.4	
ψ_{JB}	Junction-to-board characterization parameter(6)	9.9	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	2.7	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

ELECTRICAL CHARACTERISTICS

T_J = –40°C to 125°C, V_{VDD} = 12 V, R_{RT} = 40 kΩ, f_{SW} = 500 kHz (unless otherwise noted),

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SUPPLY						
VDD	Input voltage range		3		20	V
IDD_{SDN}	Shutdown	$V_{ENx/SSx}$ = 0 V		200	250	µA
IDD_Q	Quiescent, non-switching	V_{FB} = 0.65 V, ENx/SSx float		6	8	mA
UVLO						
UVLO	Minimum turn-on voltage		1.21	1.24	1.27	V
$UVLO_{HYS}$	Hysteresis current		13	15	17	µA
BP REGULATOR						
BP	Regulator voltage	7 V ≤ V_{VDD} ≤ 20 V	6.2	6.5	6.8	V
V_{DO}	Regulator dropout voltage	I_{BP} = 25 mA, V_{VDD} = 3 V		50	100	mV
I_{BP}	Regulator continuous current limit(1)		100			mA
V_{BPUVLO}	Regulator output UVLO		2.40	2.70	2.95	V
$V_{BPUVLO-HYS}$	Regulator output UVLO hysteresis		180	210	250	mV
OSCILLATOR/ RAMP GENERATOR						
f_{SW}	Oscillator frequency		100		1000	kHz
		R_{RT} = 40 kΩ	450	500	550	kHz
V_{RAMP}	Ramp amplitude (peak-to-peak)	3 V < V_{VDD} < 20 V		VDD/8.5		V
V_{VAL}	Valley voltage			0.85		V
f_{SYNC}	SYNC frequency range		200		2000	kHz
$t_{PW(sync)}$	SYNC input minimum pulse width		100			ns
$V_{H(sync)}$	Rising edge threshold to set sync pulse		2			V
$V_{L(sync)}$	Falling edge threshold to reset sync pulse				0.8	V
f_{MASTER}	Master clock frequency		200		2000	kHz
Δf_{SYNC}	Percent of master frequency for synchronization		–20%		20%	
V_{PHSET}	Master	0°/180° phase shift			0.5	V
	Slave	0°/180° phase shift	0.6		2.0	V
	Slave	90°/270° phase shift	2.1			V
PWM						
PWM(off)	Minimum PWM off-time			90	130	ns
$t_{ON(min)}$	Minimum controllable pulse width	See (1)		90		ns
t_{DEAD}	Output driver dead time	HDRV off to LDRV on	20	35	40	ns
t_{DEAD}	Output driver dead time	LDRV off to HDRV on	20	35	40	ns
ERROR AMPLIFIER AND VOLTAGE REFERENCE						
V_{FB}	FB input voltage	0°C < T_J < 70°C	597	600	603	mV
		–40°C < T_J < 125°C	594	600	606	
I_{FB}	FB input bias current			20	75	nA
GBWP	Unity gain bandwidth	See (1)		24		MHz
AVOL	Open loop gain	See (1)	80			dB
I_{OH}	High-level output current			3		mA
I_{OL}	Low-level output current			9		mA

(1) Specified by design. Not production tested.

ELECTRICAL CHARACTERISTICS (continued)

T_J = –40°C to 125°C, V_{VDD} = 12 V, R_{RT} = 40 kΩ, f_{SW} = 500 kHz (unless otherwise noted),

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
ENABLE/SOFT START						
V_{IH}	High-level input voltage		0.55	0.70	1.00	V
V_{IL}	Low-level input voltage		0.23	0.26	0.30	V
I_{SS}	Soft-start source current		8	10	12	µA
V_{SS}	Soft-start voltage level			0.8		V
I_{DISCHG}	Soft-start discharge current			130		µA
OVERCURRENT PROTECTION						
I_{ILIM}	ILIM program current	T_J = 25°C	9.5	10.0	10.5	µA
t_{HICCUP}	Hiccup cycles to recover			6		Cycles
CURRENT SENSE AMPLIFIER						
V_{DIFF}	Differential input voltage range		–60		60	mV
V_{CM}	Input common mode range		0		5.6	V
A_{CS}	Current sensing gain			15		V/V
V_{CSOUT}	Current sense amplifier output	V_{CSIN} = 20 mV, T_J = 25°C	270	300	330	mV
f_{C0}	Closed loop bandwidth(2)		3			MHz
	Current sense amplifier output difference between CH1 and CH2	V_{CSIN} = 20 mV to both CS1 and CS2	–15		15	mV
OVERVOLTAGE/UNDERVOLTAGE PROTECTION						
V_{OVP}	Feedback voltage limit for OVP		679	700	735	mV
V_{UVP}	Feedback voltage limit for UVP		475	500	525	mV
GATE DRIVERS						
R_{HDHI}	High-side driver pull-up resistance	$V_{BOOT} – V_{SW}$ = 6.5 V, I_{HDRV} = –40 mA	0.8	1.5	2.5	Ω
R_{HDLO}	High-side driver pull-down resistance	$V_{BOOT} – V_{SW}$ = 6.5 V, I_{HDRV} = 40 mA	0.5	1.0	1.6	Ω
R_{LDHI}	Low-side driver pull-up resistance	I_{LDRV} = –40 mA	0.8	1.5	2.5	Ω
R_{LDLO}	Low-side driver pull-down resistance	I_{LDRV} = 40 mA	0.35	0.60	1.30	Ω
t_{HRISE}	High-side driver rise time	C_{LOAD} = 5 nF, See (2)		15		ns
t_{HFALL}	High-side driver fall time	C_{LOAD} = 5 nF, See (2)		12		ns
t_{LRISE}	Low-side driver rise time	C_{LOAD} = 5 nF, See (2)		15		ns
t_{LFALL}	Low-side driver fall time	C_{LOAD} = 5 nF, See(2)		10		ns
BOOT SWITCH						
V_{DFWD}	Bootstrap switch voltage drop	I_{BOOT} = 5 mA		0.1		V
REMOTE SENSE						
V_{IOFSET}	Input offset voltage	V_{DIFFO} = 0.9 V	–2		2	mV
Gain	Differential gain		0.995		1.005	V/V
BW	Close loop bandwidth(2)		2.00			MHz
V_{DIFFO}	Output voltage at DIFFO pin				V_{BP6} – 0.2	V
I_{SRC}	Output source current				1	mA
I_{SNK}	Output sink current				1	mA
POWERGOOD						
V_{OV}	Feedback voltage limit for PGOOD		650	675	697	mV
V_{UV}	Feedback voltage limit for PGOOD		510	525	545	mV
$V_{PGD(hyst)}$	PGOOD hysteresis voltage at FB			25	40	mV
R_{RGD}	PGOOD pull down resistance			50	70	Ω
$I_{PGD(leak)}$	PGOOD leakage current				20	µA
THERMAL SHUTDOWN						
T_{SD}	Junction shutdown temperature	See (2)		150		°C
$T_{SD(hyst)}$	Hysteresis	See (2)		20		°C

(2) Specified by design. Not production tested.

TYPICAL CHARACTERISTICS

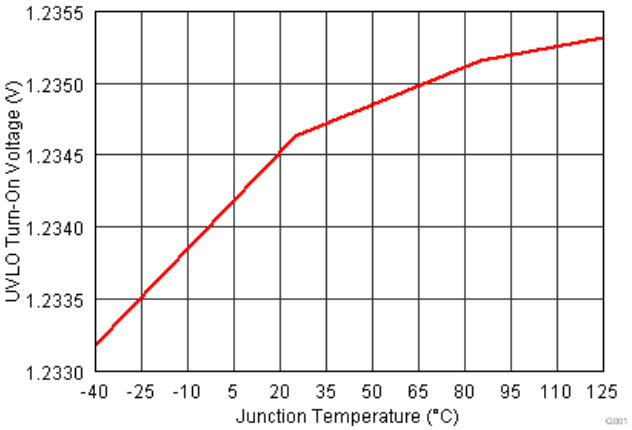


Figure 1. UVLO Turn-On Voltage vs. Junction Temperature

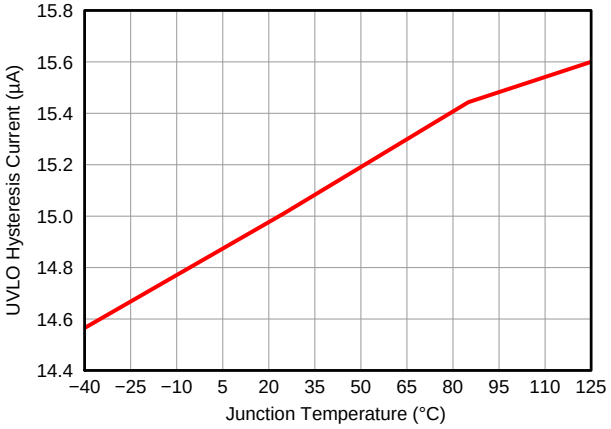


Figure 2. UVLO Hysteresis Current vs. Junction Temperature

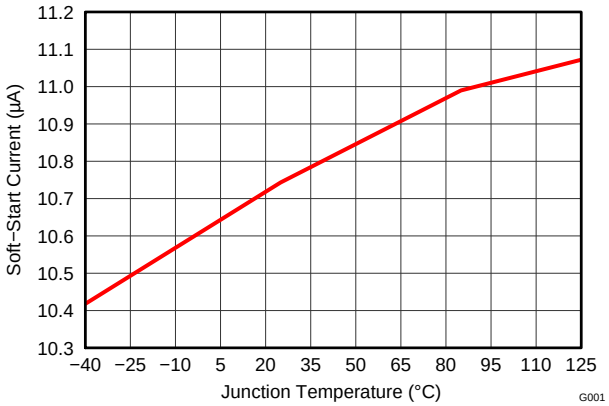


Figure 3. Soft-Start Current vs. Junction Temperature

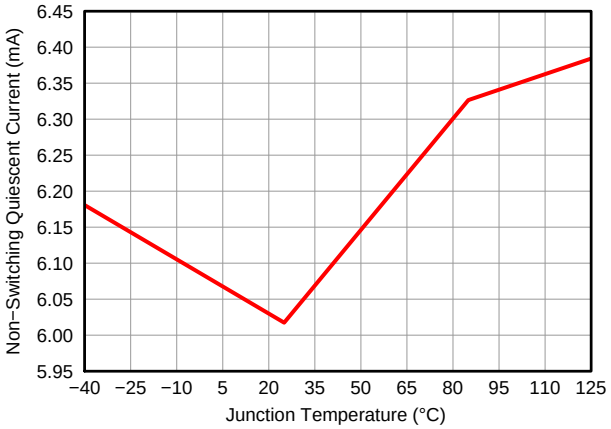


Figure 4. Non-Switching Quiescent Current vs. Junction Temperature

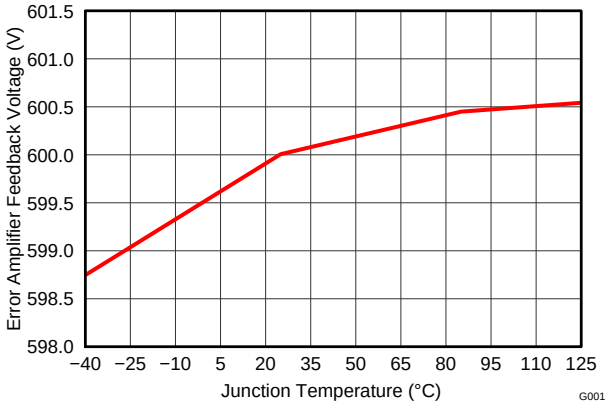


Figure 5. Error Amplifier Feedback Voltage vs. Junction Temperature

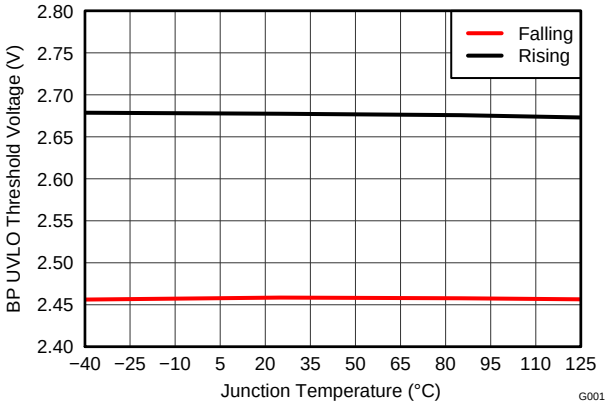


Figure 6. BP UVLO Threshold vs. Junction Temperature

TYPICAL CHARACTERISTICS (continued)

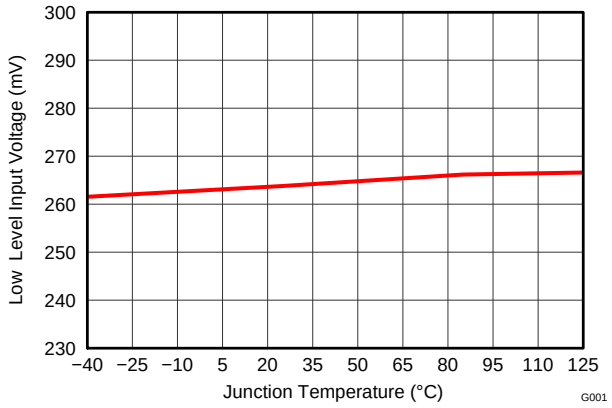


Figure 7. ENx Low-Level Inout Voltage vs. Junction Temperature

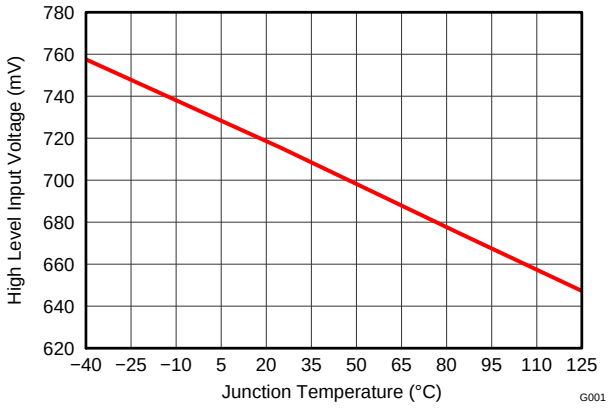


Figure 8. ENx High-Level Inout Voltage vs. Junction Temperature

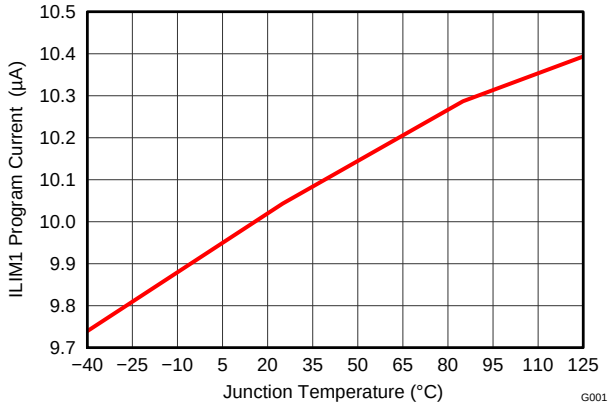


Figure 9. Current Limit vs. Junction Temperature

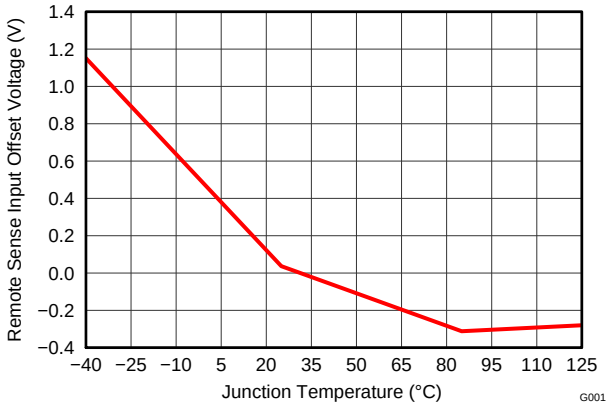


Figure 10. Remote Sense Input Offset Voltage vs. Junction Temperature

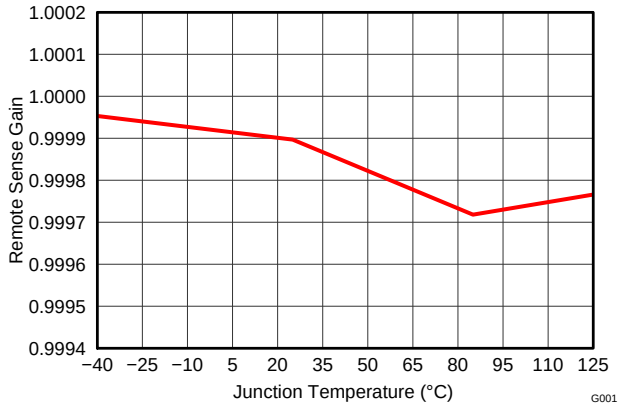


Figure 11. Remote Sense Gain vs. Junction Temperature

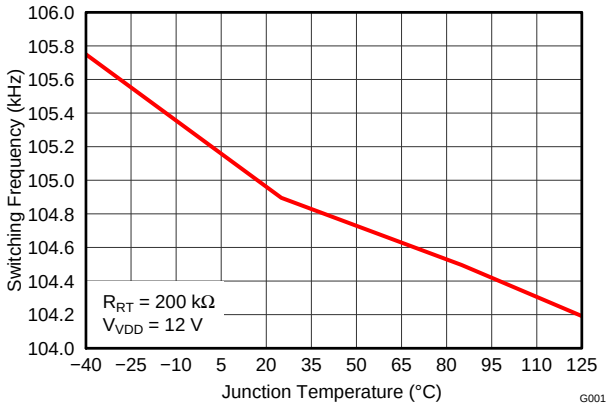


Figure 12. Frequency vs. Junction Temperature

TYPICAL CHARACTERISTICS (continued)

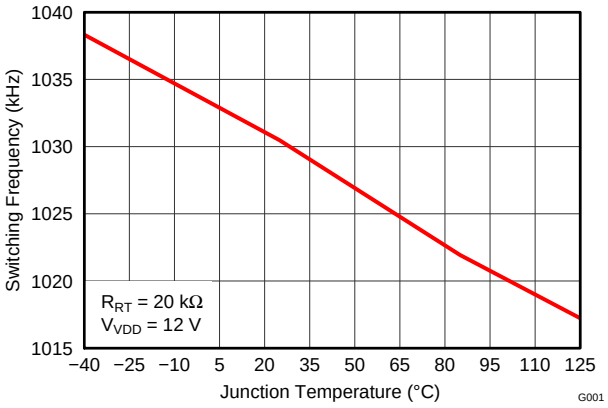


Figure 13. Frequency vs. Junction Temperature

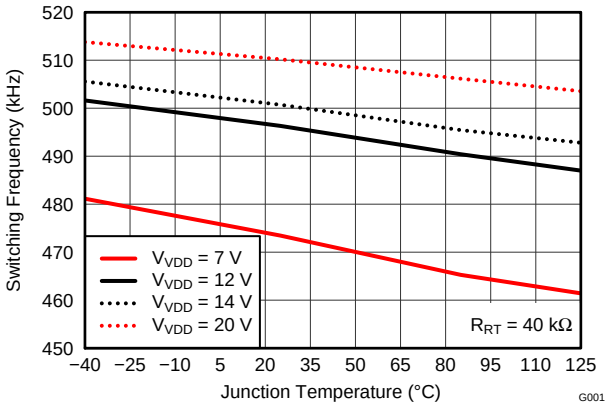
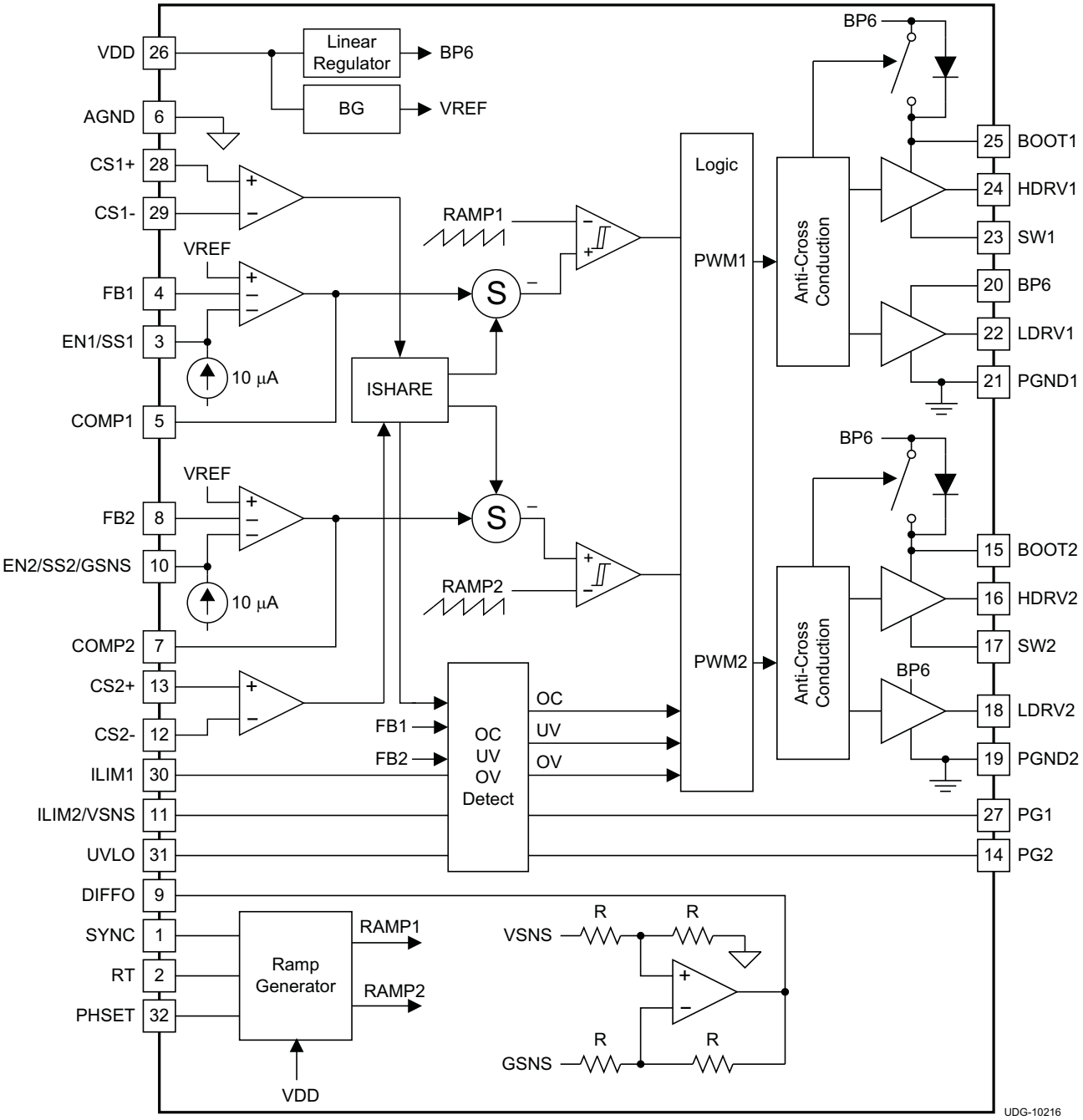


Figure 14. Frequency vs. Junction Temperature

DEVICE INFORMATION

FUNCTIONAL BLOCK DIAGRAM



NOTE

- In two-phase mode, the EN2/SS2/GSNS pin becomes the GSNS pin and the ILIM2/VSNS pin becomes the VSNS pin.
- The two channels are identical unless specified otherwise.
- The following naming conventions are used to better describe the functions. For example, COMPx refers to COMP1 and COMP2, FBx refers to FB1 and FB2.

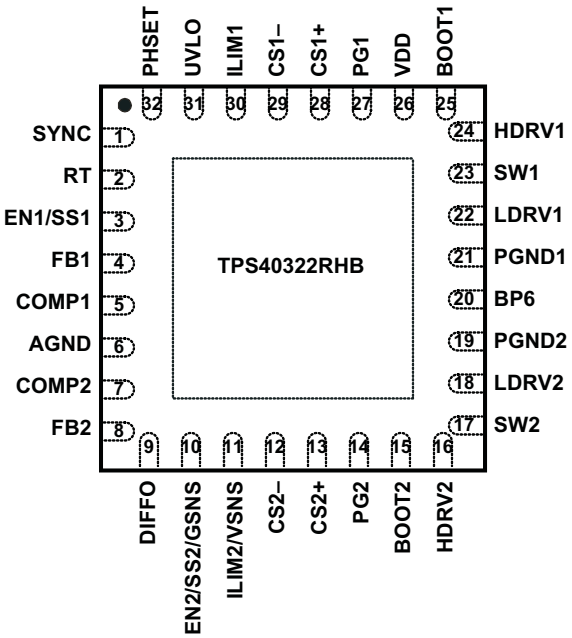


Table 1. PIN FUNCTIONS

NAME	PIN	I/O	DESCRIPTION
AGND	6	–	Low noise ground connection to the controller.
BOOT1	25	I	BOOT1 provides a bootstrapped supply for the high-side FET driver for channel 1 (CH1). Connect a capacitor (0.1 µF typical) from BOOT1 to SW1 pin.
BOOT2	15	I	BOOT2 provides a bootstrapped supply for the high-side FET driver for channel 2 (CH2). Connect a capacitor (0.1 µF typical) from BOOT2 to SW2 pin.
BP6	20	O	Output bypass for the internal regulator. Connect a low ESR bypass ceramic capacitor with a value of 3.3 µF or greater from this pin to the power ground plane.
COMP1	5	O	Output of the error amplifier 1 and connection node for loop feedback components.
COMP2	7	O	Output of the error amplifier 2 and connection node for loop feedback components.
CS1–	29	I	Negative terminal of current sense amplifier for CH1
CS1+	28	I	Positive terminal of current sense amplifier for CH1
CS2–	12	I	Negative terminal of current sense amplifier for CH2
CS2+	13	I	Positive terminal of current sense amplifier for CH2
DIFFO	9	O	Output of the differential amplifier. When the device is configured for dual channel mode, the DIFFO pin must be either floating or tied to BP6
EN1/SS1	3	I	Logic level input which starts or stops CH1. Letting this pin float turns CH1 on. Pulling this pin low disables CH1. This is also the soft-start programming pin. A capacitor connected from this pin to AGND programs the soft-start time. The capacitor is charged with an internal current source of 10 µA. The resulting voltage ramp of this pin is also used as a second non-inverting input to the error amplifier 1 after a 0.8 V (typical) level shift downwards.
EN2/SS2/GSNS	10	I	Logic level input which starts or stops CH2. Letting this pin float turns CH2 on. Pulling this pin low disables CH2. This is also the soft-start programming pin. A capacitor connected from this pin to AGND programs the soft-start time. The capacitor is charged with an internal current source of 10 µA. The resulting voltage ramp of this pin is also used as a second non-inverting input to the error amplifier 2 after a 0.8 V (typical) level shift downwards. In two-phase mode, this pin becomes GSNS as the negative terminal of a remote sense amplifier.
FB1	4	I	Inverting input to the error amplifier. During normal operation, the voltage on this pin is equal to the internal reference voltage.
FB2	8	I	Inverting input to the error amplifier. During normal operation, the voltage on this pin is equal to the internal reference voltage. Connecting the FB2 pin to the BP6 pin enables two-phase mode and disables the error amplifier 2.
HDRV1	24	O	Bootstrapped gate drive output for the high-side N-channel MOSFET for CH1. A 2-Ω resistor is recommended for a noisy environment.

Table 1. PIN FUNCTIONS (continued)

NAME	PIN	I/O	DESCRIPTION
HDRV2	16	O	Bootstrapped gate drive output for the high-side N-channel MOSFET for CH2. A 2-Ω resistor is recommended for a noisy environment.
ILIM1	30	I	Used to set the overcurrent limit for CH1 with 10 µA of current flowing through a resistor from this pin to AGND.
ILIM2/VSNS	11	I	Used to set the overcurrent limit for CH2 with 10 µA of current flowing through a resistor from this pin to AGND. In two-phase mode, this pin becomes VSNS as the positive terminal of a remote sense amplifier.
LDRV1	22	O	Gate drive output for the low-side synchronous rectifier (SR) N-channel MOSFET for CH1.
LDRV2	18	O	Gate drive output for the low-side synchronous rectifier (SR) N-channel MOSFET for CH2.
PG1	27	O	Open drain power good indicator for CH1 output voltage.
PG2	14	O	Open drain power good indicator for CH2 output voltage.
PGND1	21	-	Power ground 1. Separate power ground for CH1 and CH2 in the PCB layout could potentially reduce channel to channel interference.
PGND2	19	-	Power ground 2. Separate power ground for CH1 and CH2 in the PCB layout could potentially reduce channel to channel interference.
PHSET	32	I	Used to set master or slave mode and phase angles. The master emits a 50% duty clock to the slave. The slave synchronizes to the external clock and select the phase shift angle.
RT	2	I	Connect a resistor from this pin to AGND to set the oscillator frequency.
SW1	23	I	Connect to the switched node on converter CH1. It is the return for the CH 1 high-side gate driver.
SW2	17	I	Connect to the switched node on converter CH2. It is the return for the CH 2 high-side gate driver.
SYNC	1	I/O	In master mode, a 2x free running frequency clock is sent out on SYNC pin. In slave mode, sync to an external clock which is ±20% of the free running MASTER_CLOCK frequency. The MASTER_CLOCK frequency is 2x of the free running frequency (set by RT) and operates at 50% duty cycle. When not being used, SYNC should be left floating.
UVLO	31	I	A resistor divider from VIN determines the input voltage that the controller starts.
VDD	26	I	Power input to the controller. A low ESR bypass ceramic capacitor of 0.1 µF or greater should be connected closely from this pin to AGND.

FUNCTIONAL DESCRIPTION

General Description/Control Architecture

The TPS40322 is a flexible synchronous buck controller. It can be used as a dual-output controller, or as a two-phase, single-output controller. It operates with a wide input range from 3 V to 20 V and can generate an accurate regulated output as low as 600 mV.

In dual output mode, voltage mode control with input feed-forward architecture is implemented. With this architecture, the benefits are less noise sensitivity, no control instability issues for small DCR applications, and a smaller minimum controllable on-time, often desired for high conversion ratio applications.

In two-phase, single-output mode, a current-sharing loop is implemented to ensure a balance of current between phases. Because the induced error current signal to the loop is much smaller when compared to the PWM ramp amplitude, the control loop is modeled as voltage mode with input feed-forward.

DESIGN NOTE

- When the device is operating in dual output mode, DIFFO must be floating or tied to BP6.

Voltage Reference

The 600-mV bandgap cell is internally connected to the non-inverting input of the error amplifier. The reference voltage is trimmed with the error amplifier in a unity gain configuration to remove amplifier offset from the final regulation voltage. The 0.5-% tolerance on the reference voltage allows the user to design a very accurate power supply.

Output Voltage Setting

The output voltages of the TPS40322 are set by using external feedback resistor dividers as shown in Figure 15. The regulated output voltage (V_{OUT}) is determined by Equation 1.

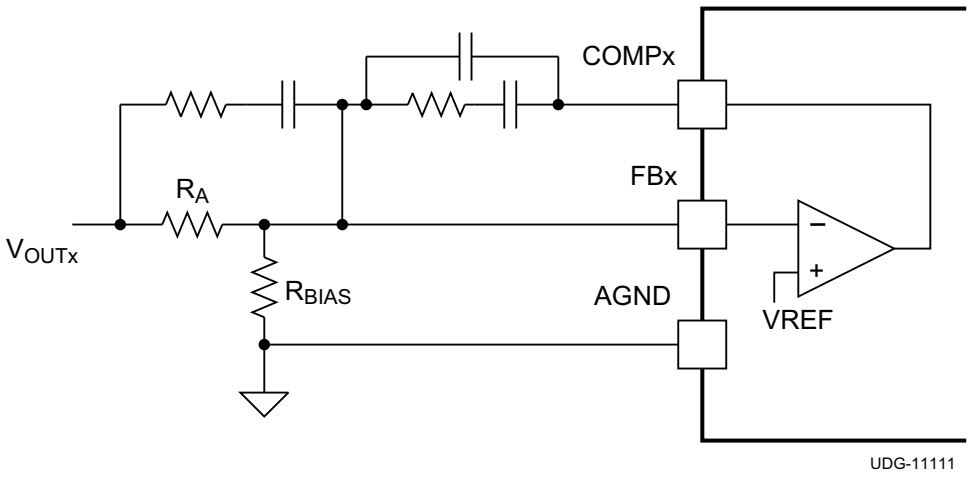


Figure 15. Setting the Output Voltage

$$V_{OUT} = 0.6\,V \times \left(1 + \frac{R_A}{R_{BIAS}}\right) \quad (1)$$

Input Voltage Feed-Forward

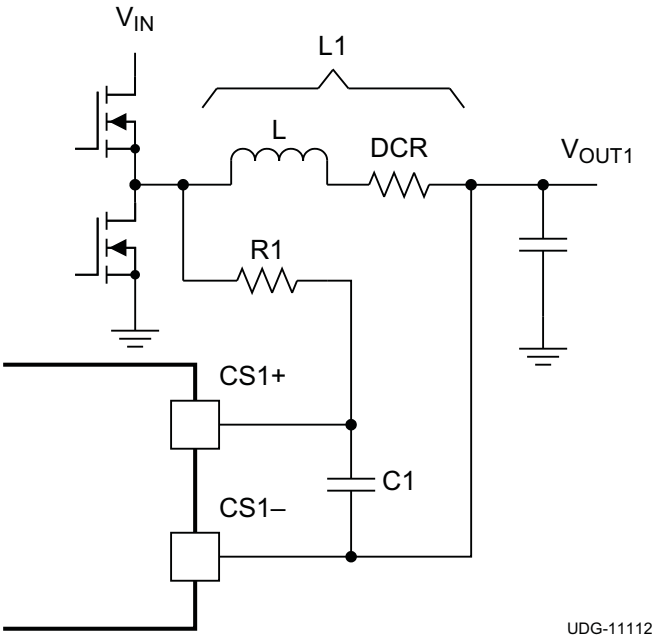
The TPS40322 uses input voltage feed-forward to maintain a constant power stage gain as the input voltage varies and provides very good response to input voltage transient disturbances. The simple constant power stage gain of the controller greatly simplifies feedback loop design because the loop characteristics remain constant as the input voltage changes, unlike a typical buck converter without voltage feed-forward. For modeling purposes, the gain from the COMP pin to the average voltage at the input of the L-C filter is typically 8.5 V/V.

Current Sensing

The TPS40322 uses a differential current sense design to sense the output current. The sense element can be either the series resistance of the power stage filter inductor or a separate current sense resistor. When using the inductor series resistance as shown in Figure 16, an R-C filter must be used to remove the large AC component voltage across the inductor so that only the component of the voltage that remains is across the resistance of the inductor. (See Figure 16)

The values of R1 and C1 for an ideal design can be calculated using Equation 2. The time constant of the R-C filter should equal the time constant of the inductor itself. If the time constants are equal, the voltage across C1 equals the current in the inductor multiplied by the inductor resistance. The inductor ripple current is reflected in the voltage across C1. Typically a capacitor with a value of 0.1-µF is recommended for C1.

Please refer to the LAYOUT CONSIDERATIONS section for proper placement of the sensing elements.



$$R1 \times C1 = \frac{L1}{DCR} \quad (2)$$

Figure 16. Inductor DCR Current Sensing

Overcurrent Protection

The TPS40322 has dedicated ILIM pins for each channel for use when operating in dual-output mode. When operating in two-phase mode, both channels share the same overcurrent level set by ILIM1. The overcurrent level is set with a resistor connected from the ILIMx pin to analog ground. The sensed current signal is amplified by the CS amplifier with a gain of 15, and then compared with the established overcurrent level to determine if there is an OC fault. This design is shown in Figure 17.

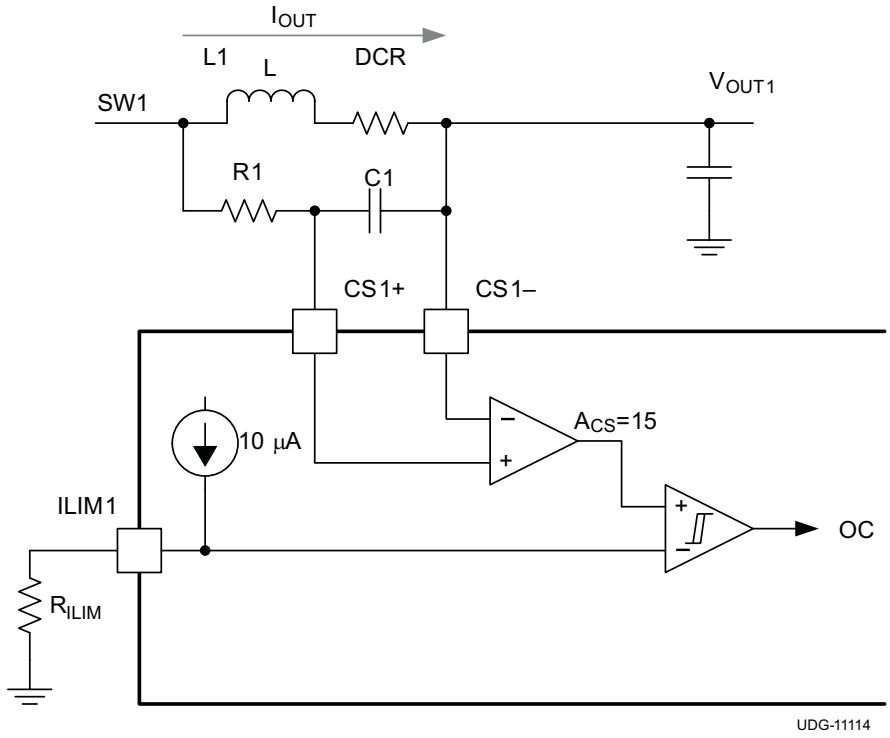


Figure 17. Overcurrent Protection

Equation 3 shows the current limit resistance (R_{LIM}) calculation for desired overcurrent limit.

$$R_{LIM} = \frac{\left(I_{OC} + \left(\frac{I_{RIPPLE}}{2}\right)\right) \times DCR \times A_{CS}}{I_{ILIM}} \quad (3)$$

where

- I_{OC} is the desired DC over current limit level
- I_{RIPPLE} is the inductor peak-peak ripple current
- DCR is the inductor DC resistance
- A_{CS} is the current sensing amplifier gain (typically 15)
- I_{ILIM} is the internal source current out of ILIMx pin (typically 10 µA)

The TPS40322 implements cycle-by-cycle current limit when the inductor peak current has exceeded the set limit. When the controller counts three consecutive clock cycles of an overcurrent condition, the high-side and low-side MOSFETs are turned off and the controller enters a hiccup mode. After six soft-start cycles, normal switching is attempted. If the overcurrent has cleared, normal operation resumes, otherwise the sequence repeats.

Two-Phase Mode, Remote Sense Amplifier, and Current Sharing Loop

The TPS40322 can be configured to operate in single-output, two-phase mode for high-current applications. With proper selection of the external MOSFETs, this device can support up to 50-A of load current in a two-phase configuration. As shown in Figure 18, to configure the TPS40322 for two-phase mode, FB2 is tied to BP6. In this mode, COMP1 must be connected to COMP2 to ensure current sharing between the two phases. For high-current applications, the remote sense amplifier is used to compensate for the parasitic offset to provide an accurate output voltage. The EN2/SS2 and ILIM2 pins are designed for multiple functions. They are used as VSNS and GSNS for remote sensing in two-phase mode. DIFFO, which is the output of the remote sensing amplifier, is connected to the resistor divider of the feedback network.

Note that BP6 powers the remote sense amplifier. The DIFFO voltage must be 0.2-V lower than the BP6 voltage under all conditions. If BP6 is lower than DIFFO voltage, the converter loses regulation. To ensure no regulation loss, use a remote sense amplifier when the application output voltage is lower than 2.2 V. For an application in which the output voltage is higher than 2.2 V, the remote sense amplifier can be bypassed and the voltage output can be connected to the feedback resistor divider directly.

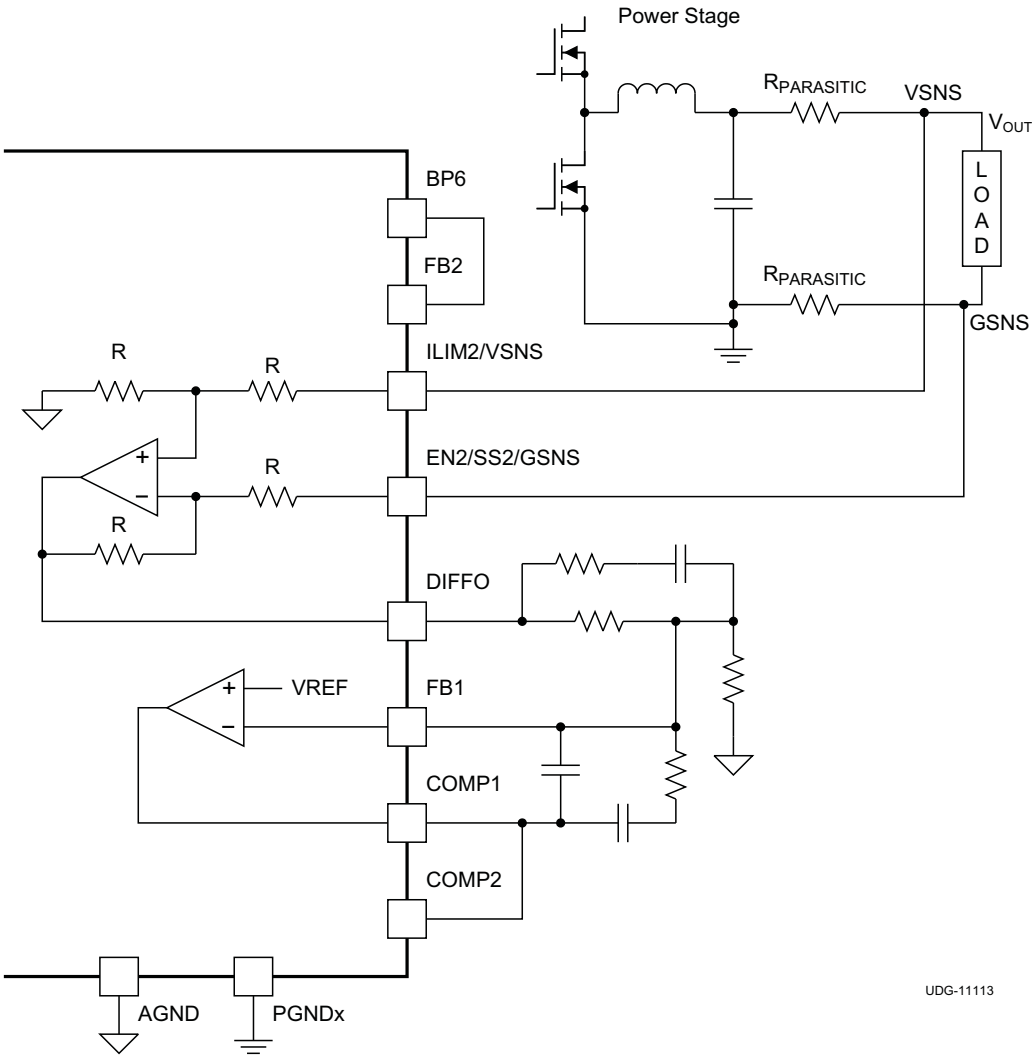


Figure 18. Two-Phase Mode Voltage Loop Configuration

When the device operates in two-phase mode, a current sharing loop as shown in Figure 19 is designed to maintain the current balance between phases. Both phases share the same comparator voltage (COMP1). The sensed current from each phase is compared first in a current share block, then each signal is summed with COMP. The resulted error voltage is compared with the voltage ramp to generate the PWM pulse for each channel.

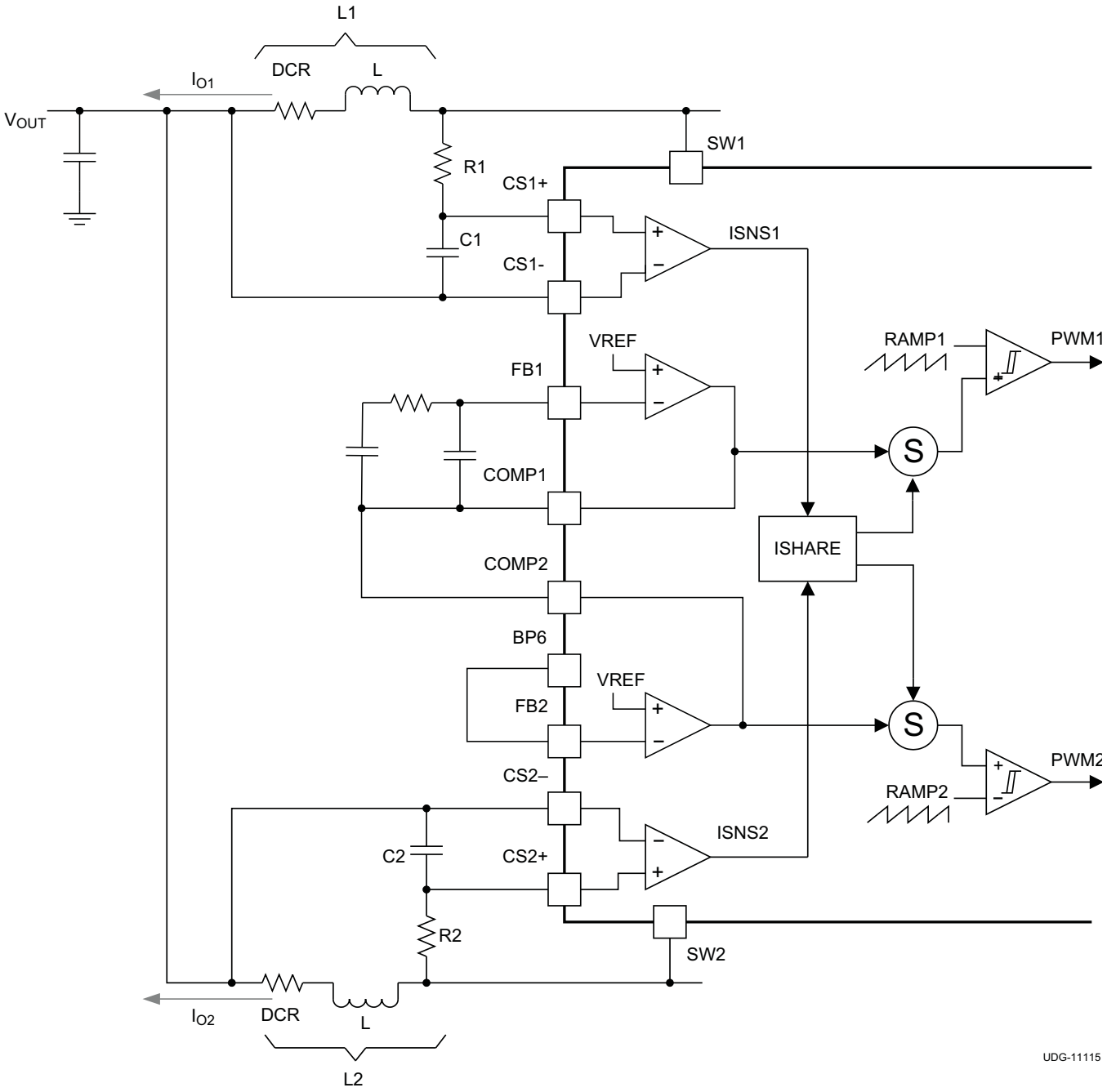


Figure 19. Two-Phase Mode Current Share Loop

Startup and Shutdown

Startup Sequence

When the ENx/SSx pin is pulled below 0.3 V, the respective channel is disabled. When ENx/SSx is released, the controller starts automatically and an internal 40-µA current source begins to charge the external soft-start capacitor. When the voltage across the soft-start capacitor is over 0.7 V, the internal BP regulator is enabled. The ENx/SSx voltage is clamped to 1.3 V while waiting for signals indicating that BP6, VDD, and the oscillator clock are good. After all the signals are confirmed, ENx/SSx is discharged to 0.4 V with a 140-µA current source, and then charged again with the internal 10-µA current source. The operation is described by the waveform shown in Figure 20. V_{SS_INT} is an internal signal level shifted from ENx/SSx and then connected to the non-inverting terminal of the error amplifier.

The soft-start time is determined by the internal charge current and the external capacitance. The actual output ramp-up time is the time for the internal current source to charge the capacitor through a 600 mV range. There is some initial lag time due to the offset (800 mV typical) from the actual ENx/SSx pin voltage to V_{SS_INT}. The soft-start sequence takes place in a closed loop fashion, meaning that the error amplifier controls the output voltage constantly during the soft-start period and the feedback loop is never open (as occurs in duty cycle limit soft-start designs). The error amplifier has two non-inverting inputs, one connected to the 600-mV reference voltage, and the other connected to the offset V_{SS_INT}. The error amplifier controls the FB pin to the lower of these two voltages. As the voltage on the ENx/SSx pin ramps up past approximately 1.4 V (800 mV offset voltage plus the 600 mV reference voltage), the 600 mV reference voltage becomes the dominant input and the converter has reached its final regulation voltage.

Equation 4 shows how to calculate the soft start capacitance.

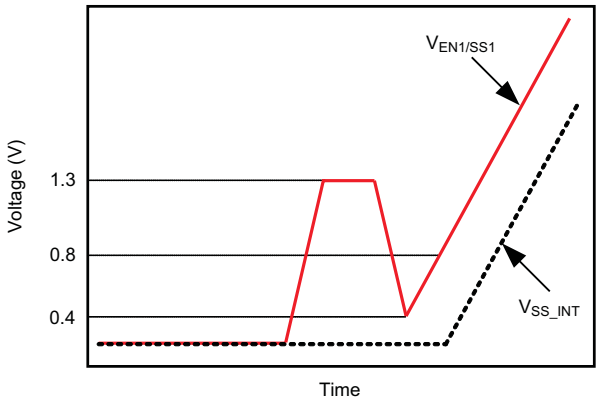


Figure 20. EN/SS Start-Up Waveform

$$C_{SS} = \frac{t_{SS} \times I_{SS}}{600\,mV} \quad (4)$$

where

- C_{SS} is the soft start capacitance connected to ENx/SSx pin
- t_{SS} is the desired soft-start time
- I_{SS} is the internal soft-start current (typically 10 µA)

Pre-Biased Output Start-Up

The TPS40322 contains a circuit that prevents current from being pulled from the output during the start-up sequence in a pre-biased output condition. There are no PWM pulses until the internal soft-start voltage rises above the error amplifier input (FBx pin), if the output is pre-biased. Once the soft-start voltage exceeds the error amplifier input, the device slowly initiates synchronous rectification by starting the synchronous rectifier with a narrow on-time. It then increments that on-time on a cycle-by-cycle basis until it coincides with the time dictated by (1-D), where D is the duty cycle of the converter. This approach prevents the sinking of current from a pre-biased output, and ensures the output voltage start-up and ramp-to-regulation sequences are smooth and controlled.

DESIGN NOTE

During the soft-start sequence, when the PWM pulse width is shorter than the minimum controllable on-time, which is generally caused by the PWM comparator and gate driver delays, pulse skipping may occur and the output might show larger ripple voltage.

Shutdown

During the shutdown sequence, BP6 is controlled by ENx/SSx. If both of ENx/SSx pins are pulled low, BP6 is turned off regardless of the input voltage remaining higher than the programmed UVLO threshold.

Switching Frequency and Master/Slave Synchronization

The switching frequency is set by the value of the resistor connected from the RT pin to AGND. The RT resistor value is calculated in Equation 5.

$$R_{RT} = \frac{20 \times 10^9}{f_{SW}} \quad (5)$$

where

- R_{RT} is the the resistor from RT pin to AGND, in Ω
- f_{SW} is the desired switching frequency, in Hz

The TPS40322 device can also synchronize to an external clock that is ±20% of the master clock frequency which is two times the free running frequency. Each TPS40322 can be set by the PHSET pin as either master or slave. The master produces a 50% duty cycle clock to the slave. The slave synchronizes to the external clock with 50% duty cycle and selects the phase shift angle as shown in Table 2.

Figure 21 shows an example on synchronizing two TPS40322 devices to generate an evenly distributed shift to reduce input ripple.

Table 2. Phase Shift Angle Selection

PHSET		MODE	PHASE ANGLE (°)	
CONNECTION	RANGE (V)		CH1	CH2
AGND	< 0.5	Master	0	180
Floating	0.6 to 2	Slave	0	180
High	> 2.1	Slave	90	270

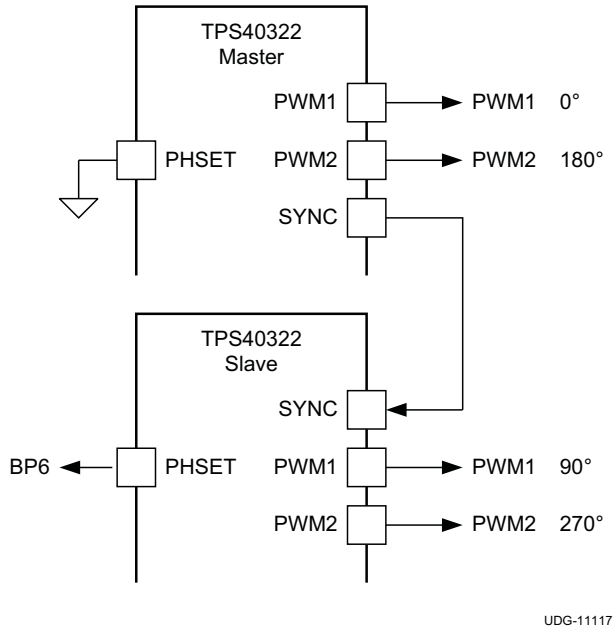


Figure 21. Synchronizing Two TPS40322 Devices

Overvoltage and Undervoltage Fault Protection

The TPS40322 has output overvoltage protection and undervoltage protection capability. The comparators that regulate the overvoltage and undervoltage conditions use the FBx pin as the output sensing point so the filtering effect of the compensation network connected from COMPx to FBx has an effect on the speed of detection. As the output voltage rises or falls below the nominal value, the error amplifier attempts to force FBx to match its reference voltage. When the error amplifier is no longer able to do this, the FB pin begins to drift and trip the overvoltage threshold (V_{OVP}) or the undervoltage threshold (V_{UVP}) as described in the ELECTRICAL CHARACTERISTICS table.

When an undervoltage fault is detected, the TPS40322 enters hiccup mode and resumes normal operation when the fault is cleared.

When an overvoltage fault is detected, the TPS40322 turns off the high-side MOSFET and latches on the low-side MOSFET to discharge the output current to the regulation level (within the power good window).

When operating in dual-channel mode, both channels have identical but independent protection schemes which means one channel would not be affected when the other channel is in fault mode.

When operating in two-phase mode, only the FB1 pin is detected for overvoltage and undervoltage fault. Therefore both channels take action together during a fault.

Input Undervoltage Lockout (UVLO)

A dedicated UVLO pin allows the user to program the desired input turn-on threshold voltage. The diagram is shown in Figure 22. The desired input turn-on threshold can be calculated using Equation 6. The input turn off hysteresis can be calculated using Equation 7.

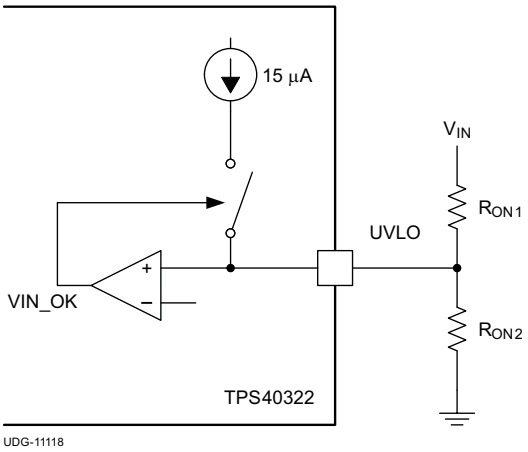


Figure 22. Input UVLO Diagram

$$VIN\_UVLO = 1.24\,V \times \left(\frac{(R_{ON1} + R_{ON2})}{R_{ON2}} \right) \quad (6)$$

$$VIN\_HYS = 15\,\mu A \times R_{ON1} \quad (7)$$

Power Good

The TPS40322 provides an indication that output is good for each channel. This is an open-drain signal that pulls low when any condition exists that would indicate that the output of the supply might be out of regulation. These conditions include:

- Feedback voltage (V_{FB}) is more than ±12.5% from nominal
- Soft-start is active

Thermal Shutdown

If the junction temperature of the device reaches the thermal shutdown limit of 150°C, the PWMs and the oscillators are turned off and HDRVs and LDRVs are driven low. When the junction cools to the required level (130°C typical), the PWM initiates soft start as during a normal power-up cycle.

LAYOUT CONSIDERATIONS

Power Stage

A synchronous BUCK power stage has two primary current loops. The input current loop carries high AC discontinuous current while the output current loop carries high DC continuous current. The input current loop includes the input capacitors, the main switching MOSFET, the inductor, the output capacitors and the ground path back to the input capacitors. To maintain the loop as small as possible, it is generally good practice to place some ceramic capacitance directly between the drain of the main switching MOSFET and the source of the synchronous rectifier (SR) through a power ground plane directly under the MOSFETs. The output current loop includes the SR MOSFET, the inductor, the output capacitors, and the ground return between the output capacitors and the source of the SR MOSFET. As with the input current loop, the ground return between the output capacitor ground and the source of the SR MOSFET should be routed under the inductor and SR MOSFET to minimize the power loop area. The SW node area should be as small as possible to reduce the parasitic capacitance and minimize the radiated emissions. The gate drive loop impedance (HDRV-gate-source-SW and LDRV-gate-source- GND) should be kept to as low as possible. The HDRV and LDRV connections should widen to 20 mils as soon as possible out from the device pin.

Device Peripheral

The TPS40322 provides separate signal ground (AGND) and power ground (PGND1 and PGND2) pins. It is required to properly separate the circuit grounds. The return path for the pins associated with the power stage should be through PGND. The other pins (especially for those sensitive pins such as FB1, FB2, RT, ILIM1, and ILIM2) should be through the low noise AGND. The AGND and PGND planes are suggested to be connected at the output capacitor with single 20-mil trace. A minimum 0.1-µF ceramic capacitor must be placed as close to the VDD pin and AGND as possible with at least 15-mil wide trace from the bypass capacitor to the AGND. A minimum value of 3.3-µF ceramic capacitor should be connected from BP6 to PGND, placed as close to the BP6 pin as possible. When DCR sensing method is applied, the sensing resistor should be placed close to the SW node and connected to the inductor with a Kelvin connection. The sensing traces from the power stage to the chip should be away from the switching components. The sensing capacitor should be placed very close to the CS+ and CS- pins for each output. The frequency setting resistor should be placed as close to RT pin and AGND as possible. In two-phase mode, the ILIM2/VSNS and EN2/SS2/GSNS pins should be directly connected to the point of load where the voltage regulation is required. A parallel pair of 10-mil traces connects the regulated voltage back to the chip. They should be away from the switching components. The PowerPAD™ should be electrically connected to AGND.

PowerPAD™ Layout

The PowerPAD™ package provides low thermal impedance for heat removal from the device. The PowerPAD™ derives its name and low thermal impedance from the large bonding pad on the bottom of the device. The circuit board must have an area of solder-tinned-copper underneath the package. The dimensions of this area depend on the size of the PowerPAD™ package.

Thermal vias connect this area to internal or external copper planes and should have a drill diameter sufficiently small so that the via hole is effectively plugged when the barrel of the via is plated with copper. This plug is needed to prevent wicking the solder away from the interface between the package body and the solder-tinned area under the device during solder reflow. Drill diameters of 0.33 mm (13 mils) works well when 1-oz. copper is plated at the surface of the board while simultaneously plating the barrel of the via. If the thermal vias are not plugged when the copper plating is performed, then a solder mask material should be used to cap the vias with a diameter equal to the via diameter plus 0.1 mm minimum. This capping prevents the solder from being wicked through the thermal vias and potentially creating a solder void under the package. Refer to PowerPAD™ Thermally Enhanced Package (TI LIterature Number SLMA002) for more information on the PowerPAD™ package.

TPS40322 Design Example 1

Dual-Output Configuration from 12-V Nominal to 1.2-V and 1.8-V DC-to-DC Converter Using the TPS40322

The following example illustrates the design process and component selection for a dual output synchronous buck converter using the TPS40322 controller. The design goal parameters are listed in Table 3.

Table 3. TPS40322 Dual Output Design Example Specification

PARAMETER		TEST CONDITION	MIN	NOM	MAX	UNIT
INPUT CHARACTERSTICS						
V_{IN}	Input voltage		8	12	15	V
$V_{IN(ripple)}$	Input ripple	$I_{OUT1} = I_{OUT2} = 10$ A			0.25	V
OUTPUT 1 CHARACTERSTICS						
V_{OUT1}	Output voltage	$I_{OUT1(min)} \le I_{OUT1} \le I_{OUT1(max)}$		1.2		V
	Line regulation	$V_{IN(min)} \le V_{IN} \le V_{IN(max)}$			0.5%	
	Load regulation	$I_{OUT1(min)} \le I_{OUT1} \le I_{OUT1(max)}$			0.5%	
$V_{RIPPLE1}$	Output ripple	$I_{OUT1} = I_{OUT1(max)}$			24	mV
V_{OVER1}	Output overshoot	$\Delta I_{OUT1} = 5$ A		40		mV
V_{UNDER1}	Output undershoot	$\Delta I_{OUT1} = 5$A		40		mV
I_{OUT1}	Output current	$V_{IN(min)} \le V_{IN} \le V_{IN(max)}$	0		10	A
I_{SCP1}	Short circuit current trip point			15		A
OUTPUT 2 CHARACTERSTICS						
V_{OUT2}	Output voltage	$I_{OUT2(min)} \le I_{OUT2} \le I_{OUT2(max)}$		1.8		V
	Line regulation	$V_{IN(min)} \le V_{IN} \le V_{IN(max)}$			0.5%	
	Load regulation	$I_{OUT2(min)} \le I_{OUT2} \le I_{OUT2(max)}$			0.5%	
$V_{RIPPLE2}$	Output ripple	$I_{OUT2} = I_{OUT2(max)}$			36	mV
V_{OVER2}	Output overshoot	$\Delta I_{OUT2} = 5$ A		40		mV
V_{UNDER2}	Output undershoot	$\Delta I_{OUT2} = 5$ A		40		mV
I_{OUT2}	Output current	$V_{IN(min)} \le V_{IN} \le V_{IN(max)}$	0		10	A
I_{SCP2}	Short circuit current trip point			15		A
GENERAL CHARACTERSTICS						
t_{SS}	Soft-start time	$V_{IN} = 12$ V		2		ms
η	Efficiency	$V_{IN} = 12$ V, $I_{OUT1} = I_{OUT2} = 10$ A		88%		
f_{SW}	Switching frequency			500		kHz

Design Procedure

Equations and calculations are shown regarding V_{OUT1}. V_{OUT2} values can be calculated using similar equations.

Selecting a Switching Frequency

To maintain acceptable efficiency and meet minimum on-time requirements, a 500kHz switching frequency is selected.

Inductor Selection (L1)

Synchronous BUCK power inductors are typically sized for approximately 20% - 40% peak-to-peak ripple current (I_{RIPPLE}). Given a target ripple current of 30%, the required inductor size, at maximum rated output current, can be calculated using Equation 8.

$$L1 \approx \frac{V_{IN(max)} - V_{OUT1}}{0.3 \times I_{OUT1}} \times \frac{V_{OUT1}}{V_{IN(max)}} \times \frac{1}{f_{SW}} = \frac{15\,V - 1.2\,V}{0.3 \times 10\,A} \times \frac{1.2\,V}{15\,V} \times \frac{1}{500\,kHz} = 0.736\,\mu H \quad (8)$$

Selecting a standard, readily available inductor, with a rated inductance is 0.88 µH at 10 A, $I_{RIPPLE1} = 2.5$ A

The RMS current through the inductor is approximated by the equation:

$$I_{L1(rms)} = \sqrt{\left(I_{L1(avg)}\right)^2 + \left(\tfrac{1}{12} \times I_{RIPPLE1}\right)^2} = \sqrt{\left(I_{OUT1}\right)^2 + \left(\tfrac{1}{12} \times I_{RIPPLE1}\right)^2} = \sqrt{10^2 + \left(\tfrac{1}{12} \times 2.5\right)^2} = 10.026\,A \quad (9)$$

Output Capacitor Selection (C10 through C16)

The selection of the output capacitor is typically driven by the output transient response requirement. Equation 10 and Equation 11 over-estimate the voltage deviation to account for delays in the loop bandwidth and can be used to determine the required output capacitance:

$$V_{OVER1} < \frac{\Delta I_{OUT1}}{C_{OUT1}} \times \Delta t = \frac{\Delta I_{OUT1}}{C_{OUT1}} \times \frac{\Delta I_{OUT1} \times L1}{V_{OUT1}} = \frac{\left(\Delta I_{OUT1}\right)^2 \times L1}{V_{OUT1} \times C_{OUT1}} \quad (10)$$

$$V_{UNDER1} < \frac{\Delta I_{OUT1}}{C_{OUT1}} \times \Delta t = \frac{\Delta I_{OUT1}}{C_{OUT1}} \times \frac{\Delta I_{OUT1} \times L1}{V_{IN} - V_{OUT1}} = \frac{\left(\Delta I_{OUT1}\right)^2 \times L1}{\left(V_{IN} - V_{OUT1}\right) \times C_{OUT1}} \quad (11)$$

When $V_{IN(min)} > 2 \times V_{OUT1}$, use the overshoot equation, V_{OVER1}, to calculate minimum output capacitance. When $V_{IN(min)} < 2 \times V_{OUT1}$ use Equation 11, V_{UNDER1}, to calculate minimum output capacitance. In this design example, $V_{IN(min)}$ is much larger than $2 \times V_{OUT1}$ so Equation 12 is used to determine the required minimum output capacitance.

$$C_{OUT1(min)} = \frac{\left(\Delta I_{OUT1}\right)^2 \times L1}{V_{OUT} \times V_{OVER1}} = \frac{5^2 \times 0.88\,\mu H}{1.2 \times 40\,mV} = 458\,\mu F \quad (12)$$

With a minimum capacitance, the maximum allowable ESR is determined by the maximum ripple voltage and is approximated by Equation 13.

$$ESR_{MAX} = \frac{V_{RIPPLE1} - V_{RIPPLE(cap)}}{I_{RIPPLE1}} = \frac{V_{RIPPLE1} - \left(\frac{I_{RIPPLE1}}{8 \times C_{OUT1} \times f_{SW}}\right)}{I_{RIPPLE1}} = \frac{24\,mV - \left(\frac{2.5\,A}{8 \times 458\,\mu F \times 500\,kHz}\right)}{2.5\,A} = 9\,m\Omega \quad (13)$$

Two 220-µF, 4-V, aluminum electrolytic capacitors were chosen for load response requirements. Additionally two 0805 10-µF, X7R, along with two 0603, 3.3-µF X5R, and one 1-µF, X5R ceramic capacitors are selected for low ESR and high frequency decoupling.

Peak Current Rating of Inductor

With the output capacitance known, it is possible to calculate the charge current during start-up and determine the minimum saturation current rating for the inductor. The start-up charging current is approximated using Equation 14.

$$I_{CHARGE} = \frac{V_{OUT1} \times C_{OUT1}}{t_{SS}} = \frac{1.2\,V \times \left(2 \times 220\,\mu F + 2 \times 10\,\mu F + 2 \times 3.3\,\mu F + 1\mu F\right)}{2ms} = 0.281A \quad (14)$$

$$I_{L1(peak)} = I_{OUT1(max)} + \left(\tfrac{1}{2} \times I_{RIPPLE1}\right) + I_{CHARGE} = 10\,A + \left(\tfrac{1}{2} \times 2.5A\right) + 0.281A = 11.53\,A \quad (15)$$

Table 4. Inductor Requirements Summary

PARAMETER		VALUE	UNITS
L1	Inductance	0.88	µH
IL1_RMS	RMS current (thermal rating)	10.026	A
IL1_PEAK	Peak current (saturation rating)	11.53	A

A 744314110 from Wurth-Midcom with 1.1-µH zero current inductance is selected. Inductance for this part is 0.88-µH at 10 A bias. This 15-A, 3.15 mΩ inductor exceeds the minimum inductor ratings in a 7 mm x 7 mm package.

Input Capacitor Selection (C3 through C6)

The input voltage ripple is divided between the capacitance and ESR of the input capacitor. For this design $V_{RIPPLE(cap)}$ = 200 mV and $V_{RIPPLE(esr)}$ = 50 mV. The minimum capacitance and maximum ESR are estimated using Equation 16.

$$C_{IN1(min)} = \frac{I_{OUT1} \times V_{OUT1}}{V_{RIPPLE(cap)} \times V_{IN(min)} \times f_{SW}} = \frac{10\,A \times 1.2\,V}{200\,mV \times 8\,V \times 500\,kHz} = 15\,\mu F \quad (16)$$

$$ESR_{MAX} = \frac{V_{RIPPLE(esr)}}{I_{OUT1} + \left(\frac{1}{2} \times I_{RIPPLE1}\right)} = \frac{50\,mV}{11.25\,A} = 4.44\,m\Omega \quad (17)$$

The RMS current in the input capacitors is estimated using Equation 18.

$$I_{RMS(cin1)} = I_{OUT1} \times \sqrt{D \times (1-D)} = 10\,A \times \sqrt{0.15 \times (1-0.15)} = 3.57\,A \quad (18)$$

$$D = \frac{V_{OUT1}}{V_{IN(min)}} \quad (19)$$

To achieve these goals, two 0805, 10-µF capacitors, one 0605, 1.0-µF capacitor and one 0402, 0.1-µF X5R ceramic capacitor are combined at the input.

MOSFET Selection (Q1)

Texas Instruments CSD86330, 20-A power block device was chosen. This device incorporates the high-side and low-side MOSFETs in a single 3 mm x 3 mm package. The high-side MOSFET has an on-resistance ($R_{DS(on)}$) of 8.8 mΩ, while the low-side on-resistance ($R_{DS(on)}$) is 4.6 mΩ, both at 4.5 V gate voltage. A 5.11-Ω gate resistor is used on the HDRV pin on each device for added noise immunity.

ILIM Resistor (R2)

The output current is sensed across the DCR of the L1 output inductor. An RC combination having a time constant equal to that of the L1 inductance and the DCR is used to extract the current information as a voltage. A standard capacitor value of 0.1-µF is used. The resistor, R13, can be calculated using Equation 20.

$$R13 = \frac{L1}{C \times V_{DCR}} = \frac{0.88\,\mu H}{0.1\,\mu F \times 3.15\,m\Omega} = 2.8\,k\Omega \quad (20)$$

A standard 3.09-kΩ resistor was selected.

This design limits the maximum voltage drop across the current sense inputs, $V_{CS(max)}$, to 50 mV. If the voltage drop across the DCR of the inductor is greater than $V_{CS(max)}$, after allowing for 30% overshoot spikes and a 20% variation in the DCR value, then a resistor is added to divide the voltage down to 50 mV. The divider resistor, R15, is calculated by Equation 21.

$$R15 = \frac{R13 \times V_{CS(max)}}{\left(V_{DCR} - V_{CS(max)}\right)}$$

where

$$V_{DCR} = (DCR \times 1.2) \times \left(I_{L(peak)} \times 1.3\right) \quad (22) \quad (22)$$

The maximum DCR voltage drop is given by Equation 23.

$$V_{OC} = \left[\left(I_{OUT1} + \frac{I_{RIPPLE1}}{2}\right) \times 1.2\right] \times (DCR \times 1.2) = \left[\left(10\,A + \frac{2.5\,A}{2}\right) \times 1.2\right] \times (3.15\,m\Omega \times 1.2) = 51.05\,mV \quad (23)$$

The current limit resistor is calculated using the minimum ILIM programming current, $I_{ILIM(min)}$, the maximum current sense amplifier gain, A_{CS}, and assuming a current sense amplifier minimum input offset voltage, $V_{OS(min)}$ equal to –3 mV.

$$R_{LIM} = \frac{\left(V_{OC} - V_{OS(min)}\right) \times A_{CS}}{I_{ILIM(min)}} = \frac{\left(51.05\,mV - \left(-3\,mV\right)\right) \times 15\,V/V}{9.5\,\mu A} = 85.3\,k\Omega \cong 86.6\,k\Omega \quad (24)$$

Feedback Divider (R10, R14)

The TPS40322 controller uses a full operational amplifier with an internally fixed 0.600-V reference. Tha value for R10 is selected between 10-kΩ and 50-kΩ for a balance of feedback current and noise immunity. With the R10 resistor set to 20-kΩ, the output voltage is programmed with a resistor divider given by Equation 25.

$$R14 = \frac{V_{FB} \times R10}{V_{OUT1} - V_{FB}} = \frac{0.600\,V \times 20.0\,k\Omega}{1.2\,V - 0.600\,V} = 20\,k\Omega \quad (25)$$

Compensation: (R11, R12, C17, C19, C21)

Using the ***TPS40k Loop Stability Tool*** for an 85-kHz bandwidth and 50° of phase margin with an R10 value of 20.0 kΩ, and measuring the theoretical results in the laboratory and modifying accordingly for system optimization yields the following values.

- C21 = 10 pF
- C17 = 220 pF
- C19 = 470 pF
- R12 = 4.42 kΩ
- R11 = 82.5 kΩ

Boot-Strap Capacitor (C7)

To ensure proper charging of the high-side FET gate, limit the ripple voltage on the boost capacitor to < 100 mV.

$$C_{BOOST} = \frac{Q_{G1}}{V_{BOOT(ripple)}} = \frac{7\,nC}{100\,mV} = 70\,nF \approx 100\,nF \quad (26)$$

General Device Components

Synchronization (SYNC Pin)

The SYNC pin should be left open for independent dual outputs.

RT Resistor (R6)

The desired switching frequency is programmed by the current through R_{RT} to GND. the value of R_{RT} is calculated using Equation 27.

$$R_{RT} = \frac{20^9}{f_{SW}} = \frac{20^9}{500\,kHz} = 40\,k\Omega \approx 40.2\,k\Omega \quad (27)$$

Differential Amplifier Out (DIFFO Pin)

In dual output configuration the DIFFO pin is not used and must remain open (unconnected).

EN/SS Timing Capacitors (C8)

The soft-start capacitor provides smooth ramp of the error amplifier reference voltage for controlled start-up. The soft-start capacitor is selected using Equation 28.

$$C_{SS} = \frac{t_{SS} \times I_{SS}}{V_{FB}} = \frac{2\,ms \times 10\,\mu A}{0.6\,V} \approx 33\,nF \quad (28)$$

Power Good (PG1, PG2 Pins)

PG1 and PG2 can each be pulled up to BP6 through a 100-kΩ resistor, or remain not-connected. For sequencing the start-up of output 1 before output 2, connect PG1 to EN2/SS2; for sequencing the startup of output 2 before output 1, connect PG2 to EN1/SS1.

Phase Set (PHSET Pin)

The PHSET pin can be connected to ground or connected to the BP6 pin.

UVLO Programming Resistors (R1 and R3)

The UVLO hysteresis level is programmed by R1 with Equation 29 and Equation 30.

$$R_{UVLO(hys)} = \frac{V_{UVLO(on)} - V_{UVLO(off)}}{I_{UVLO}} = \frac{8\,V - 7\,V}{15\,\mu A} = 66.7\,k\Omega \approx 68.1\,k\Omega \quad (29)$$

$$R_{UVLO(set)} > R_{UVLO(hys)} \times \frac{V_{UVLO(max)}}{\left(V_{UVLO(on\_min)} - V_{UVLO(max)}\right)} = 68.1\,k\Omega \frac{1.25\,V}{\left(8.0\,V - 1.25\,V\right)} = 12.6\,k\Omega \approx 12.7\,k\Omega \quad (30)$$

VDD Bypass Capacitor (C2)

As shown in the ELECTRICAL CHARACTERISTICS table, a 0.1-µF, 50-V, X7R capacitor has been selected for VDD bypass.

VBP6 Bypass Capacitor (C18)

Per the TPS40322 datasheet, select a 3.3-µF (or greater) low ESR capacitor for BP6. For this design a 3.3-µF, X5R ceramic capacitor was chosen

Schematic

Figure 23 shows the dual output converter schematic for this design example

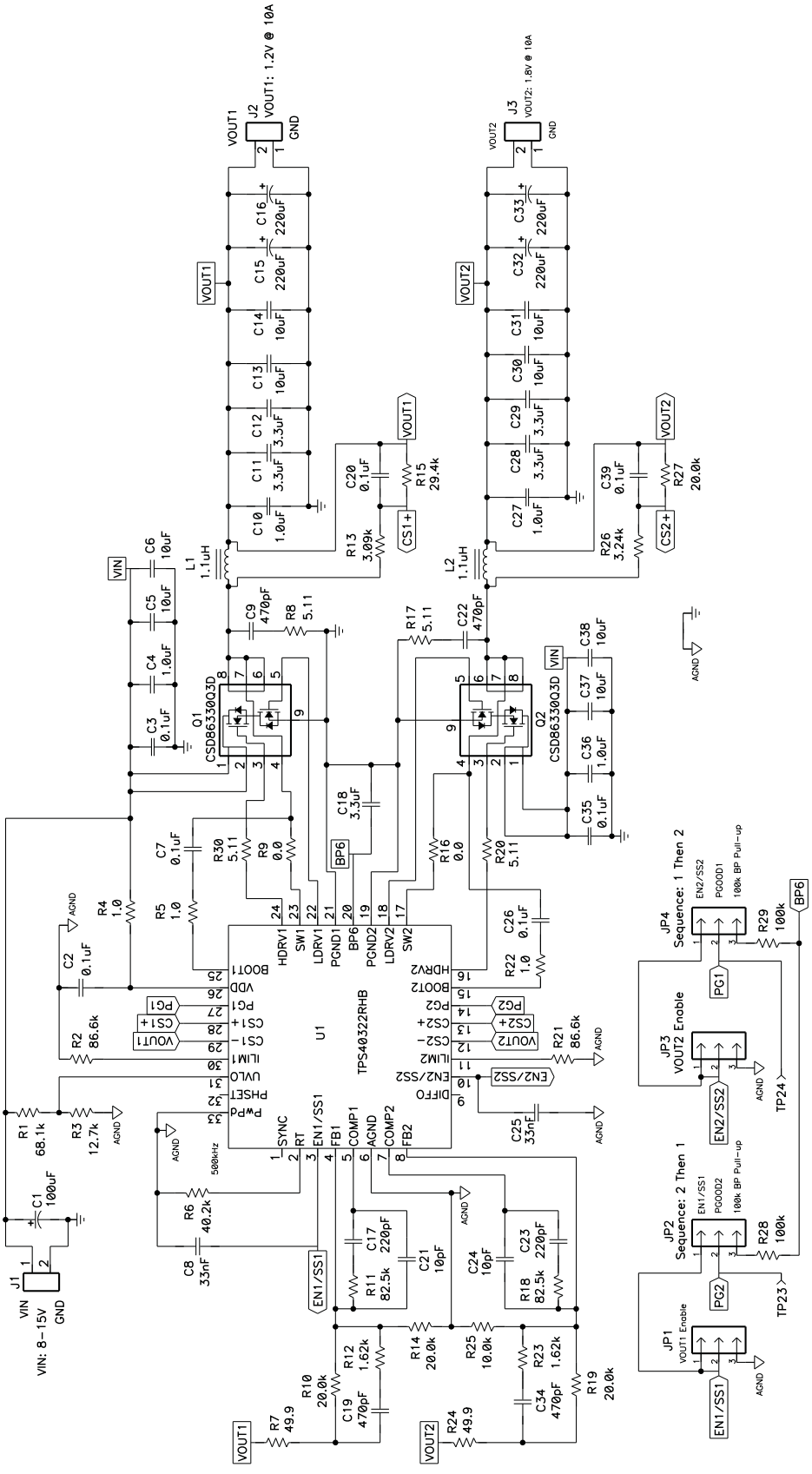


Figure 23. Design Example 1, Dual Output Converter Schematic

Typical Performance Characteristics

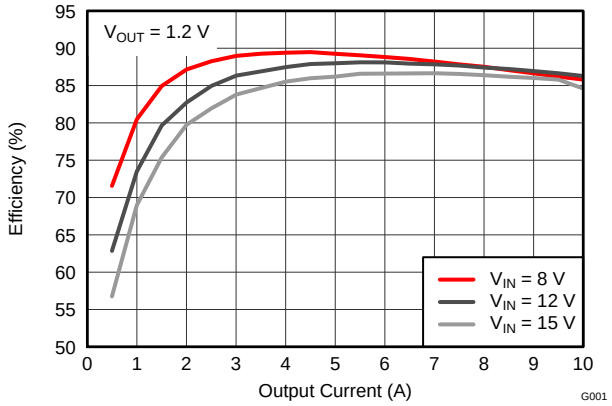


Figure 24. Efficiency vs Load Current (8 V to 15 V to 1.2 V at 10 A, Design Example 1)

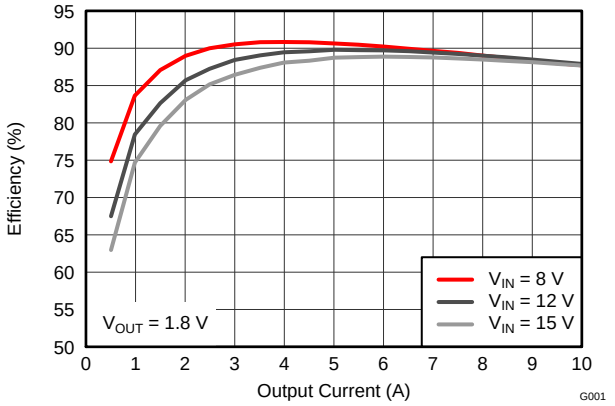


Figure 25. Efficiency vs Load Current (8 V to 15 V to 1.8 V at 10 A, Design Example 1)

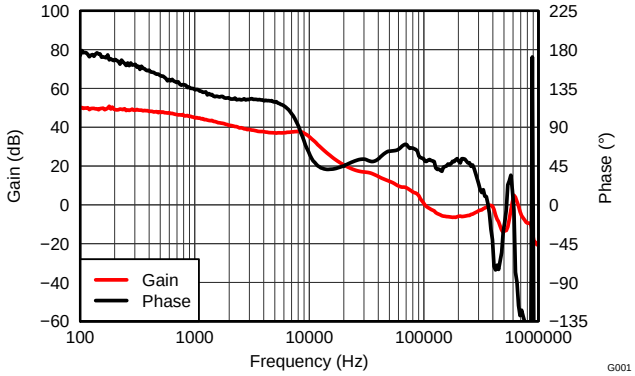


Figure 26. Design Example 1 Loop Response V_{IN} = 12 V, V_{OUT1} = 1.2 V, I_{OUT1} = 10 A, 80-kHz Bandwidth, 50° Phase Margin

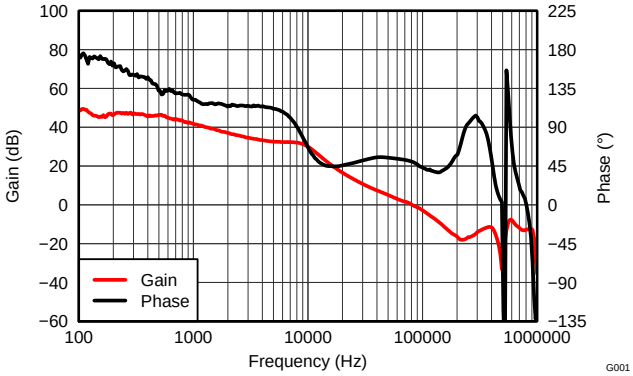


Figure 27. Design Example 1 Loop Response V_{IN} = 12 V, V_{OUT2} = 1.8 V, I_{OUT2} = 10 A, 80-kHz Bandwidth, 50° Phase Margin

Figure 28 shows the switching waveform, V_{IN} = 12 V, I_{OUT1} = I_{OUT2} = 10 A, Ch.1 = HDRV1, Ch.2 = LDRV1, Ch.3 = VOUT1 ripple. The high-frequency noise is caused by parasitic inductive and capacitive elements interacting with the high energy, rapidly switching power elements resulting in ringing at the transition points. Capacitive filtering at the load input will successfully attenuate these noise spikes.

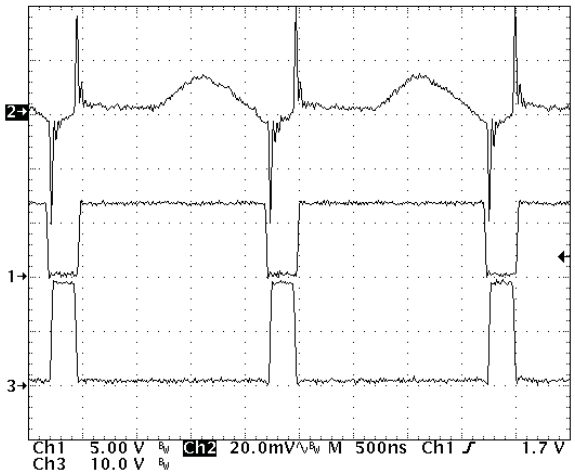


Figure 28. Design Example 1 Switching Waveform

Table 5. Design Example 1, *Dual-Output* List of Materials

REFERENCE DESIGNATOR	QTY	DESCRIPTION	PART NUMBER	MFR
C1	1	Capacitor, Aluminum, 100 µF, 35 V, ±20%, 0.328 x 0.328 inch	EEV-FK1V101GP	Panasonic - ECG
C2, C7, C20, C26, C39	5	Capacitor, Ceramic, 0.1 µF, 50 V, X7R, ±10%, 0603	Std	Std
C3, C35	2	Capacitor, Ceramic, 0.1 µF, 25 V, X5R, ±10%, 0402	Std	Std
C4, C36	2	Capacitor, Ceramic, 1.0 µF, 25 V, X7R, ±10%, 0603	Std	Std
C5, C6, C37, C38	4	Capacitor, Ceramic, 10 µF, 25 V, X5R, ±10%, 0805	Std	Std
C8, C25	2	Capacitor, Ceramic, 33 nF, 16 V, X7R, ±10%, 0603	Std	Std
C9, C19, C22, C34	4	Capacitor, Ceramic, 470 pF, 25 V, C0G, NP0, ±5%, 0603	Std	Std
C10, C27	2	Capacitor, Ceramic, 1.0 µF, 6.3 V, X5R, ±10%, 0402	Std	Std
C11, C12, C18, C28, C29	5	Capacitor, Ceramic, 3.3 µF, 10 V, X5R, ±10%, 0603	C1608X5R1A335K	TDK Corporation
C13, C14, C30, C31	4	Capacitor, Ceramic, 10 µF, 6.3 V, X7R, ±10%, 0805	Std	Std
C15, C16, C32, C33	4	Capacitor, Polymer Aluminum, 220 µF, 4 V, ±20%, 5mM ESR	EEF-SE0G221ER	Panasonic - ECG
C17, C23	2	Capacitor, Ceramic, 220 pF, 50 V, C0G, NP0, ±5%, 0603	Std	Std
C21, C24	2	Capacitor, Ceramic, 10 pF, 50 V, C0G, NP0, ±5%, 0603	Std	Std
C40	1	Capacitor, Ceramic, 1.0 nF, 25 V, C0G, NP0, ±5%, 0603	Std	Std
L1, L2	2	Inductor, Power Choke, 1.1 µH, ±20%, 3.15mΩ, 7.0 x 6.9 mm	744314110	Wurth Elektronik
Q1, Q2	2	MOSFET, Synchronous Buck NexFET Power Block, QFN-8 POWER	CSD86330Q3D	Texas Instruments
R1	1	Resistor, Chip, 68.1 kΩ, 1/10W, ±1%, 0603	Std	Std
R2, R21	2	Resistor, Chip, 86.6 kΩ, 1/10W, ±1%, 0603	Std	Std
R3	1	Resistor, Chip, 12.7 kΩ, 1/10W, ±1%, 0603	Std	Std
R4, R5, R22	3	Resistor, Chip, 1.00 Ω, 1/10W, ±1%, 0603	Std	Std
R6	1	Resistor, Chip, 40.2 kΩ, 1/10W, ±1%, 0603	Std	Std
R7, R24	2	Resistor, Chip, 49.9 Ω, 1/10W, ±1%, 0603	Std	Std
R8, R17	2	Resistor, Chip, 5.11 Ω, 1/8W, ±1%, 0805	Std	Std
R9, R16	2	Resistor, Chip, 0 Ω, 1/10W, ±1%, 0603	Std	Std
R10, R14, R19, R27	4	Resistor, Chip, 20.0 kΩ, 1/10W, ±1%, 0603	Std	Std
R11, R18	2	Resistor, Chip, 82.5 kΩ, 1/10W, ±1%, 0603	Std	Std
R12, R23	2	Resistor, Chip, 1.62 kΩ, 1/10W, ±1%, 0603	Std	Std
R13	1	Resistor, Chip, 3.09 kΩ, 1/10W, ±1%, 0603	Std	Std
R15	1	Resistor, Chip, 29.4 kΩ, 1/10W, ±1%, 0603	Std	Std
R20, R30	2	Resistor, Chip, 5.11 Ω, 1/10W, ±1%, 0603	Std	Std
R25	1	Resistor, Chip, 10.0 kΩ, 1/10W, ±1%, 0603	Std	Std
R26	1	Resistor, Chip, 3.24 kΩ, 1/10W, ±1%, 0603	Std	Std
R28, R29	2	Resistor, Chip, 100 kΩ, 1/10W, ±1%, 0603	Std	Std
U1	1	TPS40322 Dual Synchronous Buck Controller, QFN-32	TPS40322RHB	Texas Instruments

TPS40322 Design Example 2

Two-Phase, Single Output Configuration from 12-V nominal to 1.2-V DC-to-DC Converter Using the TPS40322

The following example shows the schematic, waveforms, and components for a two-phase, single output synchronous buck converter using the TPS40322 controller. The design goal parameters are given in Table 6.

Table 6. TPS40322 Design Example Specification

PARAMETER		TEST CONDITION	MIN	NOM	MAX	UNIT
V_{IN}	Input voltage		4.5		15	V
V_{OUT}	Output voltage	$I_{OUT(min)} \le I_{OUT} \le I_{OUT(max)}$		1.2		V
	Line regulation	$V_{IN(min)} \le V_{IN} \le V_{IN(max)}$			0.5%	
	Load regulation	$I_{OUT(min)} \le I_{OUT} \le I_{OUT(max)}$			0.5%	
V_{RIPPLE}	Output ripple	$I_{OUT1} = I_{OUT1(max)}$			12	mV
V_{OVER}	Output overshoot	ΔI_{OUT1} = 5 A		40		mV
V_{UNDER}	Output undershoot	ΔI_{OUT1} = 5A		40		mV
I_{OUT}	Output current	$V_{IN(min)} \le V_{IN} \le V_{IN(max)}$	0		30	A
t_{SS}	Soft-start time	V_{IN} = 12 V		2		ms
η	Efficiency	V_{IN} = 12 V, I_{OUT1}= I_{OUT2} = 10 A		88%		
f_{SW}	Switching frequency			500		kHz

Figure 29 shows the two-phase converter schematic described in design example 2.

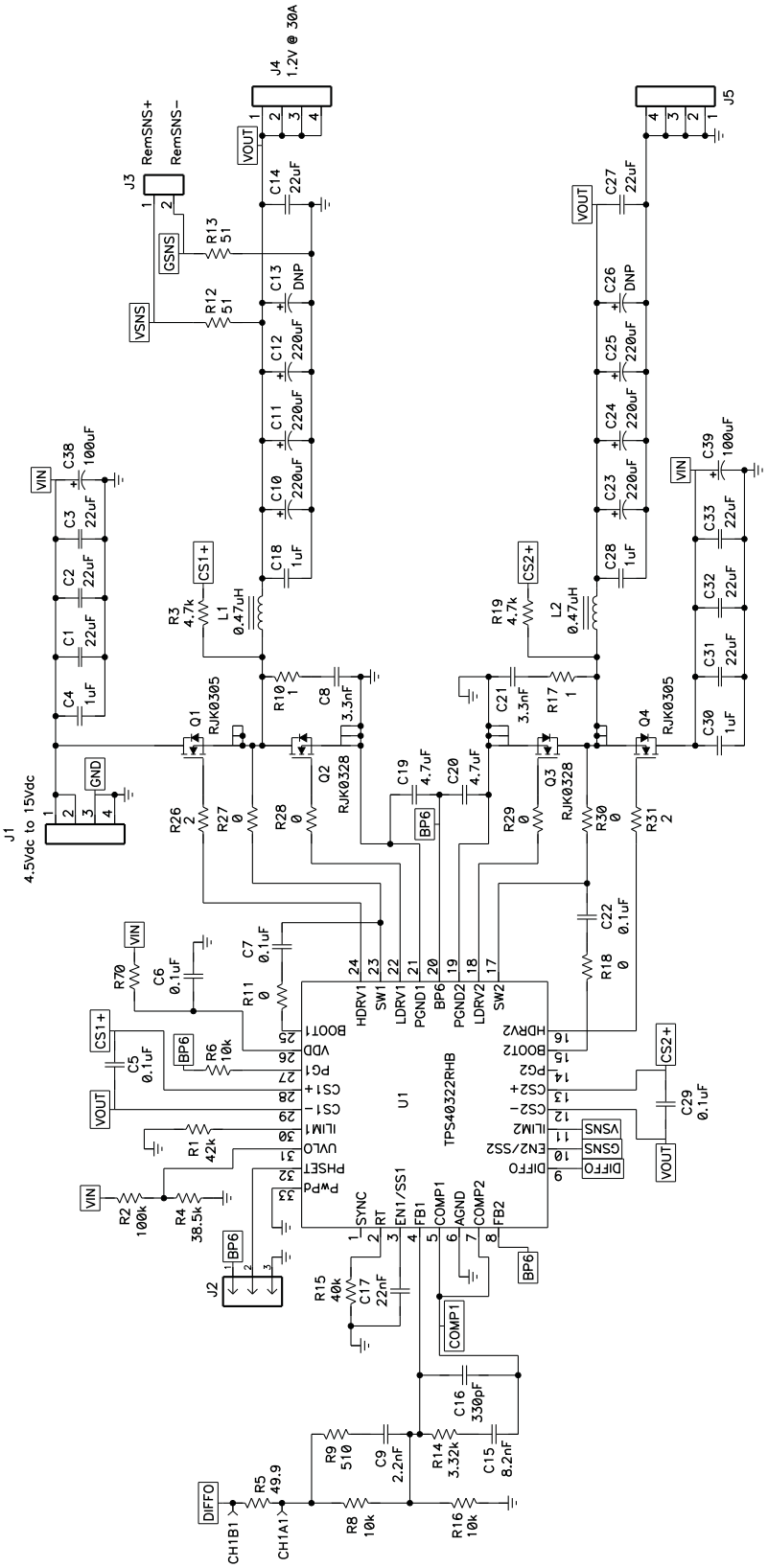


Figure 29. Design Example 2, Two-Phase Converter Schematic

Design Example 2 Characterization

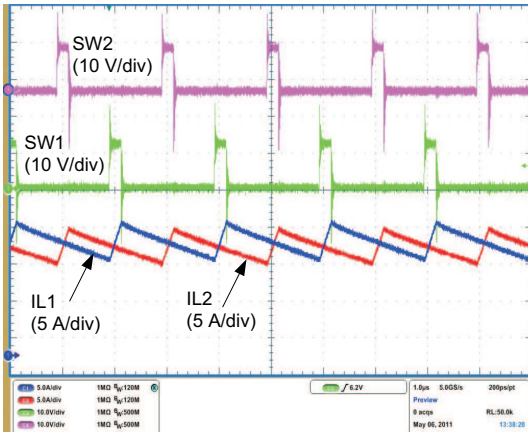


Figure 30. Steady-State Switching and Current Sharing

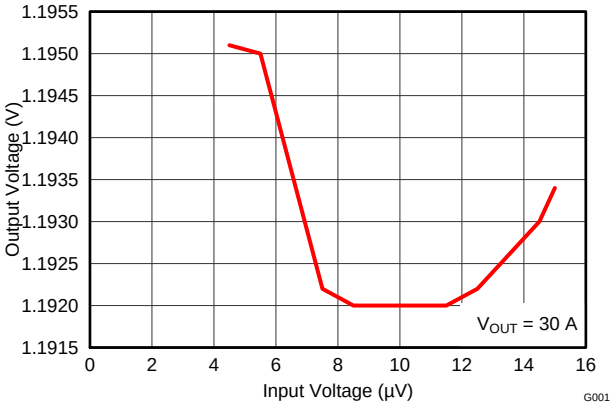


Figure 31. Line Regulation

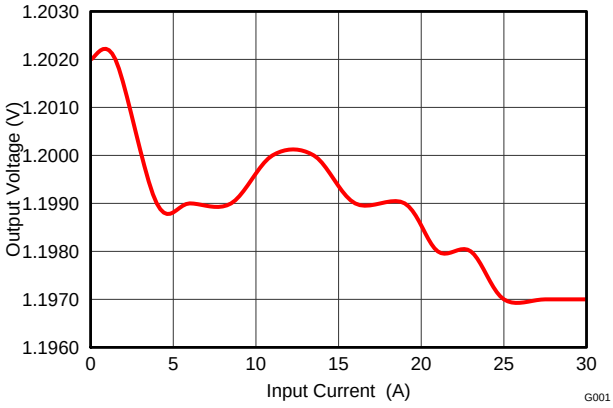


Figure 32. Load Regulation

Table 7. TPS40322 Design Example 2, *Two-Phase, Single Output* Bill of Materials

REFERENCE DESIGNATOR	QTY	DESCRIPTION	PART NUMBER	MFR
C1, C2, C3, C31, C32, C33	6	Capacitor, Ceramic, 22 µF, 25V, X5R, ±20%, 1210	Std	Std
C4, C18, C28, C30	4	Capacitor, Ceramic, 1 µF, 50V, X7R, ±10%, 0603	Std	Std
C5, C6, C7, C22, C29	5	Capacitor, Ceramic, 0.1 uF, 50V, X7R, ±10%, 0603	Std	Std
C8, C21	2	Capacitor, Ceramic, 6.8 nF, 50V, X7R, ±10%, 0805	Std	Std
C9	1	Capacitor, Ceramic, 2.2 nF, 16V, X7R, ±10%, 0603	Std	Std
C10, C11, C12, C13, C23, C24, C25, C26	8	Capacitor, Polymer Aluminum, 220 µF, 4V, ±20%, 5mM ESR	EEFSE0G221R	Panasonic - ECG
C14, C27	2	Capacitor, Ceramic, 22 µF, 6.3 V, X5R, ±10%, 0805	Std	Std
C15	1	Capacitor, Ceramic, 8.2 nF, 16 V, X7R, ±10%, 0603	Std	Std
C16	1	Capacitor, Ceramic, 330 pF, 16 V, X7R, ±10%, 0603	Std	Std
C17	1	Capacitor, Ceramic, 22 nF, 50 V, X7R, ±10%, 0603	Std	Std
C19, C20	2	Capacitor, Ceramic, 4.7 µF, 16 V, X7R, ±10%, 0805	Std	Std
C38, C39	2	Capacitor, Aluminum, 100 µF, 25 V, ±20%, F8	ECE-V1EA101XP	Panasonic - ECG
L1, L2	2	Inductor, SMT, 0.47 µH, ±20%, 1.2 mΩ, 0.512 x 0.571"	IHLP5050FDERR47M01	Vishay/Dale
Q1, Q4	2	MOSFET, N-channel, 30 V, 30 A, 8mΩ, 5-LFPAK	RJK0305	Renesas Electronics
Q2, Q3	2	MOSFET, N-channel, 30 V, 60 A, 2.1 mΩ, 5-LFPAK	RJK0328	Renesas Electronics
R1	1	Resistor, Chip, 42 kΩ, 1/10W, ±1%, 0603	Std	Std
R2	1	Resistor, Chip, 100 kΩ, 1/10W, ±1%, 0603	Std	Std
R3, R19	2	Resistor, Chip, 4.7 kΩ, 1/10W, ±1%, 0603	Std	Std
R4	1	Resistor, Chip, 38.5 kΩ, 1/10W, ±1%, 0603	Std	Std
R5	1	Resistor, Chip, 49.9 Ω, 1/10W, ±1%, 0603	Std	Std
R6, R8, R16	3	Resistor, Chip, 10 kΩ, 1/10W, ±1%, 0603	Std	Std
R7, R27, R28, R29, R30	5	Resistor, Chip, 0 Ω, 1/10W, ±1%, 0603	Std	Std
R9	1	Resistor, Chip, 511 Ω, 1/10W, ±1%	Std	Std
R10, R17	1	Resistor, Chip, 1.00 Ω, 1/8W, ±1%, 0805	Std	Std
R11, R18	2	Resistor, Chip, 5.11 Ω, 1/10W, ±1% 0603	603	Std
R12, R13	2	Resistor, Chip, 51 Ω, 1/10W, ±1%, 0603	Std	Std
R14	1	Resistor, Chip, 3.32 kΩ, 1/10W, ±1%, 0603	Std	Std
R15	1	Resistor, Chip, 40 kΩ, 1/10W, ±1%, 0603	Std	Std
R26, R31	2	Resistor, Chip, 2 Ω, 1/10W, ±1%, 0603	Std	Std
R20, R21, R22, R23, R24, R25,	0	not used	Std	Std
U1	1	Dual synchronous buck controller, QFN-32	TPS40322RHB	Texas Instruments

REVISION HISTORY

Changes from Revision C (JANUARY 2013) to Revision D **Page**

- Added information regarding the appropriate output voltage range when using the remote sense amplifier in the Two-Phase Mode, Remote Sense Amplifier, and Current Sharing Loop section 15

Changes from Revision B (JUNE 2012) to Revision C **Page**

- Added clarity to ABSOLUTE MAXIMUM RATINGS table 2

Changes from Revision A (JANUARY 2012) to Revision B **Page**

- Changed all references of "multi-phase" to "two-phase" throughout document 1
- Added clarity to SIMPLIFIED APPLICATION CIRCUIT. 1
- Added clarity to Functional Block Diagram 9
- Added "When not being used, SYNC should be left floating" to SYNC description in PIN FUNCTIONS table. 11
- Added clarity to Figure 15 12
- Added clarity to Figure 16 13
- Added clarity to Figure 17 14
- Added clarity to Figure 18 15
- Added clarity to Figure 19 16
- Changed "This design limits the maximum voltage drop across the current sense inputs, $V_{CS(max)}$, to 60 mV." to "This design limits the maximum voltage drop across the current sense inputs, $V_{CS(max)}$, to 50 mV." in ILIM Resistor (R2) section. 23
- Changed Equation 24 24
- Changed Output current = 10 (max) to Output current = 30 (max) in Table 6 30

Changes from Original (JUNE 2011) to Revision A **Page**

- Added clarity to Functional Block Diagram 9
- Added clarity to Figure 18 15

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS40322RHBR	ACTIVE	VQFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 40322	Samples
TPS40322RHBT	ACTIVE	VQFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 40322	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

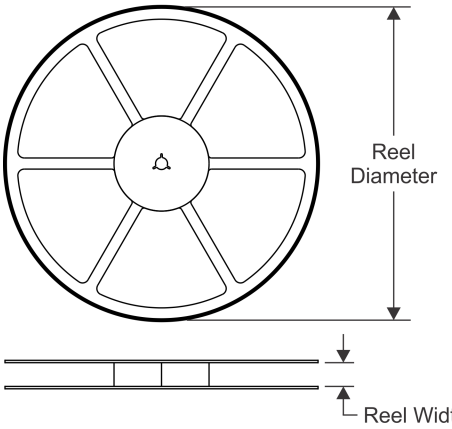
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

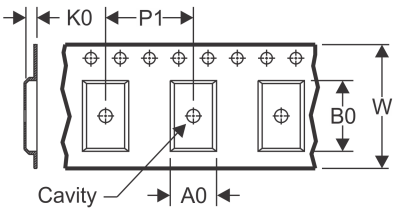
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

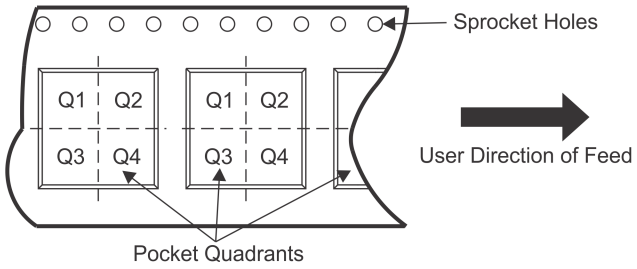


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

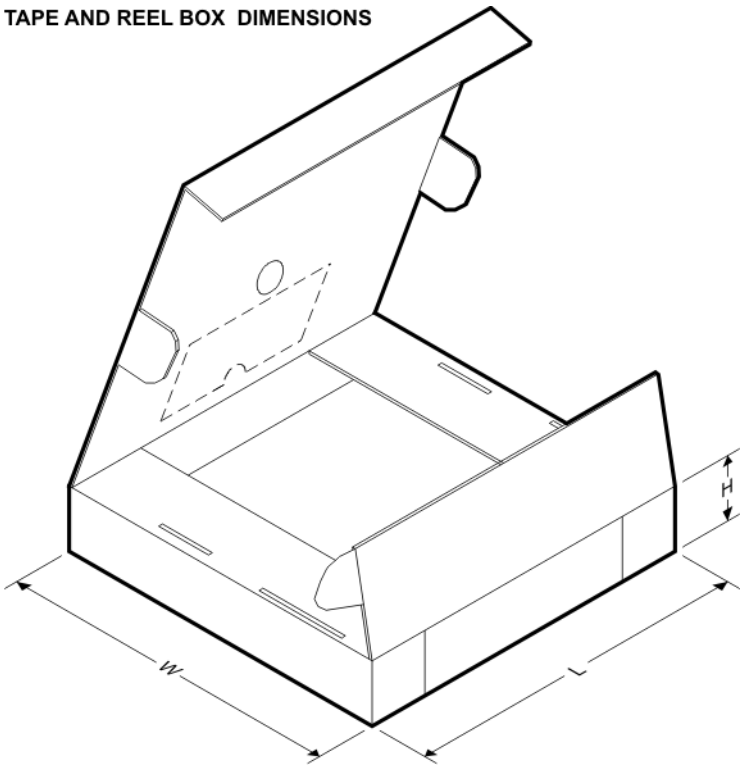
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS40322RHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
TPS40322RHBT	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

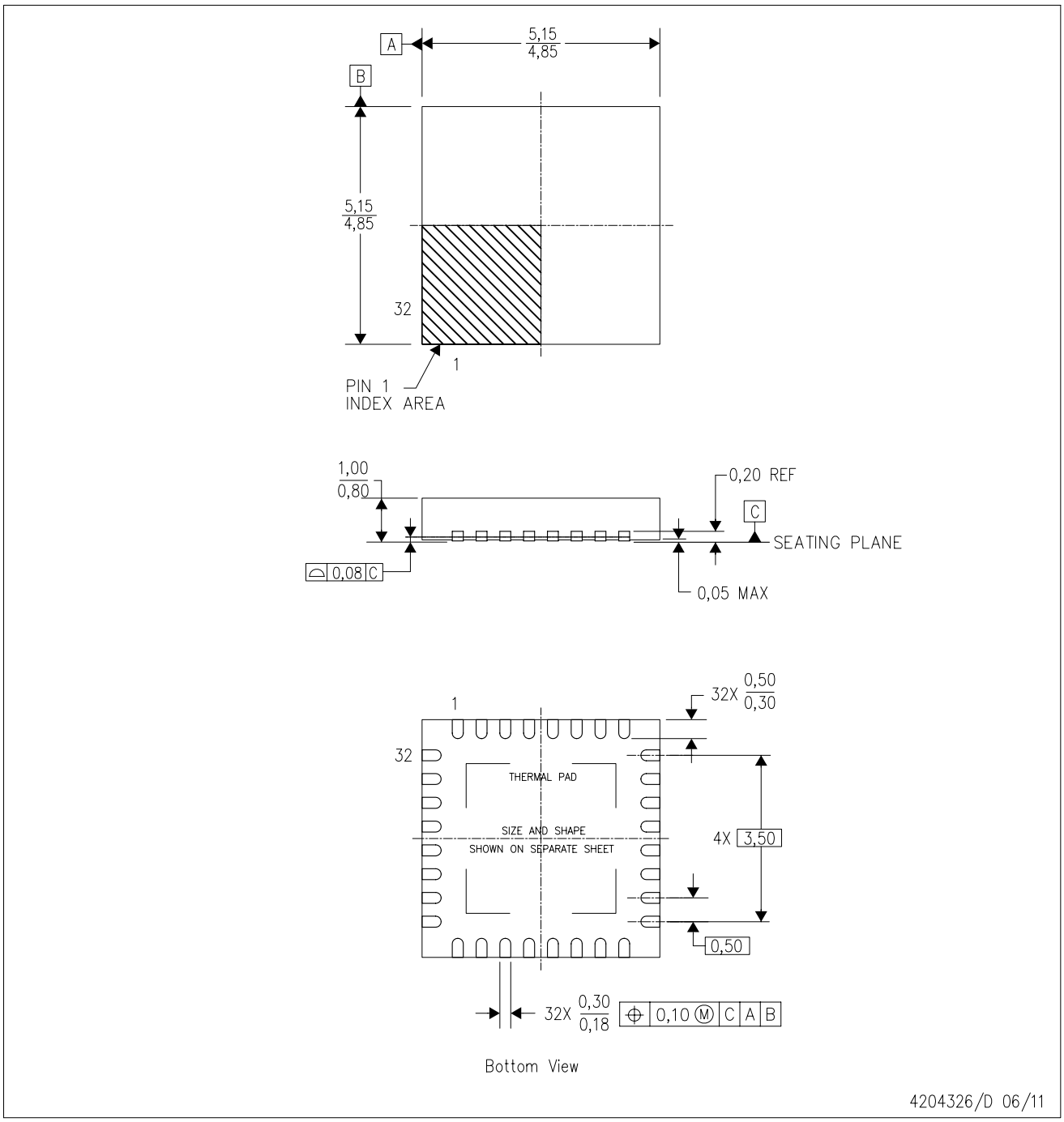
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS40322RHBR	VQFN	RHB	32	3000	367.0	367.0	35.0
TPS40322RHBT	VQFN	RHB	32	250	210.0	185.0	35.0

RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

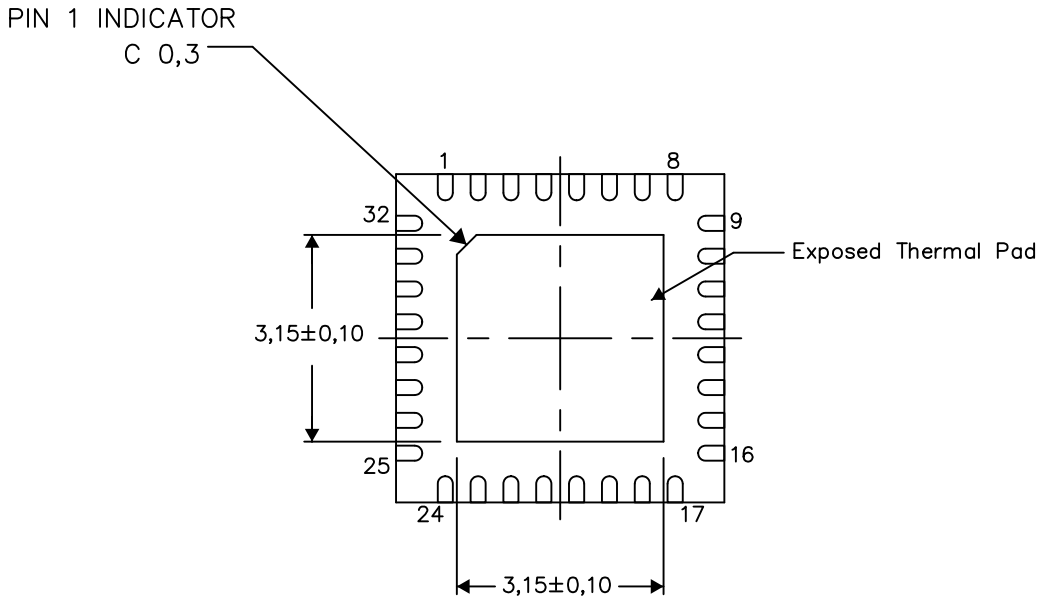
RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



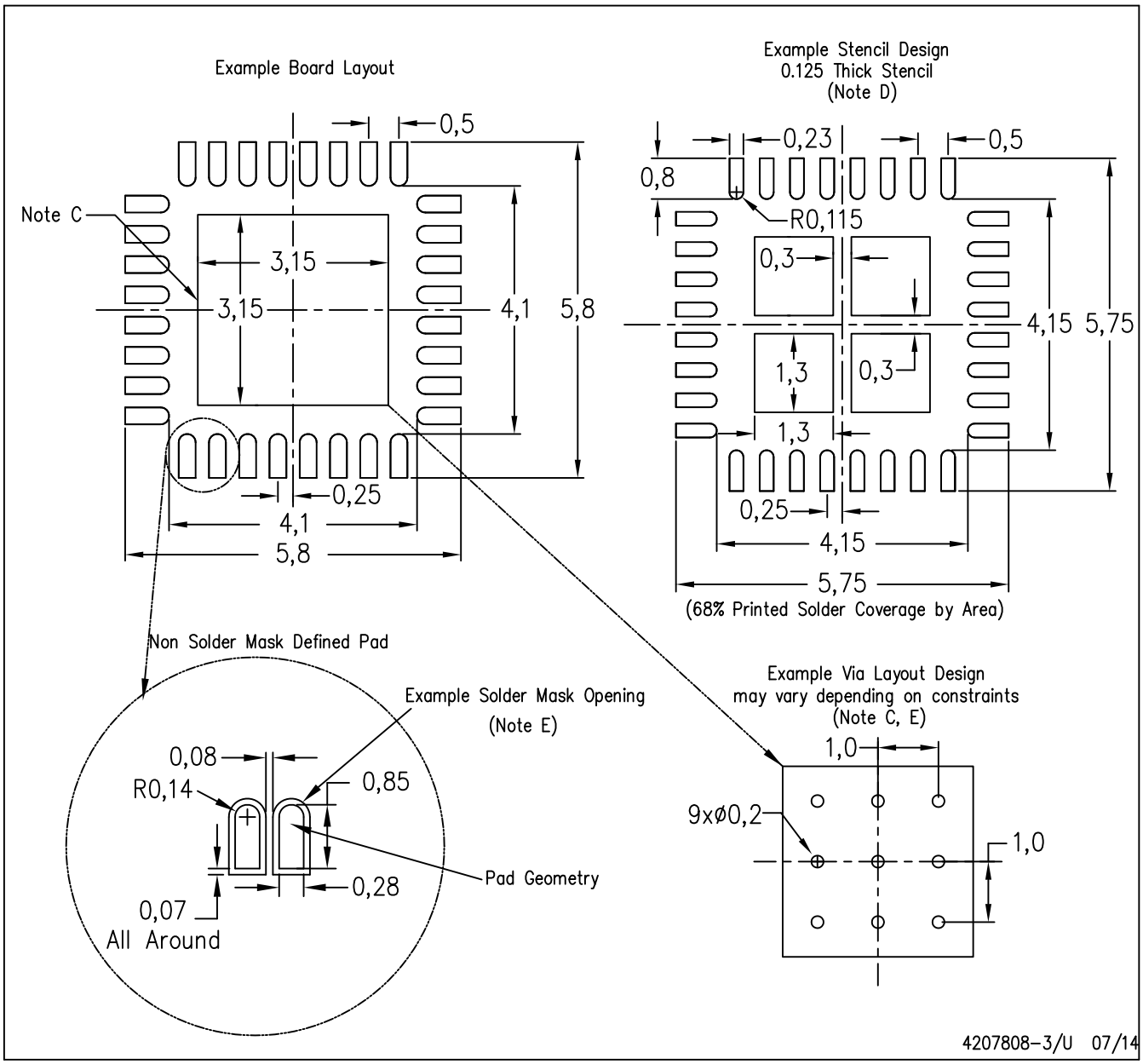
Bottom View

Exposed Thermal Pad Dimensions

4206356–3/AB 07/14

NOTE: A. All linear dimensions are in millimeters

RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
E. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for any larger diameter vias placed in the thermal pad.

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