TPS63700 DC-DC Inverter

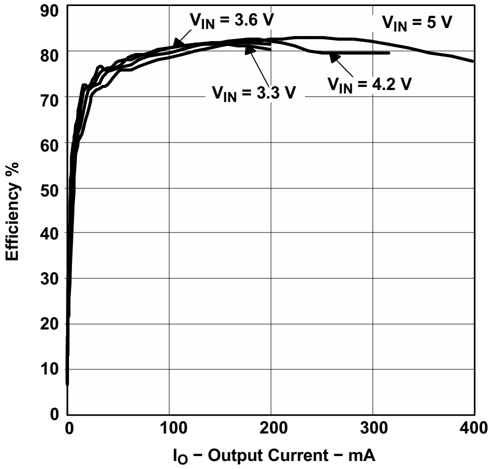
1 Features

- Adjustable Output Voltage Down to –15 V
- 2.7-V to 5.5-V Input Voltage Range
- Up to 360-mA Output Current
- 1000-mA Typical Switch Current Limit
- Up to 84% Efficiency
- Typical 1.4-MHz Fixed-Frequency PWM Operation
- Thermal Shutdown
- Typical –19-V Output Overvoltage Protection
- 1.5-μA Shutdown Current
- Small 3-mm × 3-mm SON-10 Package (DRC)

2 Applications

- Generic Negative Voltage Supply
- Small-to-Medium Size OLED Displays
- Bias Supply

Efficiency vs Output Current



3 Description

The TPS63700 is an inverting DC/DC converter generating a negative output voltage down to –15 V with output currents up to 360 mA, depending on input-voltage to output-voltage ratio. With a peak efficiency of 84%, the device is ideal for portable battery-powered equipment. The input voltage range of 2.7 V to 5.5 V allows the TPS63700 to be directly powered from a Li-ion battery, from 3-cell NiMH/NiCd, from a 3.3-V or 5-V supply rail.

The inverter operates with a fixed-frequency pulse width modulation (PWM) control topology. The device has an internal current limit, overvoltage protection, and a thermal shutdown for highest reliability under fault conditions.

A switching frequency of typically 1.4 MHz allows the use of small external components enabling a small solution size.

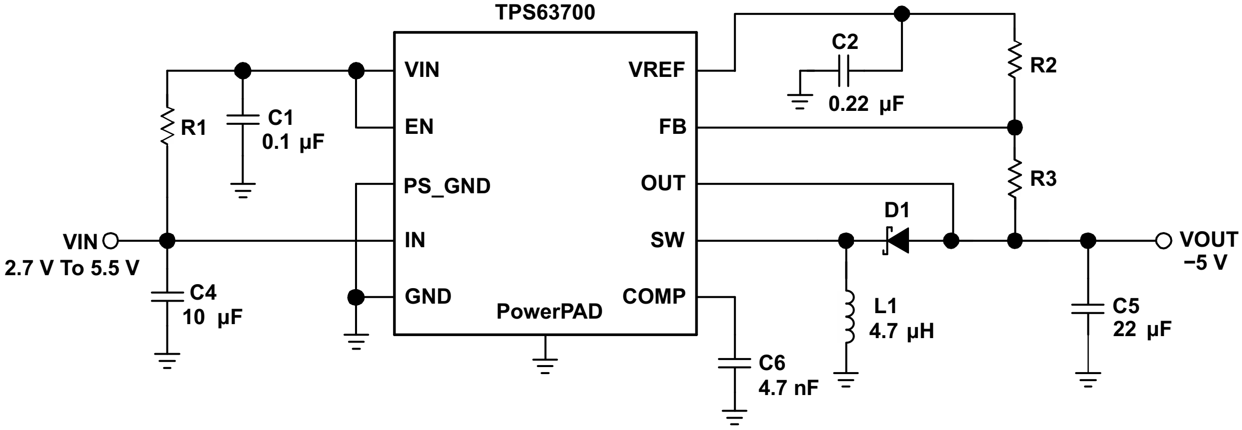
The TPS63700 comes in a small 3-mm × 3-mm SON-10 package.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS63700	VSON (10)	3.00 mm x 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Typical Application Schematic



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4 Revision History

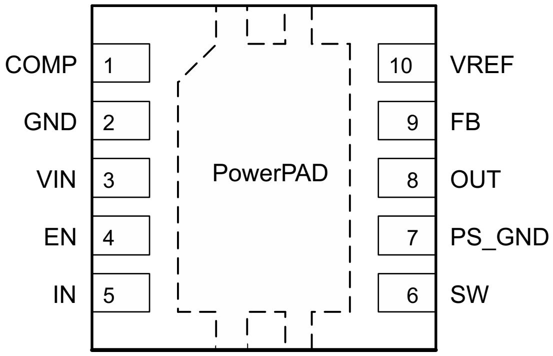
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (June 2013) to Revision D	Page
• Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

Changes from Revision B (November 2007) to Revision C	Page
• Deleted Dissipation Ratings table and added Thermal Information table.	4

5 Pin Configuration and Functions

DRC Package
10-Pin VSON With PowerPAD™
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
COMP	1	I/O	Compensation pin for control, connect a 4.7 nF capacitor between this pin and GND
GND	2	—	Ground pin
VIN	3	I	Supply voltage input for control logic, connect a RC circuit of 10R and 100 nF to filter this supply voltage
EN	4	I	Enable pin (EN = GND: disabled; EN = VIN: enabled)
IN	5	I	Supply voltage for the power switch
SW	6	O	Inverter switch output
PS_GND	7	I	Connect to GND for control logic
OUT	8	I	Output voltage sense input
FB	9	I	Feedback pin for the voltage divider
VREF	10	O	Reference voltage output. Connect a 220-nF capacitor to ground. Connect the lower resistor of the negative output voltage divider to this pin.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range unless otherwise noted[1]

	MIN	MAX	UNIT
Input voltage at VIN[2]	–0.3	6	V
Input voltage at IN[2]		VIN	V
Minimum voltage at OUT [2]		–18	V
Voltage at EN, FB, COMP, PS_GND [2]	–0.3	V_{IN} + 0.3	V
Differential voltage between OUT to VIN [2]		24	V
Operating virtual junction temperature, T_J	–40	150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network ground terminal, unless otherwise noted.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

	MIN	MAX	UNIT
Input voltage range, V_{IN}	2.7	5.5	V
Operating free-air temperature, T_A	–40	85	°C
Operating virtual junction temperature, T_J	–40	125	°C

6.4 Thermal Information

THERMAL METRIC[1]		TPS63700 DRC (VSON) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	41.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	62.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	16.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	16.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	4.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

–40°C to 85°C, over recommended input voltage range, typical at an ambient temperature of 25°C (unless otherwise noted)

PARAMETER[(1)]			TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY							
V_{IN}	Input voltage range		Pin VIN, IN	2.7		5.5	V
$I_{(Q)}$	Quiescent current	VIN	V_{IN} = 3.6 V, I_{OUT} = 0, EN = V_{IN}, no switching V_{OUT} = –5 V		330	400	μA
		IN			640	750	μA
I_{SD}	Shutdown supply current		EN = GND		0.2	1.5	μA
UVLO	Undervoltage lockout threshold			2.1	2.35	2.7	V
T_{SD}	Thermal shutdown temperature				150		°C
	Thermal Shutdown hysteresis		Junction temperature decreasing		5		°C
CONTROL STAGE							
V_{EN}	High level input voltage			1.4			V
V_{EN}	Low level input voltage					0.4	V
I_{EN}	Input current		EN = V_{IN} or GND		0.01	0.1	μA
POWER SWITCH							
I_{LIM}	Inverter switch current limit		2.7 V < V_{IN} < 5.5 V	860	1000	1140	mA
$R_{DS(ON)}$	Inverter switch on-resistance		V_{IN} = 3.6 V		440	600	mΩ
			V_{IN} = 5 V		370	500	
D_{MAX}	Maximum duty cycle inverting converter				87.5%		
D_{MIN}	Minimum duty cycle inverting converter				12.5%		
f_S	Oscillator frequency			1250	1380	1500	kHz
OUTPUT							
V_{OUT}	Adjustable output voltage range			–15		–2	V
V_{OUT}	DC output accuracy		PWM mode, device switching		±3%		
V_{REF}	Reference voltage		I_{REF} = 10 μA	1.2	1.213	1.225	V
V_{OVP}	Output overvoltage protection				–19		V
V_{FB}	Negative feedback regulation voltage		V_{IN} = 2.7 V to 5.5 V	–0.024	0	0.024	V
I_{FB}	Negative feedback input bias current		V_{FBN} = 0.1 V_{REF}		2		nA

(1) Parameter does not include tolerance of external resistors.

6.6 Typical Characteristics

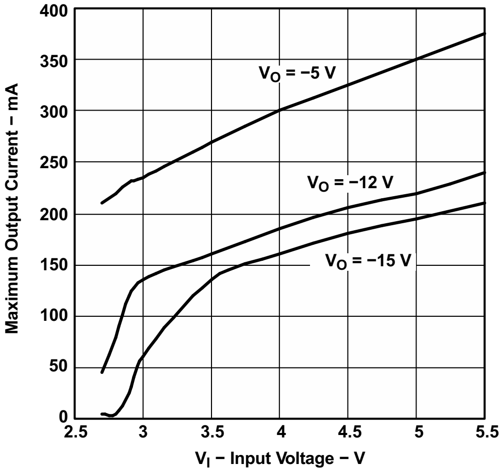


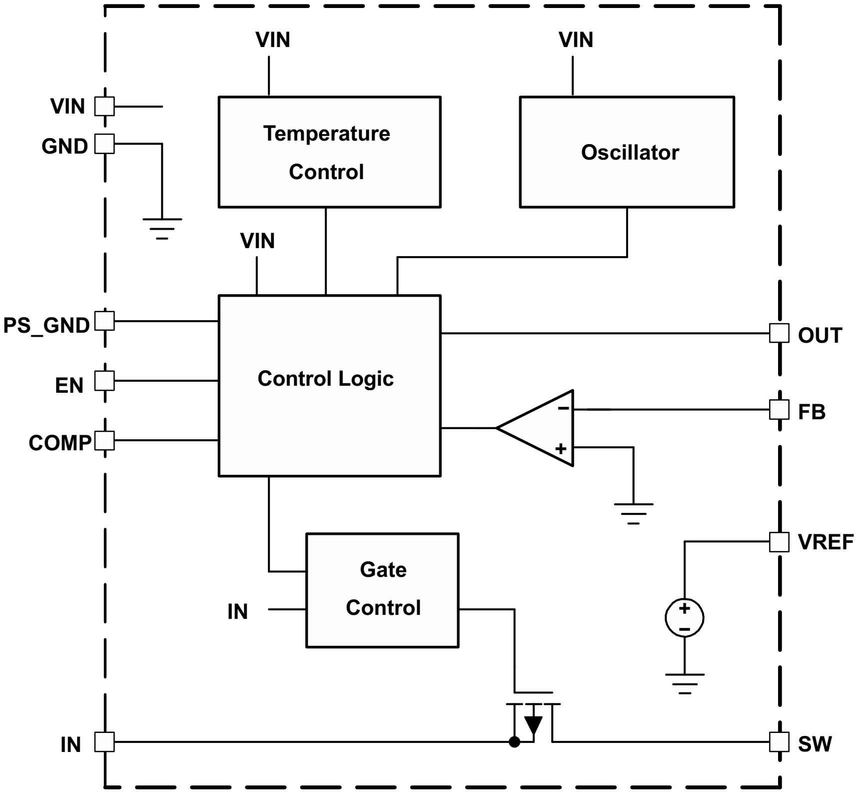
Figure 1. Maximum Output Current vs Input Voltage

7 Detailed Description

7.1 Overview

The TPS63700 is a DC/DC converter for negative output voltages using buck-boost topology. It operates with an input voltage range of 2.7 V to 5.5 V and generates a negative output voltage down to –15 V. The output is controlled by a fixed-frequency, pulse-width-modulated (PWM) regulator. In normal operation mode, the converter operates at continuous conduction mode (CCM). At light loads it can enter discontinuous conduction mode (DCM).

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Enable

Applying GND signal at the EN pin disables the converter, where all internal circuitry is turned off. The device now just consumes low shutdown current flowing into the VIN pin. The output load of the converter is also disconnected from the battery as described in *Load Disconnect*. Pulling the EN pin to V_{IN} enables the converter. Internal circuitry, necessary to operate the converter, is then turned on.

7.3.2 Load Disconnect

The device supports complete load disconnection when the converter is disabled. The converter turns off the internal PMOS switch, thus no DC current path remains between load and input voltage source.

7.3.3 Output Overvoltage Protection

The converter has an output overvoltage protection implemented. The output voltage is limited to –19 V in case the feedback connection from the output to the FB pin is open.

Feature Description (continued)

7.3.4 Undervoltage Lockout

An undervoltage lockout prevents the device from starting up and operating if the supply voltage at VIN is lower than the programmed threshold shown in the *Electrical Characteristics* table. The device automatically shuts down the converter when the supply voltage at VIN falls below this threshold. Nevertheless, parts of the control circuits remain active, which is different than device shutdown using EN inputs. The undervoltage lockout function is implemented to prevent device malfunction.

7.3.5 Overtemperature Shutdown

The device automatically shuts down if the implemented internal temperature detector detects a chip temperature above the programmed threshold shown in the electrical characteristics table. It starts operating again when the chip temperature decreases. A built-in temperature hysteresis avoids undefined operation caused by ringing from over-temperature shutdown.

7.4 Device Functional Modes

7.4.1 Soft-Start

The converter has a soft-start function. When the converter is enabled, the implemented switch current limit ramps up slowly to its nominal value. Soft-start is implemented to limit the input current during start-up to avoid high peak currents at the battery which could interfere with other systems connected to the same battery.

Without soft-start, uncontrolled input peak currents flow to charge up the output capacitors and to supply the load during start-up. This would cause significant voltage drops across the series resistance of the battery and its connections.

7.4.2 PWM Operation

The converter operates in a fixed-frequency, pulse-width-modulated control scheme. The on-time of the switches varies depending on input-to-output voltage ratio and the load. During this on-time, the inductor connected to the converter is charged with current. In the remaining time, the time period set by the fixed operating frequency, the inductor discharges into the output capacitor via the rectifier diode. At medium to heavy loads the inductor current is continuous and the device operates in continuous conduction mode (CCM).

7.4.3 Power Save Mode Operation

As the load current decreases, the converter enters Power Save Mode. Entering Power Save Mode happens at the boundary to discontinuous conduction mode (DCM). During light load, the inductor current of this converter can become discontinuous. In this case, the control circuit of the controller output automatically takes care of these changing conditions to always operate with an optimum control setup.

7.4.4 Control

The controller circuit of the converter is based on a fixed-frequency, multiple-feed-forward controller topology. Input voltage, output voltage, and voltage drop across the switch are monitored and forwarded to the regulator. Changes in the operating conditions of the converter directly affect the duty cycle.

The error amplifier compares the voltage at FB pin with GND to generate an accurate and stable output voltage. The error amplifier is internally compensated. At light loads, the converter operates in discontinuous conduction mode (DCM).

If the load will be further decreased, the energy transmitted to the output capacitor cannot be absorbed by the load and would lead to an increase of the output voltage. In this case, the converter limits the output voltage increase by skipping switch pulses.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS63700 DC/DC converter is intended for systems typically powered by a single-cell Li-ion or Li-polymer battery with a terminal voltage between 2.7 V up to 4.2 V. Due to the recommended input voltage going up to 5.5 V, the device is also suitable for 3-cell alkaline, NiCd,or NiMH batteries, as well as regulated supply voltages of 3.3 V or 5 V.

8.2 Typical Application

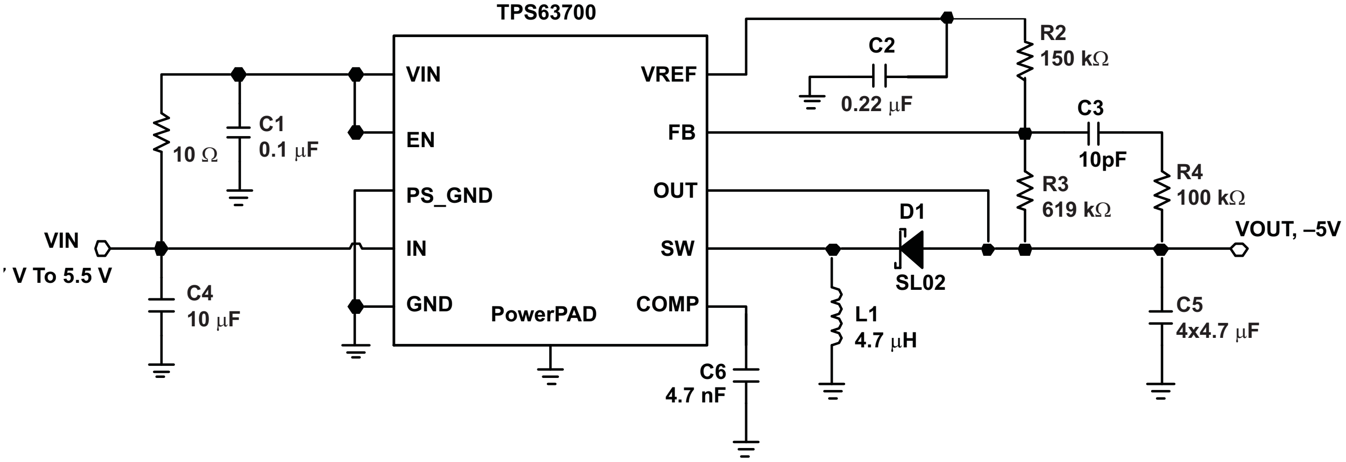


Figure 2. Circuit for –5-V Output

8.2.1 Design Requirements

The design of the inverter can be adapted to different output voltage and load current needs by choosing external components appropriately. The following design procedure is adequate for the whole V_{IN}, V_{OUT} and load current range of TPS63700.

Table 1 shows the list of components for the *Application Curves*.

Table 1. List of Components

REFERENCE	DESCRIPTION
C1, C2, C3, C4,	X7R/X5R ceramic
C5	4 × 4.7 μF X7R/X5R ceramic
D1	SL03/SL02 Vishay
L1	–5V: TDK VLF4012 4R7, TDK SLF6025-4R7, Coilcraft LPS4018-472,
	–12V: Sumida CDRH5D18 10 μH

8.2.2 Detailed Design Procedure

8.2.2.1 Programming the Output Voltage: Converter

The output voltage of the TPS63700 converter can be adjusted with an external resistor divider connected to the FB pin. The reference point of the feedback divider is the reference voltage V_{REF} with 1.213 V. The typical value of the voltage at the FB pin is 0 V. The minimum recommended output voltage at the converter is –15 V. The feedback divider current should be 10 µA. The voltage across R2 is 1.213 V. Based on those values, the recommended value for R2 should be 120 kΩ to 200 kΩ in order to set the divider current at the required value. The value of the resistor R3 can then be calculated using Equation 1, depending on the needed output voltage (V_{OUT}).

$$R3 = R2 \times \left(\frac{V_{REF} - V_{OUT}}{V_{REF}} - 1 \right) \tag{1}$$

For example, if an output voltage of –5 V is needed and a resistor of 150 kΩ has been chosen for R2, a 619-kΩ resistor is needed to program the desired output voltage.

8.2.2.1.1 Inductor Selection

An inductive converter normally requires two main passive components for storing energy during the conversion. An inductor and a storage capacitor at the output are required.

The average inductor current depends on the output load, the input voltage V_{IN}, and the output voltage V_{OUT}. It can be estimated with Equation 2, which shows the formula for the inverting converter.

$$I_{Lavg} = \frac{V_{IN} - V_{OUT}}{V_{IN} \times 0.8} \times I_{OUT}$$

where

- I_{Lavg}= Average inductor current (2)

An important parameter for choosing the inductor is the desired current ripple in the inductor.

A ripple current value between 20% and 80% of the average inductor current can be considered as reasonable, depending on the application requirements. A smaller ripple reduces the losses in the inductor, as well as output voltage ripple and EMI. But in the same way, the inductor becomes larger and more expensive.

Keeping those parameters in mind, the possible inductor value can be calculated using Equation 3.

$$L = \frac{V_{IN} \times V_{OUT}}{\Delta I_L \times (V_{OUT} - V_{IN}) \times f}$$

where

- ΔI_L = Peak-to-peak ripple current
- f = Switching frequency
- L = Inductor value (3)

With the known inductor current ripple, the peak inductor value can be approximated with Equation 4. The peak current through the switch and the inductor depends also on the output load, the input voltage V_{IN}, and the output voltage V_{OUT}. To select the right inductor, it is recommended to keep the possible peak inductor current below the current-limit threshold of the power switch. For example, the current-limit threshold of the TPS63700 switch for the inverting converter is nominally 1000 mA.

$$I_{Lmax} = \frac{V_{IN} - V_{OUT}}{V_{IN} \times 0.8} \times I_{OUT} + \frac{\Delta I_L}{2}$$

where

- I_{LMAX} = Peak inductor current
- ΔI_L = Peak-to-peak ripple current (4)

With Equation 5, the inductor current ripple at a given inductor can be approximated.

$$\Delta I_L = \frac{V_{IN} \times V_{OUT}}{L \times (V_{OUT} - V_{IN}) \times f}$$

where

- ΔI_L = Peak-to-peak ripple current
- L = Inductor value
- f = Switching frequency (5)

Care has to be taken for the possibility that load transients and losses in the circuit can lead to higher currents as estimated in Equation 4. Also, the losses caused by magnetic hysteresis losses and copper losses are a major parameter for total circuit efficiency.

The following inductor series from different suppliers have been tested with the TPS63700 converter, see Table 2.

Table 2. List of Inductors

Output Voltage	Vendor	SUGGESTED INDUCTOR
–5 V	TDK	VLF4012 4.7 µH
		SLF6025-4.7 µH
–5 V	Coilcraft	LPS4018 4.7 µH
		LPS3015 4.7 µH
–12 V	Sumida	CDRH5D18 10 µH
–12 V	Coilcraft	MOS6020 10 µH

8.2.2.2 Capacitor Selection

8.2.2.2.1 Input Capacitor

At least a 10-µF ceramic input capacitor is recommended for a good transient behavior of the regulator, and EMI behavior of the total power supply circuit.

8.2.2.2.2 Output Capacitors

One of the major parameters necessary to define the capacitance value of the output capacitor is the maximum allowed output voltage ripple of the converter. This ripple is determined by two parameters of the capacitor, the capacitance and the ESR. It is possible to calculate the minimum capacitance needed for the defined ripple, supposing that the ESR is zero, by using Equation 6 for the inverting converter output capacitor.

$$C_{min} = \frac{I_{OUT} \times V_{OUT}}{f_S \times \Delta V \times (V_{OUT} - V_{IN})}$$

where

- f = Switching frequency
- ΔV = Maximum allowed ripple
- C_{min} = Minimum capacitance (6)

With a chosen ripple voltage in the range of 10 mV, a minimum capacitance of 12 µF is needed. The total ripple is larger due to the ESR of the output capacitor. This additional component of the ripple can be calculated using Equation 7 .

$$\Delta V_{ESR} = I_{OUT} \times R_{ESR}$$

where

- ΔV_{ESR} = Voltage ripple caused by R_{ESR} of capacitor
- R_{ESR} = Equivalent series resistance of capacitor (7)

An additional ripple of 2 mV is the result of using a typical ceramic capacitor with an ESR in a 10-mΩ range. The total ripple is the sum of the ripple caused by the capacitance, and the ripple caused by the ESR of the capacitor. In this example, the total ripple is 12 mV. Additional ripple is caused by load transients. When the load current increases rapidly, the output capacitor must provide the additional current until the inductor current has been increased by the control loop by setting a higher on-time at the main switch (duty cycle). The higher duty cycle results in longer inductor charging periods, but the rate of increase of the inductor current is also limited by the inductance itself. When the load current decreases rapidly, the output capacitor needs to store the excessive energy (stored in the inductor) until the regulator has decreased the inductor current by reducing the duty cycle. The recommendation is to use higher capacitance values, as the previous calculations show.

8.2.2.3 Stabilizing the Control Loop

8.2.2.3.1 Feedback Divider

To speed up the control loop, a feed-forward capacitor of 10 pF is recommended in the feedback divider, parallel to R3.

To avoid coupling noise into the control loop from the feed-forward capacitor, the feed-forward effect can be bandwidth-limited by adding series resistor R4. A value in the range of 100 kΩ is suitable. The higher the resistance, the lower the noise coupled into the control loop system.

8.2.2.3.2 Compensation Capacitor

The control loop of the converter is completely compensated internally. However the internal feed-forward system requires an external capacitor. A 4.7-nF capacitor at the COMP pin of the converter is recommended.

8.2.3 Application Curves

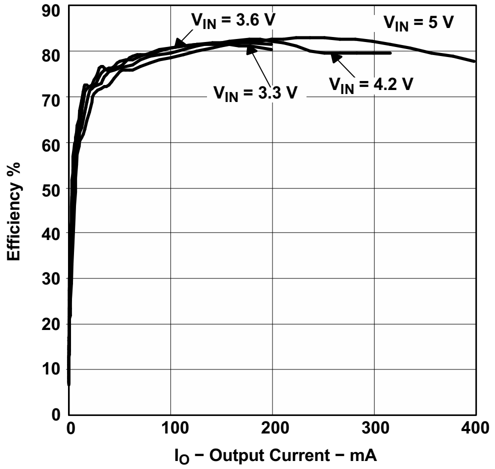


Figure 3. Efficiency vs Output Current, VOUT –5 V

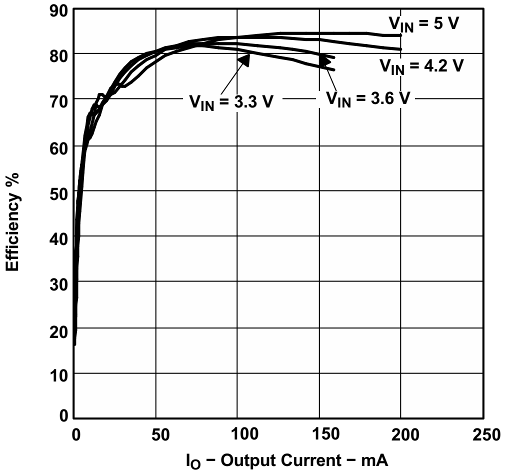


Figure 4. Efficiency vs Output Current, VOUT –12 V

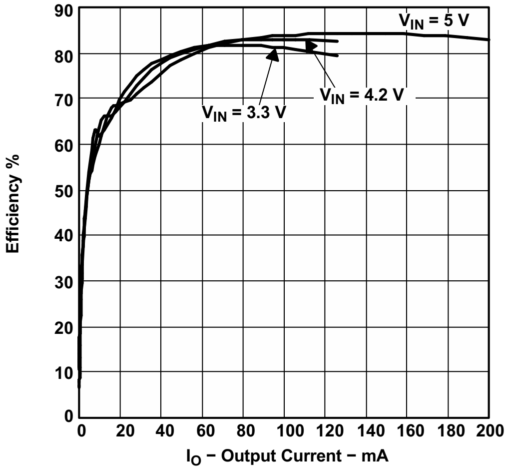


Figure 5. Efficiency vs Output Current, VOUT –15 V

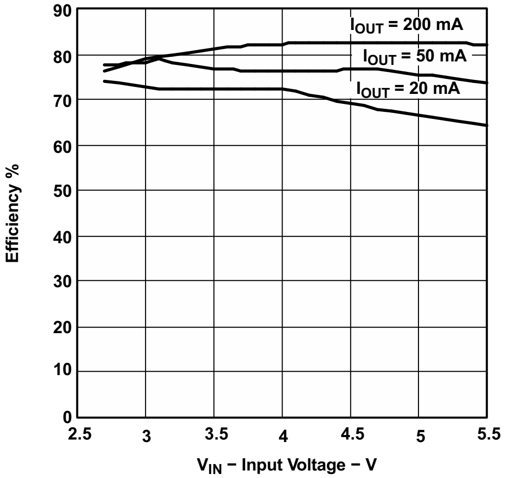


Figure 6. Efficiency vs Input Voltage, VOUT –5 V

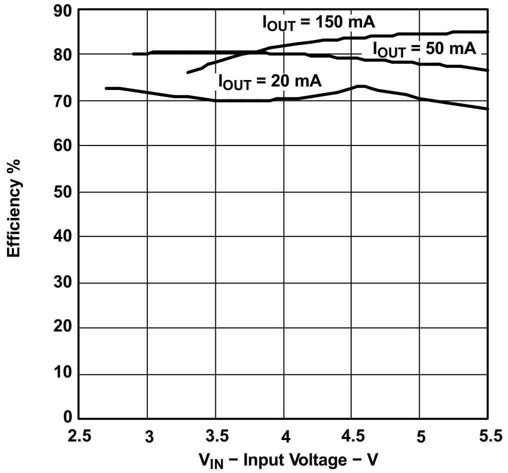


Figure 7. Efficiency vs Input Voltage, VOUT –12 V

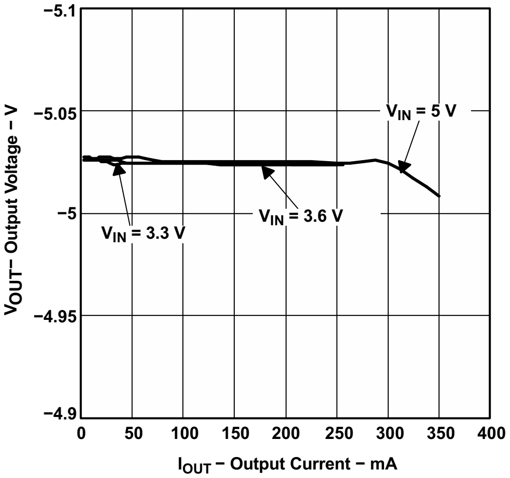


Figure 8. Output Voltage vs Output Current

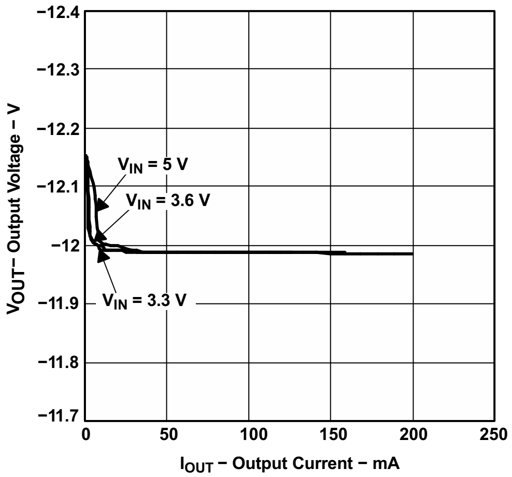


Figure 9. Output Voltage vs Output Current

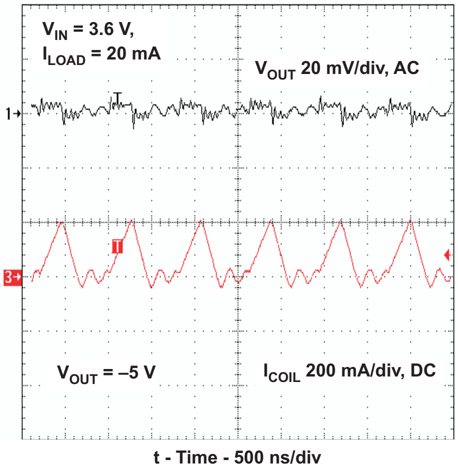


Figure 10. Output Voltage in Discontinuous Conduction Mode

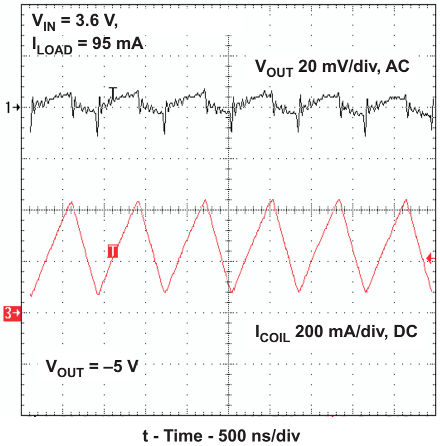


Figure 11. Output Voltage in Continuous Conduction Mode

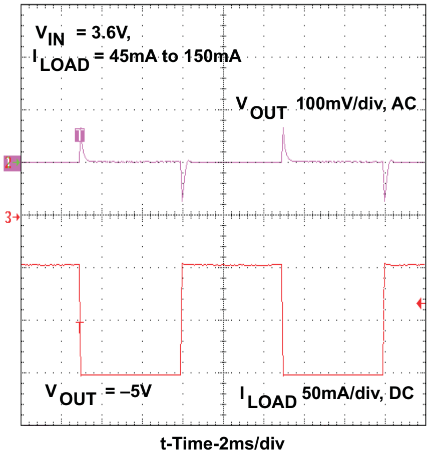


Figure 12. Load Transient Response, –5 V, 45 to 150 mA

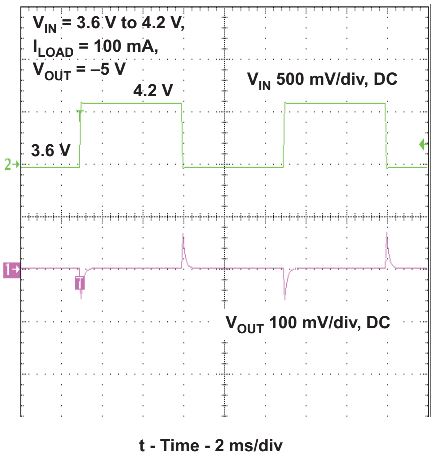


Figure 13. Line Transient Response, –5 V

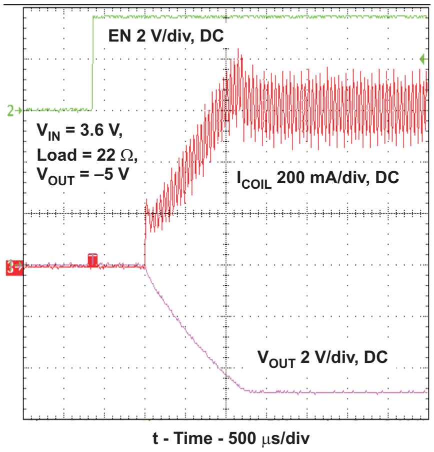


Figure 14. Start-Up After Enable, –5 V

8.3 System Example

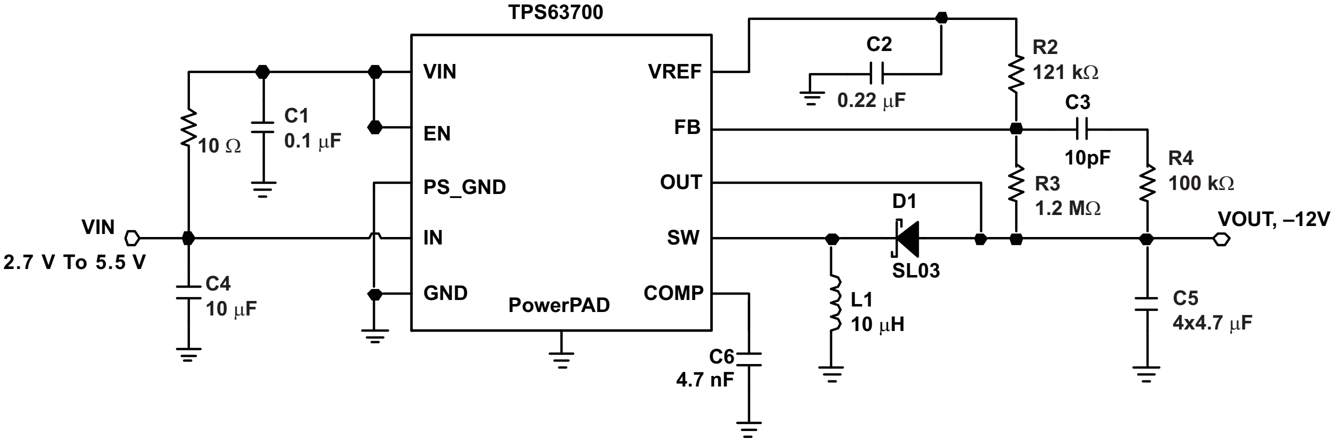


Figure 15. Circuit for –12-V Output

9 Power Supply Recommendations

The power supply to the TPS63700 needs to have a current rating according to the input supply voltage, output voltage and output current of the TPS63700.

10 Layout

10.1 Layout Guidelines

For all switching power supplies the layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the regulator could show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current paths, and for the power-ground tracks. The input and output capacitors should be placed as close as possible to the IC. The diode need to be connected closest to the SW pin to minimize parasitic inductance. For low noise operation small bypass capacitors $C_{IN\ BP}$ and $C_{OUT\ BP}$ in the nF range can be added close to the IC.

The feedback divider should be placed as close as possible to the V_{REF} pin of the IC. Use short traces when laying out the control ground. Figure 18 shows the layout of the EVM board.

10.2 Layout Example

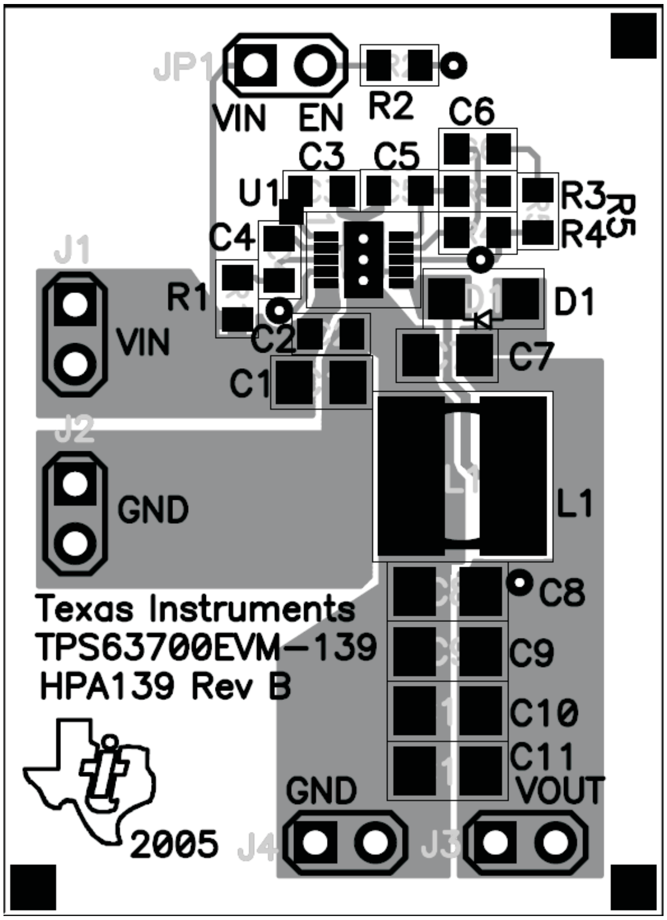


Figure 16. Layout Considerations, Top View

Layout Example (continued)

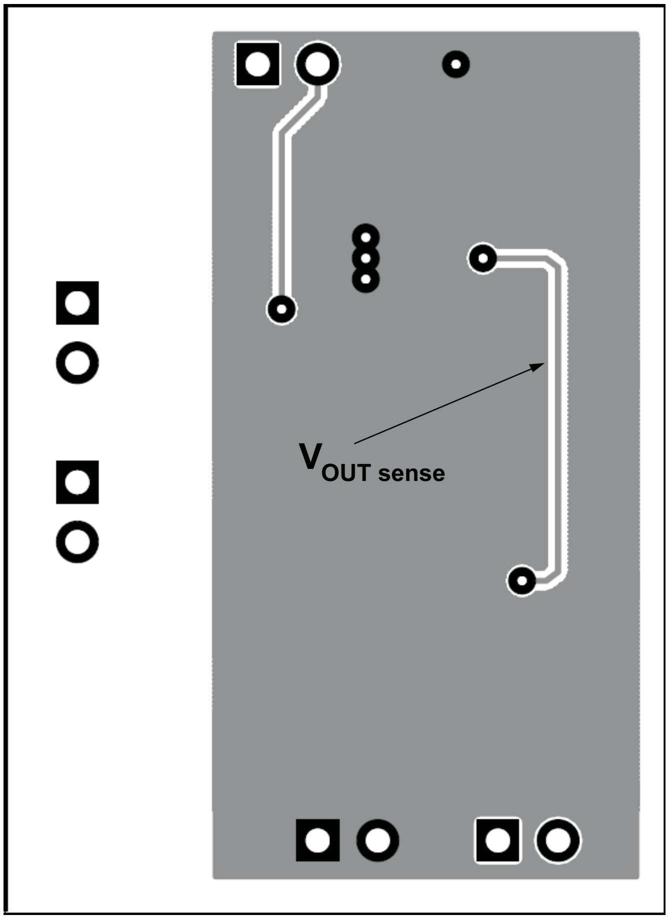


Figure 17. Layout Considerations, Bottom View

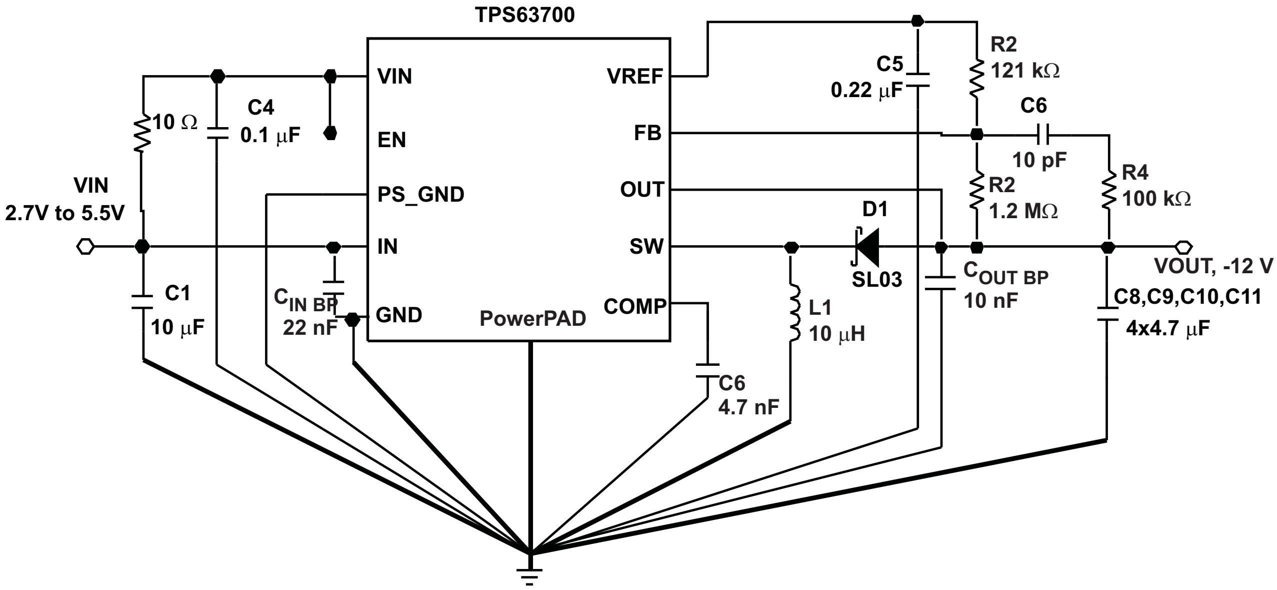


Figure 18. Layout Circuit

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.
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11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS63700DRCR	ACTIVE	VSON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	NUB	Samples
TPS63700DRCRG4	ACTIVE	VSON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	NUB	Samples
TPS63700DRCT	ACTIVE	VSON	DRC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	NUB	Samples
TPS63700DRCTG4	ACTIVE	VSON	DRC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	NUB	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

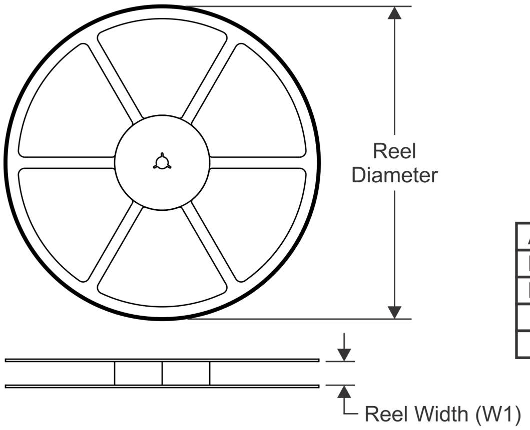
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

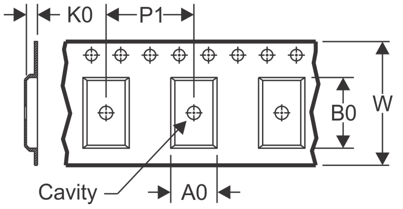
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

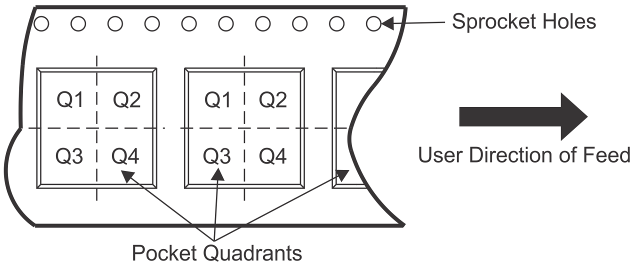


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

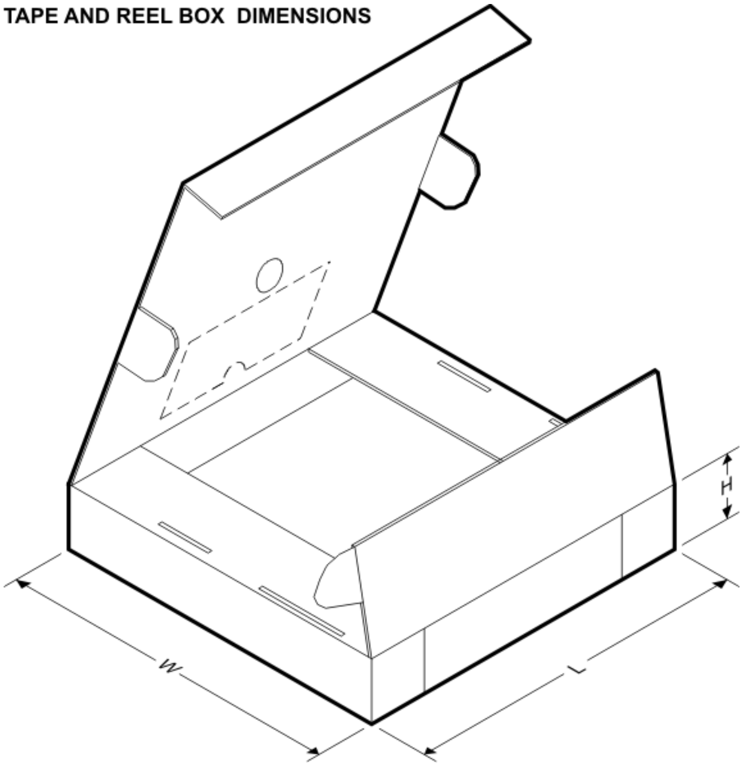
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS63700DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS63700DRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

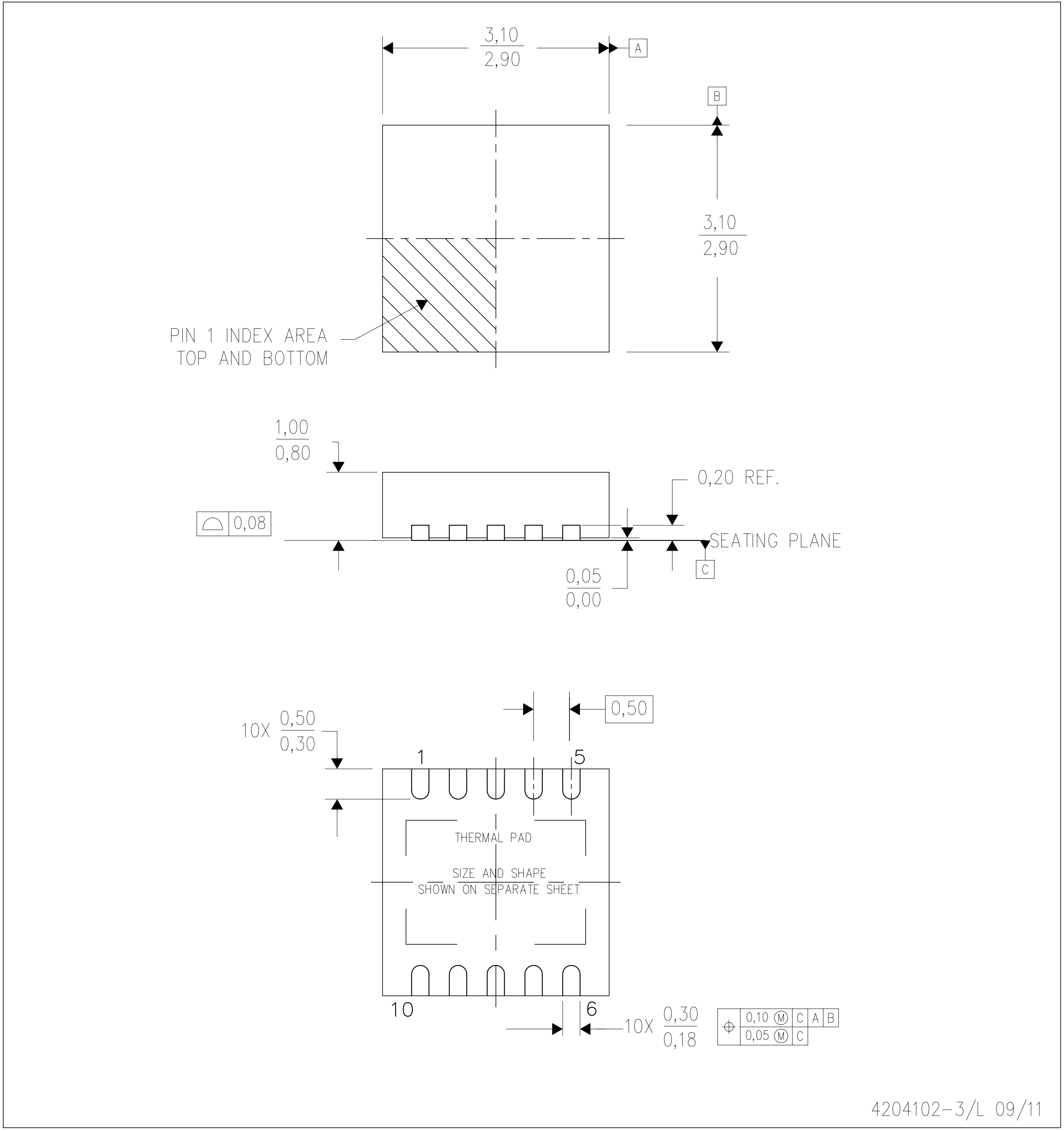
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS63700DRCR	VSON	DRC	10	3000	367.0	367.0	35.0
TPS63700DRCT	VSON	DRC	10	250	210.0	185.0	35.0

DRC (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. Small Outline No–Lead (SON) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance, if present.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions, if present

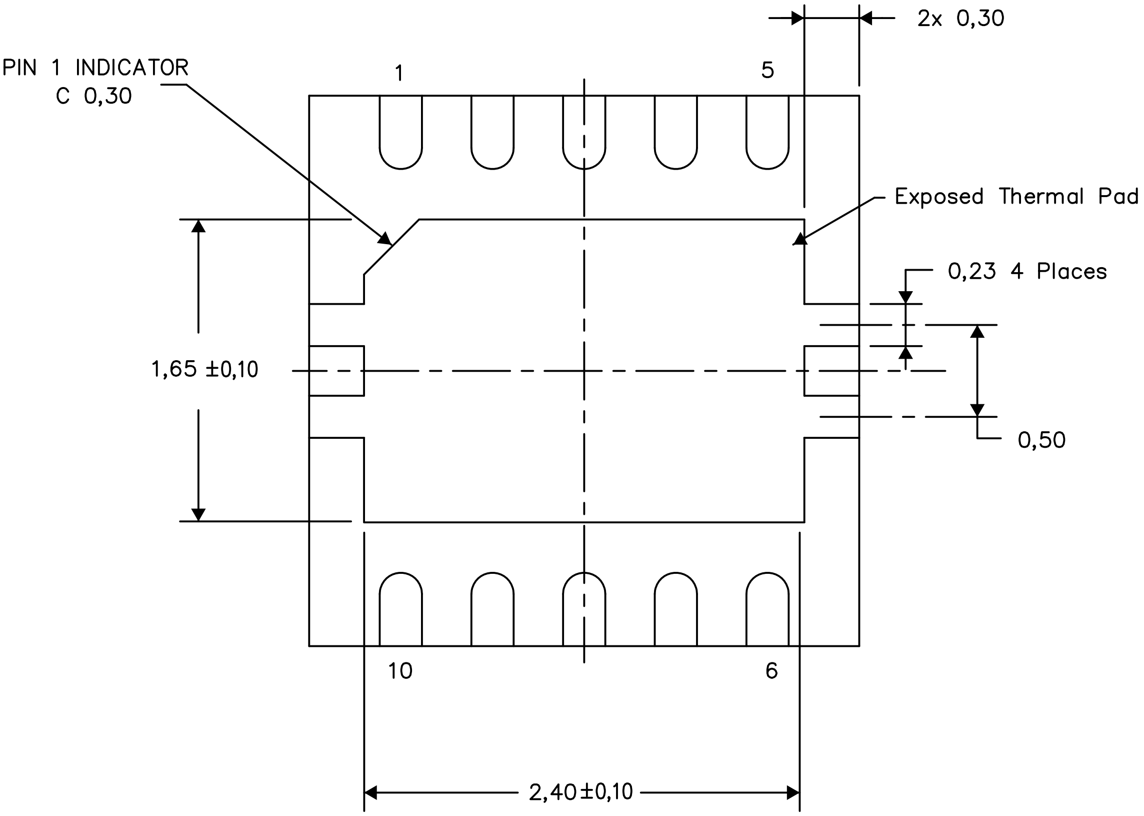
DRC (S-PVSON-N10) PLASTIC SMALL OUTLINE NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



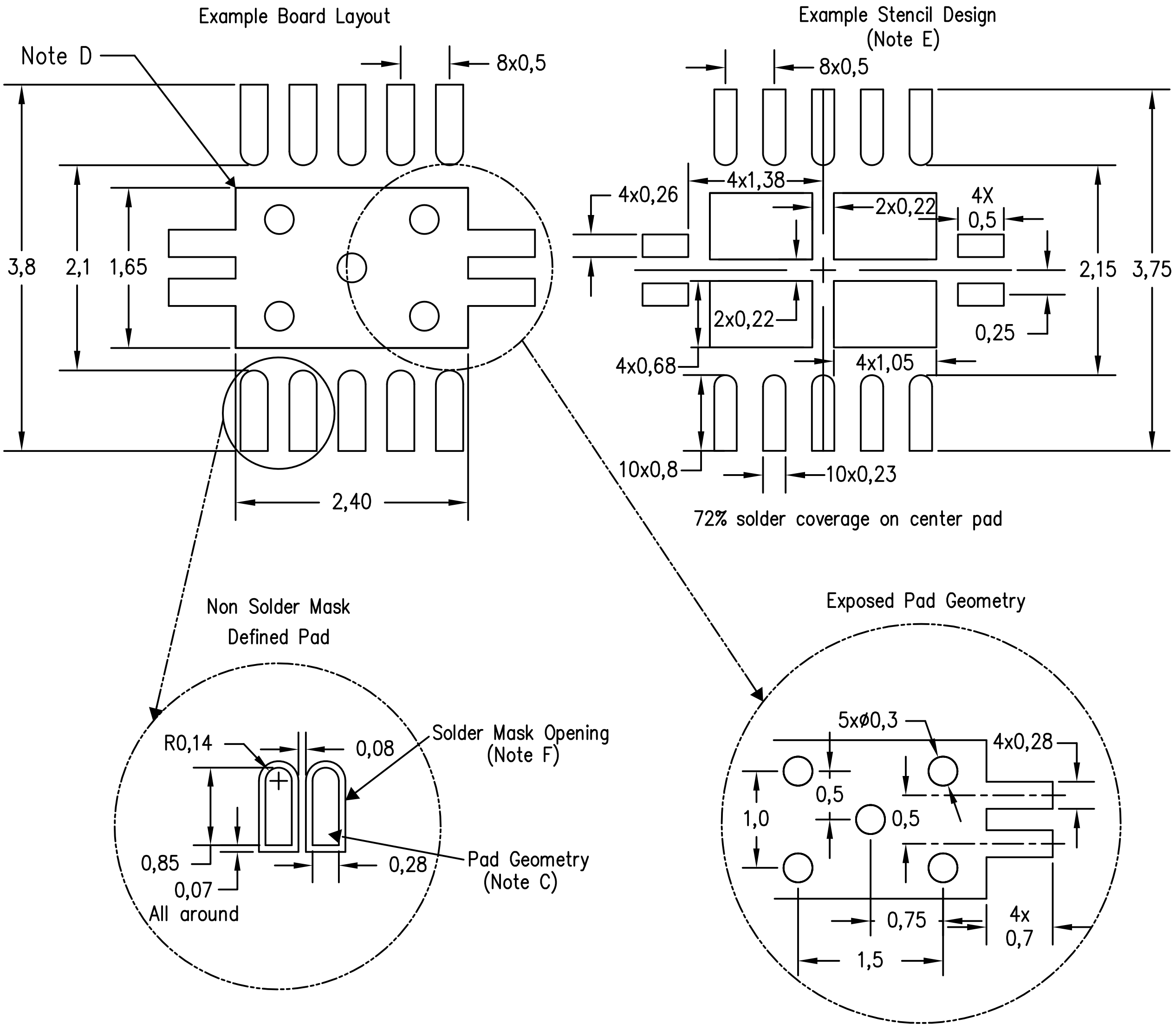
Bottom View

Exposed Thermal Pad Dimensions

4206565-3/Y 08/15

NOTE: A. All linear dimensions are in millimeters

DRC (S-PVSON-N10) PLASTIC SMALL OUTLINE NO-LEAD



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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