TPS65150 Low Input Voltage, Compact LCD Bias IC With VCOM Buffer

1 Features

- 1.8-V to 6-V Input Voltage Range
- Integrated VCOM Buffer
- High-voltage Switch to Isolate $V_{(VGH)}$
- Gate-Voltage Shaping of $V_{(VGH)}$
- 2-A Internal MOSFET switch
- Main Output $V_{(VS)}$ up to 15 V With <1% Output Voltage Accuracy
- Virtual-Synchronous Converter Technology
- Regulated Negative Charge Pump Driver $V_{(VGL)}$
- Regulated Positive Charge Pump Driver $V_{(CPI)}$
- Adjustable Power-On Sequencing
- Adjustable Fault Detection Timing
- Gate Drive Signal for External Isolation MOSFET
- Out-of-Regulation Protection
- Overvoltage Protection
- Thermal Shutdown
- Available in HTSSOP-24 Package
- Available in VQFN-24 Package

2 Applications

- TFT LCD Displays for Notebooks
- TFT LCD Displays for Monitors
- Car Navigation Displays

3 Description

The TPS65150 device offers a very compact and small power supply solution that provides all three voltages required by thin film transistor (TFT) LCD displays. With an input voltage range of 1.8 V to 6 V the device is ideal for notebooks powered by a 2.5-V or 3.3-V input rail or monitor applications with a 5-V input voltage rail. Additionally the TPS65150 device provides an integrated high current buffer to provide the VCOM voltage for the TFT backplane.

Two regulated adjustable charge pump driver provide the positive $V_{(VGH)}$ and negative $V_{(VGL)}$ bias voltages for the TFT. The device incorporates adjustable power-on sequencing for $V_{(VGL)}$ as well as for $V_{(VGH)}$. This avoids any additional external components to implement application specific sequencing. The device has an integrated high-voltage switch to isolate $V_{(VGH)}$.

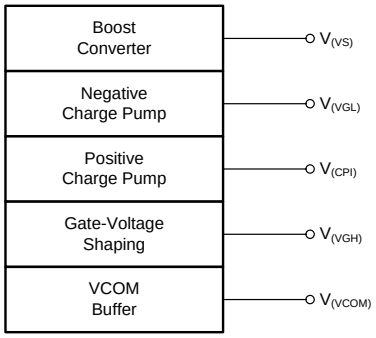
The same internal circuit can also be used to provide a gate shaping signal of $V_{(VGH)}$ for the LCD panel controlled by the signal applied to the CTRL input. For highest safety, the TPS65150 device has an integrated adjustable shutdown latch feature, which allows application-specific flexibility. The device monitors the outputs ($V_{(VS)}$, $V_{(VGL)}$, $V_{(VGH)}$); and, as soon as one of the outputs falls below its power good threshold, the device enters shutdown latch, after its adjustable delay time has passed by.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS65150	HTSSOP (24)	7.80 mm × 4.40 mm
	VQFN (24)	4.00 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Block Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (September 2005) to Revision A	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

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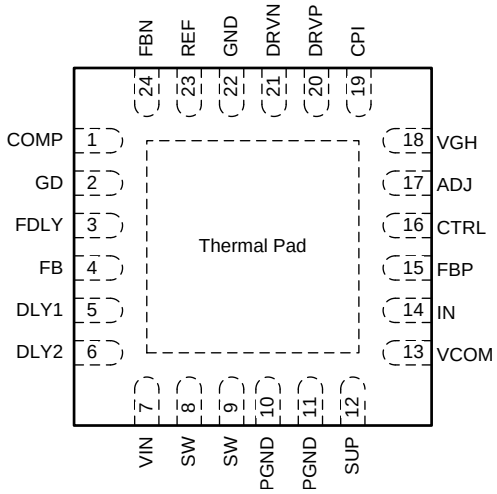
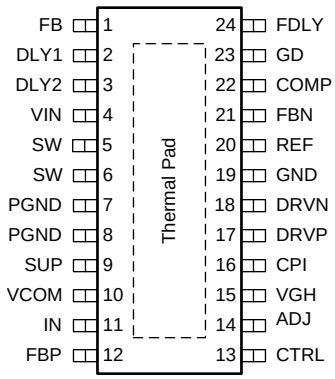
5 Pin Configuration and Functions

RGE Package
24-Pin VQFN
Top View



PWP Package
24-Pin HTSSOP
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	VQFN	HTSSOP		
ADJ	17	14	I/O	Gate voltage shaping circuit. Connecting a capacitor to this pin sets the fall time of the positive gate voltage $V_{(VGH)}$.
COMP	1	22	O	This is the compensation pin for the main boost converter. A small capacitor and if required a series resistor is connected to this pin.
CPI	19	16	I	Input of the VGH isolation switch and gate voltage shaping circuit.
CTRL	16	13	I	Control signal for the gate voltage shaping signal. Apply the control signal for the gate voltage control. Usually the timing controller of the LCD panel generates this signal. If this function is not required, this pin must be connected to V_I. By doing this, the internal switch between CPI and VGH provides isolation for the positive charge pump output $V_{(VGH)}$. DLY2 sets the delay time for $V_{(VGH)}$ to come up.
DLY1	5	2	I/O	Power-on sequencing adjust. Connecting a capacitor from this pin to ground allows to set the delay time between the boost converter output $V_{(VS)}$ and the negative charge pump $V_{(VGL)}$ during start-up.
DLY2	6	3	I/O	Power-on sequencing adjust. Connecting a capacitor from this pin to ground allows to set the delay time between the negative charge pump $V_{(VGL)}$ and the positive charge pump during start-up. Note that Q5 in the gate voltage shaping block only turns on when the positive charge pump is within regulation. (This provides input-output isolation of $V_{(VGH)}$).
DRVN	21	18	I/O	Negative charge pump driver.
DRVP	20	17	I/O	Positive charge pump driver.
FB	4	1	I	Boost converter feedback sense input.
FBN	24	21	I	Negative charge pump feedback sense input.
FBP	15	12	I	Positive charge pump feedback sense input.
FDLY	3	24	I/O	Fault delay. Connecting a capacitor from this pin to V_I sets the delay time from the point when one or more of the of the outputs $V_{(VS)}$, $V_{(VGH)}$, $V_{(VGL)}$ drops below its power good threshold until the device shuts down. To restart the device, the input voltage must be cycled to ground. This feature can be disabled by connecting the FDLY pin to V_I.
GD	2	23	I	Active-low, open-drain output. This output is latched low when the boost converter output is in regulation. This signal can be used to drive an external MOSFET to provide isolation for $V_{(VS)}$.
GND	22	19		Analog ground.

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Pin Functions (continued)

PIN			I/O	DESCRIPTION
NAME	VQFN	HTSSOP		
IN	14	11	I	Input of the VCOM buffer. If this pin is connected to ground, the VCOM buffer is disabled.
PGND	10, 11	7, 8		Power ground.
REF	23	20	O	Internal reference output, typically 1.213 V.
SUP	12	9	I/O	Supply pin of the positive, negative charge pump and boost converter gate drive circuit. This pin should be connected to the output of the main boost converter.
SW	8, 9	5, 6	I	Switch pin of the boost converter.
VCOM	13	10	O	VCOM buffer output. Typically a 1-µF output capacitor is required on this pin.
VGH	18	15	O	Positive output voltage to drive the TFT gates with an adjustable fall time. This pin is internally connected with a MOSFET switch to the positive charge pump input CPI.
VIN	7	4	I	This is the input voltage pin of the device.
Thermal Pad	—	—		The thermal pad must to be soldered to GND

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Voltages on pin VIN(2)	–0.3	7	V
Voltages on pin SUP	–0.3	15.5	V
Voltage on pin SW		20	V
Voltage on CTRL	–0.3	7	V
Voltage on GD		15.5	V
Voltage on CPI		32	V
Continuous power dissipation	See *Thermal Information*		—
Lead temperature (soldering, 10 s)		260	°C
Operating junction temperature	–40	150	°C
Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_I	Input voltage range	1.8		6	V
V_O	Boost converter output voltage			15	V
L	Inductor(1)		4.7		µH
T_A	Operating ambient temperature	–40		85	°C
T_J	Operating junction temperature	–40		125	°C

(1) Refer to application section for further information.

6.4 Thermal Information

THERMAL METRIC(1)		TPS65150		UNIT
		PWP (HTSSOP)	RGE (VQFN)	
		24 PINS	24 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	36.4	34.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	18.8	36.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	15.9	12	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.4	0.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	15.7	12.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.3	3.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

V_I = 3.3 V, $V_{(VS)}$ = 10 V, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
V_I	Input voltage (VIN)			1.8		6	V
	Supply current (VIN)	Device not switching			14	25	µA
	Supply current (SUP)	Device not switching			1.9	3	mA
	Supply current (VCOM buffer)				750	1500	µA
V_{IT-}	Undervoltage lockout threshold (VIN)	V_I falling			1.6	1.8	V
V_{IT+}	Undervoltage lockout threshold (VIN)	V_I rising			1.7	1.9	V
	Thermal shutdown temperature threshold	T_J rising			155		°C
	Thermal shutdown temperature hysteresis				10		°C
LOGIC SIGNALS							
V_{IH}	High-level input voltage (CTRL)			1.6			V
V_{IL}	Low-level input voltage (CTRL)					0.4	V
I_{IH}, I_{IL}	Input current (CTRL)	CTRL = V_I or GND			0.01	0.2	µA
BOOST CONVERTER							
V_O	Output voltage					15	V
V_{ref}	Boost converter reference voltage (FB)			1.136	1.146	1.154	V
I_{IB}	Input bias current (FB)				10	100	nA
$r_{DS(on)}$	Drain-source on-state resistance (Q1)	I_{DS} = 500 mA	V_O = 10 V		200	300	mΩ
			V_O = 5 V		305	450	
$r_{DS(on)}$	Drain-source on-state resistance (Q2)	I_{DS} = 500 mA	V_O = 10 V		8	15	Ω
			V_O = 5 V		12	22	
I_{DS}	Drain-source current rating (Q2)			1			A
	Current limit (SW)			2	2.5	3.4	A

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Electrical Characteristics (continued)

V_I = 3.3 V, $V_{(VS)}$ = 10 V, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{(SW)(off)}$	Off-state current (SW)	$V_{(SW)}$ = 15 V			1	10	µA
V_{IT+}	Overvoltage protection threshold (SUP)	$V_{(SUP)}$ rising		16		20	V
$\Delta V_{O(\Delta VI)}$	Line regulation	V_I = 1.8 V to 5 V	I_O = 1 mA		0.007		%/V
$\Delta V_{O(\Delta IO)}$	Load regulation	V_I = 5 V	I_O = 0 A to 400 mA		0.16		%/A
V_{IT+}	Gate drive threshold (FB)(1)			–12% of V_{ref}		–4% of V_{ref}	V
NEGATIVE CHARGE PUMP							
V_O	Output voltage					–2	V
$V_{(REF)}$	Reference output voltage (REF)			1.205	1.213	1.219	V
V_{ref}	Feedback regulation voltage (FBN)			–36	0	36	mV
I_{IB}	Input bias current (FBN)				10	100	nA
$r_{DS(on)}$	Drain-source on-state resistance (Q4)	I_{DS} = 20 mA			4.4		Ω
$V_{(DRVN)}$	Current sink voltage drop(2)	$V_{(FBN)}$ = 5% above nominal voltage	$I_{(DRVN)}$ = 50 mA		130	300	mV
			$I_{(DRVN)}$ = 100 mA		280	450	
$\Delta V_{O(\Delta IO)}$	Load regulation	V_O = –5 V	I_O = 0 mA to 20 mA		0.016		%/mA
POSITIVE CHARGE PUMP							
V_O	Output voltage	CTRL = GND	VGH = open			30	V
V_{ref}	Feedback regulation voltage (FBP)	CTRL = GND	VGH = open	1.187	1.214	1.238	V
I_{IB}	Input bias current (FBP)	CTRL = GND	VGH = open		10	100	nA
$r_{DS(on)}$	Drain-source on-state resistance (Q3)	I_{DS} = 20 mA			1.1		Ω
$V_{(SUP)} – V_{(DRVP)}$	Current sink voltage drop(2)	$V_{(FBP)}$ = 5% below nominal voltage	$I_{(DRVP)}$ = 50 mA		420	650	mV
			$I_{(DRVP)}$= 100 mA		900	1400	
$\Delta V_{O(\Delta IO)}$	Load regulation	V_O = 24 V	I_O = 0 mA to 20 mA		0.07		%/mA
GATE-VOLTAGE SHAPING							
$r_{DS(on)}$	Drain-source on-state resistance (Q5)	I_O = –20 mA			12	30	Ω
$I_{(ADJ)}$	Capacitor charge current	$V_{(ADJ)}$ = 20 V	$V_{(CPI)}$ = 30 V	160	200	240	µA
$V_O$min	Minimum output voltage	$V_{(ADJ)}$ = 0 V	I_O = –10 mA		2		V
I_{OM}	Maximum output current			20			mA
TIMING CIRCUITS DLY1, DLY2, FDLY							
$I_{(DLY1)}$	Drive current into delay capacitor (DLY1)	$V_{(DLY1)}$ = 1.213 V		3	5	7	µA
$I_{(DLY2)}$	Drive current into delay capacitor (DLY1)	$V_{(DLY2)}$ = 1.213 V		3	5	7	µA
$R_{(FDLY)}$	Fault time delay resistor			250	450	650	kΩ
GATE DRIVE (GD)							
V_{OL}	Low-level output voltage (GD)	I_{OL} = 500 µA				0.5	V
I_{OH}	Off-state current (GD)	V_{OH} = 15 V			0.001	1	µA
VCOM BUFFER							
V_{ISR}	Single-ended input voltage (IN)			2.25		$V_{(SUP)}$ – 2 V	V
V_{IO}	Input offset voltage (IN)	I_O = 0 mA		–25		25	mV

(1) The GD signal is latched low when the main boost converter output is within regulation. The GD signal is reset when the voltage on the VIN pin goes below the UVLO threshold voltage..
(2) The maximum charge pump output current is half the drive current of the internal current source or sink.

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Electrical Characteristics (continued)

V_I = 3.3 V, $V_{(VS)}$ = 10 V, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\Delta V_{O(\Delta IO)}$	Load regulation	I_O = ±25 mA	–37		37	mV
		I_O = ±50 mA	–77		55	
		I_O = ±100 mA	–85		85	
		I_O = ±150 mA	–110		110	
I_{IB}	Input bias current (IN)		–300	–30	300	nA
I_{OM}	Maximum output current (VCOM)	$V_{(SUP)}$ = 15 V	1.2			A
		$V_{(SUP)}$ = 10 V	0.65			
		$V_{(SUP)}$ = 5 V	0.15			

6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Oscillator frequency		1.02	1.2	1.38	MHz
Duty cycle (DRVN)			50%		
Duty cycle (DRVP)			50%		

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6.7 Typical Characteristics

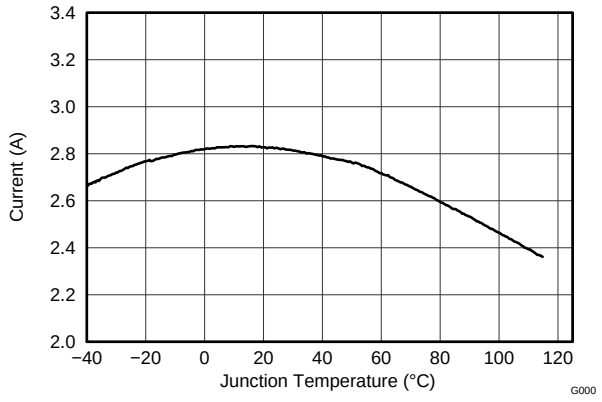

Figure 1. Boost Converter Switch (Q1) Current Limit

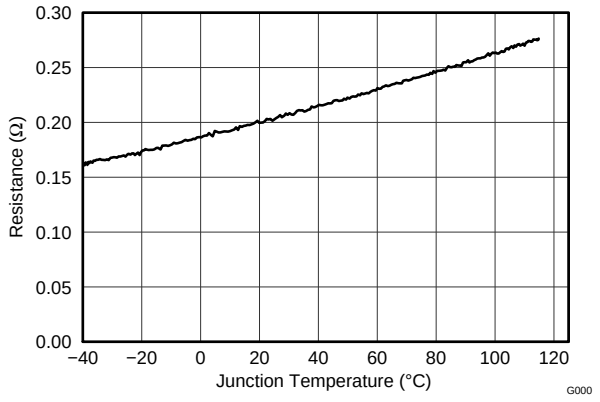

Figure 2. Boost Converter Switch (Q1) $r_{DS(on)}$ vs Temperature

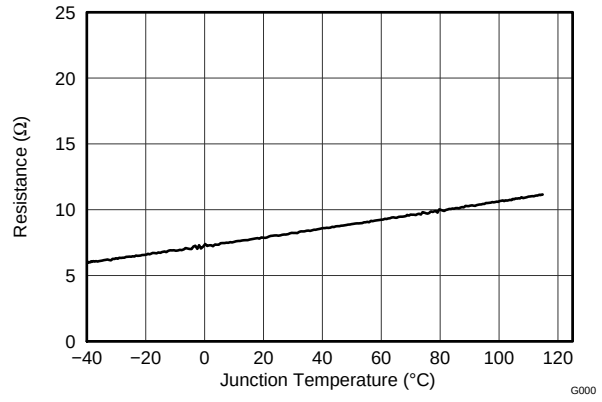

Figure 3. Boost Converter Rectifier (Q2) $r_{DS(on)}$ vs Temperature

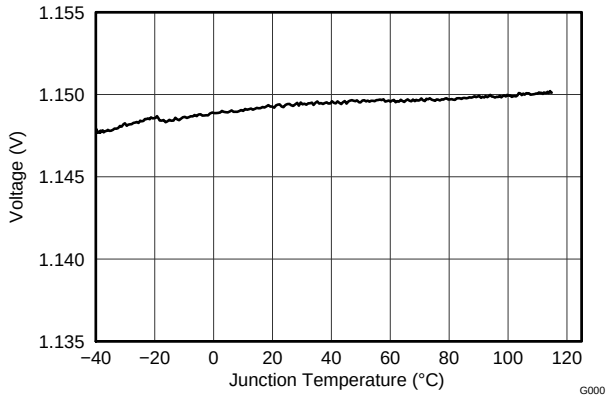

Figure 4. Boost Converter Reference Voltage vs Temperature

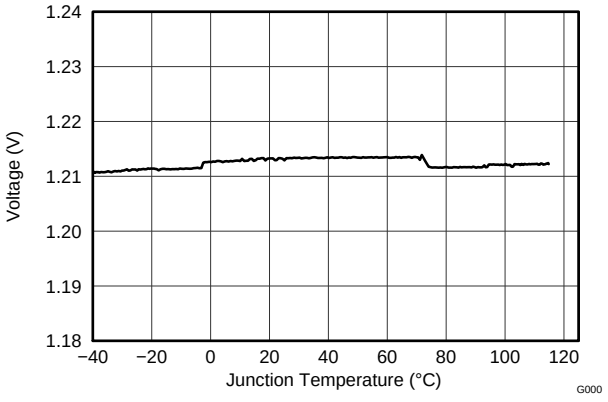

Figure 5. Positive Charge Pump Reference Voltage vs Temperature

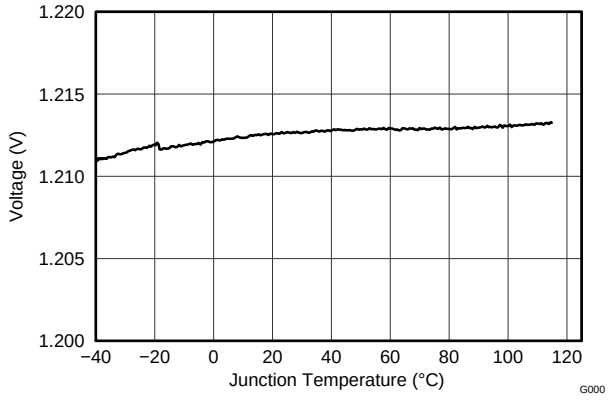

Figure 6. REF Pin Voltage vs Temperature

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Typical Characteristics (continued)

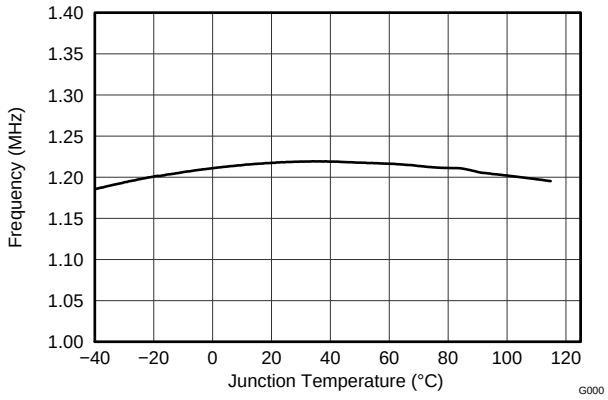

Figure 7. Oscillator Frequency vs Temperature

7 Detailed Description

7.1 Overview

The TPS65150 device is a complete bias supply for LCD displays. The device generates supply voltages for the source driver and gate driver ICs in the display as well as generating the display's common plane voltage (V_{COM}). The device also features a gate-voltage shaping function that can be used to reduce image sticking and improve picture quality. The use of external components to control power-up sequencing, fault detection time, and boost converter compensation allows the device to be optimized for a variety of applications.

The device has been designed to work from input supply voltages as low as 1.8 V and is therefore ideal for use in applications where it is supplied from fixed 2.5-V, 3.3-V, or 5-V supplies or from a single-cell Li-Ion battery.

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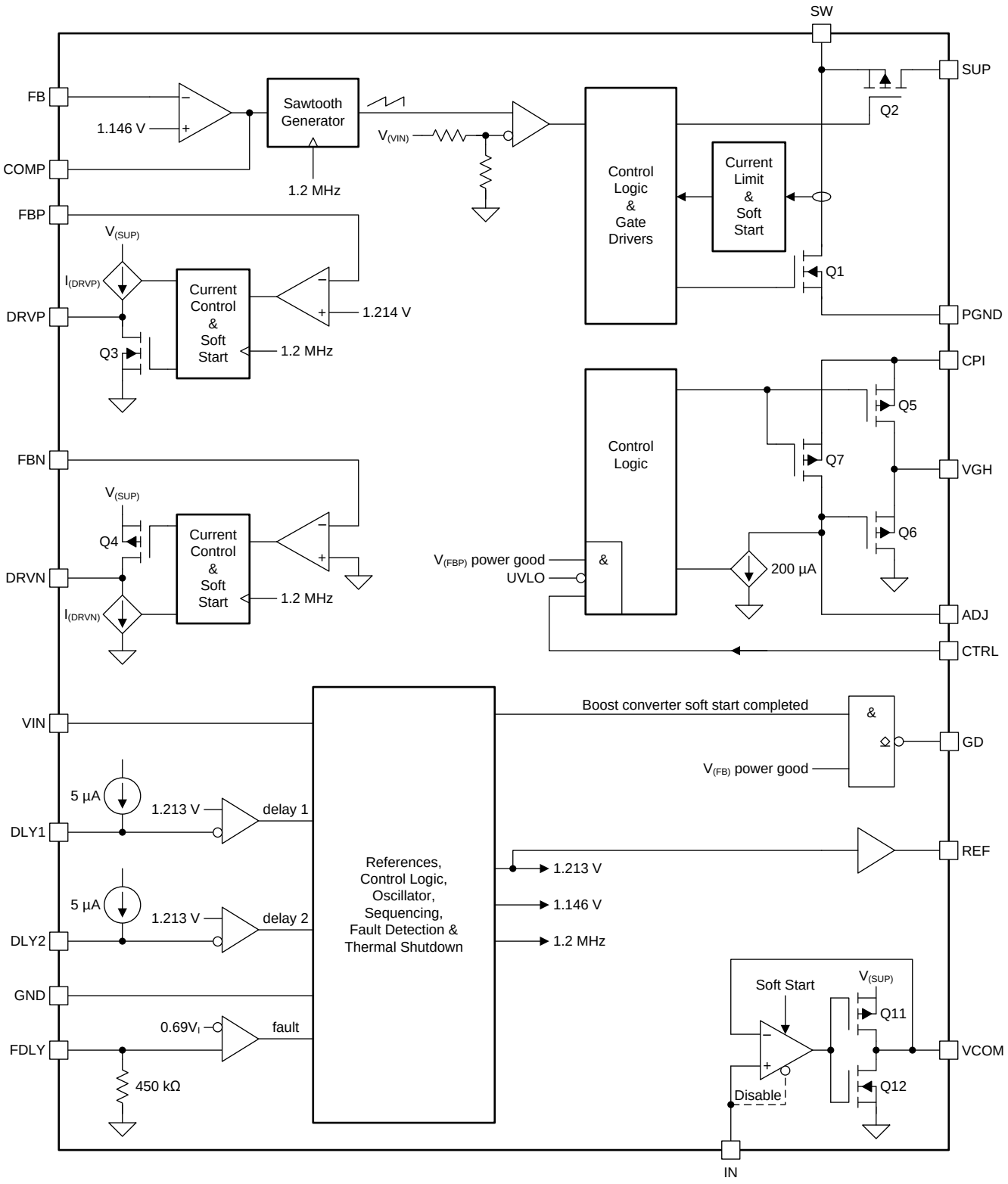
7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Boost Converter

Figure 8 shows a simplified block diagram of the boost converter.

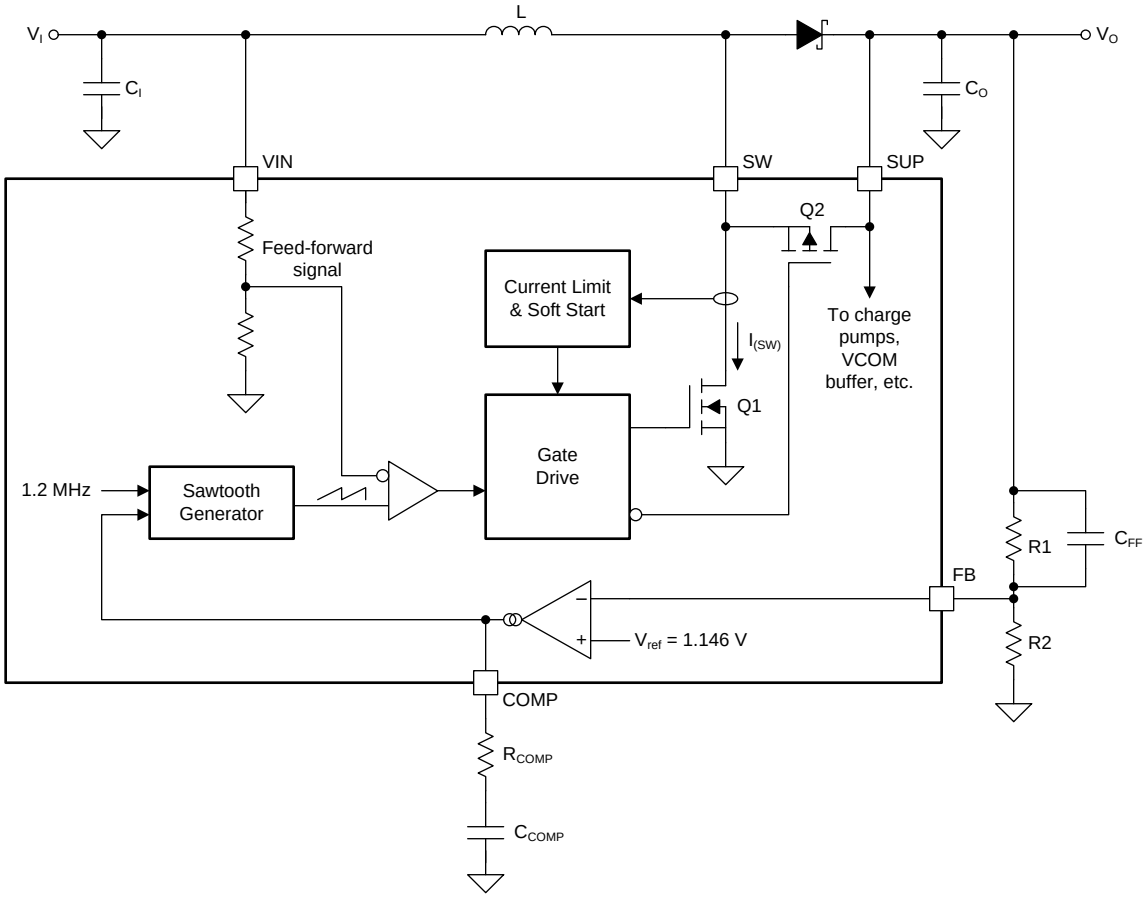


Figure 8. Boost Converter Block Diagram

The boost converter uses a unique fast-response voltage-mode controller scheme with input feedforward to achieve excellent line and load regulation, while still allowing the use of small external components. The use of external compensation adds flexibility and allows the boost converter's response to be optimized for a wide range of external components.

The TPS65150 device uses a virtual-synchronous topology that allows the boost converter to operate in continuous conduction mode (CCM) even at light loads. This is achieved by including a small MOSFET (Q2) in parallel with the external rectifier diode. Under light-load conditions, Q2 allows the inductor current to become negative, maintaining operation in CCM. By operating always in CCM, boost converter compensation is simplified, ringing on the SW pin at low loads is avoided, and additional charge pump stages can be driven by the SW pin. The boost converter duty cycle is given by Equation 1.

$$D = 1 - \frac{\eta V_I}{V_O} \quad (1)$$

where

- η is the boost converter efficiency (either taken from data in *Application Curves* or a worst-case assumption of 75%).
- V_I is the boost converter input supply voltage.
- V_O is the boost converter output voltage.

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Feature Description (continued)

Use Equation 2 to calculate the boost converter peak switch current.

$$I_{(SW)M} = \frac{DV_I}{2fL} + \frac{I_O}{1 - D} \quad (2)$$

where

- f = 1.2 MHz (the boost converter switching frequency);
- I_O is the boost converter output current; and
- L is the boost converter inductance.

7.3.1.1 Setting the Boost Converter Output Voltage

The boost converter output voltage is set by the R1/R2 resistor divider, and is calculated using Equation 3.

$$V_O = \left(1 + \frac{R1}{R2}\right) V_{ref} \quad (3)$$

where

- V_{ref} = 1.146 V (the boost converter internal reference voltage).

To minimize quiescent current consumption, the value of R1 should be in the range of 100 kΩ to 1 MΩ.

7.3.1.2 Boost Converter Rectifier Diode

The diode's reverse voltage rating should be higher than the maximum output voltage of the converter, and its average forward current rating should be higher than the boost converter's output current. Use Equation 4 to calculate the rectifier diode repetitive peak forward current.

$$I_{FRM} = I_{(SW)M} \quad (4)$$

Use Equation 5 to calculate the power dissipated in the rectifier diode.

$$P_D = V_F I_O$$

where

- V_F is the rectifier diode forward voltage. (5)

The main diode parameters affecting converter efficiency are its forward voltage and reverse leakage current, and both should be as low as possible.

7.3.1.3 Choosing the Boost Converter Output Capacitance

The boost converter's output capacitance smooths the output voltage and supplies transient output current demands that are outside the converter's loop bandwidth. Generally speaking, larger output currents and/or smaller input supply voltages require larger output capacitances. Use Equation 6 to calculate the boost converter's output voltage ripple.

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Feature Description (continued)

$$V_{O(PP)} = \frac{DI_O}{fC_O}$$

where

- C_O is the boost converter output capacitance. (6)

7.3.1.4 Compensation

The boost converter requires a series R-C network connected between the COMP pin and ground to compensate its feedback loop. The COMP pin is the output of the boost converter's error amplifier, and the compensation capacitor determines the amplifier's low-frequency gain and the resistor its high-frequency gain. Because the converter gain changes with the input voltage, different compensation capacitors may be required: lower input voltages require a higher gain, and therefore a smaller compensation capacitor value. If an application's input supply voltage changes (for example, if the TPS65150 device is supplied from a battery), choose compensation components suitable for a supply voltage midway between the minimum and maximum values. In all cases, verify that the values selected are suitable by performing transient tests over the full range of operating conditions.

Table 1. Recommended Compensation Components for Different Input Supply Voltages

V_I	C_{COMP}	R_{COMP}	FEED-FORWARD ZERO CUT-OFF FREQUENCY
2.5 V	470 pF	68 kΩ	8.8 kHz
3.3 V	470 pF	33 kΩ	7.8 kHz
5 V	2.2 nF	0 kΩ	11.2 kHz

A feed-forward capacitor C_{FF} in parallel with the upper feedback resistor R1 adds an additional zero to the loop response, which improves transient performance. Table 1 suggests suitable values for the cut-off frequency of the feedforward zero; however, these are only guidelines. In any application, variations in input supply voltage, inductance, and output capacitance all affect circuit operation, and the optimum value must be verified with transient tests before being finalized.

The cut-off frequency of the feed-forward zero is determined using Equation 7.

$$f_{co} = \frac{1}{2\pi(R1)C_{FF}}$$

where

- f_{co} is the cutoff frequency of the feedforward zero formed by R1 and C_{FF}. (7)

7.3.1.5 Soft Start

The boost converter features a soft-start function that limits the current drawn from the input supply during start-up. During the first 2048 switching cycles, the boost converter's switch current is limited to 40% of its maximum value; during the next 2048 cycles, it is limited to 60% of its maximum value; and after that it is as high as it must be to regulate the output voltage (up to 100% of the maximum). In typical applications, this results in a start-up time of about 5 ms (see Figure 9).

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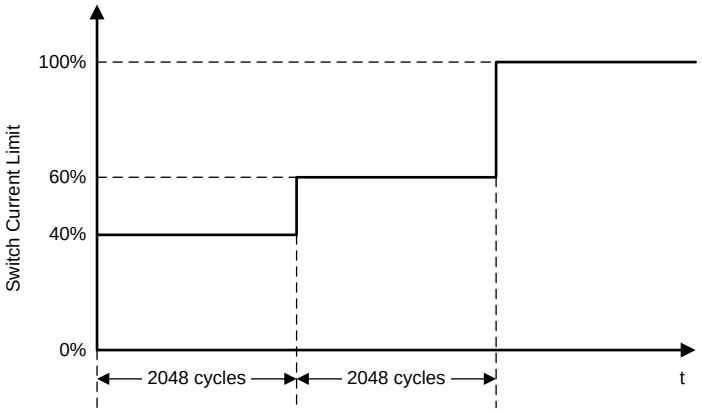

Figure 9. Boost Converter Switch Current Limit During Soft-Start

7.3.1.6 Gate Drive Signal

The GD pin provides a signal to control an external P-channel enhancement MOSFET, allowing the boost converter's output to be isolated from its input when disabled (see Figure 36). The GD pin is an open-drain type whose output is latched low as soon as the boost converter's output voltage reaches its power-good threshold. The GD pin goes high impedance whenever the input voltage falls below the undervoltage lockout threshold or the device shuts down as the result of a fault condition (see *Adjustable Fault Delay*).

7.3.2 Negative Charge Pump

Figure 10 shows a simplified block diagram of the negative charge pump.

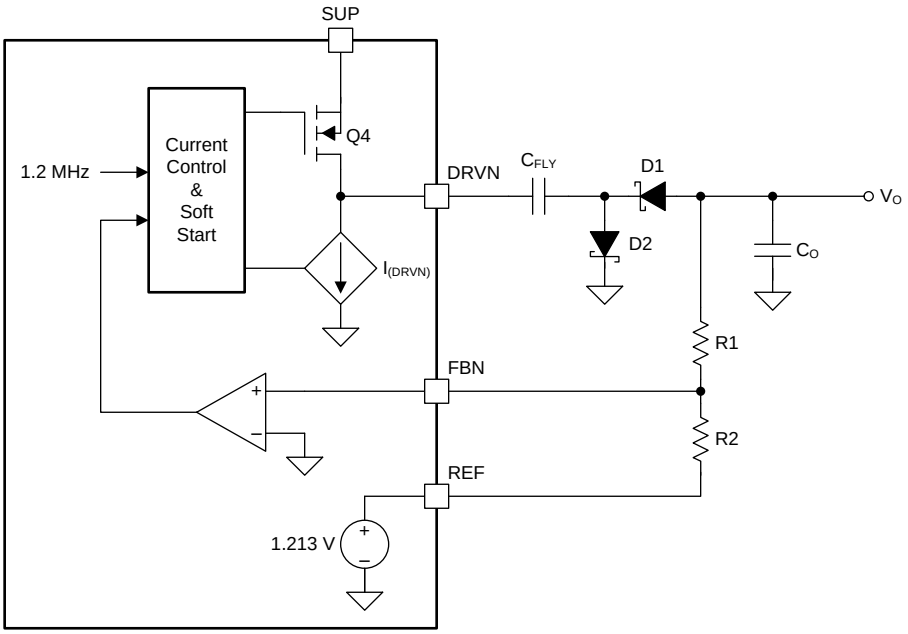

Figure 10. Negative Charge Pump Block Diagram

The negative charge pump operates with a fixed frequency of 1.2 MHz and a 50% duty cycle in two distinct phases. During the charge phase, transistor Q4 is turned on, controlled current source $I_{(DRVN)}$ is turned off, and flying capacitance C_{FLY} charges up to approximately $V_{(SUP)}$. During the discharge phase, Q4 is turned off, $I_{(DRVN)}$ is turned on, and a negative current of $I_{(DRVN)}$ flows through D1 to the output. The output voltage is fed back through R1 and R2 to an error amplifier that controls $I_{(DRVN)}$ so that the output voltage is regulated at the correct value.

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7.3.2.1 Negative Charge Pump Output Voltage

The negative charge pump output voltage is set by resistors R1 and R2 and is given by

$$V_O = -\left(\frac{R1}{R2}\right) V_{(REF)}$$

where

- $V_{(REF)}$ = 1.213 V (the voltage on the REF pin). (8)

Resistor R2 should be in the range 39 kΩ to 150 kΩ. Smaller values load the REF pin too heavily and larger values may cause stability problems.

7.3.2.2 Negative Charge Pump Flying Capacitance

The flying capacitance transfers charge from the SUP pin to the negative charge pump output. TI recommends a flying capacitance of at least 100 nF for output currents up to 20 mA. Smaller values can be used with smaller output currents.

7.3.2.3 Negative Charge Pump Output Capacitance

The output capacitance smooths the discontinuous current delivered by the flying capacitance to generate a dc output voltage. In general, higher output currents require larger output capacitances. Use Equation 9 to calculate the negative charge pump output voltage ripple.

$$V_{O(PP)} = \frac{I_O}{2fC_O}$$

where

- I_O is the negative charge pump output current.
- C_O is the negative charge pump output capacitance.
- f = 1.2 MHz (the negative charge pump switching frequency). (9)

7.3.2.4 Negative Charge Pump Diodes

Both diodes' average forward current is equal to the negative charge pump output current. The repetitive peak forward current in D1 is equal to twice the output current; the repetitive forward current in D2 varies with the value of the flying capacitance. If the recommended flying capacitance (or larger) is used, the repetitive peak current in D2 will be less than four times the output current.

7.3.3 Positive Charge Pump

Figure 11 shows a simplified block diagram of the positive charge pump, which works in a similar way to the negative charge pump except that the positions of the current source I_{DRVP} and the MOSFET Q3 are reversed.

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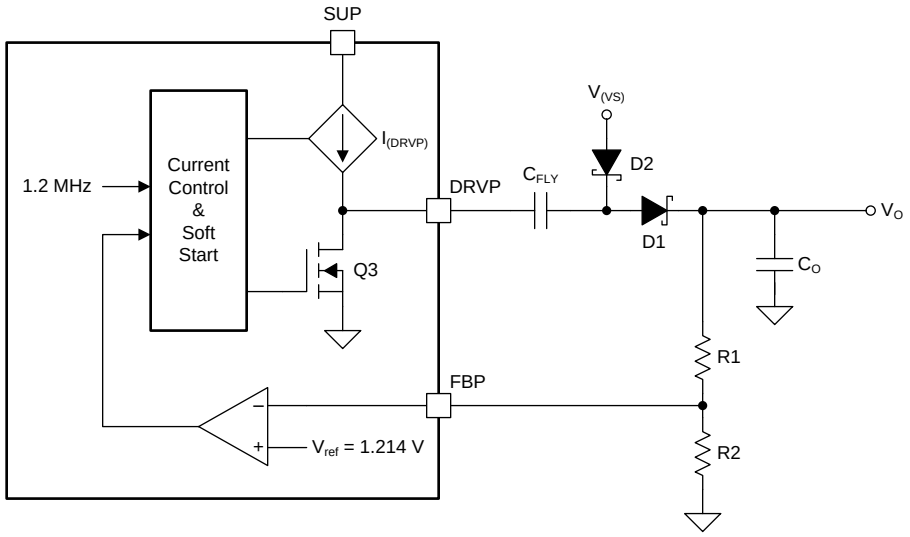

Figure 11. Positive Charge Pump Block Diagram

If higher output voltages are required another charge pump stage can be added to the output, as shown in Figure 34 at the end of the data sheet.

7.3.3.1 Positive Charge Pump Output Voltage

The positive charge pump output voltage is set by resistors R1 and R2 and is calculated using Equation 10:

$$V_O = \left(1 + \frac{R1}{R2}\right) V_{ref} \quad (10)$$

where

- V_{ref} = 1.214 V (the positive charge pump reference voltage).

TI recommends choosing a value for R2 not greater than 1 MΩ.

7.3.3.2 Positive Charge Pump Flying Capacitance

The flying capacitance transfers charge from the SUP pin to the charge pump output. TI recommends a flying capacitance of at least 330 nF (1) for output currents up to 20 mA. Smaller values can be used with smaller output currents.

7.3.3.3 Positive Charge Pump Output Capacitance

The positive charge pump output voltage ripple is given by

$$V_{O(PP)} = \frac{I_O}{2fC_O} \quad (11)$$

where

- I_O is the positive charge pump output current.
- C_O is the positive charge pump output capacitance.
- f = 1.2 MHz (the positive charge pump switching frequency).

(1) The minimum recommended flying capacitance for the positive charge pump is larger than for the negative charge pump because the $r_{DS(on)}$ of Q3 is smaller than the $r_{DS(on)}$ of Q4.

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7.3.3.4 Positive Charge Pump Diodes

Both diodes' average forward current is equal to the positive charge pump output current. The repetitive peak forward current in D1 is equal to twice the output current; the repetitive forward current in D2 varies with the value of the flying capacitance. If the recommended flying capacitance (or larger) is used, the repetitive peak current in D2 will be less than four times the output current.

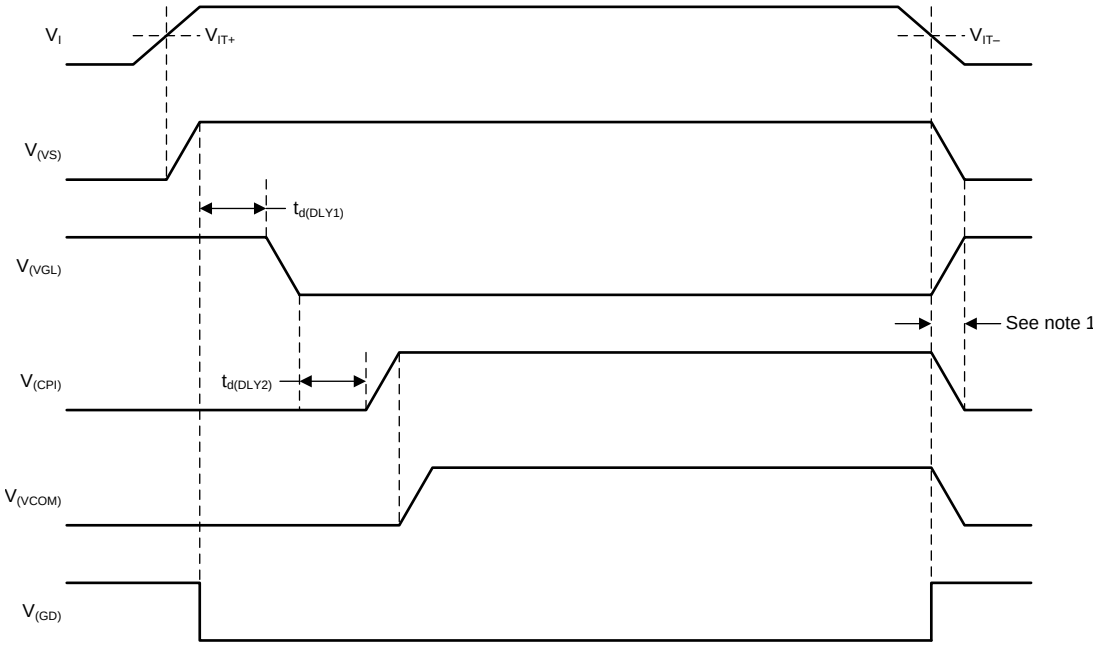
7.3.4 Undervoltage Lockout

An undervoltage lockout (UVLO) function inhibits the TPS65150 device if the input supply voltage is too low for proper operation. The UVLO function senses the voltage on the VIN.

7.3.5 Power-On Sequencing, DLY1, DLY2

The boost converter starts as soon as the input supply voltage exceeds the rising UVLO threshold. The negative charge pump starts $t_{d(DLY1)}$ seconds after the boost converter output voltage has reached its final value, and the positive charge pump starts $t_{d(DLY2)}$ seconds after the negative charge pump's output has reached its final value. The VCOM buffer starts up as soon as the positive charge pump's output voltage ($V_{(CPI)}$) has reached its final value.

Delay times $t_{d(DLY1)}$ and $t_{d(DLY2)}$ are set by capacitors connected between the DLY1 and DLY2 pins and ground.



Notes
1. The fall times of $V_{(VS)}$, $V_{(VGL)}$, $V_{(CPI)}$ depend on their respective load currents and feedback resistances.

Figure 12. Start-Up Sequencing With CTRL = H

The delay times $t_{d(DLY1)}$ and $t_{d(DLY2)}$ are set by the capacitors connected to the DLY1 and DLY2 pins respectively. Each of these pins is connected to its own 5-µA current source ($I_{(DLY1)}$ and $I_{(DLY2)}$) that causes the voltage on the external capacitor to ramp up linearly. The delay time is defined by how long it takes the voltage on the external capacitor to reach the reference voltage, and is given by

$$t_{d(DLY1)} = \frac{C_{DLY1} V_{ref}}{I_{(DLY1)}} \text{ and } t_{d(DLY2)} = \frac{C_{DLY2} V_{ref}}{I_{(DLY2)}} \quad (12)$$

where

- V_{ref} = 1.213 V (the internal reference voltage);
- $I_{(DLY1)}$ = 5 µA (the DLY1 pin output current); and
- $I_{(DLY2)}$ = 5 µA (the DLY2 pin output current).

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7.3.6 Gate Voltage Shaping

The gate voltage shaping function can be used to reduce crosstalk between LCD pixels by reducing the gate drivers' input supply voltage between lines. Figure 13 shows a simplified block diagram of the gate voltage shaping function. Gate voltage shaping is controlled by a logic-level signal applied to the CTRL pin. When CTRL is high, Q5 and Q7 are on and Q6 is off, and the output of the positive charge pump is connected to the VGH pin. When CTRL is low, Q5 and Q7 are off and Q6 is on. Q6 operates as a source follower and tracks the voltage on the ADJ pin, which ramps down linearly as the current sink $I_{(ADJ)}$ discharges external capacitor C_{ADJ} (see Figure 14). The peak-to-peak voltage on the VGH pin is determined by the value of C_{ADJ} and the duration of the low level applied to the CTRL pin, and is calculated using Equation 13.

$$V_{(VGH)(PP)} = \frac{I_{(ADJ)} t_{w(CTRL)}}{C_{ADJ}} \quad (13)$$

where

- $I_{(ADJ)}$ = 200 µA (ADJ pin output current)
- $t_{w(CTRL)}$ is the duration of the low-level signal connected to the CTRL pin
- C_{ADJ} is the capacitance connected to the ADJ pin

When the input supply voltage is below the UVLO threshold or the device enters a shutdown condition because of a fault on one or more of its outputs, Q5 and Q6 turn off and the VGH pin is high impedance.

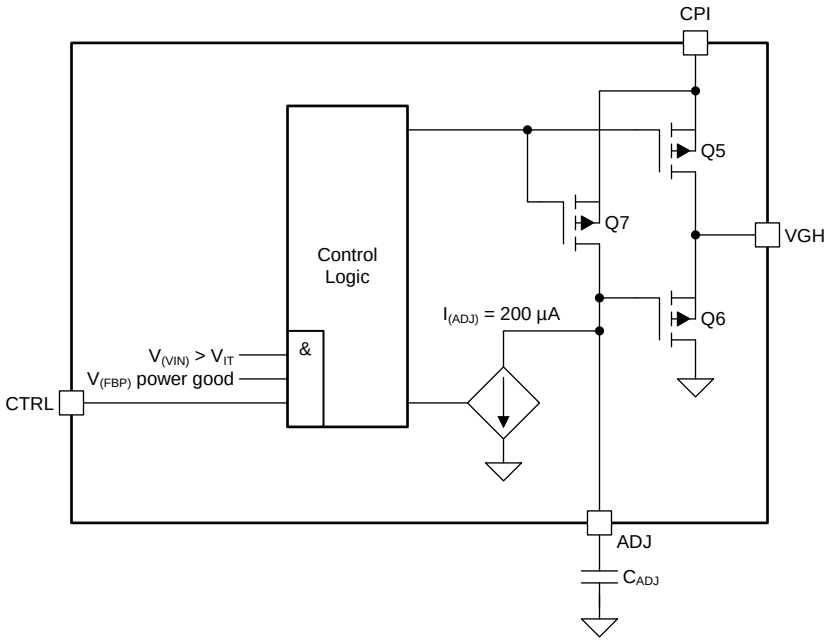

Figure 13. Gate Voltage Shaping Block Diagram

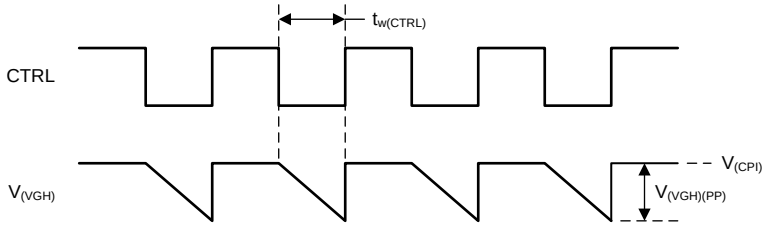

Figure 14. Gate Voltage Shaping Timing

7.3.7 VCOM Buffer

The VCOM Buffer is a transconductance amplifier designed to drive capacitive loads. The IN pin is the input of the VCOM buffer. The VCOM buffer features a soft-start function that reduces the current drawn from the SUP pin when the amplifier starts up.

If the VCOM buffer is not required for certain applications, it is possible to shut down the VCOM buffer by connecting IN to ground, reducing the overall quiescent current. The IN pin cannot be pulled dynamically to ground during operation.

7.3.8 Protection

7.3.8.1 Boost Converter Overvoltage Protection

The boost converter features an overvoltage protection function that monitors the voltage on the SUP pin and forces the TPS65150 device to enter fault mode if the boost converter output voltage exceeds the overvoltage threshold.

7.3.8.2 Adjustable Fault Delay

The TPS65150 device detects a fault condition and shuts down if the boost converter output or either of the charge pump outputs falls out of regulation for longer than the fault delay time $t_{d(FDLY)}$. Fault conditions are detected by comparing the voltage on the feedback pins with the internal power-good thresholds. Outputs that fall below their power-good threshold but recover within less than $t_{d(FDLY)}$ seconds are not detected as faults and the device does not shut down in such cases. The output fault detection function is active during start-up, so the device will shut down if any of its outputs fails to reach its power-good threshold during start-up. Shut-down following an output voltage fault is a latched condition, and the input supply voltage must be cycled to recover normal operation after it occurs.

The fault detection delay time is set by the capacitor connected between the FDLY and VIN pins and is given by

$$t_{d(FDLY)} = R_{(FDLY)} C_{FDLY} \quad (14)$$

where

- $R_{(FDLY)}$ = 450 kΩ (the internal resistance connected to the FDLY pin).
- C_{FDLY} is the external capacitance connected to the FDLY pin.

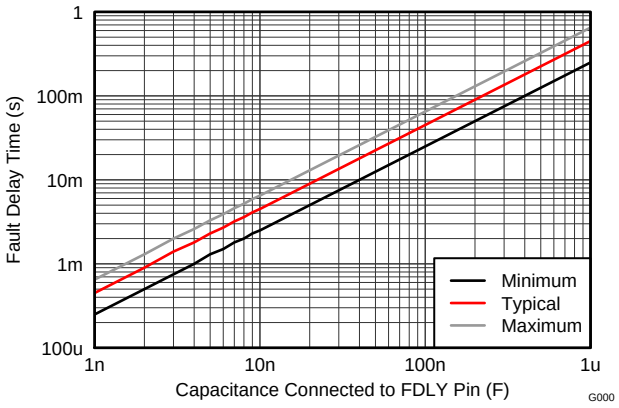

Figure 15. Adjustable Fault Delay Time

7.3.8.3 Thermal Shutdown

A thermal shutdown is implemented to prevent damage because of excessive heat and power dissipation. Typically, the thermal shutdown threshold is 155°C. When this threshold is reached, the device enters shutdown. The device can be enabled again by cycling the input supply voltage.

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7.3.8.4 Undervoltage Lockout

The TPS65150 device has an undervoltage lockout (UVLO) function. The UVLO function stops device operation if the voltage on the VIN pin is less than the UVLO threshold voltage. This makes sure that the device only operates when the supply voltage is high enough for correct operation.

7.4 Device Functional Modes

The TPS65150 device's functional modes are illustrated in Figure 16.

7.4.1 $V_I > V_{IT+}$

When the input supply voltage is above the undervoltage lockout threshold, the device is on and all its functions are enabled. Note that full performance may not be available until the input supply voltage exceeds the minimum value specified in *Recommended Operating Conditions*.

7.4.2 $V_I < V_{IT-}$

When the input supply voltage is below the undervoltage lockout threshold, the TPS65150 device is off and all its functions are disabled.

7.4.3 Fault Mode

The TPS65150 device immediately enters fault mode when any of the following is detected:

- boost converter overvoltage
- overtemperature

The TPS65150 device also enters fault mode if any of the following conditions is detected and persists for longer than $t_{d(FDLY)}$:

- boost converter output out of regulation
- negative charge pump output out of regulation
- positive charge pump output out of regulation

The TPS65150 device does not function during fault mode. Cycle the input supply voltage to exit fault mode and recover normal operation.

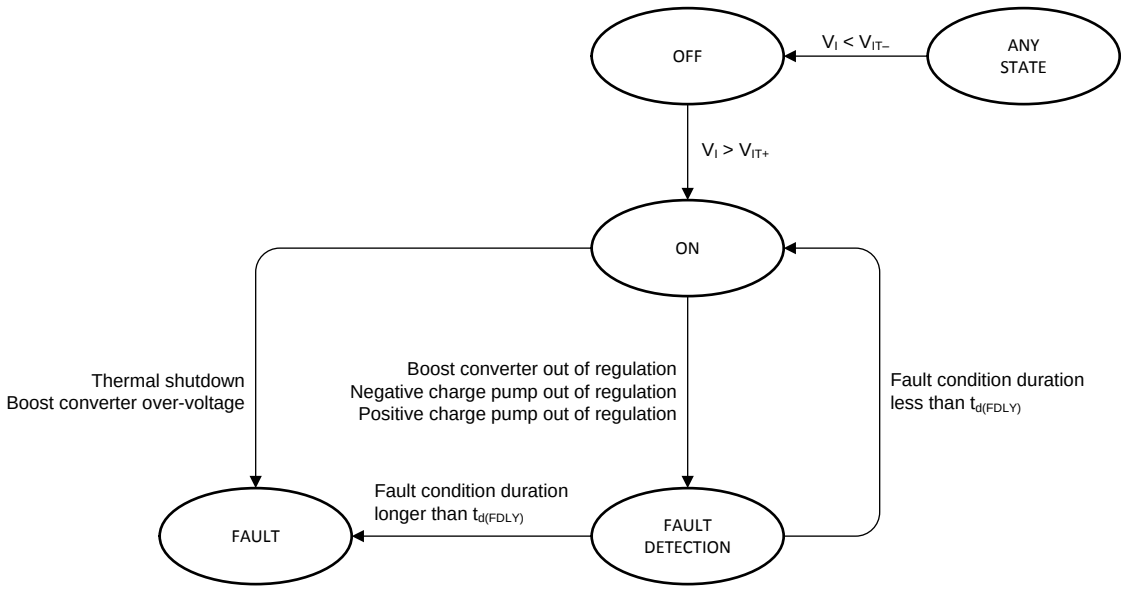

Figure 16. Functional Modes

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS65150 device has been designed to provide the input supply voltages for the source drivers and gate drivers plus the voltage for the common plane in LCD display applications. In addition, the device provides a gate voltage shaping function that can be used to modulate the gate drivers' positive supply to reduce image sticking.

8.2 Typical Application

Figure 17 shows a typical application circuit for a monitor display powered from a 5-V supply. It generates up to 450 mA at 13.5 V to power the source drivers, and 20 mA at 23 V and –5 V to power the gate drivers.

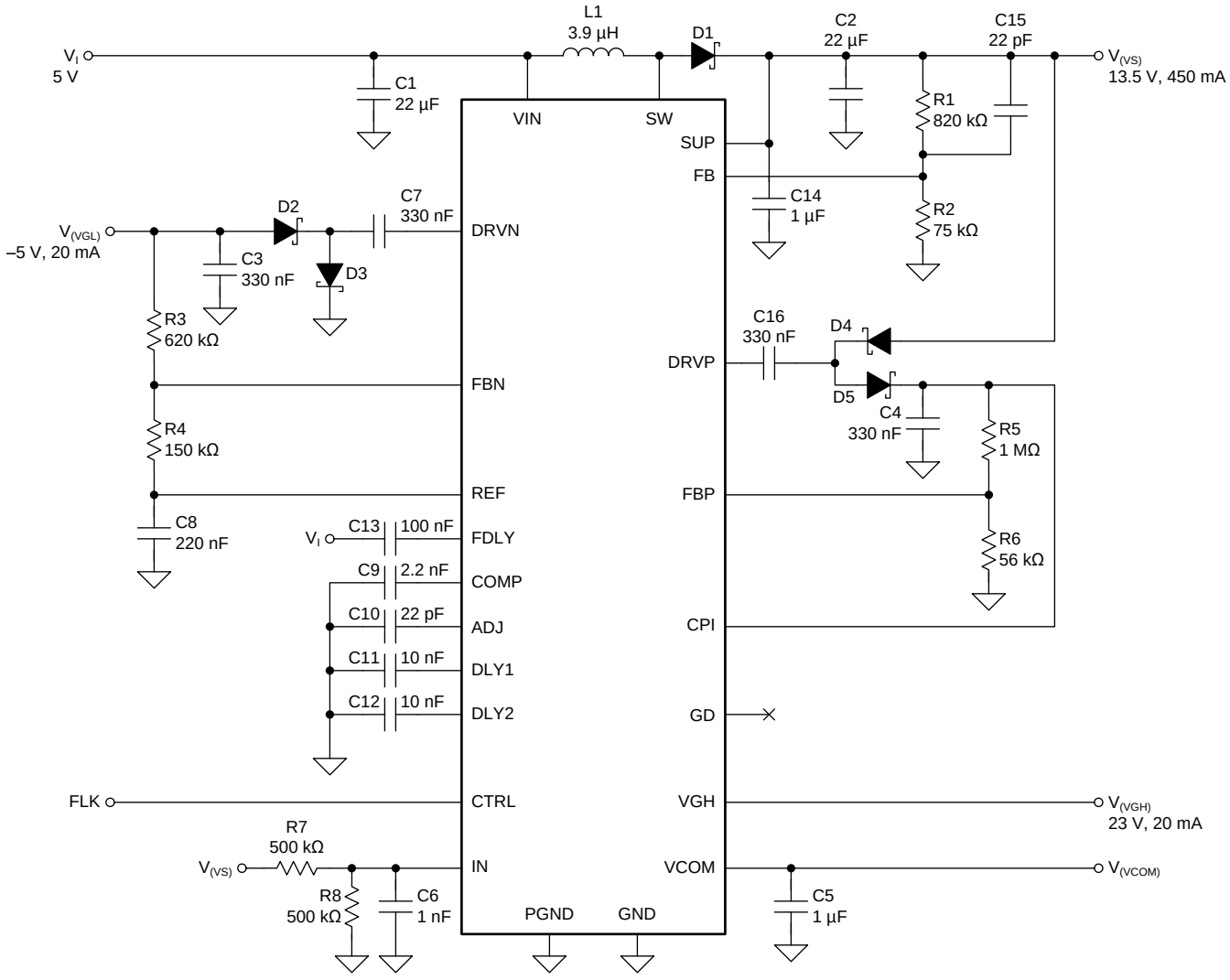

Figure 17. Monitor LCD Supply Powered from a 5-V Rail

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Typical Application (continued)

8.2.1 Design Requirements

Table 2 shows the design parameters for this example.

Table 2. Design Requirements

PARAMETER	SYMBOL	VALUE
Input supply voltage	V_I	5 V
Boost converter output voltage and current	$V_{(VS)}$	13.5 V at 450 mA
Boost converter peak-to-peak output voltage ripple	$V_{(VS)(PP)}$	10 mV
Positive charge pump output voltage and current	$V_{(CPI)}$	23 V at 20 mA
Positive charge pump peak-to-peak output voltage ripple	$V_{(VGH)(PP)}$	100 mV
Negative charge pump output voltage and current	$V_{(VGL)}$	–5 V at 20 mA
Negative charge pump peak-to-peak output voltage ripple	$V_{(VGL)(PP)}$	100 mV
Negative charge pump start-up delay time	t_{d1}	1 ms
Positive charge pump start-up delay time	t_{d2}	1 ms
Fault delay time	$t_{d(fault)}$	45 ms
Gate voltage shaping slope		10 V/µs

8.2.2 Detailed Design Procedure

8.2.2.1 Boost Converter Design Procedure

8.2.2.1.1 Inductor Selection

Several inductors work with the TPS65150, and with external compensation the performance can be adjusted to the specific application requirements.

The main parameter for the inductor selection is the inductor saturation current, which should be higher than the peak switch current as calculated in Equation 2 with additional margin to cover for heavy load transients. The alternative, more conservative approach, is to choose the inductor with a saturation current at least as high as the maximum switch current limit of 3.4 A.

The second important parameter is the inductor DC resistance. Usually, the lower the DC resistance the higher the efficiency. It is important to note that the inductor DC resistance is not the only parameter determining the efficiency. For a boost converter, where the inductor is the energy storage element, the type and material of the inductor influences the efficiency as well. Especially at a switching frequency of 1.2 MHz, inductor core losses, proximity effects, and skin effects become more important. Usually, an inductor with a larger form factor gives higher efficiency. The efficiency difference between different inductors can vary from 2% to 10%. For the TPS65150, inductor values from 3.3 µH and 6.8 µH are a good choice, but other values can be used as well. Possible inductors are shown in Table 3. Equivalent parts can also be used.

Table 3. Inductor Selection

INDUCTANCE	I_{SAT}	DCR	MANUFACTURER	PART NUMBER	DIMENSIONS
4.7 µH	2.6 A	54 mΩ	Coilcraft	DO1813P-472HC	8.89 mm × 6.1 mm × 5 mm
4.2 µH	2.2 A	23 mΩ	Sumida	CDRH5D28 4R2	5.7 mm × 5.7 mm × 3 mm
4.7 µH	1.6 A	48 mΩ	Sumida	CDC5D23 4R7	6 mm × 6 mm × 2.5 mm
4.2 µH	1.8 A	60 mΩ	Sumida	CDRH6D12 4R2	6.5 mm × 6.5 mm × 1.5 mm
3.9 µH	2.6A	20 mΩ	Sumida	CDRH6D28 3R9	7 mm × 7 mm × 3 mm
3.3 µH	1.9 A	50 mΩ	Sumida	CDRH6D12 4R2	6.5 mm × 6.5 mm × 1.5 mm

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The first step in the design procedure is to verify whether the maximum possible output current of the boost converter supports the specific application requirements. A simple approach is to estimate the converter efficiency, by taking the efficiency numbers from the provided efficiency curves, or use a worst case assumption for the expected efficiency, for example, 75%.

From Figure 19, it can be seen that the boost converter efficiency is about 85% when operating under the target application conditions. Inserting these values into Equation 1 yields

$$D = 1 - \frac{(0.85)(5\ V)}{13.5\ V} = 0.69 \tag{15}$$

and from Equation 2, the peak switch current can be calculated as

$$I_{(SW)M} = \frac{(0.69)(5\ V)}{2(1.2\ MHz)(3.9\ \mu H)} + \frac{(0.45\ A)}{1 - 0.69} = 1.8\ A \tag{16}$$

The peak switch current is the peak current that the integrated switch, inductor, and rectifier diode must be able to handle. The calculation must be done for the minimum input voltage where the peak switch current is highest. For the calculation of the maximum current delivered by the boost converter, it must be considered that the positive and negative charge pumps as well as the VCOM buffer run from the output of the boost converter as well.

8.2.2.2 Rectifier Diode Selection

The rectifier diode reverse voltage rating should be higher than the maximum output voltage of the converter (13.5 V in this application); its average forward current rating should be higher than the maximum boost converter output current of 450 mA, and its repetitive peak forward current should be greater than or equal to the peak switch current of 1.8 A. Not all diode manufacturers specify repetitive peak forward current; however, a diode with an average forward current rating of 1 A or higher is suitable for most practical applications.

From Equation 5, the power dissipated in the rectifier diode is given by

$$P_D = I_O V_F = (0.45\ A)(0.5\ V) = 0.225\ W \tag{17}$$

Table 4 lists a number of suitable rectifier diodes, any of which would be suitable for this application. Equivalent parts can also be used.

Table 4. Rectifier Diode Selection

$I_{F(AV)}$	V_R	V_F	MANUFACTURER	PART NUMBER
2 A	20 V	0.44 V at 2 A	Vishay Semiconductor	SL22
2 A	20 V	0.5 V at 2 A	Fairchild Semiconductor	SS22
1 A	30 V	0.44 V at 2 A	Fairchild Semiconductor	MBRS130L
1 A	20 V	0.45 V at 1 A	Microsemi	UPS120
1 A	20 V	0.45 V at 1 A	ON Semiconductor	MBRM120

8.2.2.3 Setting the Output Voltage

Rearranging Equation 3 and inserting the application parameters, we get

$$\frac{R1}{R2} = \frac{13.5\ V}{1.146\ V} - 1 = 10.78 \tag{18}$$

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Standard values of R1 = 820 kΩ and R2 = 75 kΩ result in a nominal output voltage of 13.68 V and satisfy the recommendation that the value R1 be lower than 1 MΩ.

8.2.2.4 Output Capacitor Selection

For best output voltage filtering, a low ESR output capacitor is recommended. Ceramic capacitors have a low ESR value, but tantalum capacitors can be used as well, depending on the application. A 22-µF ceramic output capacitor works for most applications. Higher capacitor values can be used to improve the load transient regulation. See Table 5 for the selection of the output capacitor.

Rearranging Equation 6 and inserting the application parameters, the minimum value of output capacitance is given by Equation 19.

$$C_O = \frac{1 - 0.69}{(1.2\ \text{MHz})(10\ \text{mV})}\left(1.8\ \text{A} - 0.45\ \text{A} - \left(\frac{13.5\ \text{V} - 5\ \text{V}}{3.9\ \mu\text{H}}\right)\left(\frac{1 - 0.69}{1.2\ \text{MHz}}\right)\right) = 20.3\ \mu\text{F} \quad (19)$$

The closest standard value is 22 µF. In practice, TI recommends connecting an additional 1-µF capacitor directly to the SUP pin to ensure a clean supply to the internal circuitry that runs from this supply voltage.

8.2.2.5 Input Capacitor Selection

For good input voltage filtering, low ESR ceramic capacitors are recommended. A 22-µF ceramic input capacitor is sufficient for most applications. For better input voltage filtering, this value can be increased. See Table 5 for input capacitor recommendations. Equivalent parts can also be used.

Table 5. Input and Output Capacitance Selection

CAPACITANCE	VOLTAGE RATING	MANUFACTURER	PART NUMBER	SIZE
22 µF	16 V	Taiyo Yuden	EMK325BY226MM	1206
22 µF	6.3 V	Taiyo Yuden	JMK316BJ226	1206

8.2.2.6 Compensation

From Table 1, it can be seen that the recommended values for C9 and R9 when V_I = 5 V are 2.2 nF and 0 Ω respectively, and that a feedforward zero at 11.2 kHz should be added.

Rearranging Equation 7, we get

$$C15 = \frac{1}{2\pi f_{co}(R1)} \quad (20)$$

Inserting f_{co} = 11.2 kHz and R1 = 820 kΩ, we get

$$C15 = \frac{1}{2\pi(11.2\ \text{kHz})(820\ \text{k}\Omega)} = 17\ \text{pF}$$

In this case, a standard value of 22 pF was used.

8.2.2.7 Negative Charge Pump

8.2.2.7.1 Choosing the Output Capacitance

Rearranging Equation 9 and inserting the application parameters, the minimum recommended value of C3 is given by

$$C3 = \frac{I_O}{2fV_{O(PP)}} = \frac{20\ mA}{2(1.2\ MHz)(100\ mV)} = 83\ nF \quad (21)$$

In this application, a capacitance of 330 nF was used to allow the same value to be used for all charge pump capacitances.

8.2.2.7.2 Choosing the Flying Capacitance

A minimum flying capacitance of 100 nF is recommended. In this application, a capacitance of 330 nF was used to allow the same value to be used for all charge pump capacitances.

8.2.2.7.3 Choosing the Feedback Resistors

From Equation 22, the ratio of R3 to R4 required to generate an output voltage of –5 V is given by

$$R3 = -\left(\frac{V_O}{V_{(REF)}}\right)R4 = -\left(\frac{-5\ V}{1.213\ V}\right)R4 = (4.122)R4 \quad (22)$$

Values of R3 = 620 kΩ and R4 = 150 kΩ generate a nominal output voltage of –5.014 V and load the REF pin with only 8 µA.

8.2.2.7.4 Choosing the Diodes

The average forward current in D2 and D3 is equal to the output current and therefore a maximum of 20 mA. The peak repetitive forward current in D3 – the peak current in D2 is always smaller – is less than four times the output current, that is, less than 80 mA.

The BAT54S comprises two Schottky diodes in a small SOT-23 package and easily meets the current requirements of this application.

8.2.2.8 Positive Charge Pump

8.2.2.8.1 Choosing the Flying Capacitance

A minimum flying capacitance of 100 nF is recommended. In this application, a value of 330 nF was used to allow the same value to be used for all charge pump capacitances.

8.2.2.8.2 Choosing the Output Capacitance

Rearranging Equation 10 and inserting the application parameters, we get

$$C4 = \frac{(20\ mA)}{2(1.2\ MHz)(100\ mV)} = 83\ nF \quad (23)$$

In this application, a nominal value of 330 nF was used to allow the same value to be used for all charge pump capacitances.

8.2.2.8.3 Choosing the Feedback Resistors

Rearranging Equation 8 and inserting the application parameters, we get

$$\frac{R5}{R6} = \frac{23\ V}{1.214\ V} - 1 = 17.95 \quad (24)$$

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Standard values of 1 MΩ and 56 kΩ result in a nominal output voltage of 22.89 V.

8.2.2.8.4 Choosing the Diodes

The average forward current in D4 and D5 is equal to the output current and therefore a maximum of 20 mA. The peak repetitive forward current in D4 – the peak current in D5 is always smaller – is less than five times the output current, that is, less than 100 mA.

The BAT54S comprises two Schottky diodes in a small SOT-23 package and easily meets the current requirements of this application.

8.2.2.9 Gate Voltage Shaping

Rearranging Equation 13 and inserting $I_{(ADJ)}$ = 200 µA and slope = 10 V/µs, we get

$$C10 = \frac{I_{(ADJ)}}{\text{slope}} = \frac{200\ \mu A}{10\ V/\mu s} = 20\ pF \tag{25}$$

The closest standard value for C10 is 22 pF.

8.2.2.10 Power-On Sequencing

Rearranging Equation 12 and inserting $t_{d1} = t_{d2}$ = 1 ms and V_{ref2} = 1.213 V, we get

$$C11 = C12 = \frac{(5\ \mu A)(2.5\ ms)}{1.213\ V} = 10.31\ nF \tag{26}$$

10 nF is the closest standard value.

8.2.2.11 Fault Delay

Rearranging Equation 14 and inserting $t_{d(FDLY)}$ = 45 ms, we get

$$C_{FDLY} = \frac{45\ ms}{450\ k\Omega} = 100\ nF \tag{27}$$

100 nF is a standard value.

8.2.2.12 Undervoltage Lockout Function

The TPS65150 device contains an undervoltage lockout (UVLO) function that stops the device operating if the voltage on the VDD pin is too low.

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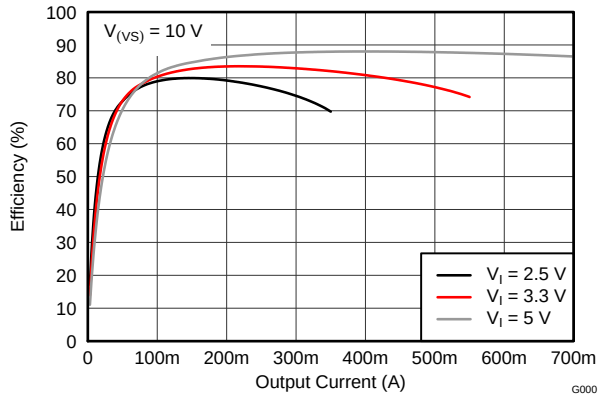
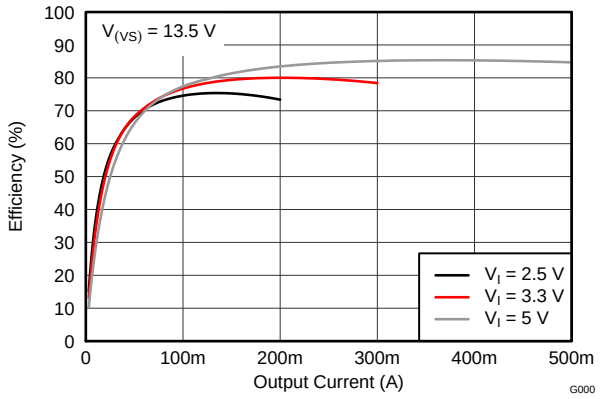
8.2.3 Application Curves



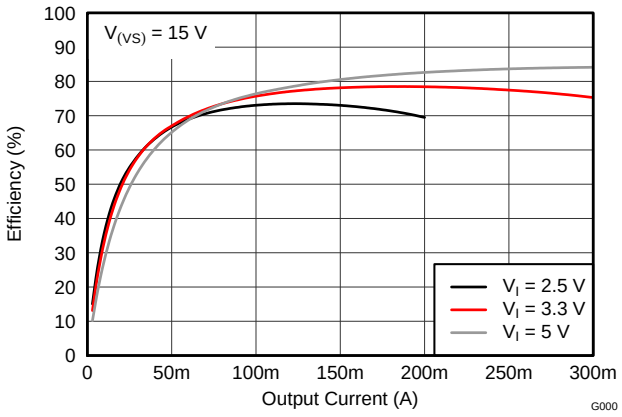
$I_{(VGH)}$ = 0 mA $I_{(VGL)}$ = 0 mA

Figure 18. Boost Converter Efficiency ($V_{(VS)}$ = 10 V)



$I_{(VGH)}$ = 0 mA $I_{(VGL)}$ = 0 mA

Figure 19. Boost Converter Efficiency ($V_{(VS)}$ = 13.5 V)



$I_{(VGH)}$ = 0 mA $I_{(VGL)}$ = 0 mA

Figure 20. Boost Converter Efficiency ($V_{(VS)}$ = 15 V)

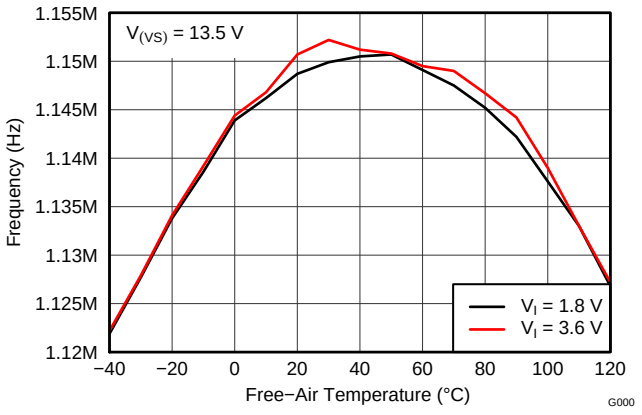


Figure 21. Boost Converter Switching Frequency

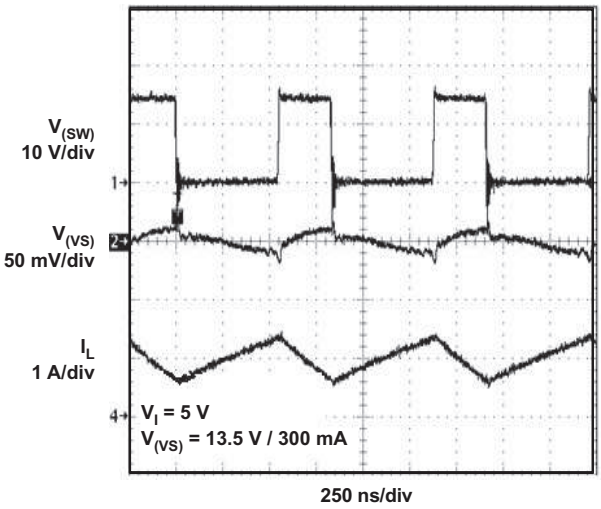


Figure 22. Boost Converter Operation (Nominal Load)

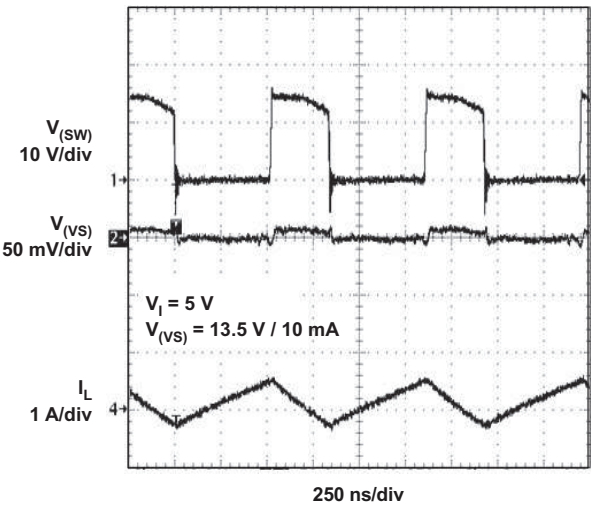


Figure 23. Boost Converter Operation (Light Load)

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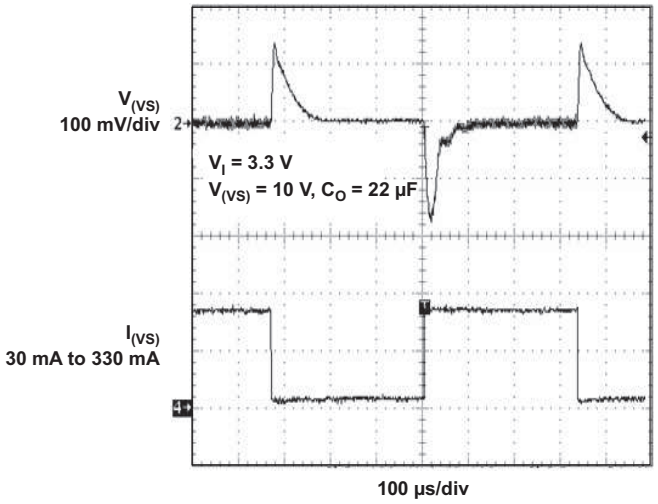

Figure 24. Boost Converter Load Transient Response

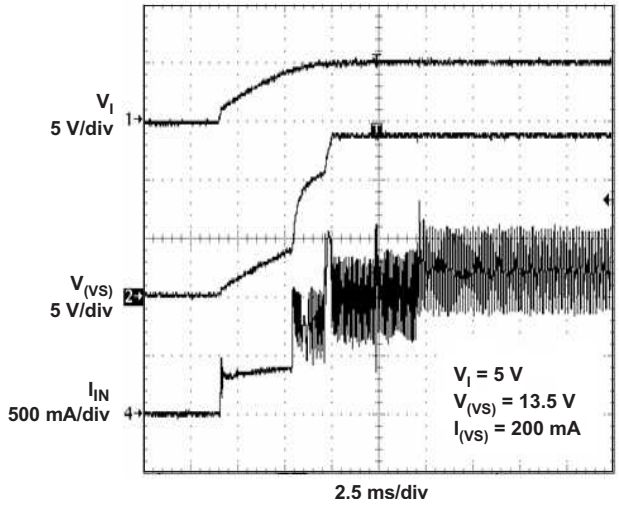

Figure 25. Boost Converter Soft Start

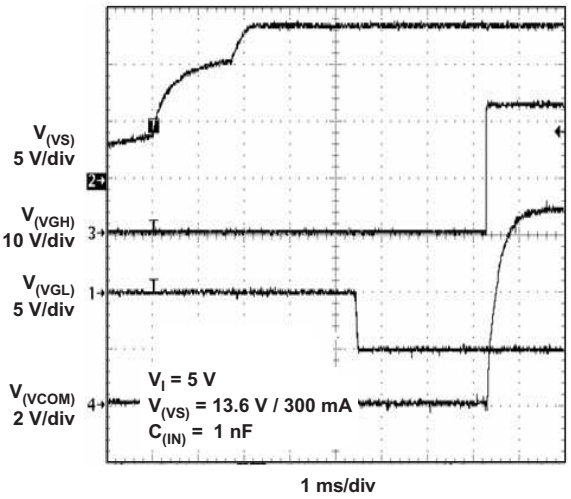

Figure 26. Power-On Sequencing

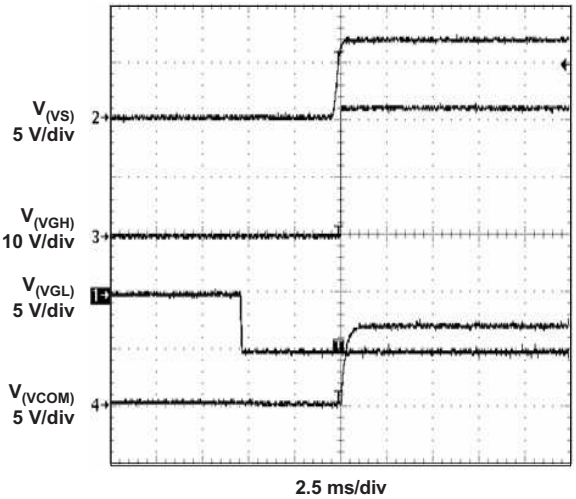

Figure 27. Power-On Sequencing With External Isolation MOSFET

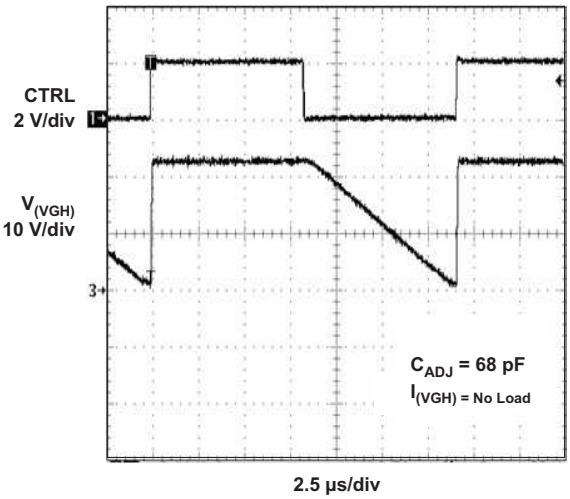

Figure 28. Gate Voltage Shaping

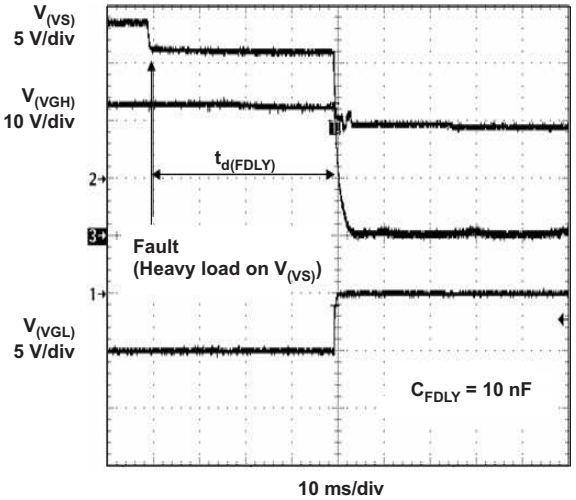

Figure 29. Adjustable Fault Detection Time

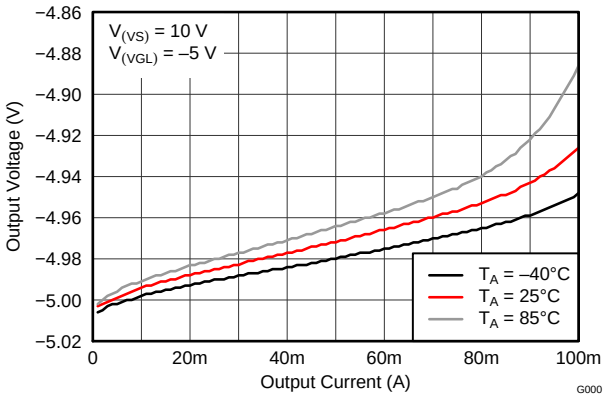

Figure 30. Negative Charge Pump Load Regulation

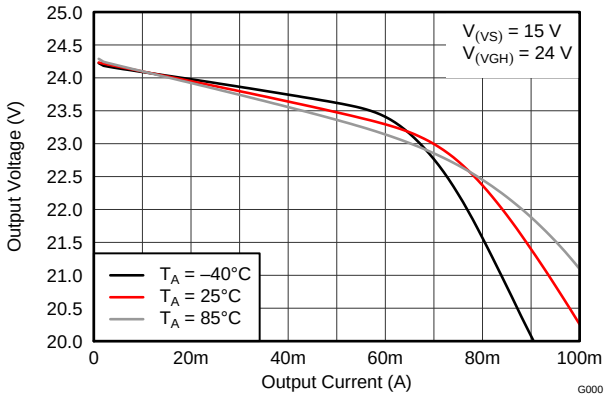

Figure 31. Positive Charge Pump Load Regulation (×2)

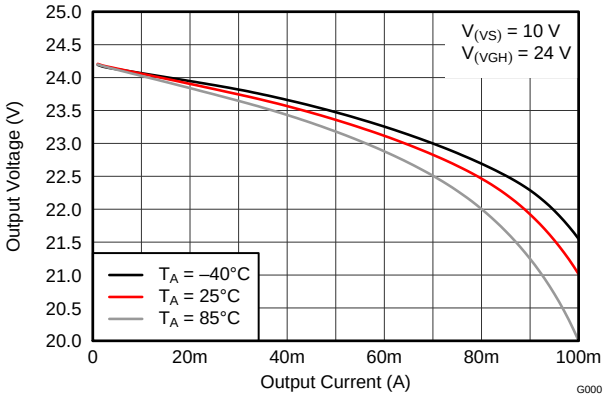

Figure 32. Positive Charge Pump Load Regulation (×3)

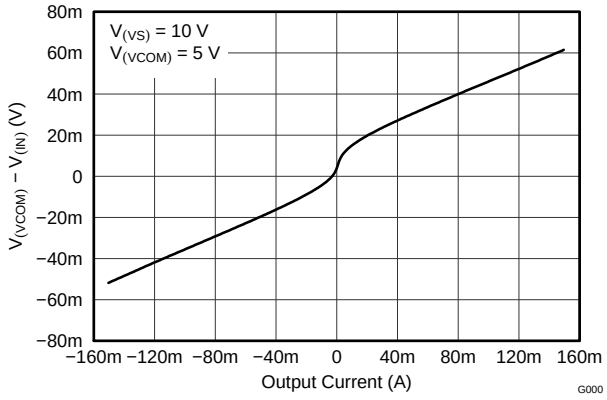

Figure 33. VCOM Buffer Load Regulation

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8.3 System Examples

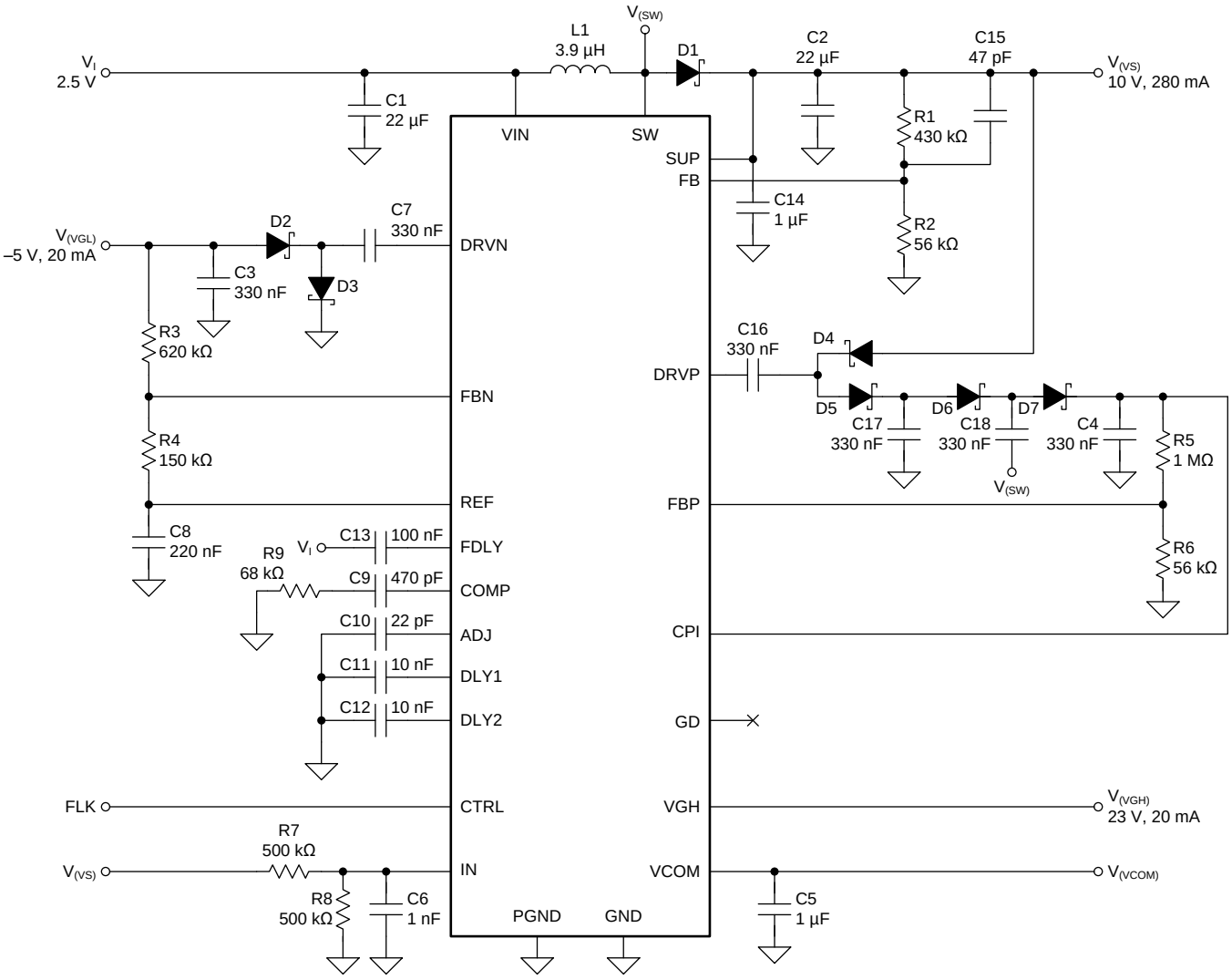

Figure 34. Notebook LCD Supply Powered from a 2.5-V Rail

System Examples (continued)

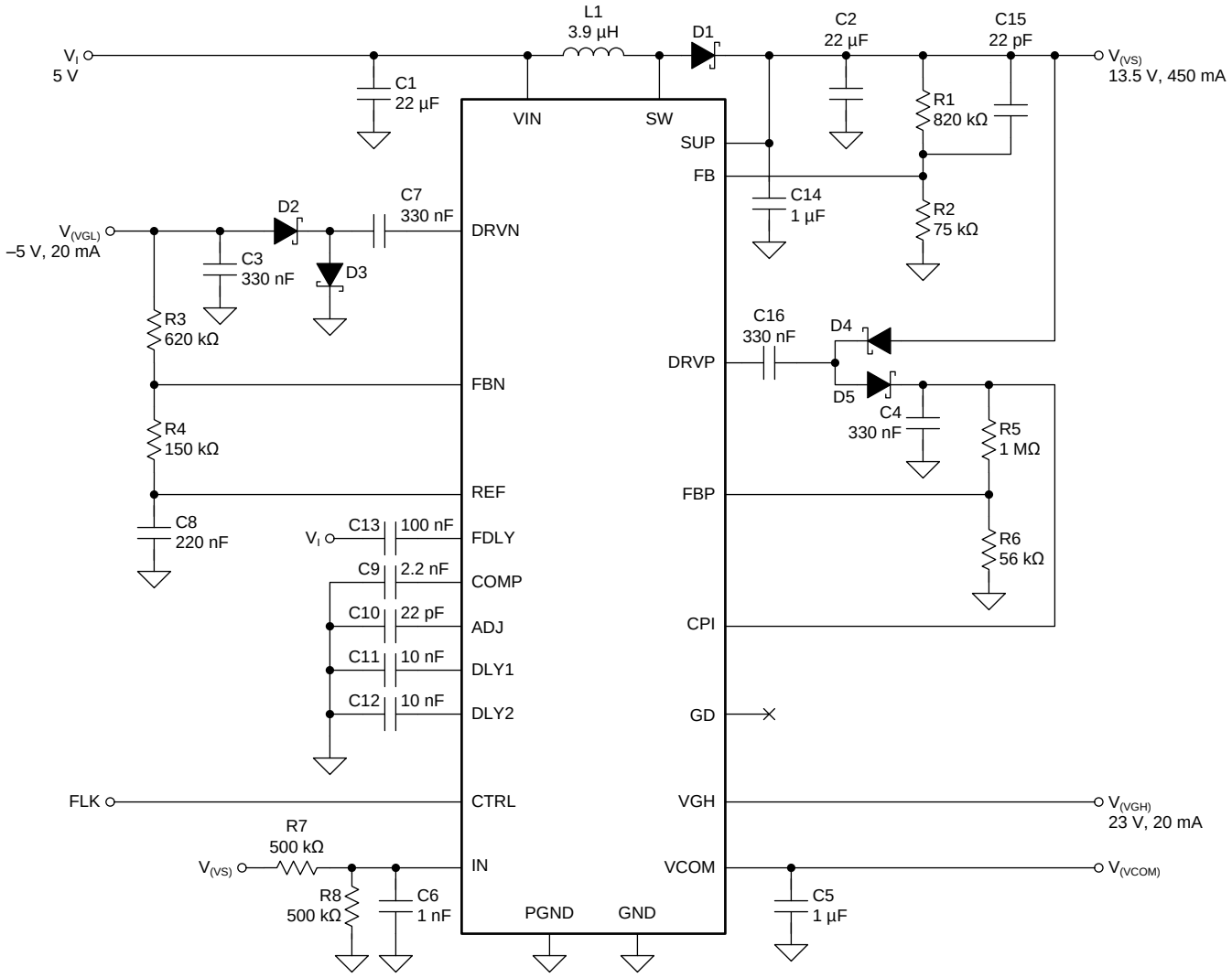

Figure 35. Monitor LCD Supply Powered from a 5-V Rail

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System Examples (continued)

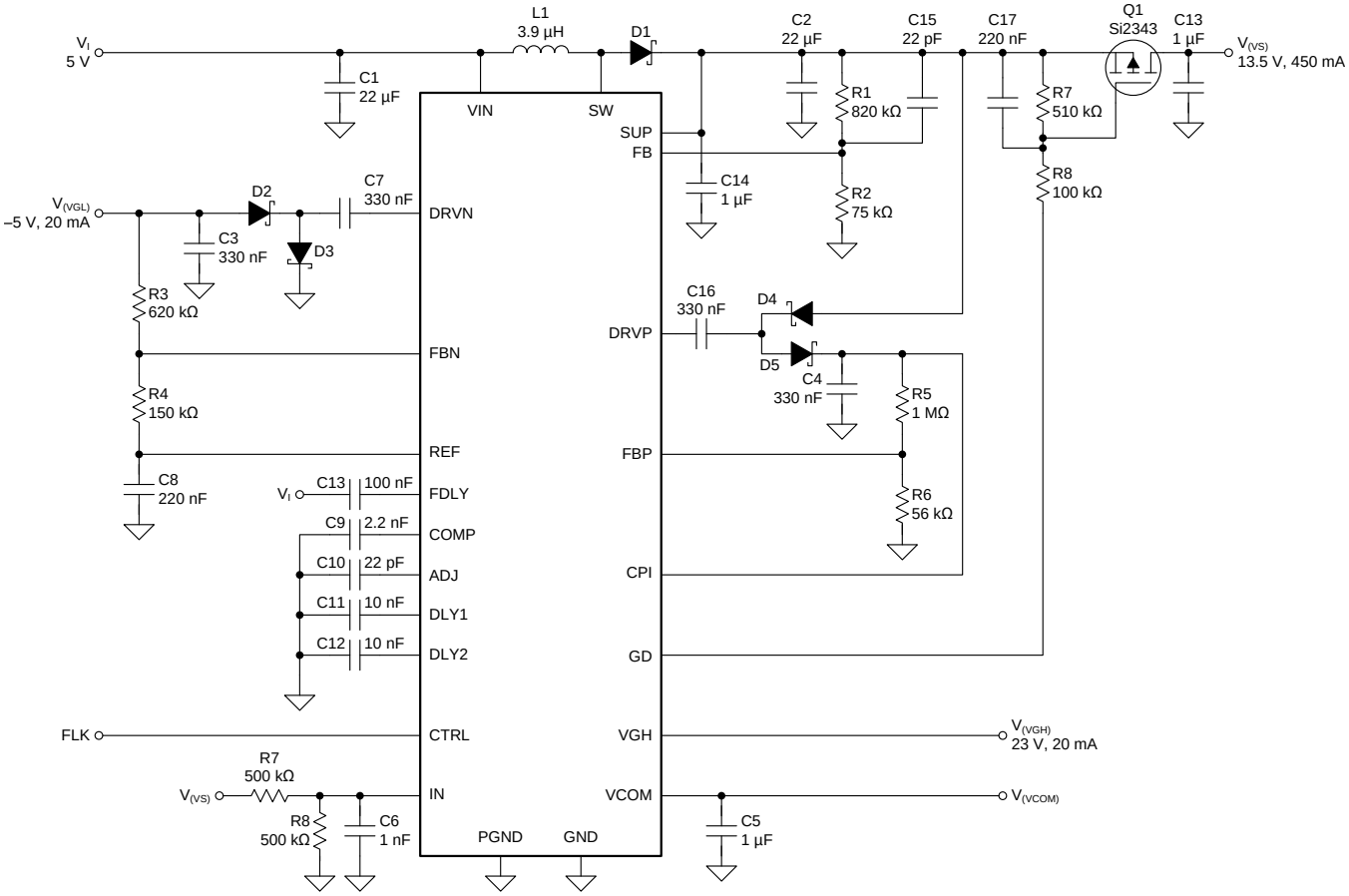

Figure 36. Typical Isolation and Short Circuit Protection Switch for $V_{(VS)}$ Using Q1 and Gate Drive Signal (GD)

9 Power Supply Recommendations

The TPS65150 device is designed to operate with input supplies from 1.8 V to 6 V. Like most integrated circuits, the input supply should be stable and free of noise if the device's full performance is to be achieved. If the input is located more than a few centimeters away from the device, additional bulk capacitance may be required. The input capacitance shown in the application schematics in this data sheet is sufficient for typical applications.

10 Layout

10.1 Layout Guidelines

The PCB layout is an important step in the power supply design. An incorrect layout could cause converter instability, load regulation problems, noise, and EMI issues. Especially with a switching DC-DC converter at high load currents, too-thin PCB traces can cause significant voltage spikes. Good grounding is also important. If possible, TI recommends using a common ground plane to minimize ground shifts between analog ground (GND) and power ground (PGND). Additionally, the following PCB design layout guidelines are recommended for the TPS65150 device:

1. Boost converter output capacitor, input capacitor and Power ground (PGND) should form a star ground or should be directly connected together on a common power ground plane.
2. Place the input capacitor directly from the input pin (VIN) to ground.
3. Use a bold PCB trace to connect SUP to the output Vs.
4. Place a small bypass capacitor from the SUP pin to ground.
5. Use short traces for the charge-pump drive pins (DRVN, DRVP) of VGH and VGL because these traces carry switching currents.
6. Place the charge pump flying capacitors as close as possible to the DRVP and DRVN pin, avoiding a high voltage spikes at these pins.
7. Place the Schottky diodes as close as possible to the device and to the flying capacitors connected to DRVP and DRVN.
8. Carefully route the charge pump traces to avoid interference with other circuits because they carry high voltage switching currents .
9. Place the output capacitor of the VCOM buffer as close as possible to the output pin (VCOM).
10. The thermal pad must be soldered to the PCB for correct thermal performance.

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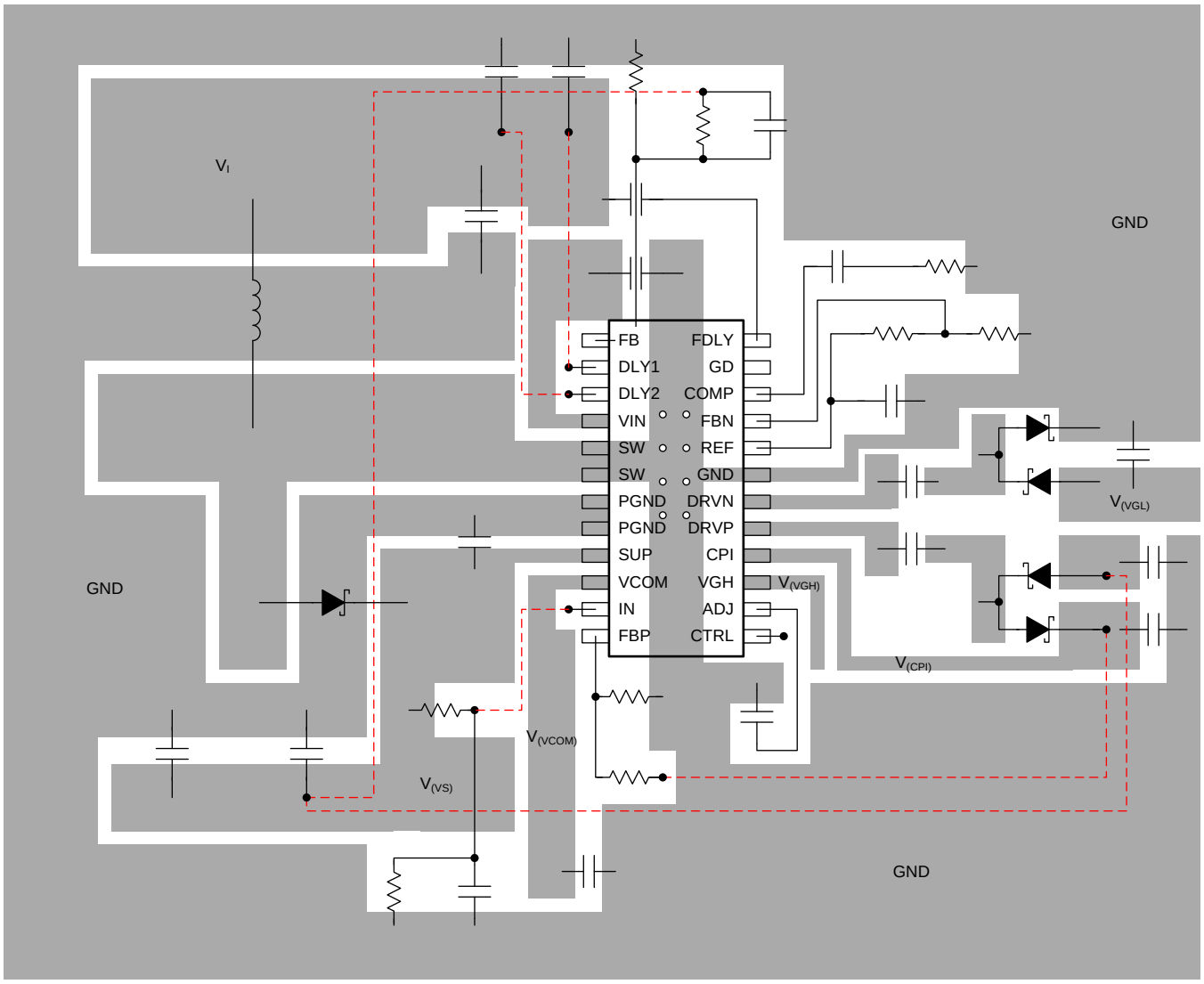
10.2 Layout Example



● Via to inner / bottom signal layer
○ Thermal via to copper pour on inner / bottom signal layer

Figure 37. PCB Layout Example

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS65150PWP	ACTIVE	HTSSOP	PWP	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS65150	Samples
TPS65150PWPG4	ACTIVE	HTSSOP	PWP	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS65150	Samples
TPS65150PWPR	ACTIVE	HTSSOP	PWP	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS65150	Samples
TPS65150PWPRG4	ACTIVE	HTSSOP	PWP	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS65150	Samples
TPS65150RGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 65150	Samples
TPS65150RGERG4	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 65150	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS65150 :

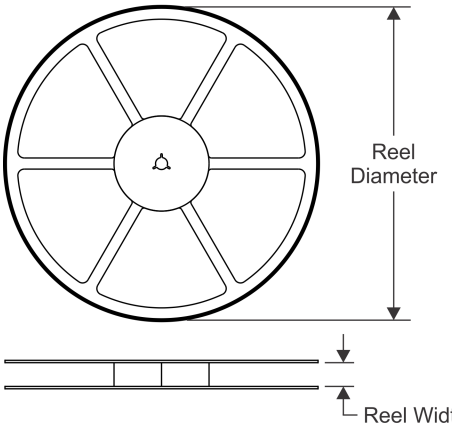
- Automotive: TPS65150-Q1

NOTE: Qualified Version Definitions:

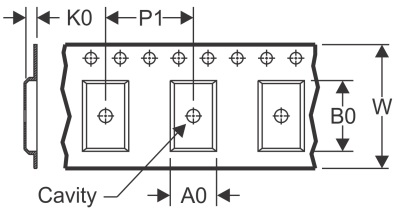
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

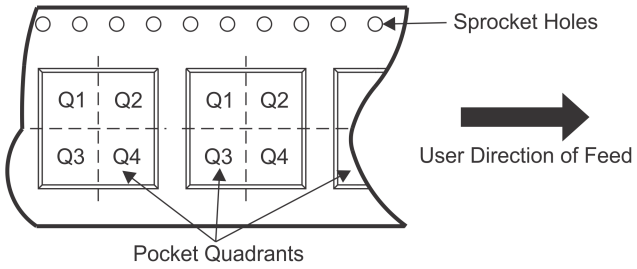


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

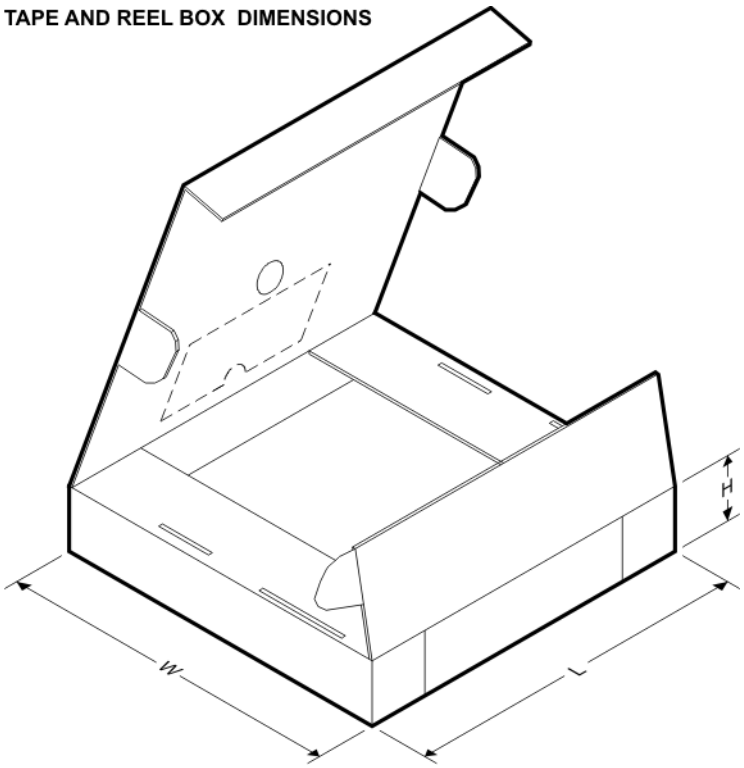
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65150PWPR	HTSSOP	PWP	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
TPS65150RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS65150RGER	VQFN	RGE	24	3000	330.0	12.4	4.35	4.35	1.1	8.0	12.0	Q2

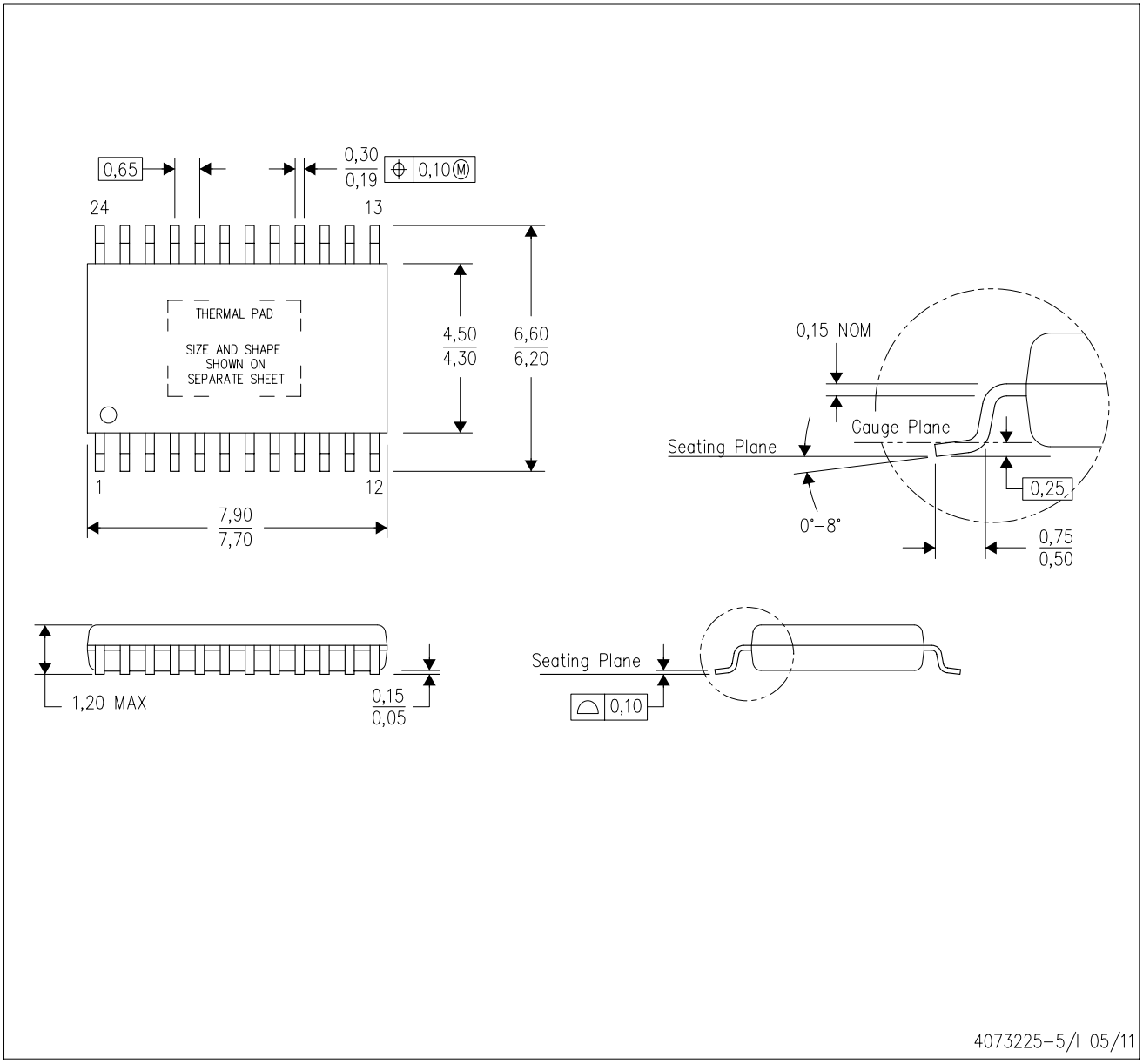
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65150PWPR	HTSSOP	PWP	24	2000	367.0	367.0	38.0
TPS65150RGER	VQFN	RGE	24	3000	367.0	367.0	35.0
TPS65150RGER	VQFN	RGE	24	3000	338.0	355.0	50.0

PWP (R–PDSO–G24) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

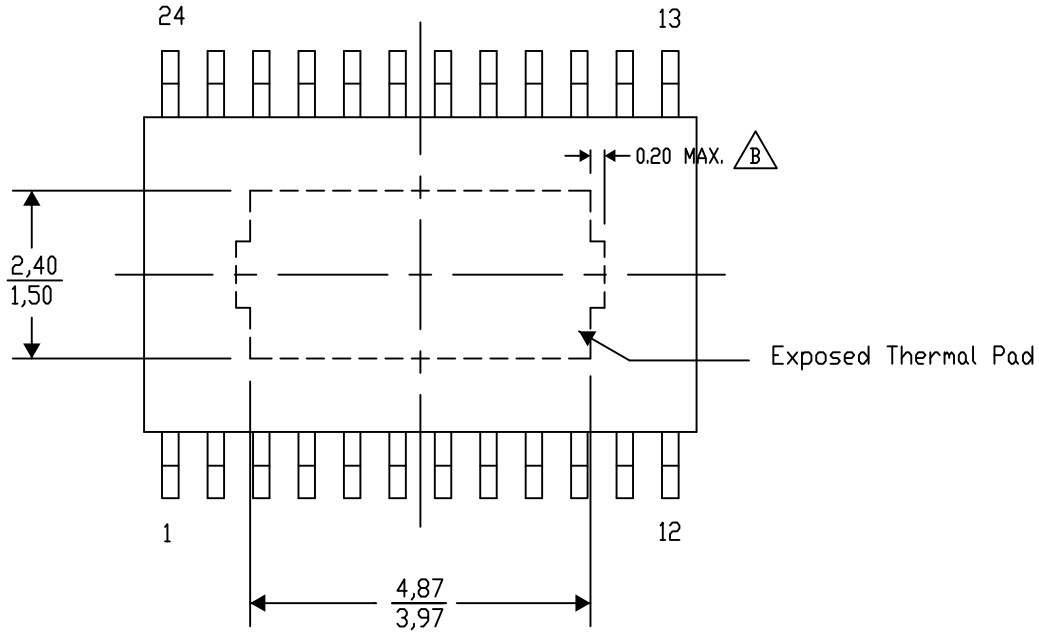
PWP (R–PDSO–G24) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

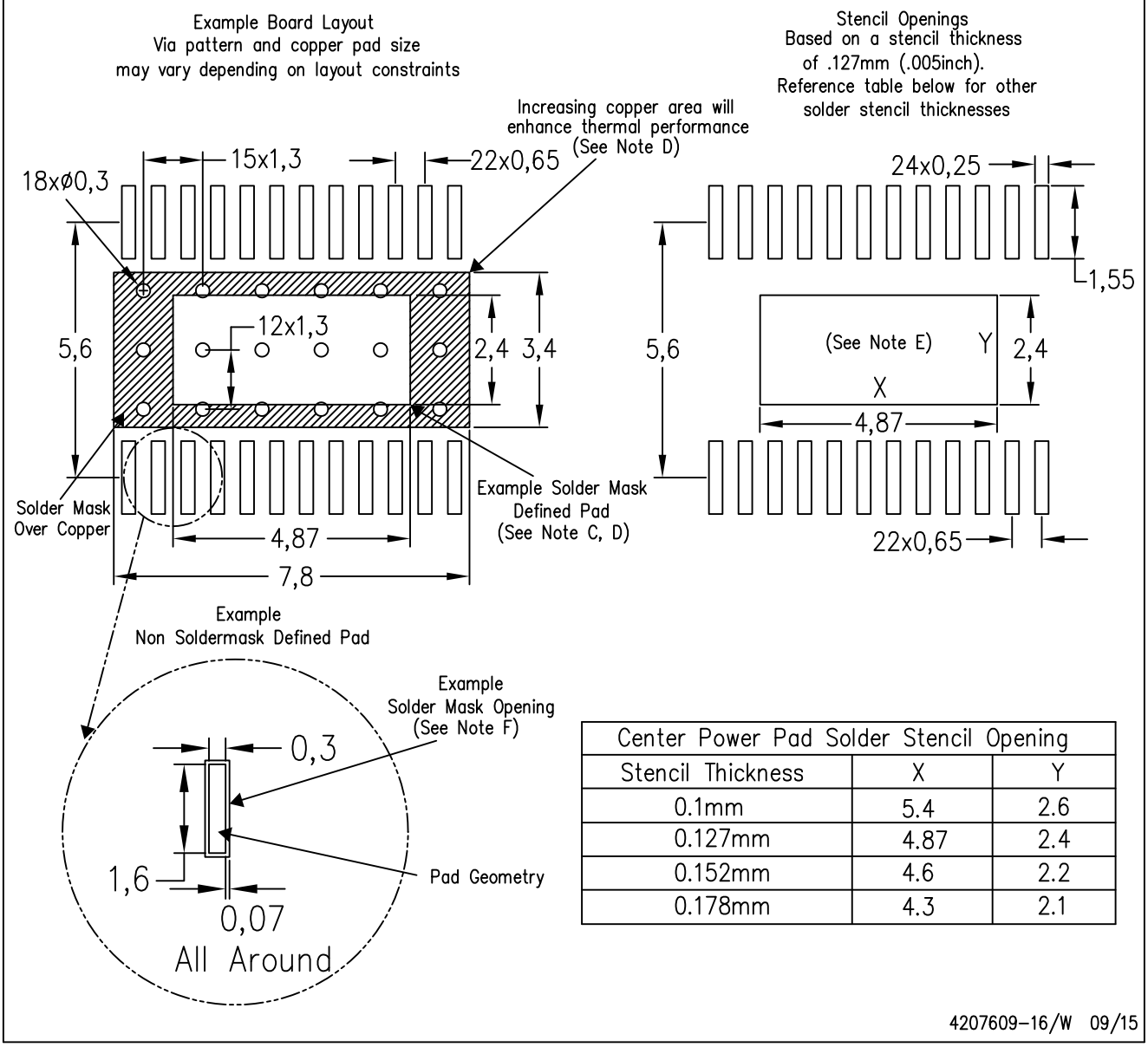
4206332–29/AN 10/15

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R–PDSO–G24) PowerPAD™ PLASTIC SMALL OUTLINE

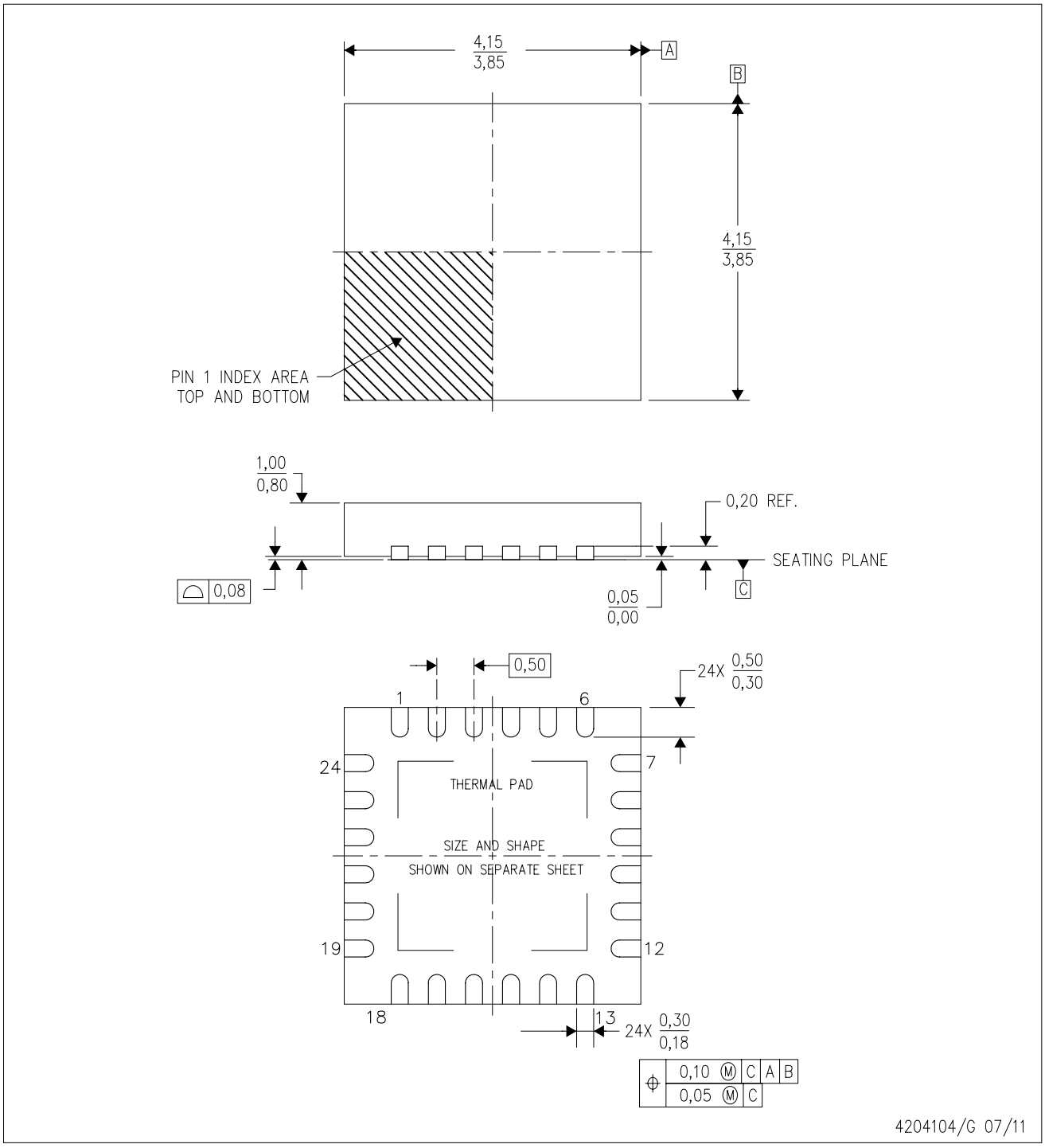


Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	5.4	2.6
0.127mm	4.87	2.4
0.152mm	4.6	2.2
0.178mm	4.3	2.1

4207609–16/W 09/15

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

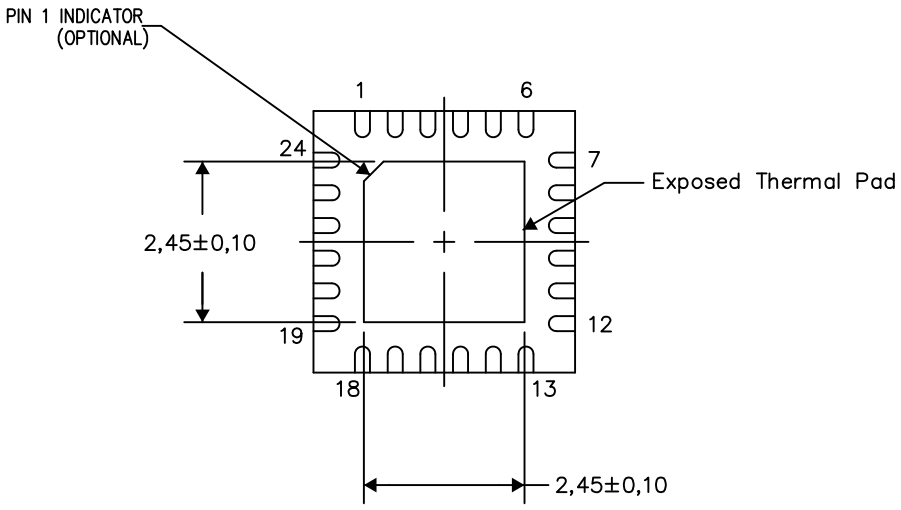
RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



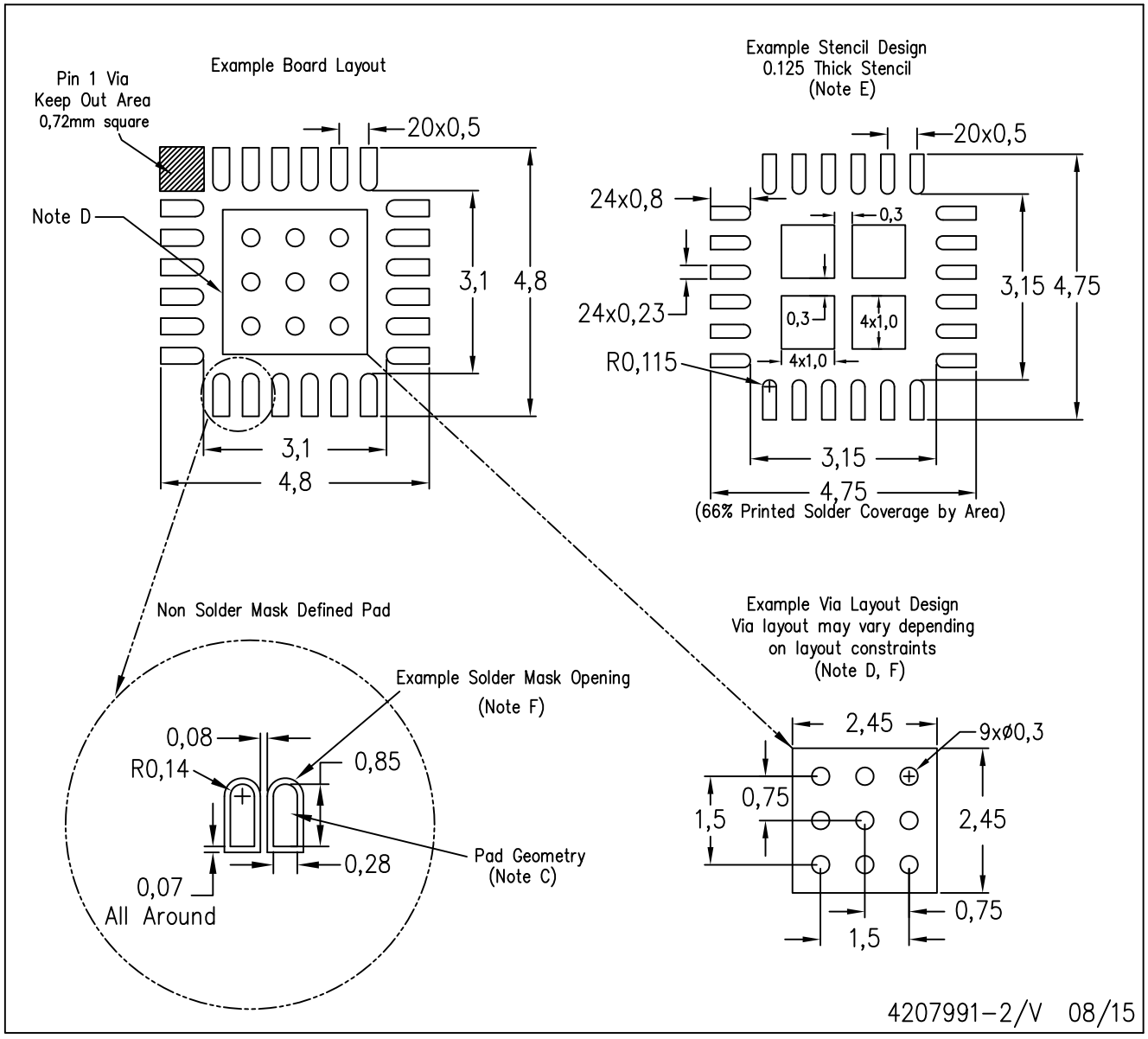
Bottom View

Exposed Thermal Pad Dimensions

4206344–3/AK 08/15

NOTES: A. All linear dimensions are in millimeters

RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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