# LOW-POWER BATTERY BACKUP IC WITH INTEGRATED BOOST CONVERTER

## FEATURES

- **Power-Path Switch to Select Main Battery or Backup Battery for Real-Time Clock (RTC)**
- **Integrated Boost DC/DC Converter**
  - **Modulation Select by Control Pin (PWMON), Pulse Frequency Modulation (PFM) or Pulse Width Modulation (PWM)**
  - **Fixed Switching Frequency (PWM, 750 kHz)**
  - **Peak Current Mode Control (PWM)**
  - **Low Power Consumption (PFM)**
- **Four Integrated Low Dropout (LDO) Voltage Regulators for 1.2 V/1.8 V/3.3 V**
- **Two Integrated Indicators**
  - **CS: Monitors the Voltage Level of Main Battery (VBAT) and Output voltage level of Boost Converter (VO_BT)**
  - **XRESET: Monitors the Output voltage Level of 3.3V LDO (VOUT)**
- **16-Pin QFN (3mm × 3mm) Package**
- **Operating Temperature –35°C to 85°C**
- **Protection**
  - **Overcurrent Protection (OCP)**
  - **Overvoltage Protection (OVP)**
  - **Thermal Shutdown (TSD)**
  - **Undervoltage Lockout (UVLO)**

## APPLICATIONS

- **Digital Still Cameras**
- **Portable Systems With Backup Battery**

## DESCRIPTION

The TPS65510 offers a suitable solution for power switch to select the main battery or the backup battery.

This device automatically selects the power path. It depends on the voltage level of the VO_BT pin. When the main battery is removed, the power path of the VOUT pin is automatically changed from the output of 3.3-V low droppout (LDO) voltage regulator to the backup battery.

The backup battery is charged from the power path of the VRO pin (output of 3.3-V LDO) via an external diode and resistor. The input of the LDO voltage regulator comes from the internal boost converter.

The 1.2-V output LDO and 1.8-V output LDO voltage regulators have a enable pin, V_CTRL. If these outputs are not necessary, V_CTRL should be connected to AGND to save power consumption. The self-power consumption is less than 3 μA (maximum) using the backup battery.

This device has two indicators. One is CS, which monitors the voltage level of the VBAT pin and VO_BT pin. The other is XRESET, which monitors voltage level of the VOUT pin. These indicators should be connected to CPU/DSP to reset them.

This device reduces the total solution area and extends the lifetime of the backup battery.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## APPLICATION CIRCUIT

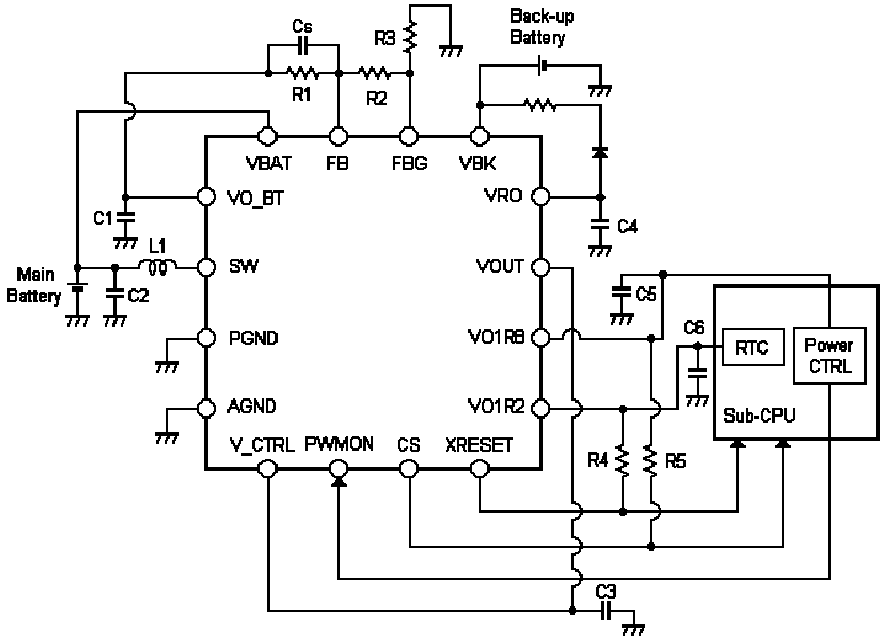



**Figure 1. Typical Application Circuit (1.2-V/1.8-V Output)**

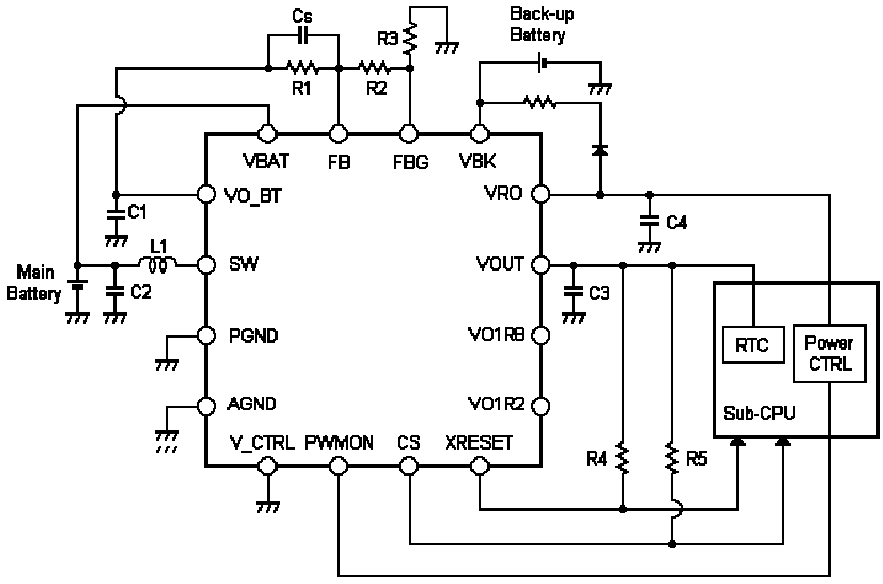



**Figure 2. Typical Application Circuit (3.3-V Output)**

## ORDERING INFORMATION

| $T_A$ | PACKAGE MARKING | PACKAGE | PART NUMBER |
|---|---|---|---|
| –35°C to 85°C | CGK | 16-pin QFN | TPS65510RGT |

## ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| VBAT, VBK | Input voltage range | –0.3 | 6 | V |
| SW | | –0.3 | 7 | |
| FB, FBG | | –0.3 | 6 | |
| PWMON, V_CTRL | | –0.3 | 6 | |
| XRESET, CS | Output voltage range | –0.3 | 6 | V |
| VRO, VOUT, VO1R8, VO1R2 | | –0.3 | 3.6 | |
| VO_BT | | –0.3 | 6 | V |
| SW | Switch current | | 1.3 | A |
| | Maximum junction temperature range | | 125 | °C |
| | Storage temperature range | –40 | 150 | °C |

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## DISSIPATION RATINGS

| PACKAGE | $R_{\theta JA}$(1) | POWER RATING $T_A$ < 25°C | POWER RATING $T_A$ = 85°C |
|---|---|---|---|
| QFN | 47.4°C/W | 2.11 W | 0.844 W |

(1) The thermal resistance, $R_{\theta JA}$, is based on a soldered PowerPAD™ on 2S2P JEDEC board using thermal vias.

## RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

| | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| VBAT | Supply voltage | 2.65 | | 5.5 | V |
| VBK | | 1.8 | | 5.5 | |
| VIH | High-level digital input voltage at PWMON | 1.4 | | 5.5 | V |
| | High-level digital input voltage at V_CTRL | 1.4 | | VOUT | |
| VIL | Low-level digital input voltage at PWMON | | | 0.4 | V |
| | Low-level digital input voltage at V_CTRL | | | 0.4 | |
| | Operating free-air temperature range | –35 | | 85 | °C |

## ELECTRICAL CHARACTERISTICS

$T_A$ = 25°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{CC1}$ | Consumption current at VO_BT | $V_{(VO\_BT)}$: 3.6 V, VOUT: No load<br>$V_{(PWMON)}$: AGND (PFM mode) | | 60 | 100 | µA |
| $I_{CC2}$ | Consumption current at VO_BT | $V_{(VO\_BT)}$: 5 V, VOUT: No load<br>$V_{(PWMON)}$: VOUT (PWM mode) | | 250 | 350 | µA |
| $I_{CC3}$ | Consumption current at VBK | $V_{(VO\_BT)}$ : 3.6 V, $V_{(VBK)}$: 3 V<br>VOUT: No load | | 0.1 | 1 | µA |
| $I_{CC4}$ | Consumption current at VBK | VO_BT: Open, $V_{(VBK)}$: 3 V<br>VOUT: No load, $V_{(V\_CTRL)}$: VOUT | | 2.5 | 5 | µA |
| $I_{CC5}$ | Consumption current at VBK | VO_BT: Open, $V_{(VBK)}$: 3 V<br>VOUT: No load, $V_{(V\_CTRL)}$: AGND | | 1.2 | 3 | µA |
| $I_{CC6}$ | Consumption current at VBAT | $V_{(VBAT)}$: 3.6 V, $V_{(VO\_BT)}$: 3.5 V | | 5 | 10 | µA |
| $I_{(SINK\_CS)}$ | Sink current at CS | $V_{(CS)}$: 0.5 V, CS pin: Low-Z | 1 | 1.5 | | mA |
| $I_{(LEAK\_CS)}$ | Leakage current at CS | $V_{(CS)}$: 5.5 V, CS pin: Hi-Z | | | 1 | µA |
| $I_{(SINK\_XRESET)}$ | Sink current at XRESET | $V_{(XRESET)}$: 0.5 V, XRESET pin: Low-Z | 1 | 1.5 | | mA |
| $I_{(LEAK\_XRESET)}$ | Leak current at XRESET | $V_{(XRESET)}$: 5.5 V, XRESET pin: Hi-Z | | | 1 | µA |
| $I_{(LEAK\_VBK)}$ | Leak current at VBK | $V_{(VO\_BT)}$: 5.5 V, $V_{(VBK)}$: 0 V | | | 1 | µA |
| $V_{(UVLO\_DET)}$ | UVLO/CS detection level at VBAT | $V_{(VBAT)}$: from 0 V to 5.5 V | 2.50 | 2.70 | 2.90 | V |
| $V_{(UVLO\_HYS)}$ | UVLO/CS hysteresis at VBAT | $V_{(VBAT)}$: from 5.5 V to 0 V | –250 | –200 | –150 | mV |
| $V_{(CS\_DET)}$ | CS detection level at VO_BT | $V_{(VO\_BT)}$: from 5 V to 0 V | 3.071 | 3.150 | 3.229 | V |
| $V_{(CS\_HYS)}$ | CS hysteresis at VO_BT | $V_{(VO\_BT)}$: from 0 V to 5 V | 50 | 100 | 150 | mV |
| $V_{(XRESET\_DET)}$ | XRESET detection level | $V_{(VOUT)}$: from 3.3 V to 0 V | 2.048 | 2.100 | 2.153 | V |
| $V_{(XRESET\_HYS)}$ | XRESET hysteresis | $V_{(VOUT)}$: from 0 V to 3.3 V | 50 | 100 | 150 | mV |
| $V_{(SW1)}$ | Change the power path for VOUT | Monitoring at VO_BT | 2.94 | 3.00 | 3.06 | V |
| $V_{(SW2)}$ | CS output disable level | Monitoring at VOUT | 3.072 | 3.135 | 3.198 | V |
| $V_{(WAKE\_DET)}$ | Threshold of WAKE mode | $V_{(VO\_BT)}$: from 0 V to 3.6 V | 2.38 | 2.50 | 2.63 | V |
| $V_{(WAKE\_HYS)}$ | WAKE mode hysteresis | $V_{(VO\_BT)}$: from 3.6 V to 0 V | –150 | –100 | –50 | mV |
| $R_{(ON\_VBK)}$ | On resistance between VBK and VOUT | VO_BT: Open, $V_{(VBK)}$: 3 V,<br>$I_{(VOUT)}$: 2 mA | | 30 | 60 | Ω |
| TSD(1) | Thermal shutdown detection temperature | | | 150 | | °C |

(1) Specified by design. Not production tested.

## ELECTRICAL CHARACTERISTICS (continued)

$T_A$ = 25°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **Boost DC/DC Converter** | | | | | | |
| $V_{(FB)}$ | Reference voltage | $V_{(PWMON)}$: AGND (PFM mode) | 1.213 | 1.250 | 1.288 | V |
| | | $V_{(PWMON)}$: VOUT (PWM mode) | 1.225 | 1.250 | 1.275 | |
| | Overvoltage protection threshold | Monitoring at FB | 1.30 | 1.35 | 1.40 | V |
| | Overcurrent protection threshold | $V_{(PWMON)}$: AGND (PFM mode) | 0.48 | 0.60 | 0.72 | A |
| | | $V_{(PWMON)}$: VOUT (PWM mode) | 0.8 | 1.0 | 1.2 | |
| OSC | Internal OSC frequency | $V_{(PWMON)}$: VOUT (PWM mode) | 675 | 750 | 825 | kHz |
| $R_{(ON\_P)}$ | P-ch FET ON resistance | $V_{(VO\_BT)}$: 5 V | | 500 | 700 | mΩ |
| $R_{(ON\_N)}$ | N-ch FET ON resistance | $V_{(VO\_BT)}$: 5 V | | 200 | 250 | mΩ |
| $R_{(ON\_FBG)}$ | FBG ON resistance | $V_{(PWMON)}$: VOUT (PWM mode) | | 1 | 1.5 | kΩ |
| $I_{(LEAK\_FBG)}$ | Leakage current at FBG | $V_{(PWMON)}$: AGND (PFM mode) | | | 1 | µA |
| **3.3-V Output LDO (VOUT)** | | | | | | |
| $V_{(VOUT)}$ | Output voltage of VOUT | $V_{(VO\_BT)}$: 5 V, $I_{(VOUT)}$: 1 mA | 3.234 | 3.300 | 3.366 | V |
| $I_{(VOUT)}$ | Output current of VOUT | $V_{(VO\_BT)}$: 5 V, $V_{(VOUT)}$ ≥ 3.156 V | | | 30 | mA |
| | Overcurrent protection threshold | | | 50 | | mA |
| **3.3-V Output LDO (VRO)** | | | | | | |
| $V_{(VRO)}$ | Output voltage of VRO | $V_{(VO\_BT)}$: 5 V, $I_{(VRO)}$: 1 mA | 3.234 | 3.300 | 3.366 | V |
| $I_{(VRO)}$ | Output current of VRO | $V_{(VO\_BT)}$: 5 V, $V_{(VRO)}$ ≥ 3.156 V | | 10 | 30 | mA |
| | Overcurrent protection threshold | | | 50 | | mA |
| **1.8-V Output LDO (VO1R8)** | | | | | | |
| $V_{(VO1R8)}$ | Output voltage of VO1R8 | $V_{(V\_CTRL)}$: VOUT, $V_{(VO\_BT)}$: 5 V, $I_{(VO1R8)}$: 100 µA | 1.71 | 1.80 | 1.89 | V |
| $I_{(VO1R8)}$ | Output current of VO1R8 | $V_{(V\_CTRL)}$: VOUT | | | 100 | µA |
| **1.2-V Output LDO (VO1R2)** | | | | | | |
| $V_{(VO1R2)}$ | Output voltage of VO1R2 | $V_{(V\_CTRL)}$: VOUT, $V_{(VO\_BT)}$: 5 V, $I_{(VO1R2)}$: 100 µA | 1.1 | 1.2 | 1.3 | V |
| $I_{(VO1R2)}$ | Output current of VO1R2 | $V_{(V\_CTRL)}$: VOUT | | | 100 | µA |

## SWITCHING CHARACTERISTICS

$T_A$ = 25°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $T_{CS}$ (1) | Detection delay at CS | $V_{(VO\_BT)}$: from 3.6 V to 2.0 V | | 55 | | µs |
| $T_{XRESET}$ (1) | Detection delay at XRESET | $V_{(VOUT)}$: from 1.5 V to 3.0 V | | 25 | | µs |

(1) Specified by design. Not production tested.

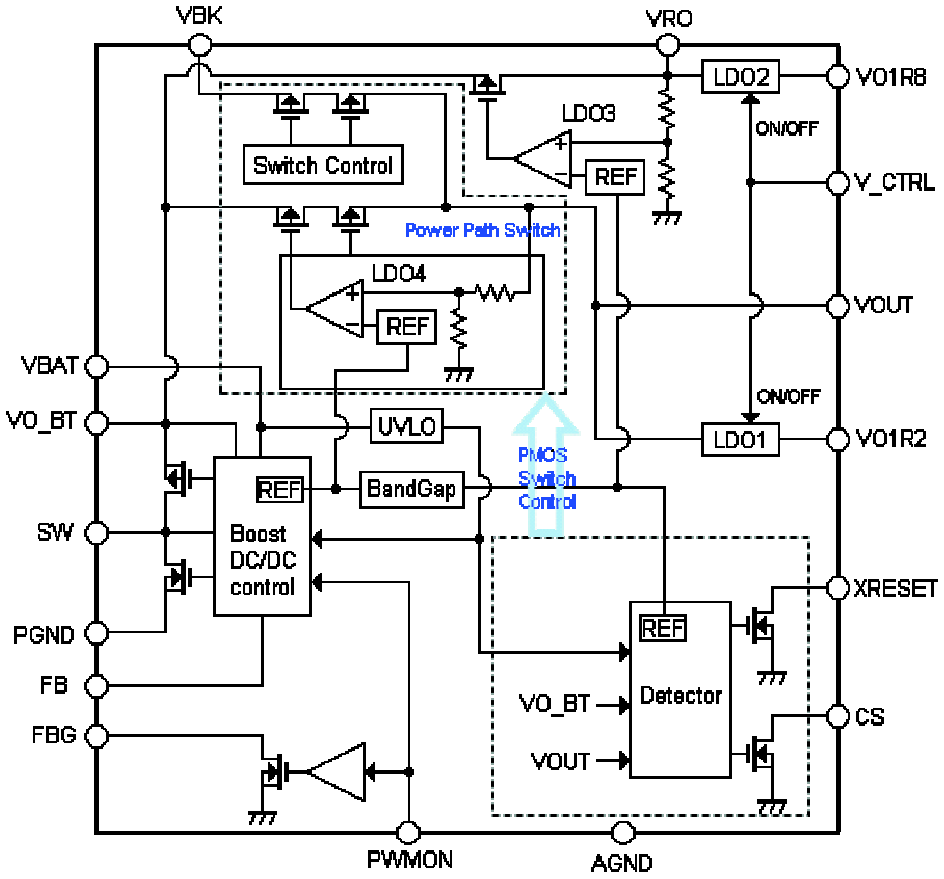
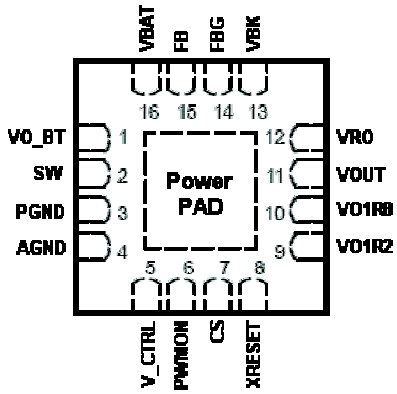



**Figure 3. Block Diagram**

## PIN ASSIGNMENTS

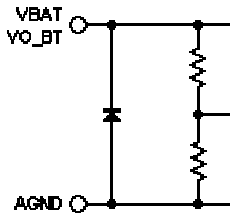
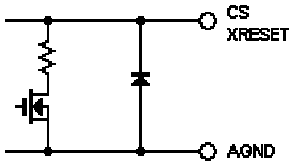
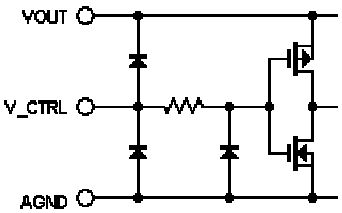
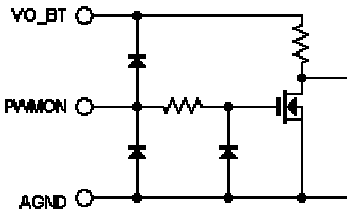
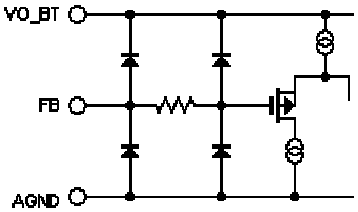
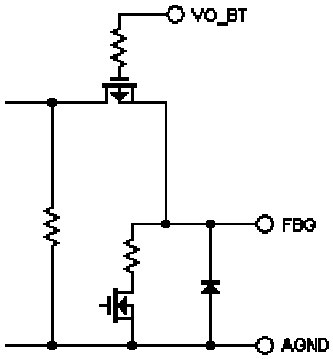
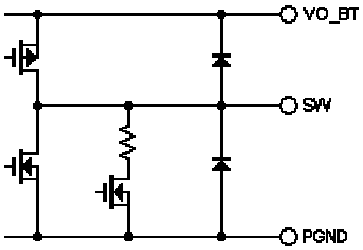
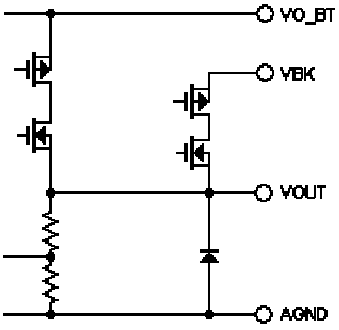



### TERMINAL FUNCTIONS

| TERMINAL | | I/O(1) | DESCRIPTION |
|---|---|---|---|
| NO. | NAME | | |
| 1 | VO_BT | O | Boost converter output. This voltage is defined by the ration of external resistors. Please see the description in detail. |
| 2 | SW | I | Switching terminal for boost converter. This terminal should be connected to the external inductor. |
| 3 | PGND | G | Power ground. Connect to the ground plane. |
| 4 | AGND | G | Analog ground. Connect to the ground lane. |
| 5 | V_CTRL | I | LDO Enable/Disable input. When the input level is Low, it disables the operation of LDOs regarding VO1R8 and VO1R2. When the input level is high, it enables the operation of LDOs regarding VO1R8 and VO1R2. |
| 6 | PWMON | I | Modulation select pin. When the input level is low, the boost converter operates as PFM mode. When the input level is high, the boost converter operates as PWM mode. |
| 7 | CS | O | Indicator which monitors VBAT pin and VO_BT pin. CS is an open-drain output that goes low when the voltage level of VO_BT pin or VBAT pin is lower than the threshold. The threshold is specified with the Electrical Characteristics. |
| 8 | XRESET | O | Indicator that monitors VOUT; the output of 3.3-V LDO or backup battery. XRESET is an open-drain output that goes low when the voltage level of VOUT is lower than the threshold. The threshold is specified with the Electrical Characteristics. |
| 9 | VO1R2 | O | 1.2-V output regulated by LDO. The voltage level sets 1.2 V internally. |
| 10 | VO1R8 | O | 1.8-V output regulated by LDO. The voltage level sets 1.8 V internally. |
| 11 | VOUT | O | 3.3-V output regulated by LDO or the voltage from backup battery. This output is selected by internal power switch. The selection depends on the output voltage of boost converter. |
| 12 | VRO | O | 3.3-V output regulated by LDO. The voltage level sets 3.3 V internally. |
| 13 | VBK | I | Backup battery input. The recommended input voltage at VBK is from 1.8V to 5.5V. |
| 14 | FBG | I | Boost converter output adjustable pin. When the level of PWMON pin is low, the impedance of FBG is high impedance. When the level of PWMON pin is high, the impedance of FBG is almost GND level. |
| 15 | FB | I | Feedback voltage from boost converter output. |
| 16 | VBAT | I | Power supply from main battery. The recommended input voltage at VBAT is from 2.65V to 5.5V. |

(1) I： Input pin, O： Output pin, P： Power supply pin, G： GND pin

## I/O Equivalent Circuits

| VBAT/VO_BT | CS/XRESET |
|---|---|
|  |  |
| **V_CTRL** | **PWMON** |
|  |  |
| **FB** | **FBG** |
|  |  |
| **SW** | **VOUT** |
|  |  |

**I/O Equivalent Circuits (continued)**

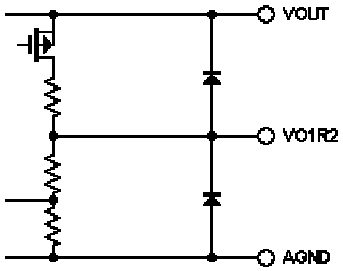
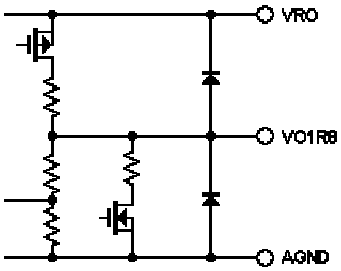
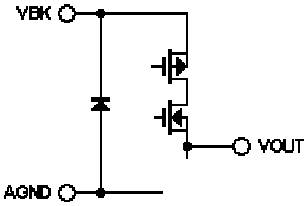
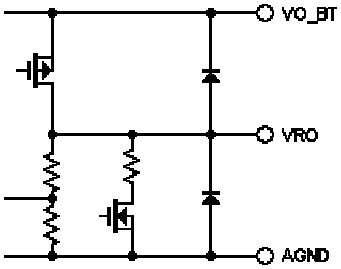
| VO1R2 | VO1R8 |
|---|---|
|  |  |
| **VBK** | **VRO** |
|  |  |

**Figure 4. I/O Equivalent Circuits**

# FUNCTIONAL DESCRIPTION

## Power-Path Switch

The TPS65510 has the switch to select a power path of VOUT pin from main battery or backup battery. These switches consist of P-ch MOSFET. Also, these switches avoid the reverse current from output side to battery side.

When the voltage of VO_BT pin (output of boost converter) is higher than the threshold specified by $V_{(SW1)}$ in Electrical Characteristics, the power path of VOUT comes from main battery via internal boost converter. The voltage of VOUT pin sets 3.3 V with internal LDO.

When a voltage of VO_BT pin is lower than the threshold specified by $V_{(SW1)}$ in Electrical Characteristics, the power path of VOUT comes from backup battery at VBK pin. Before the voltage of VO_BT pin reaches $V_{(SW1)}$, the switch to select a power path cannot change the power path route.

The voltage coming from backup battery is not regulated internally. When the voltage of VOUT is lower than the threshold specified by $V_{(XRESET\_DET)}$ and $V_{(XRESET\_HYS)}$ in Electrical Characteristics, the voltage of XRESET pin goes low (see the description of STATUS INDICATORS).

At the start of boost converter operation, the power path is different to avoid the power supply from backup battery. In this situation, the power path of VOUT comes from main battery via internal boost converter even if the output voltage of VO_BT is lower than threshold for CS signal specified by $V_{(sw1)}$ in Electrical Characteristics.

## Boost Converter

The TPS65510 has the boost converter, and the power path comes from the main battery. It has four operation modes, WAKE mode, Pulse Frequency Modulation (PFM) mode, Pulse Width Modulation (PWM) mode and THROUGH mode.

At first, this converter operates as WAKE mode until the voltage of VO_BT pin is less than the threshold specified by $V_{(WAKE\_DET)}$ and $V_{(WAKE\_HYS)}$ in Electrical Characteristics. The switching frequency of WAKE mode is fixed. Only N-ch MOSFET operates during WAKE mode until the voltage of VO_BT pin reaches the threshold specified by $V_{(WAKE\_DET)}$ and $V_{(WAKE\_HYS)}$ in Electrical Characteristics.

After the voltage of VO_BT pin reaching more than the threshold specified by $V_{(WAKE\_DET)}$ and $V_{(WAKE\_HYS)}$ in Electrical Characteristics, the operation mode is shifted from WAKE mode to other modes selected by the level of PWMON pin. When the voltage of PWMON pin is low level, the boost converter operates as PFM mode. When the voltage of PWMON pin is high level, the boost converter operates as PWM mode. When the voltage of main battery is higher than the voltage of VO_BT pin, the converter operates as THROUGH mode to reduce the consumption current at VO_BT pin. At this mode, The TPS65510 forces P-ch MOSFET to be ON and N-ch MOSFET to be OFF. It means that the voltage of VO_BT pin is not regulated.

The boost converter has the reversed current protection to monitor the different voltage between VO_BT pin and SW pin. The protection monitors the difference at both PFM mode and PWM mode. When the voltage of SW pin is larger than that of VO_BT pin, the protection is activated. When the protection is activated, the internal P-ch MOSFET turns OFF. This means that the voltage of SW pin converges the battery voltage naturally.

The output voltage of boost converter depends on the operation mode. When the boost converter operates as PFM mode, the impedance of FBG pin goes Hi-Z and the output voltage is defined by R1, R2 and R3 shown in Figure 1 and Figure 2. When the boost converter operates as PWM mode, the impedance of FBG pin goes almost zero and the output voltage is defined by R1 and R2 shown in Figure 1 and Figure 2. The output voltage is calculated by Equation 1 and Equation 2.

PFM mode:

$$V_{VO\_BT} = \left(1 + \frac{R_1}{R_2 + R_3}\right) \bullet V_{FB} \quad (1)$$

PWM mode:

$$V_{VO\_BT} = \left(1 + \frac{R_1}{R_2}\right) \bullet V_{FB} \quad (2)$$

Where:

$V_{VO\_BT}$: Voltage of VO_BT pin

$V_{FB}$: Voltage of FB pin defined by reference voltage in Electrical Characteristics

## LDO Voltage Regulators

The TPS65510 has four types of LDO voltage regulators; 1.2-V output (LDO1, shown in Figure 3), 1.8-V output (LDO2, shown in Figure 3) and 3.3-V dual output (LDO3 and LDO4, shown in Figure 3). These output voltage are set by internal feedback loop only. The device has enable/disable control pin named V_CTRL for LDO1 and LDO2. When the voltage of V_CTRL is low level, the device disables the output of LDO1 and LDO2. When the voltage of V_CTRL is high level, the device enables the output of LDO1 and LDO2.

The power paths of LDO2, LDO3, and LDO4 are fixed; from output of LDO3 for LDO2 and from output of boost converter for LDO3 and LDO4. The power path of LDO1 is selected by power path switch; when output voltage of the boost converter is higher than the threshold specified by $V_{(SW1)}$ in Electrical Characteristics, the path comes from output of LDO4. When output voltage of the boost converter is lower than the threshold specified by $V_{(SW1)}$ in Electrical Characteristics, the path comes from backup battery connected to VBK pin.

The maximum outputs current are specified by $I_{(VO1R2)}$, $I_{(VO1R8)}$, $I_{(VRO)}$ and $I_{(VOUT)}$ in Electrical Characteristics.

## Status Indicators

The TPS65510 has two device status indicators; CS and XRESET. These signal pins consist of open drain of N-ch MOSFET. Due to this, the pullup resistors should be needed. The recommended values of pullup resistors are 100 kΩ.

CS function monitors the voltage level of VBAT pin and VO_BT pin for selecting power path of VOUT. When the signal level of CS pin is high level, the power path of VOUT comes from the main battery via the boost converter. When the signal level of CS pin is low level, it comes from backup battery except the starting operation of boost converter. When the boost converter starts operation with the main battery, the P-ch MOSFET at LDO4 turns ON to avoid supplying the power from backup battery even if the voltage of VOUT is lower than the threshold specified by $V_{(SW1)}$ in Electrical Characteristics. The signal of the CS pin remains low level when the main battery is removed (including the transition) or the voltage level of VOUT does not achieve the threshold specified by $V_{(SW2)}$ in Electrical Characteristics.

XRESET function monitors the voltage level of VOUT pin for resetting the load like RTC. When the voltage of VOUT is more than the threshold specified by $V_{(XRESET\_DET)}$ and $V_{(XRESET\_HYS)}$ in Electrical Characteristics, the signal level of XRESET pin is high. When the voltage of VOUT is less than the threshold specified by $V_{(XRESET\_DET)}$ and $V_{(XRESET\_HYS)}$ in Electrical Characteristics, the signal level of XRESET pin is low. This situation requires resetting the load. The detailed waveform is shown in Figure 5.

**Summary of Status Indicator and Power-Path Switch**

| | Description | |
|---|---|---|
| CS(1) | Detection | Voltage of VO_BT pin |
| | Detect level | $V_{(CS\_DET)}$ and $V_{(CS\_HYS)}$ in Electrical Characteristics |
| Disable CS signal | Detection | Voltage of VOUT pin |
| | Detect level | $V_{(SW2)}$ in Electrical Characteristics |
| XRESET | Detection | Voltage of VOUT pin |
| | Detect level | $V_{(XRESET\_DET)}$ and $V_{(XRESET\_HYS)}$ in Electrical Characteristics |
| Power SW(2) | Detection of path change | Voltage of VO_BT pin |
| | Detect level | $V_{(SW1)}$ in Electrical Characteristics |

(1) When the voltage of VBAT pin is less than the threshold of UVLO, the output of CS pin forces low level.
(2) The Power path switch changes the path after the voltage of VO_BT is higher than $V_{(CS\_DET)}$. Before that, the power path of VOUT comes from VO_BT pin; not VBK pin.

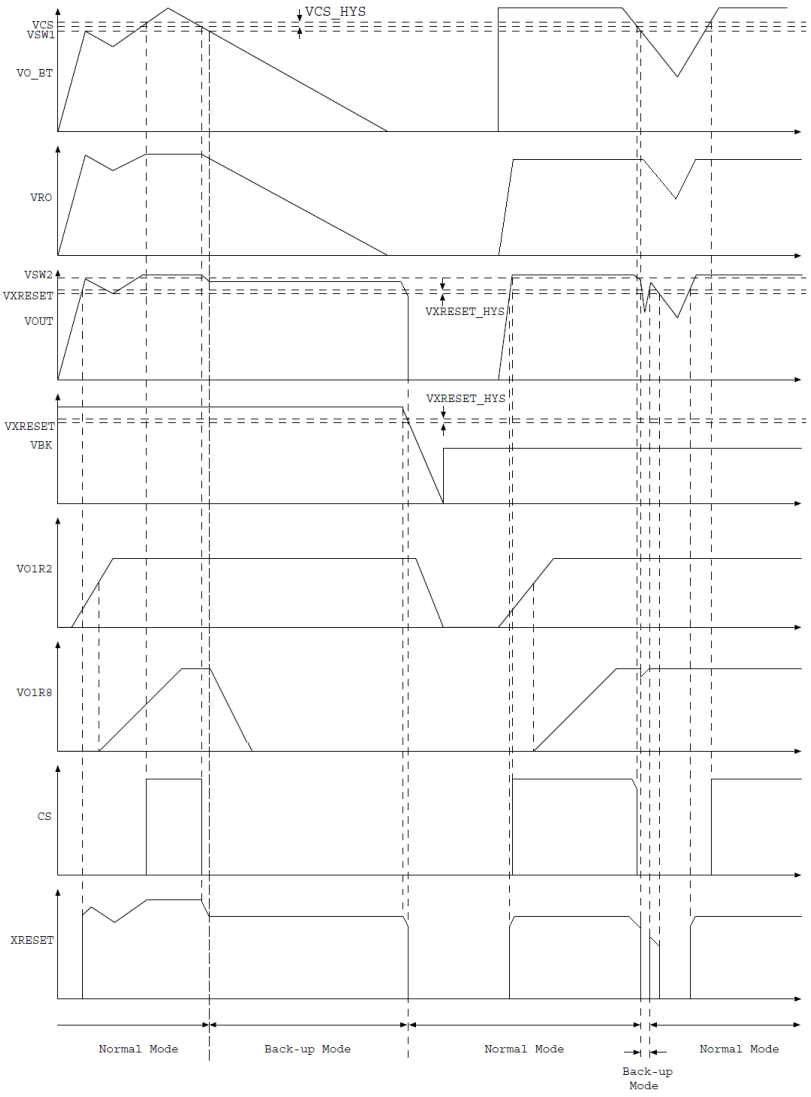



**Figure 5. Power-Path Switch Timing Chart**

## Protection

The TPS65510 has over current protection (OCP), over voltage protection (OVP) Thermal shutdown (TSD) and Under Voltage Lock Out (UVLO). See Table 1.

**Table 1. Conditions of Protections**

| PIN | PROTECTION | | CONDITION |
|---|---|---|---|
| SW | OVP | Detect condition | Voltage of FB pin is greater than the threshold. |
| | | Change mode | Operation disable without latch off |
| | | Recovery condition | Voltage of FB pin is less than the threshold (auto recovery). |
| | OCP | Detect condition | Current of SW pin is greater than the threshold with counting 64 cycles × 750 [kHz] and the output voltage of VO_BT is less than 85% compared with the target voltage. |
| | | Change mode | Operation mode changes from PWM mode to PFM mode. |
| | | Recovery condition | Current of SW pin is less than the threshold and input edge signal from low level to high level at the PWMON pin. |
| VOUT | OCP | Detect condition | Current of VOUT pin is greater than the threshold. |
| | | Change mode | Operation disable without latch off |
| | | Recovery condition | Current of VOUT pin is less than the threshold (auto recovery). |
| VRO | OCP | Detect condition | Current of VRO pin is greater than the threshold. |
| | | Change mode | Operation disable without latch off |
| | | Recovery condition | Current of VRO pin is less than the threshold (auto recovery). |
| - | TSD | Detect condition | Temperature of chip is greater than the threshold. |
| | | Change mode | Operation of boost converter shuts down with latch off. |
| | | Recovery condition | Temperature of chip is lower than the threshold. Connect the main battery after disconnecting the main battery from the system |
| VBAT | UVLO | Detect condition | Voltage of VBAT pin is less than the threshold. |
| | | Change mode | Operation of boost converter shutdown without latch off |
| | | Recovery condition | Connect the main battery after disconnecting the main battery from the system. |

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS65510RGTR | ACTIVE | QFN | RGT | 16 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | CGK | Samples |
| TPS65510RGTT | ACTIVE | QFN | RGT | 16 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | CGK | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

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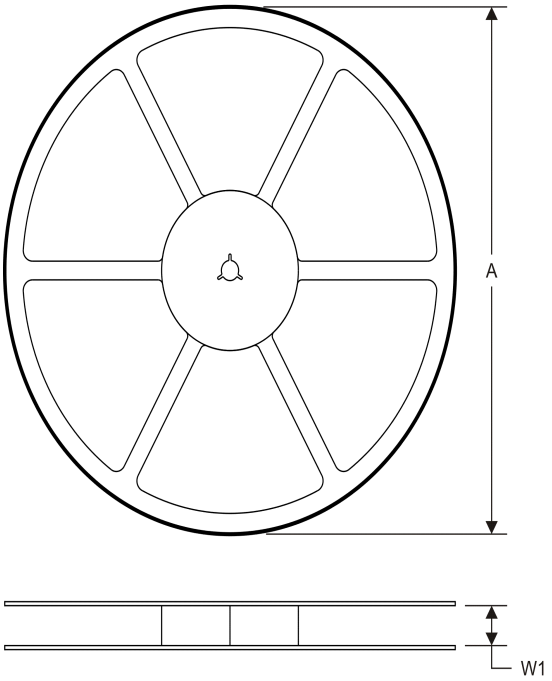
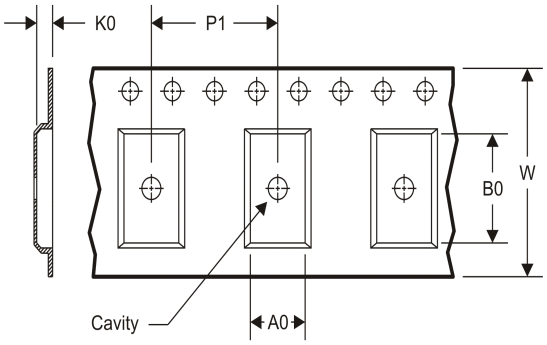



### TAPE DIMENSIONS



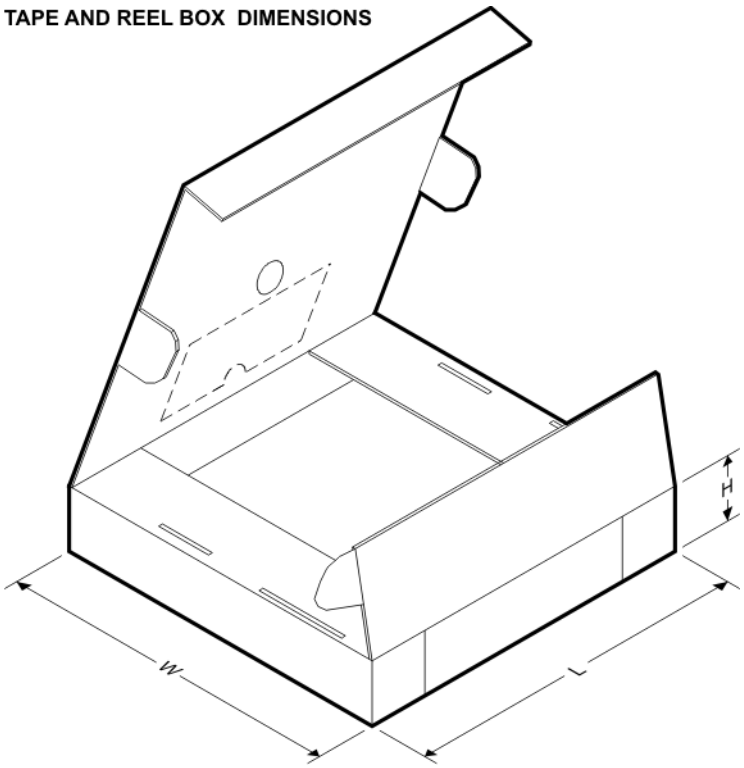

| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

### TAPE AND REEL INFORMATION

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS65510RGTR | QFN | RGT | 16 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| TPS65510RGTT | QFN | RGT | 16 | 250 | 180.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |

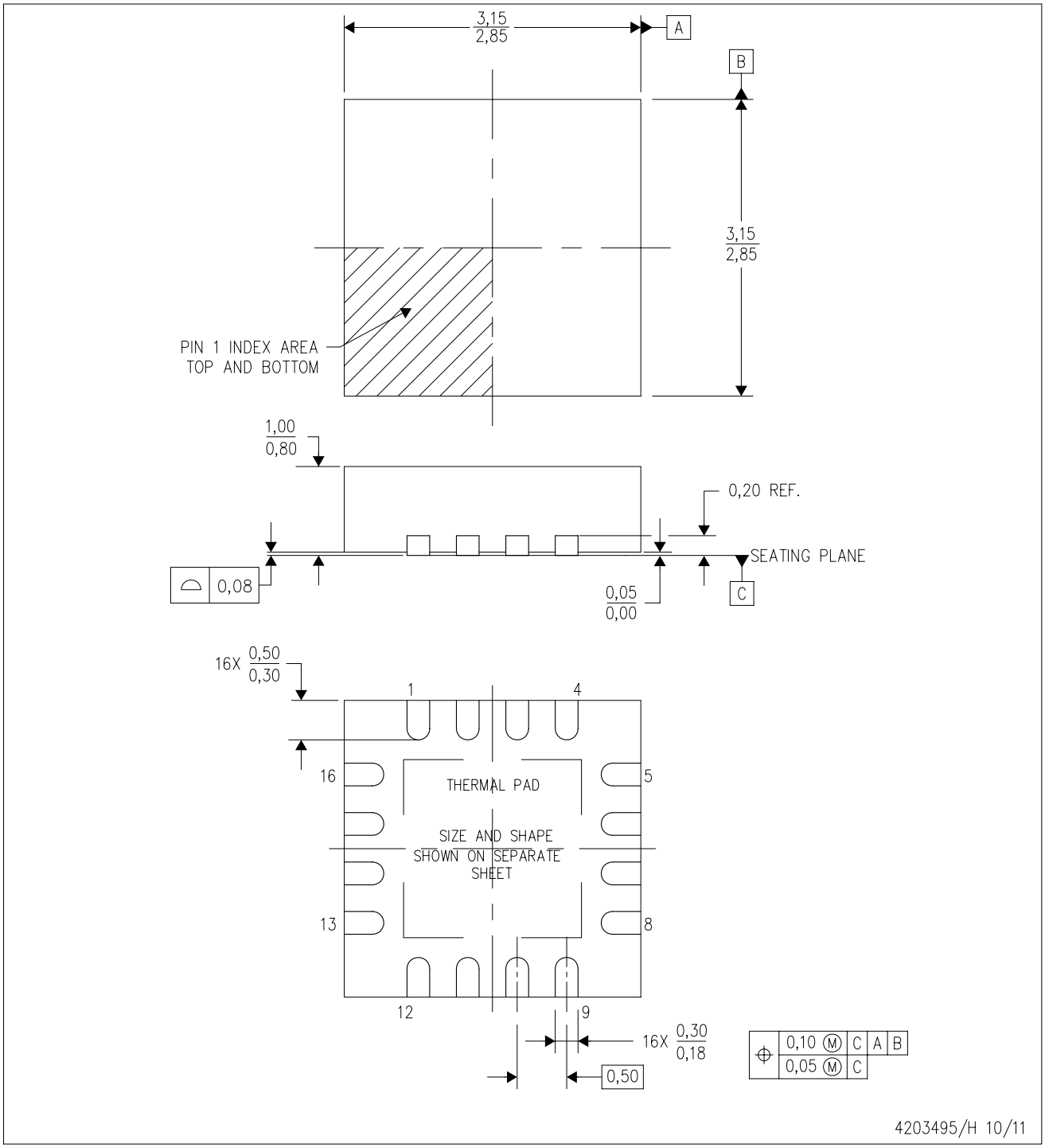
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS65510RGTR | QFN | RGT | 16 | 3000 | 367.0 | 367.0 | 35.0 |
| TPS65510RGTT | QFN | RGT | 16 | 250 | 210.0 | 185.0 | 35.0 |

RGT (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD




NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

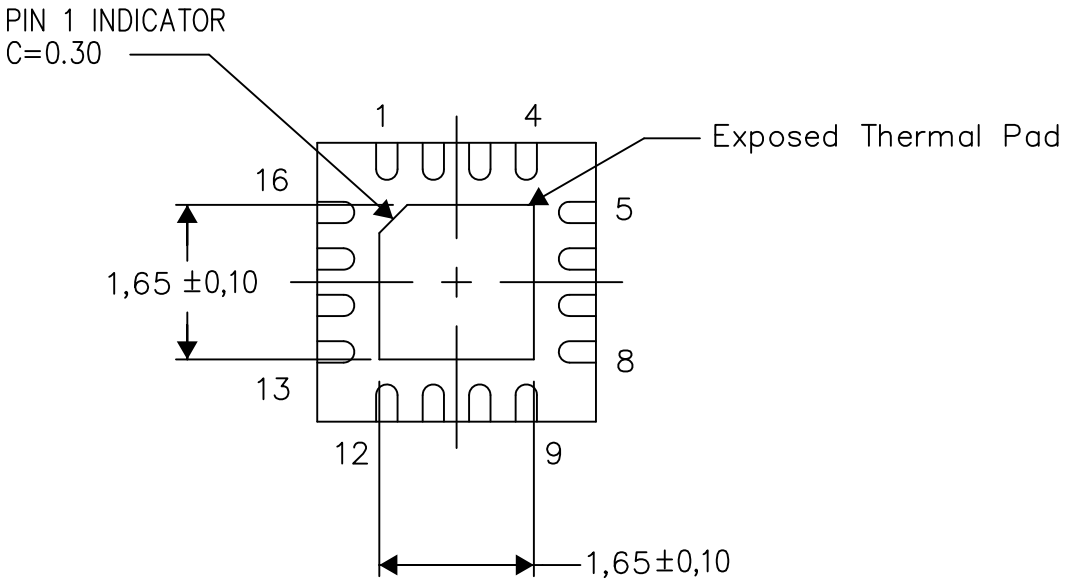
RGT (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



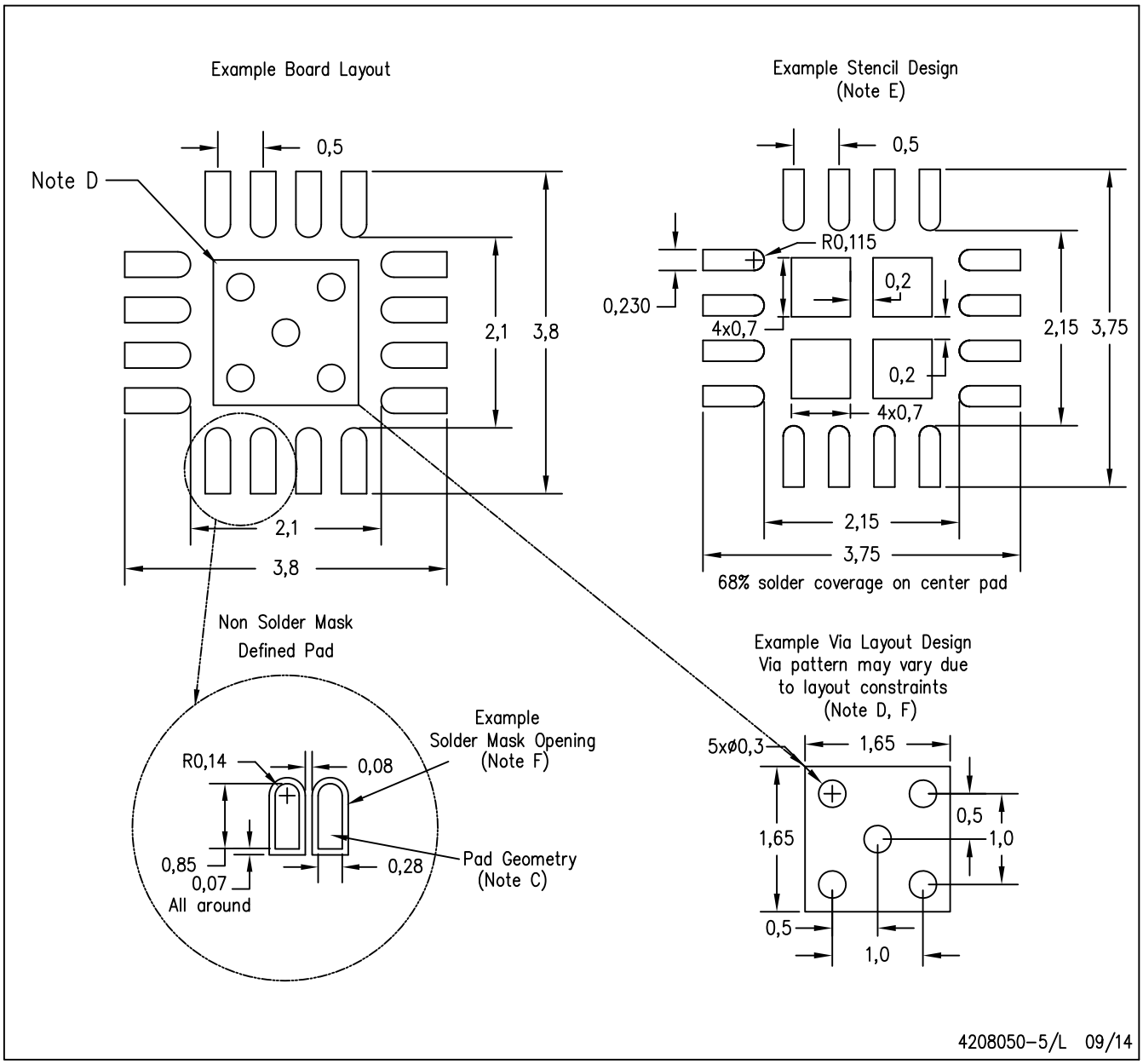

Bottom View

Exposed Thermal Pad Dimensions

4206349–7/W 10/14

NOTE: All linear dimensions are in millimeters

# RGT (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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